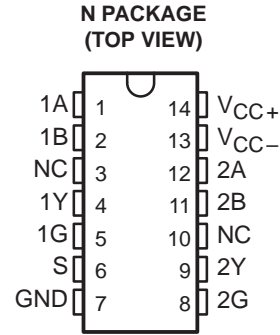


SN75207B DUAL SENSE AMPLIFIER FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

SLLS096C – JULY 1973 – REVISED MARCH 1997

- Plug-In Replacement for SN75107A and SN75107B With Improved Characteristics
- ± 10 -mV Input Sensitivity
- TTL-Compatible Circuitry
- Standard Supply Voltages . . . ± 5 V
- Differential Input Common-Mode Voltage Range of ± 3 V
- Strobe Inputs for Channel Selection
- Totem-Pole Outputs
- SN75207B Has Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

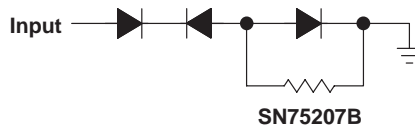


NC – No internal connection

description

The SN75207B is a terminal-for-terminal replacement for the SN75107B. The improved input sensitivity makes it more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes it more useful in line-receiver applications by allowing use of longer transmission line lengths. The SN75207B features a TTL-compatible, active-pullup output.

Input protection diodes are in series with the collectors of the differential-input transistors of the SN75207B. These diodes are useful in certain party-line systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



This would be a problem in specific systems that might have the transmission lines biased to some potential greater than 1.4 V.

This device is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| DIFFERENTIAL INPUTS A-B | STROBES | | OUTPUT Y |
|-----------------------------|---------|---|---------------|
| | G | S | |
| $V_{ID} \geq 10$ mV | X | X | H |
| -10 mV $< V_{ID} < 10$ mV | X | L | H |
| | L | X | H |
| | H | H | Indeterminate |
| $V_{ID} \leq -10$ mV | X | L | H |
| | L | X | H |
| | H | H | L |

H = high level, L = low level, X = irrelevant



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

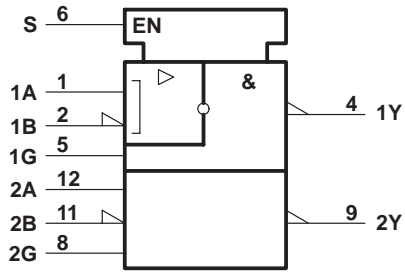
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SN75207B DUAL SENSE AMPLIFIER FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

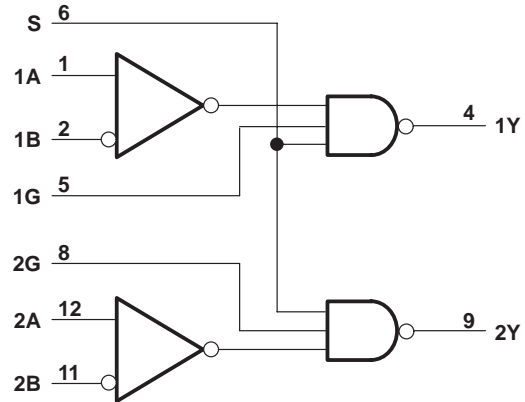
SLLS096C – JULY 1973 – REVISED MARCH 1997

logic symbol†

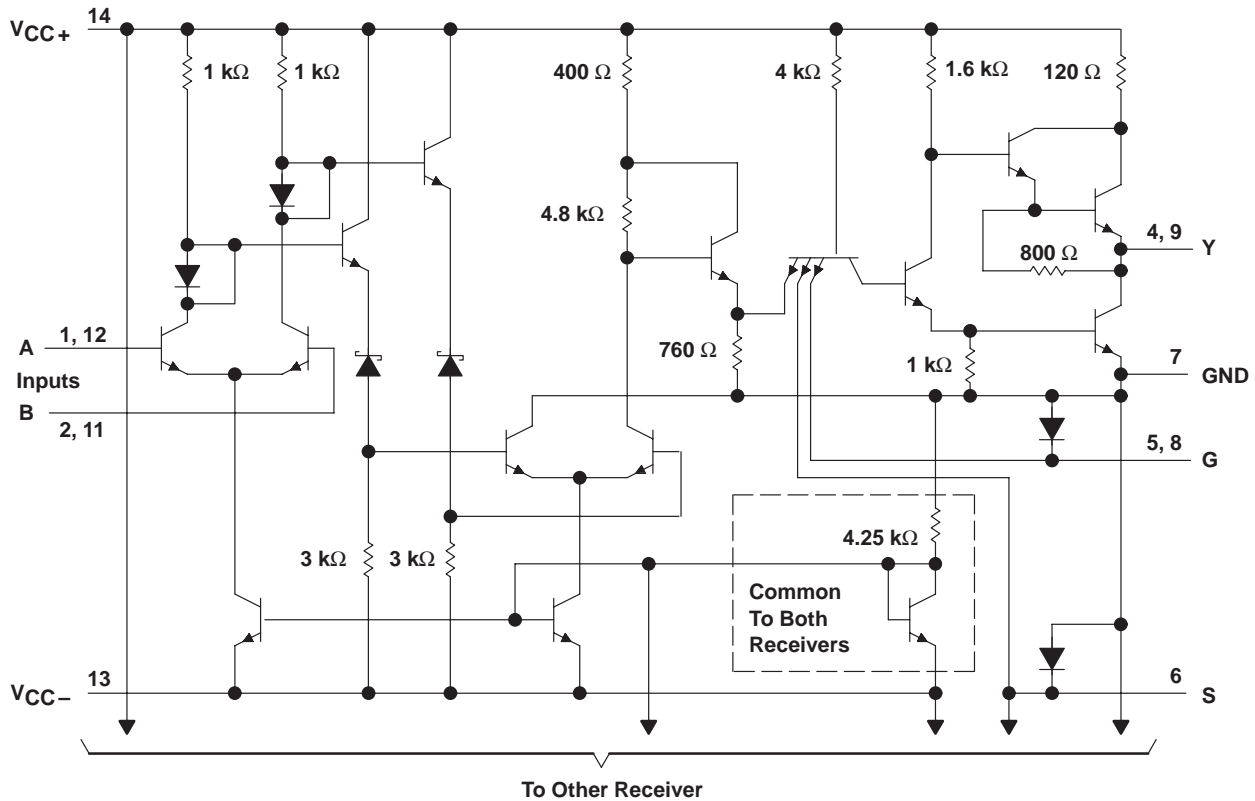


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are nominal.

design characteristics

The SN75207B line receivers/sense amplifiers are TTL-compatible, dual circuits intended for use in high-speed, data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. The dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ± 3 V. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to ensure 400 mV of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 mV typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10-mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|------------------------------|
| Supply voltage, V_{CC+} (see Note 1) | 7 V |
| Supply voltage, V_{CC-} (see Note 1) | -7 V |
| Differential input voltage, V_{ID} (see Note 2) | ± 6 V |
| Common-mode input voltage, V_{IC} (see Note 3) | ± 5 V |
| Strobe input voltage | 5.5 V |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: A. All voltage values, except differential voltages, are with respect to GND terminal.
1. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
2. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|---|--|
| N | 1050 mW | 9.2 mW/°C | 636 mW |

SN75207B DUAL SENSE AMPLIFIER FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

SLLS096C – JULY 1973 – REVISED MARCH 1997

recommended operating conditions (see Note 4)

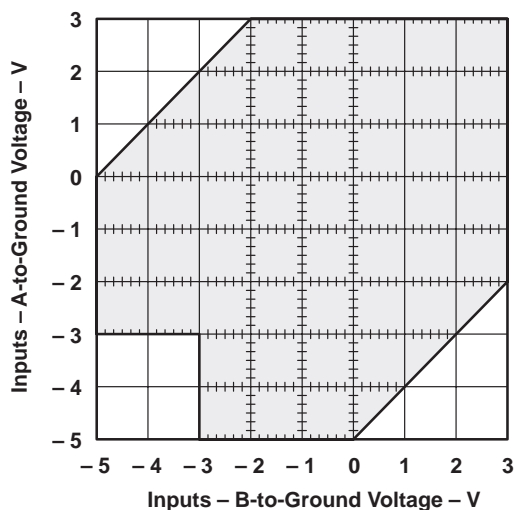
| | MIN | NOM | MAX | UNIT |
|---|-------|-----|-------|------|
| Supply voltage, V_{CC+} | 4.75 | 5 | 5.25 | V |
| Supply voltage, V_{CC-} | -4.75 | -5 | -5.25 | V |
| High-level differential input voltage, $V_{ID(H)}$ (see Note 5) | 0.01 | | 5 | V |
| Low-level differential input voltage, $V_{ID(L)}$ | -5† | | -0.01 | V |
| Common-mode input voltage, V_{IC} (see Notes 5 and 6) | -3† | | 3 | V |
| Input voltage, any differential input to ground (see Note 5) | -5† | | 3 | V |
| High-level input voltage at strobe inputs, $V_{IH(S)}$ | 2 | | 5.5 | V |
| Low-level input voltage at strobe inputs, $V_{IL(S)}$ | 0 | | 0.8 | V |
| Low-level output current, I_{OL} | | | -16 | mA |
| Operating free-air temperature, T_A | 0 | | 70 | °C |

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: B. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between -3 V and 3 V.

3. The recommended combinations of input voltages fall within the shaded area of the figure shown.

4. The common-mode voltage may be as low as -4 V provided that the more positive of the two inputs is not more negative than -3 V.



SN75207B DUAL SENSE AMPLIFIER FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

SLLS096C – JULY 1973 – REVISED MARCH 1997

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------|--|---|--|------|------|------|---------------|
| I_{IH} | High-level input current | $V_{CC\pm} = \pm 5.25\text{ V}$ | $V_{ID} = -5\text{ V}$ | | 30 | 75 | μA |
| I_{IL} | Low-level input current | $V_{CC\pm} = \pm 5.25\text{ V}$ | $V_{ID} = 5\text{ V}$ | | | -10 | μA |
| I_{IH} | High-level input current into 1G or 2G | $V_{CC\pm} = \pm 5.25\text{ V}, V_{IH(S)} = 2.4\text{ V}$ | | | | 40 | μA |
| | | $V_{CC\pm} = \pm 5.25\text{ V}, V_{IH(S)} = \pm 5.25\text{ V}$ | | | | 1 | mA |
| I_{IL} | Low-level input current into 1G or 2G | $V_{CC\pm} = \pm 5.25\text{ V}, V_{IL(S)} = 0.4\text{ V}$ | | | | -1.6 | mA |
| I_{IH} | High-level input current into S | $V_{CC\pm} = \pm 5.25\text{ V}, V_{IH(S)} = 2.4\text{ V}$ | | | | 80 | μA |
| | | $V_{CC\pm} = \pm 5.25\text{ V}, V_{IH(S)} = \pm 5.25\text{ V}$ | | | | 2 | mA |
| I_{IL} | Low-level input current into S | $V_{CC\pm} = \pm 5.25\text{ V}, V_{IL(S)} = 0.4\text{ V}$ | | | | -3.2 | mA |
| V_{OH} | High-level output voltage | $V_{CC\pm} = \pm 4.75\text{ V}, I_{OH} = -400\ \mu\text{A}, V_{IC} = -3\text{ V to }3\text{ V}$ | $V_{IL(S)} = 0.8\text{ V}, V_{ID(H)} = 10\text{ mV}$ | 2.4 | | | V |
| V_{OL} | Low-level output voltage | $V_{CC\pm} = \pm 4.75\text{ V}, I_{OL} = 16\text{ mA}, V_{IC} = -3\text{ V to }3\text{ V}$ | $V_{IH(S)} = 2\text{ V}, V_{ID(L)} = -10\text{ mV}$ | | | 0.4 | V |
| I_{OH} | High-level output current | $V_{CC\pm} = \pm 4.75\text{ V}, V_{OH} = \pm 5.25\text{ V}$ | | | | 400 | μA |
| I_{OS} | Short-circuit output current‡ | $V_{CC\pm} = \pm 5.25\text{ V}$ | | -18 | | -70 | mA |
| I_{CC+} | Supply current from V_{CC+} | $V_{CC\pm} = \pm 5.25\text{ V}, T_A = 25^\circ\text{C},$ | Outputs high | | 18 | 30 | mA |
| I_{CC-} | Supply current from V_{CC-} | $V_{CC\pm} = \pm 5.25\text{ V}, T_A = 25^\circ\text{C},$ | Outputs high | -8.4 | | -15 | mA |

† All typical values are at $V_{CC+} = 5\text{ V}, V_{CC-} = -5\text{ V}, T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC+} = 5\text{ V}, V_{CC-} = -5\text{ V}, T_A = 25^\circ\text{C}$

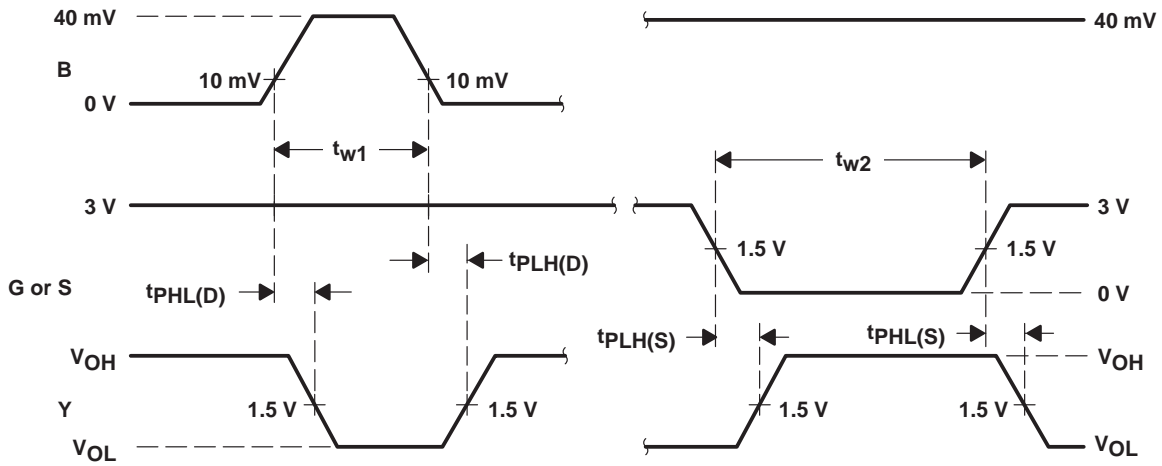
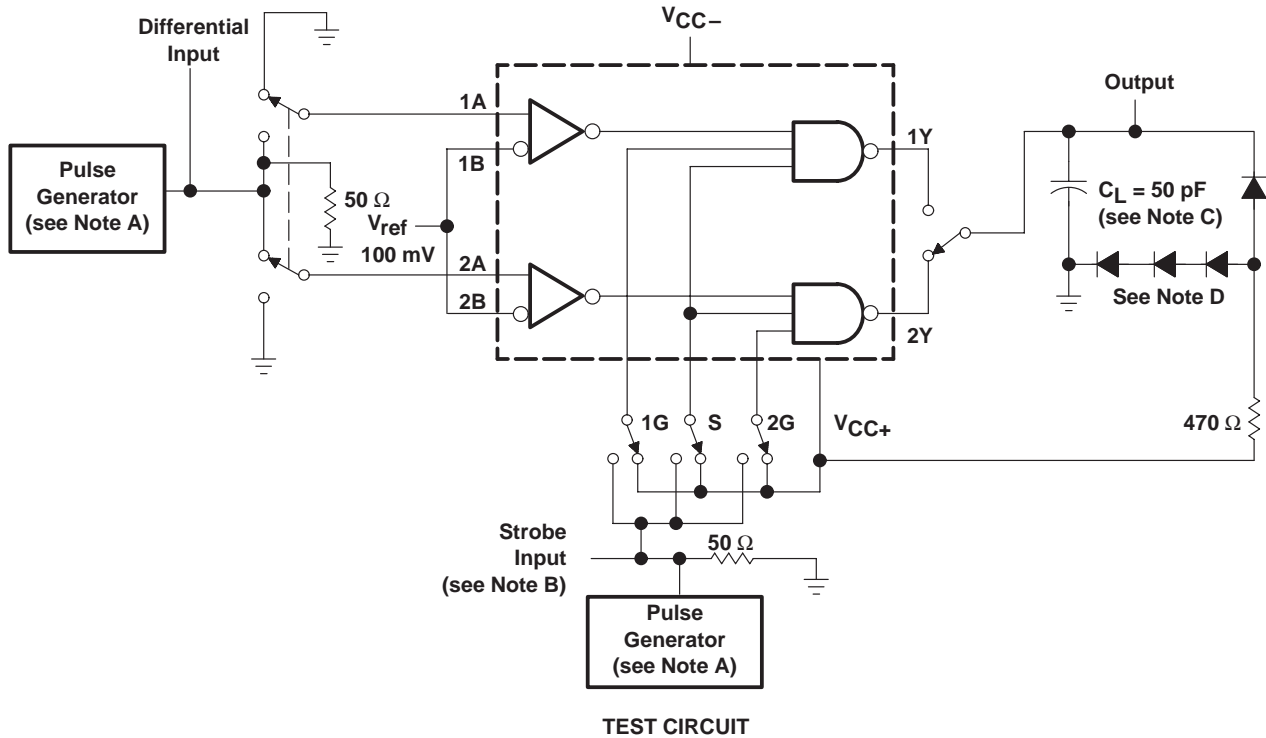
| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|--------------|---|--------------------------------------|-----------------------|-----|-----|------|
| $t_{PLH(D)}$ | Propagation delay time, low- to high-level output· from differential inputs A and B | $R_L = 470\ \Omega,$ See Figure 1 | $C_L = 50\text{ pF},$ | | 35 | ns |
| $t_{PHL(D)}$ | Propagation delay time, high- to low-level output· from differential inputs A and B | | | | 20 | ns |
| $t_{PLH(S)}$ | Propagation delay time, low- to high-level output, from strobe input G or S | | | | 17 | ns |
| $t_{PHL(S)}$ | Propagation delay time, high- to low-level output, from strobe input G or S | | | | 17 | ns |



SN75207B
DUAL SENSE AMPLIFIER FOR MOS MEMORIES
OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

SLLS096C – JULY 1973 – REVISED MARCH 1997

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generators have the following characteristics: $Z_O = 50 \Omega$, $t_r \leq 5 \text{ ns}$, $t_f \leq 5 \text{ ns}$, $t_{w1} = 500 \text{ ns}$ with $\text{PRR} = 1 \text{ MHz}$, $t_{w2} = 1 \mu\text{s}$ with $\text{PRR} = 500 \text{ kHz}$.
- B. Strobe input pulse is applied to Strobe 1G when inputs 1A–1B are being tested, to Strobe S when inputs 1A–1B or 2A–2B are being tested, and to Strobe 2G when inputs 2A–2B are being tested.
- C. C_L includes probe and jig capacitance.
- D. All diodes are 1N916.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

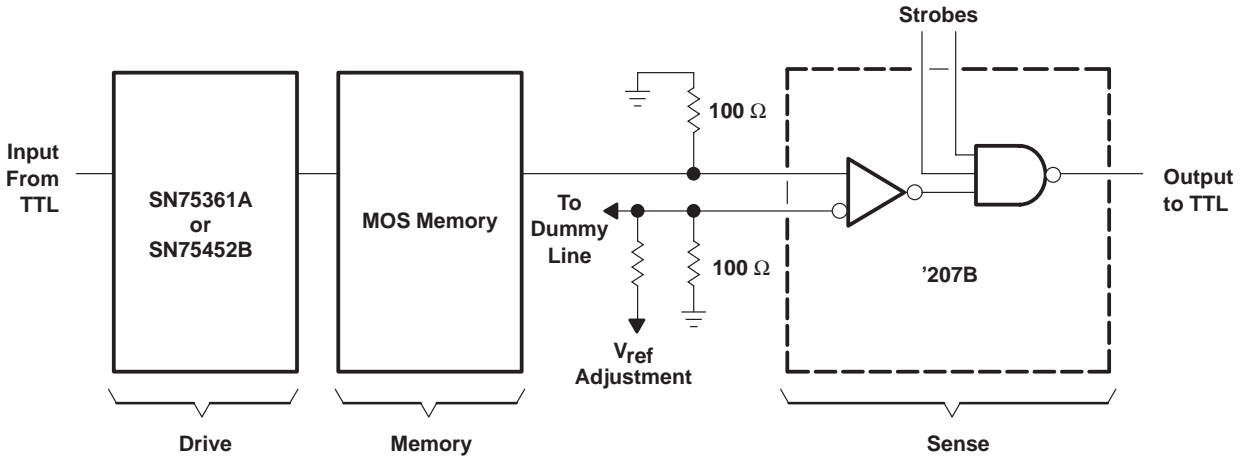
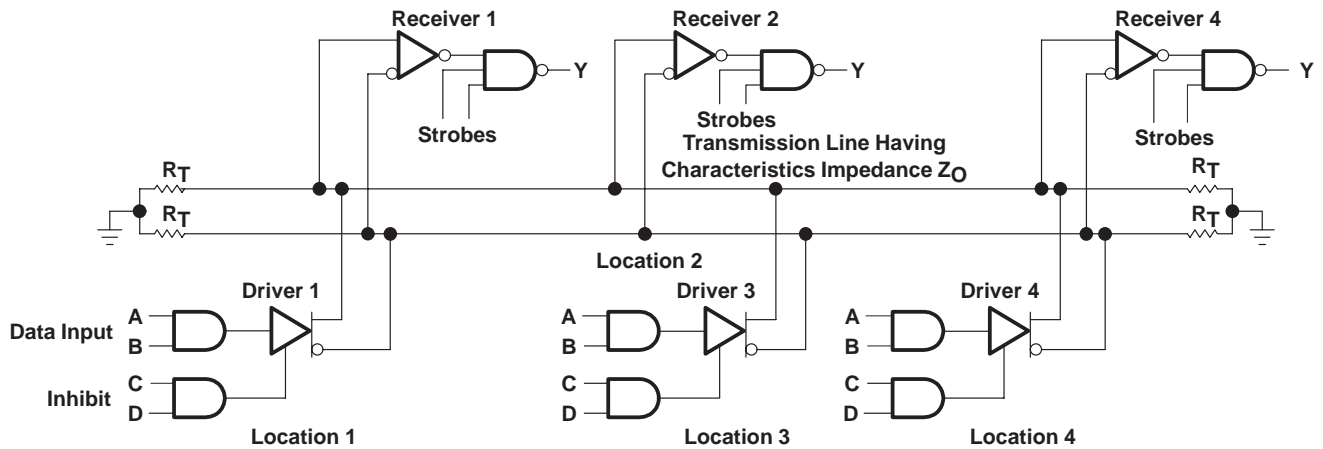


Figure 2. MOS Memory Sense Amplifier



Receivers are SN75207B; drivers are SN55109A, SN55110A, SN75110A, or SN75112.

Figure 3. Data-Bus or Parity-Line System

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between -3 V and 3 V , preferably at GND. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75207BN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75207BN | Samples |
| SN75207BNSR | ACTIVE | SOP | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75207B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75207BNSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75207BNSR | SOP | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75207BN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated