

- **Very Low Power Consumption . . . 2 mW**
Typ at $V_{DD} = 5\text{ V}$
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
Sink 100 mA Typ
Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **Single-Supply Operation From 2 V to 15 V**
- **Functionally interchangeable With the NE556; Has Same Pinout**

description

The TLC556 series are monolithic timing circuits fabricated using the TI LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

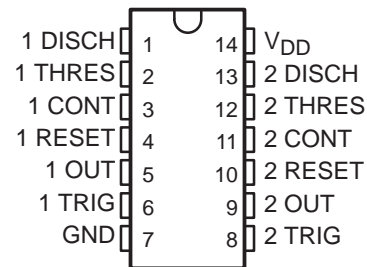
While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

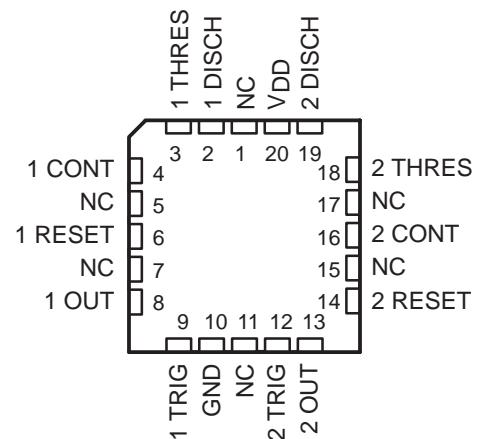
All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556C is characterized for operation from 0°C to 70°C. The TLC556I is characterized for operation from -40°C to 85°C. The TLC556M is characterized for operation over the full military temperature range of -55°C to 125°C.

**D, J, OR N PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC—No internal connection

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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TLC556, TLC556Y DUAL LinCMOS™ TIMERS

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AVAILABLE OPTIONS

| T _A RANGE | V _{DD} RANGE | PACKAGE | | | | CHIP FORM (Y) |
|-------------------------|--------------------------|----------------------|----------------------|--------------------|--------------------|------------------|
| | | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (J) | PLASTIC DIP (N) | |
| 0°C to 70°C | 2 V to 18 V | TLC556CD | | | TLC556CN | TLC556Y |
| -40°C to 85°C | 3 V to 18 V | TLC556ID | | | TLC556IN | |
| -55°C to 125°C | 5 V to 18 V | TLC556MD | TLC556MFK | TLC556MJ | TLC556MN | |

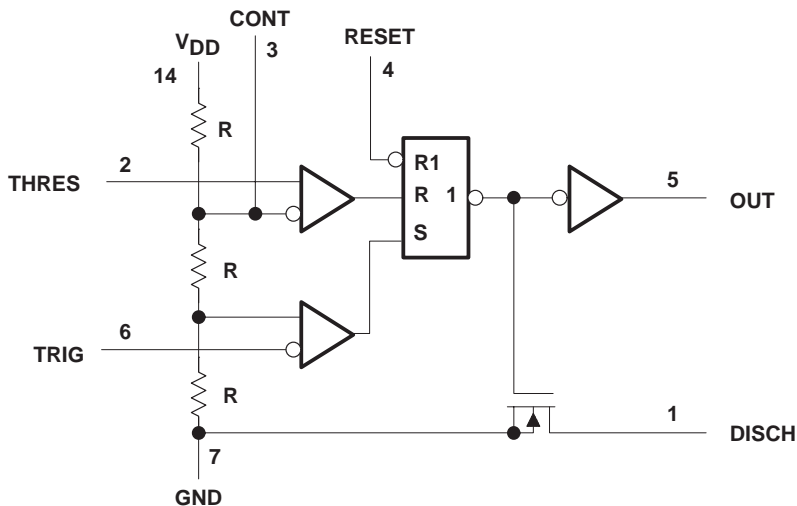
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC556CDR).

FUNCTION TABLE

| RESET VOLTAGE† | TRIGGER VOLTAGE† | THRESHOLD VOLTAGE† | OUTPUT | DISCHARGE SWITCH |
|-------------------|---------------------|-----------------------|---------------------------|---------------------|
| < MIN | Irrelevant | Irrelevant | L | On |
| > MAX | < MIN | Irrelevant | H | Off |
| >MAX | >MAX | >MAX | L | On |
| > MAX | > MAX | < MIN | As previously established | |

† For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram (each timer)

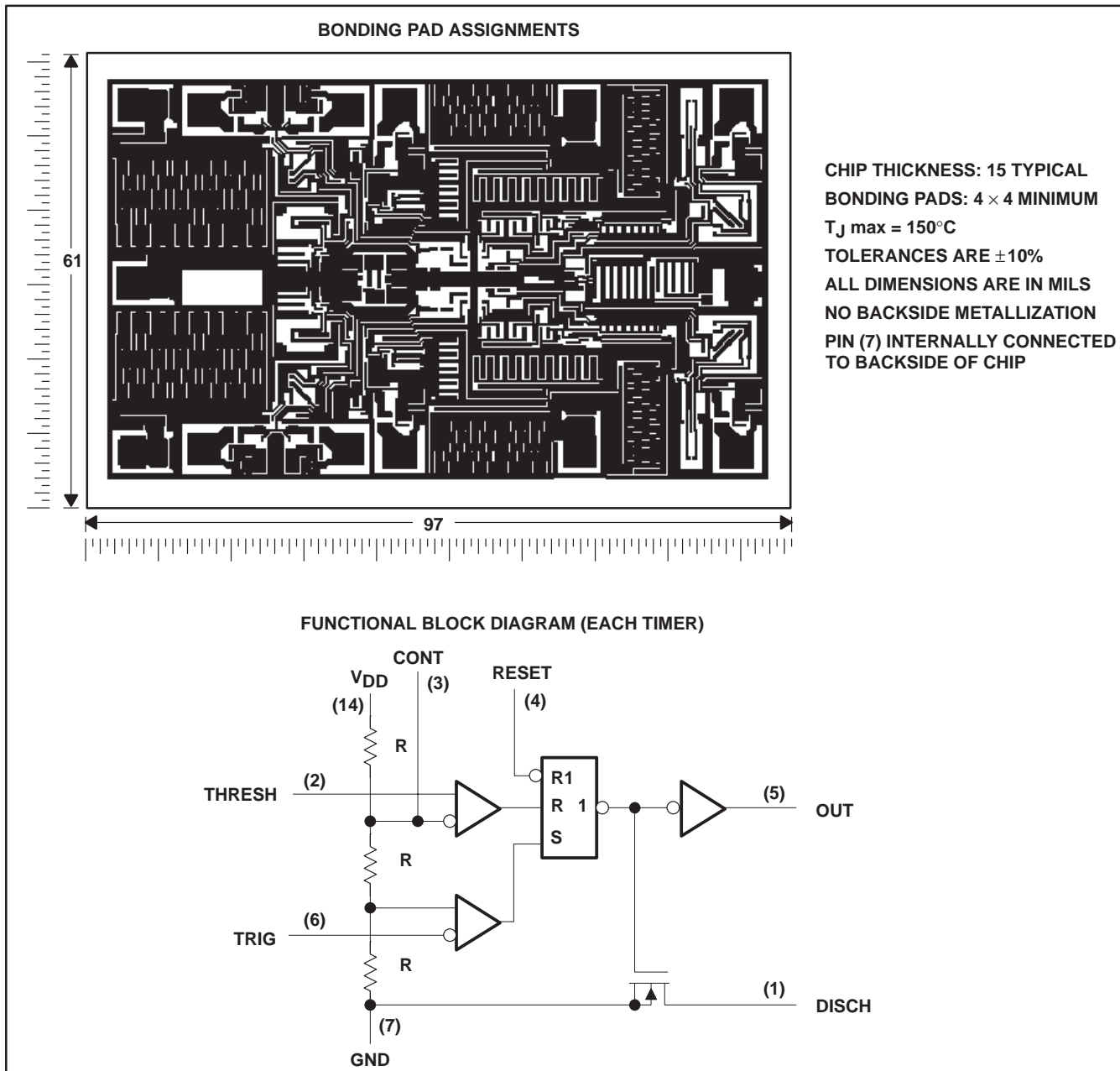


RESET can override TRIG and THRES.
TRIG can override THRES.

Pin numbers shown are for the D, J, or N packages.

TLC556Y chip information

These chips, properly assembled, display characteristics similar to the TLC556 (see electrical table). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

| | TLC556C | TLC556I | TLC556M | UNIT |
|--|------------------------------|------------------|------------------|------|
| Supply voltage, V_{DD} (see Note 1) | 18 | 18 | 18 | V |
| Input voltage range, V_I | -0.3 to V_{DD} | -0.3 to V_{DD} | -0.3 to V_{DD} | V |
| Sink current, discharge or output | 150 | 150 | 150 | mA |
| Source current, output | 15 | 15 | 15 | mA |
| Continuous total power dissipation | See Dissipation Rating Table | | | |
| Operating free-air temperature range | 0 to 70 | -40 to 85 | -55 to 125 | °C |
| Storage temperature range | -65 to 150 | -65 to 150 | -65 to 150 | °C |
| Case temperature for 60 seconds | FK package | | 260 | °C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | J package | | 300 | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D or N package | 260 | 260 | |

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|---|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW | N/A |

recommended operating conditions

| | MIN | MAX | UNIT |
|---|---------|-----|------|
| Supply voltage, V_{DD} | 2 | 15 | V |
| Operating free-air temperature range, T_A | TLC556C | 0 | 70 |
| | TLC556I | -40 | 85 |
| | TLC556M | -55 | 125 |



electrical characteristics at specified free-air temperature, $V_{DD} = 2\text{ V}$ for TLC556C, $V_{DD} = 3\text{ V}$ for TLC556I

| PARAMETER | TEST CONDITIONS | T_A † | TLC556C | | | TLC556I | | | UNIT |
|--|------------------------------|------------|---------|------|------|---------|-----|-------|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IT} Input threshold voltage | | 25°C | 0.95 | 1.33 | 1.65 | 1.6 | 2 | 2.4 | V |
| | | Full range | 0.85 | | 1.75 | 1.5 | | 2.5 | |
| Threshold current | | 25°C | 10 | | | 10 | | | pA |
| | | MAX | 75 | | | 150 | | | |
| $V_{(trigger)}$ Trigger voltage | | 25°C | 0.4 | 0.67 | 0.95 | 0.71 | 1 | 1.29 | V |
| | | Full range | 0.3 | | 1.05 | 0.61 | | 1.39 | |
| $I_{(trigger)}$ Trigger current | | 25°C | 10 | | | 10 | | | pA |
| | | MAX | 75 | | | 150 | | | |
| $V_{(reset)}$ Reset voltage | | 25°C | 0.4 | 1.1 | 1.5 | 0.4 | 1.1 | 1.5 | V |
| | | Full range | 0.3 | | 1.8 | 0.3 | | 1.8 | |
| $I_{(reset)}$ Reset current | | 25°C | 10 | | | 10 | | | pA |
| | | MAX | 75 | | | 150 | | | |
| Control voltage (open circuit) as a percentage of supply voltage | | MAX | 66.7% | | | 66.7% | | | |
| Discharge switch on-state voltage | $I_{OL} = 1\text{ mA}$ | 25°C | 0.04 | | 0.2 | 0.03 | | 0.2 | V |
| | | Full range | | | 0.25 | | | 0.375 | |
| Discharge switch off-state current | | 25°C | 0.1 | | | 0.1 | | | nA |
| | | MAX | 0.5 | | | 120 | | | |
| V_{OH} High-level output voltage | $I_{OH} = -300\ \mu\text{A}$ | 25°C | 1.5 | 1.9 | | 1.5 | 1.9 | | V |
| | | Full range | 1.5 | | 2.5 | | | | |
| V_{OL} Low-level output voltage | $I_{OL} = 1\text{ mA}$ | 25°C | 0.07 | | 0.3 | 0.07 | | 0.3 | V |
| | | Full range | | | 0.35 | | | 0.4 | |
| I_{DD} Supply current | See Note 2 | 25°C | 130 | | 500 | 130 | | 500 | μA |
| | | Full range | | | 800 | | | 1000 | |

† Full range is 0°C to 70°C for TLC556C and -40°C to 85°C for TLC556I.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

| PARAMETER | TEST CONDITIONS | T_A † | TLC556C | | | TLC556I | | | TLC556M | | | UNIT |
|--|--------------------------|------------|----------|------|------|----------|------|------|----------|------|------|---------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IT} Input threshold voltage | | 25°C | 2.8 | 3.3 | 3.8 | 2.8 | 3.3 | 3.8 | 2.8 | 3.3 | 3.8 | V |
| | | Full range | 2.7 | | 3.9 | 2.7 | | 3.9 | 2.7 | | 3.9 | |
| Threshold current | | 25°C | 10 | | | 10 | | | 10 | | | pA |
| | | MAX | 75 | | | 150 | | | 5000 | | | |
| $V_{(trigger)}$ Trigger voltage | | 25°C | 1.36 | 1.66 | 1.96 | 1.36 | 1.66 | 1.96 | 1.36 | 1.66 | 1.96 | V |
| | | Full range | 1.26 | | 2.06 | 1.26 | | 2.06 | 1.26 | | 2.06 | |
| $I_{(trigger)}$ Trigger current | | 25°C | 10 | | | 10 | | | 10 | | | pA |
| | | MAX | 75 | | | 150 | | | 5000 | | | |
| $V_{(reset)}$ Reset voltage | | 25°C | 0.4 | 1.1 | 1.5 | 0.4 | 1.1 | 1.5 | 0.4 | 1.1 | 1.5 | V |
| | | Full range | 0.3 | | 1.8 | 0.3 | | 1.8 | 0.3 | | 1.8 | |
| $I_{(reset)}$ Reset current | | 25°C | 10 | | | 10 | | | 10 | | | pA |
| | | MAX | 75 | | | 150 | | | 5000 | | | |
| Control voltage (open circuit) as a percentage of supply voltage | | MAX | 66.7% | | | 66.7% | | | 66.7% | | | |
| Discharge switch on-state voltage | $I_{OL} = 10\text{ mA}$ | 25°C | 0.15 0.5 | | | 0.15 0.5 | | | 0.15 0.5 | | | V |
| | | Full range | 0.6 | | | 0.6 | | | 0.6 | | | |
| Discharge switch off-state current | | 25°C | 0.1 | | | 0.1 | | | 0.1 | | | nA |
| | | MAX | 0.5 | | | 2 | | | 120 | | | |
| V_{OH} High-level output voltage | $I_{OH} = -1\text{ mA}$ | 25°C | 4.1 | 4.8 | | 4.1 | 4.8 | | 4.1 | 4.8 | | V |
| | | Full range | 4.1 | | | 4.1 | | | 4.1 | | | |
| V_{OL} Low-level output voltage | $I_{OL} = 8\text{ mA}$ | 25°C | 0.21 0.4 | | | 0.21 0.4 | | | 0.21 0.4 | | | V |
| | | Full range | 0.5 | | | 0.5 | | | 0.6 | | | |
| | $I_{OL} = 5\text{ mA}$ | 25°C | 0.13 0.3 | | | 0.13 0.3 | | | 0.13 0.3 | | | |
| | | Full range | 0.4 | | | 0.4 | | | 0.45 | | | |
| | $I_{OL} = 3.2\text{ mA}$ | 25°C | 0.08 0.3 | | | 0.08 0.3 | | | 0.08 0.3 | | | |
| | | Full range | 0.35 | | | 0.35 | | | 0.4 | | | |
| I_{DD} Supply current | See Note 2 | 25°C | 340 700 | | | 340 700 | | | 340 700 | | | μA |
| | | Full range | 1000 | | | 1200 | | | 1400 | | | |

† Full range is 0°C to 70°C for TLC556C, -40°C to 85°C for TLC556I, and -55°C to 125°C for TLC556M.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.



electrical characteristics at specified free-air temperature, $V_{DD} = 15\text{ V}$

| PARAMETER | | TEST CONDITIONS | T_A † | TLC556C | | | TLC556I | | | TLC556M | | | UNIT |
|-----------------|--|--------------------------|------------|---------|------|-------|---------|------|-------|---------|------|-------|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IT} | Input threshold voltage | | 25°C | 9.45 | 10 | 10.55 | 9.45 | 10 | 10.55 | 9.45 | 10 | 10.55 | V |
| | | | Full range | 9.35 | | 10.65 | 9.35 | | 10.65 | 9.35 | | 10.65 | |
| | Threshold current | | 25°C | | 10 | | | 10 | | | 10 | pA | |
| | | | MAX | | 75 | | | 150 | | | 5000 | | |
| $V_{(trigger)}$ | Trigger voltage | | 25°C | 4.65 | 5 | 5.35 | 4.65 | 5 | 5.35 | 4.65 | 5 | 5.35 | V |
| | | | Full range | 4.55 | | 5.45 | 4.55 | | 5.45 | 4.55 | | 5.45 | |
| $I_{(trigger)}$ | Trigger current | | 25°C | | 10 | | | 10 | | | 10 | pA | |
| | | | MAX | | 75 | | | 150 | | | 5000 | | |
| $V_{(reset)}$ | Reset voltage | | 25°C | 0.4 | 1.1 | 1.5 | 0.4 | 1.1 | 1.5 | 0.4 | 1.1 | 1.5 | V |
| | | | Full range | 0.3 | | 1.8 | 0.3 | | 1.8 | 0.3 | | 1.8 | |
| $I_{(reset)}$ | Reset current | | 25°C | | 10 | | | 10 | | | 10 | pA | |
| | | | MAX | | 75 | | | 150 | | | 5000 | | |
| | Control voltage (open circuit) as a percentage of supply voltage | | MAX | 66.7% | | | 66.7% | | | 66.7% | | | |
| | Discharge switch on-state voltage | $I_{OL} = 100\text{ mA}$ | 25°C | | 0.8 | 1.7 | | 0.8 | 1.7 | | 0.8 | 1.7 | V |
| | | | Full range | | | 1.8 | | | 1.8 | | | 1.8 | |
| | Discharge switch off-state current | | 25°C | | 0.1 | | | 0.1 | | | 0.1 | nA | |
| | | | MAX | | 0.5 | | | 2 | | | 120 | | |
| V_{OH} | High-level output voltage | $I_{OH} = -10\text{ mA}$ | 25°C | 12.5 | 14.2 | | 12.5 | 14.2 | | 12.5 | 14.2 | V | |
| | | | Full range | 12.5 | | | 12.5 | | | 12.5 | | | |
| | | $I_{OH} = -5\text{ mA}$ | 25°C | 13.5 | 14.6 | | 13.5 | 14.6 | | 13.5 | 14.6 | | |
| | | | Full range | 13.5 | | | 13.5 | | | 13.5 | | | |
| | | $I_{OH} = -1\text{ mA}$ | 25°C | 14.2 | 14.9 | | 14.2 | 14.9 | | 14.2 | 14.9 | | |
| | | | Full range | 14.2 | | | 14.2 | | | 14.2 | | | |
| V_{OL} | Low-level output voltage | $I_{OL} = 100\text{ mA}$ | 25°C | | 1.28 | 3.2 | | 1.28 | 3.2 | | 1.28 | 3.2 | V |
| | | | Full range | | | 3.6 | | | 3.7 | | | 3.8 | |
| | | $I_{OL} = 50\text{ mA}$ | 25°C | | 0.63 | 1 | | 0.63 | 1 | | 0.63 | 1 | |
| | | | Full range | | | 1.3 | | | 1.4 | | | 1.5 | |
| | | $I_{OL} = 10\text{ mA}$ | 25°C | | 0.12 | 0.3 | | 0.12 | 0.3 | | 0.12 | 0.3 | |
| | | | Full range | | | 0.4 | | | 0.4 | | | 0.45 | |
| I_{DD} | Supply current | See Note 2 | 25°C | | 0.72 | 1.2 | | 0.72 | 1.2 | | 0.72 | 1.2 | mA |
| | | | Full range | | | 1.6 | | | 1.8 | | | 2 | |

† Full range is 0°C to 70°C for TLC556C, -40°C to 85°C for TLC556I, and -55°C to 125°C for TLC556M.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

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electrical characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|------------------------------------|--------------------------|------|------|------|---------------|
| V_{IT} | Input threshold voltage | | 2.8 | 3.3 | 3.8 | V |
| | Threshold current | | | 10 | | pA |
| $V_{(trigger)}$ | Trigger voltage | | 1.36 | 1.66 | 1.96 | V |
| $I_{(trigger)}$ | Trigger current | | | 10 | | pA |
| $V_{(reset)}$ | Reset voltage | | 0.4 | 1.1 | 1.5 | V |
| $I_{(reset)}$ | Reset current | | | 10 | | pA |
| | Discharge switch on-state voltage | $I_{OL} = 10\text{ mA}$ | | 0.15 | 0.5 | V |
| | Discharge switch off-state current | | | 0.1 | | nA |
| V_{OH} | High-level output voltage | $I_{OH} = -1\text{ mA}$ | 4.1 | 4.8 | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 8\text{ mA}$ | | 0.21 | 0.4 | V |
| | | $I_{OL} = 5\text{ mA}$ | | 0.13 | 0.3 | |
| | | $I_{OL} = 2.1\text{ mA}$ | | 0.08 | 0.3 | |
| I_{DD} | Supply current | See Note 2 | | 3.40 | 700 | μA |

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|--|-----|-----|-----|------|
| | Initial error of timing interval † | $V_{DD} = 5\text{ V to }15\text{ V}$, $R_A = R_B = 1\text{ k}\Omega\text{ to }100\text{ k}\Omega$ | | 1% | 3% | |
| | Supply voltage sensitivity of timing interval | $C_T = 0.1\text{ }\mu\text{F}$, See Note 3 | | 0.1 | 0.5 | %/V |
| t_r | Output pulse rise time | $R_L = 10\text{ M}\Omega$, $C_L = 10\text{ pF}$ | | 20 | 75 | ns |
| t_f | Output pulse fall time | | | 15 | 60 | |
| f_{max} | Maximum frequency in astable mode | $R_A = 470\text{ }\Omega$, $C_T = 200\text{ pF}$, $R_B = 200\text{ }\Omega$, See Note 3 | 1.2 | 2.1 | | MHz |

† Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A , R_B , and C_T are as defined in Figure 3.



TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

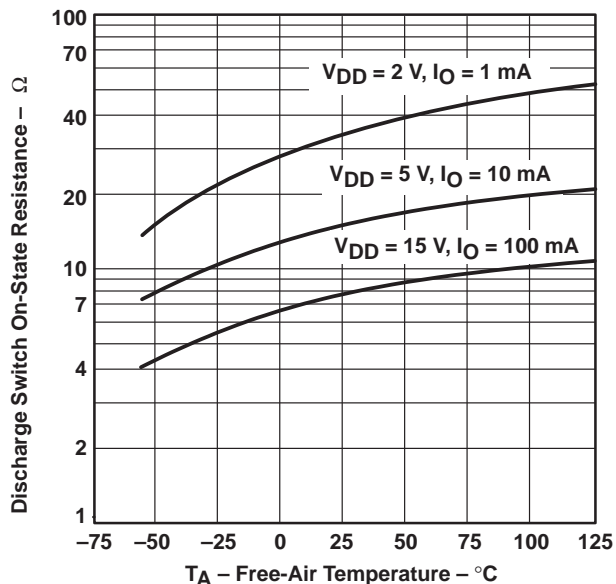
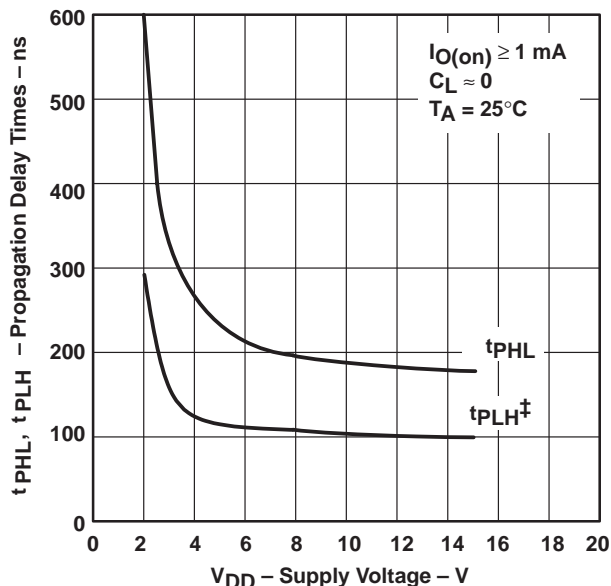


Figure 1

PROPAGATION DELAY TIMES (TO DISCHARGE
OUTPUT FROM TRIGGER AND THRESHOLD
SHORTED TOGETHER)
vs
SUPPLY VOLTAGE



‡ The effects of the load resistance on these values must be taken into account separately.

Figure 2

APPLICATION INFORMATION

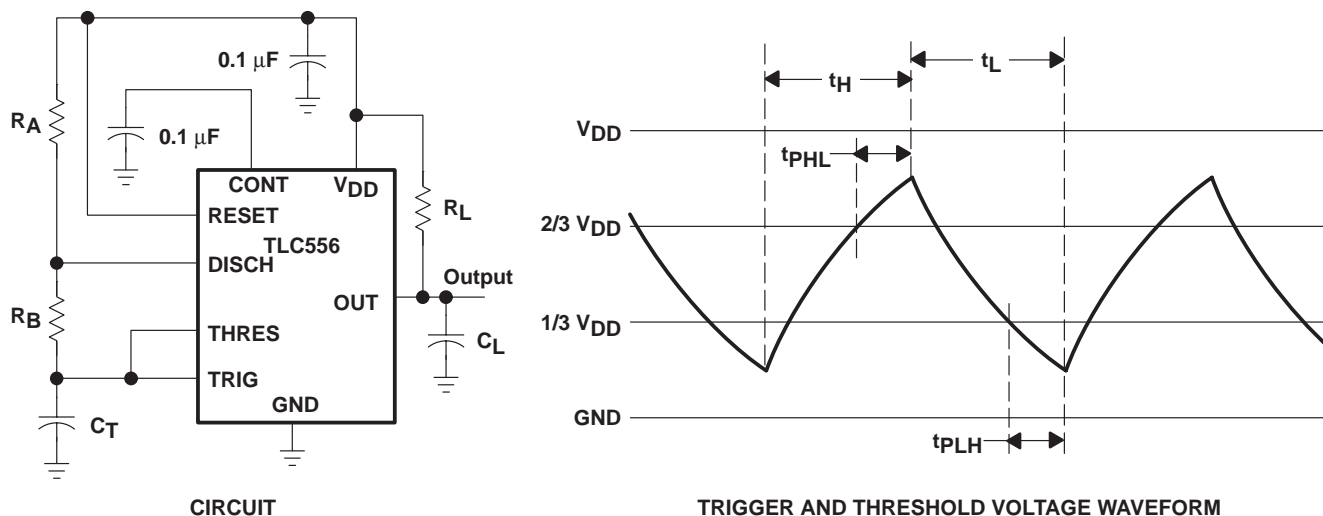


Figure 3. Astable Operation

Connecting the trigger input to the threshold input, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the threshold voltage level (approximately $0.67 V_{DD}$) and then discharges through R_B only to the value of the trigger voltage level (approximately $0.33 V_{DD}$). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A , and R_B , and C_T , as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \quad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1- μF capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})}\right) \right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)}\right) \right] + t_{PLH}$$

APPLICATION INFORMATION

The preceding equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between $\ln 2$ at low frequencies and $\ln 3$ at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_H}{t_H + t_L}$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500- μ A bias provides good results.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|------------------------------|-------------------------|
| 5962-89503022A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-89503022A TLC556MFKB | Samples |
| 5962-8950302CA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8950302CA TLC556MJB | Samples |
| TLC556CD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC556C | Samples |
| TLC556CDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC556C | Samples |
| TLC556CN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | | TLC556CN | Samples |
| TLC556ID | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC556I | Samples |
| TLC556IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLC556I | Samples |
| TLC556IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | | TLC556IN | Samples |
| TLC556MD | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC556M | Samples |
| TLC556MDG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TLC556M | Samples |
| TLC556MDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC556M | Samples |
| TLC556MFKB | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-89503022A TLC556MFKB | Samples |
| TLC556MJ | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | TLC556MJ | Samples |
| TLC556MJB | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8950302CA TLC556MJB | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC556, TLC556M :

● Catalog : [TLC556](#)

● Military : [TLC556M](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLC556CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC556IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLC556CDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TLC556IDR | SOIC | D | 14 | 2500 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-89503022A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TLC556CD | D | SOIC | 14 | 50 | 505.46 | 6.76 | 3810 | 4 |
| TLC556CD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| TLC556CN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TLC556ID | D | SOIC | 14 | 50 | 505.46 | 6.76 | 3810 | 4 |
| TLC556IN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TLC556MD | D | SOIC | 14 | 50 | 505.46 | 6.76 | 3810 | 4 |
| TLC556MDG4 | D | SOIC | 14 | 50 | 505.46 | 6.76 | 3810 | 4 |
| TLC556MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G



J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

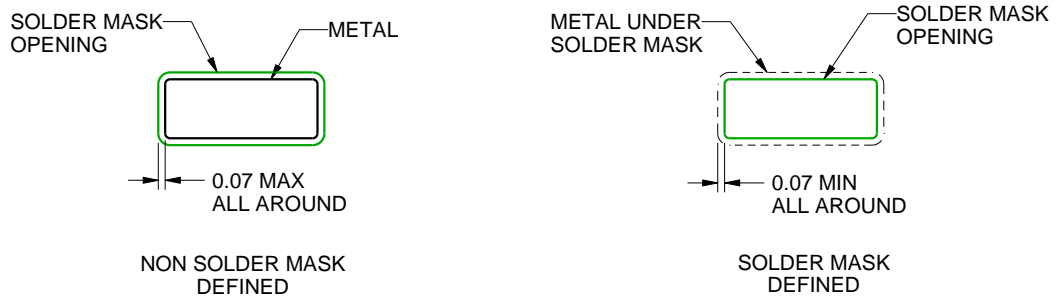
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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