Current-Limited, Power-Distribution Switches

1 Features

- Output discharge function
- 70mΩ high-side MOSFET
- 1A continuous current
- Thermal and short-circuit protection
- Accurate current limit (1.1A min, 1.9A max)
- Operating range: 2.7V to 5.5V
- 0.6ms typical rise time
- Undervoltage lockout
- Deglitched fault report ($\overline{OC}$)
- No $\overline{OC}$ glitch during power up
- 1µA maximum standby supply current
- Ambient temperature range: -40°C to 85°C
- ESD protection

2 Applications

- Heavy capacitive loads
- Short-circuit protections

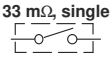
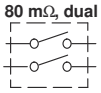
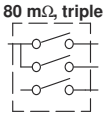
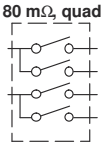
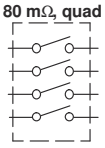
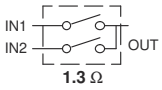
3 Description

The TPS206x-1 power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7V.

These switches provide a discharge function that provides a controlled discharge of the output voltage stored on the output capacitor.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1.5A typically.

GENERAL SWITCH CATALOG

33 mΩ, single			80 mΩ, dual			80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
	TPS201xA	0.2 A – 2 A		TPS2042B	500 mA				
	TPS202x	0.2 A – 2 A		TPS2052B	500 mA				
	TPS203x	0.2 A – 2 A		TPS2046	250 mA	TPS2080	500 mA	TPS2044B	500 mA
				TPS2056	250 mA	TPS2081	500 mA	TPS2054B	500 mA
				TPS2062	1 A	TPS2082	500 mA	TPS2048	250 mA
				TPS2066	1 A	TPS2090	250 mA	TPS2058	250 mA
				TPS2060	1.5 A	TPS2091	250 mA		
				TPS2064	1.5 A	TPS2092	250 mA		
80 mΩ, single			**260 mΩ**				TPS2043B	500 mA	TPS2085	500 mA
	TPS2014	600 mA		TPS2100/1			TPS2053B	500 mA	TPS2086	500 mA
	TPS2015	1 A		IN1	500 mA		TPS2047	250 mA	TPS2087	500 mA
	TPS2041B	500 mA		IN2	10 mA		TPS2057	250 mA	TPS2095	250 mA
	TPS2051B	500 mA		TPS2102/3/4/5					TPS2096	250 mA
	TPS2045	250 mA		IN1	500 mA				TPS2097	250 mA
	TPS2055	250 mA		IN2	100 mA					
	TPS2061	1 A								
	TPS2065	1 A								

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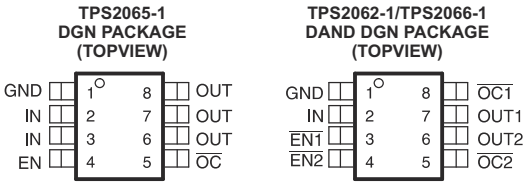
4 Pin Configuration and Functions



PIN				I/O	DESCRIPTION
NAME	TPS2065-1	TPS2062-1	TPS2066-1		
EN	4	–	–	I	Enable input, logic high turns on power switch
$\overline{EN1}$	–	3	–	I	Enable input, logic low turns on channel 1
$\overline{EN2}$	–	4	–	I	Enable input, logic high turns on channel 2
EN1	–	–	3	I	Enable input, logic high turns on channel 1
EN2	–	–	4	I	Enable input, logic high turns on channel 2
GND	1	1	1		Ground connection
IN	2, 3	2	2	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible
$\overline{OC}$	5	–	–	O	Active-low open-drain output, asserted during over-current
$\overline{OC1}$	–	8	8	O	Active-low open-drain output, asserted during over-current for channel 1
$\overline{OC2}$		5	5	O	Active-low open-drain output, asserted during over-current for channel 2
OUT	6, 7, 8	–	–	O	Power-switch output
OUT1	–	7	7	O	Power-switch output for channel 1
OUT2	–	6	6	O	Power-switch output for channel 2

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Input voltage range, $V_{I(IN)}$ (2)		–0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (2), $V_{O(OUTx)}$		-0.3 V to 6 V
Input voltage range, $V_{I(\overline{EN})}$, $V_{I(EN)}$, $V_{I(\overline{ENx})}$, $V_{I(ENx)}$		–0.3 V to 6 V
Voltage range, $V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$		–0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$		Internally limited
Operating virtual junction temperature range, T_J		-40°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Electrostatic discharge (ESD) protection	Human body model MIL-STD-883C	2 kV
	Charge device model (CDM)	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

5.2 Recommended Operating Conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$	2.7	5.5	V
Input voltage, $V_{I(\overline{EN})}$, $V_{I(EN)}$, $V_{I(\overline{ENx})}$, $V_{I(ENx)}$	0	5.5	V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$	0	1	A
Steady state current through discharge. Device disabled, measured through output pin(s)		8	mA
Operating virtual junction temperature, T_J	-40	125	°C

5.3 Thermal Information

THERMAL METRIC(1)		D (SOIC)	DGN (HVSSOP)	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.3	53.6	°C/W°
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	58.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	35.5	
ψ_{JT}	Junction-to-top characterization parameter	20.3	2.7	
ψ_{JB}	Junction-to-board characterization parameter	59.1	35.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.7	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Electrical Characteristics

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
POWER SWITCH						
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 1 A, –40°C ≤ T_J ≤ 125°C		70	135	mΩ
	Static drain-source on-state resistance, 2.7-V operation (2)	$V_{I(IN)}$ = 2.7 V, I_O = 1 A, -40°C ≤ T_J ≤ 125°C		75	150	mΩ

5.4 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
t_r [2]	Rise time, output	$V_{I(IN)}$ = 5.5 V	C_L = 1 µF, R_L = 5 Ω, T_J = 25°C		0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V			0.4	1	
t_f [2]	Fall time, output	$V_{I(IN)}$ = 5.5 V		0.05		0.5	
		$V_{I(IN)}$ = 2.7 V		0.05		0.5	
ENABLE INPUT $\overline{EN}$ OR EN							
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤5.5 V		2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V				0.8	
I_I	Input current	$V_{I(\overline{ENx})}$ = 0 V or 5.5 V, $V_{I(ENx)}$ = 0 V or 5.5 V		-0.5		0.5	µA
t_{on} [2]	Turnon time	C_L = 100 µF, R_L = 5 Ω				3	ms
t_{off} [2]	Turnoff time	C_L = 100 µF, R_L = 5 Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit	T_J = 25°C	1.1	1.5	1.9	A
			-40°C ≤ T_J ≤ 125°C	1.1	1.5	2.1	
I_{OC} [2] [4]	Overcurrent trip threshold	$V_{I(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT	TPS2062-1, TPS2065-1		2.4	3	A
SUPPLY CURRENT (TPS2065-1)							
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.5	1	µA
			-40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	T_J = 25°C		43	60	µA
			-40°C ≤ T_J ≤ 125°C		43	70	
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground[2]	T_J = 25°C		0		µA
SUPPLY CURRENT (TPS2062-1)							
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.5	1	µA
			-40°C ≤ T_J ≤ 125°C		0.5	20	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	T_J = 25°C		50	70	µA
			-40°C ≤ T_J ≤ 125°C		50	90	
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground[2]	T_J = 25°C		0.2		µA
SUPPLY CURRENT (TPS2066-1)							
Supply current, low-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.5	1	µA
			-40°C ≤ T_J ≤ 125°C		0.5	20	
Supply current, high-level output		No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	T_J = 25°C		95	120	µA
			-40°C ≤ T_J ≤ 125°C		95	120	
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground[2]	T_J = 25°C		0.2		µA

5.4 Electrical Characteristics (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT (TPS2062-1 and TPS2065-1)					
Low-level input voltage, IN		2		2.5	V
Hysteresis, IN	T_J = 25°C		75		mV
UNDERVOLTAGE LOCKOUT (TPS2066-1)					
Low-level input voltage, IN		2		2.6	V
Hysteresis, IN	T_J = 25°C		75		mV
OVERCURRENT $\overline{OC1}$ and $\overline{OC2}$					
Output low voltage, $V_{OL(OCx)}$	$I_{O(\overline{OCx})}$ = 5 mA			0.4	V
Off-state current[2]	$V_{O(\overline{OCx})}$ = 5 V or 3.3 V			1	µA
$\overline{OC}$ deglitch[2]	$\overline{OCx}$ assertion or deassertion	4	8	15	ms
Discharge resistance	V_{CC} = 5 V, disabled, I_O = 1 mA		100		Ω
THERMAL SHUTDOWN[3]					
Thermal shutdown threshold[2]		135			°C
Recovery from thermal shutdown[2]		125			°C
Hysteresis[2]			10		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design.
(3) The thermal shutdown only reacts under overcurrent conditions.
(4) TPS2066-1 does not have overcurrent trip threshold. Current limit is defined by I_{OS}. See Section 7.7 for more details.

5.5 Typical Characteristics

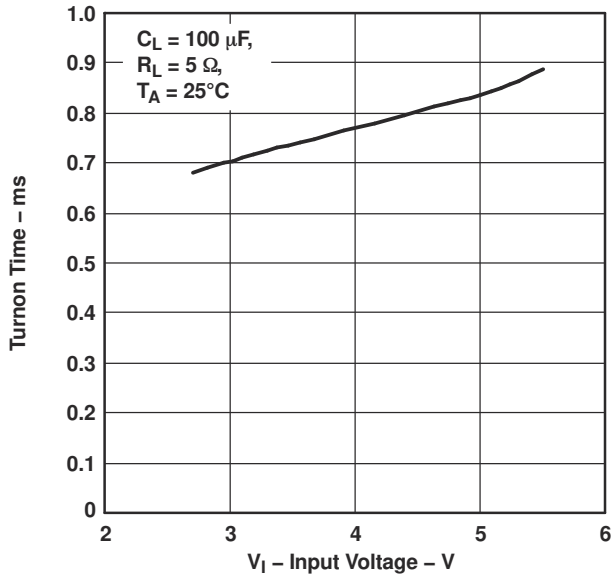


Figure 5-1. TURNON TIME vs INPUT VOLTAGE

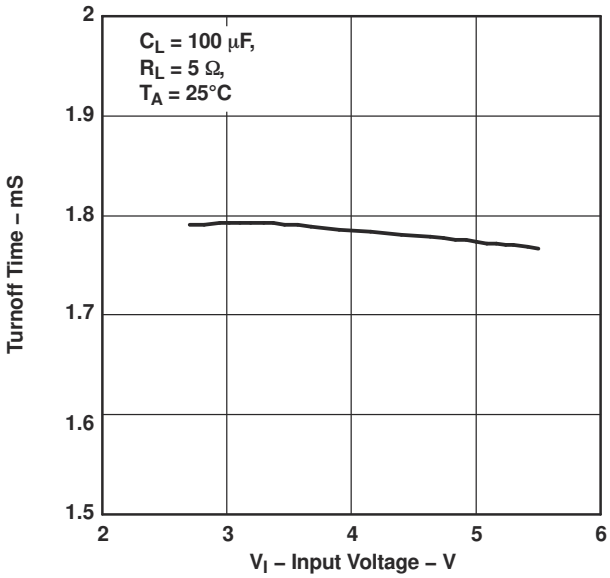


Figure 5-2. TURNOFF TIME vs INPUT VOLTAGE

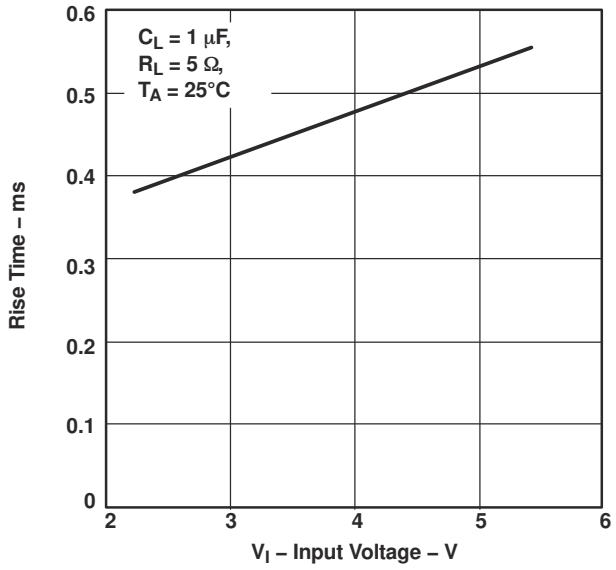


Figure 5-3. RISE TIME vs INPUT VOLTAGE

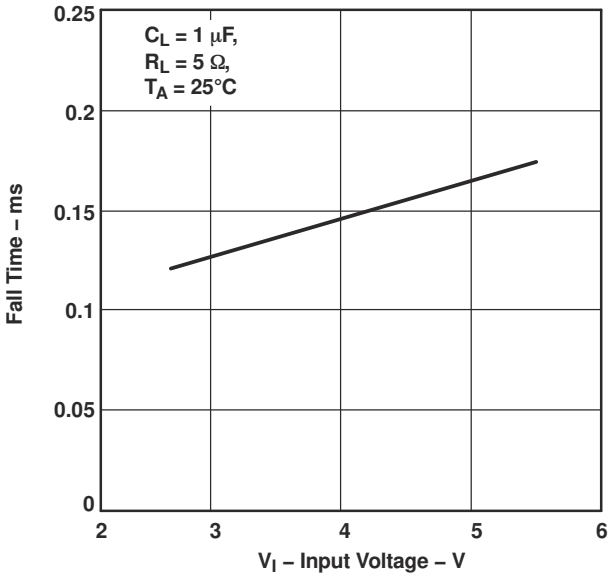


Figure 5-4. FALL TIME vs INPUT VOLTAGE

5.5 Typical Characteristics (continued)

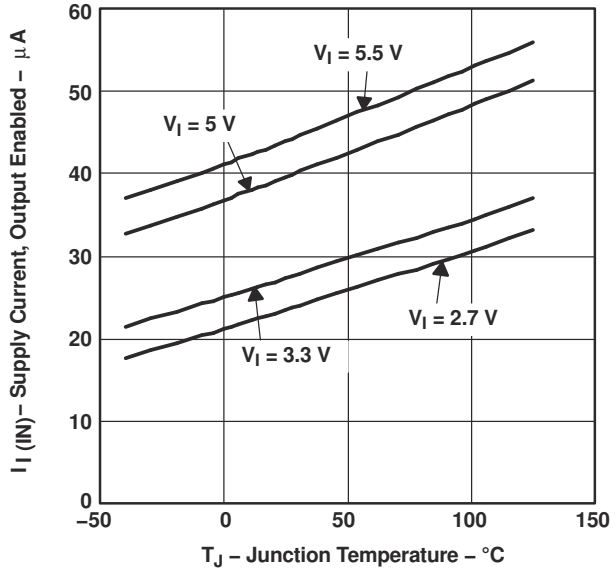


Figure 5-5. TPS2061, TPS2065-1 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

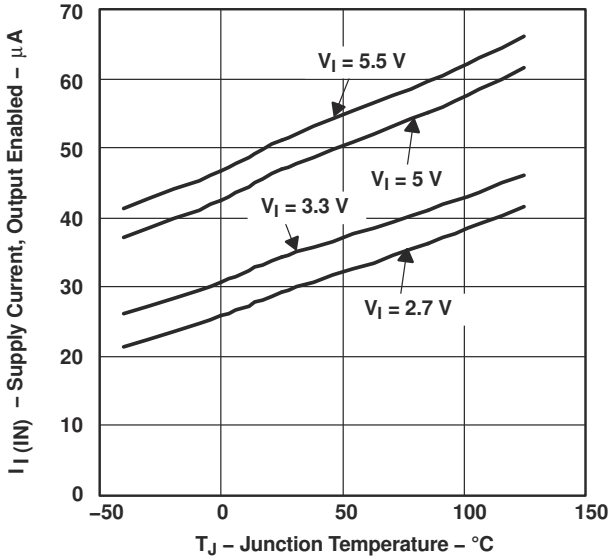


Figure 5-6. TPS2062-1, TPS2066-1 SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

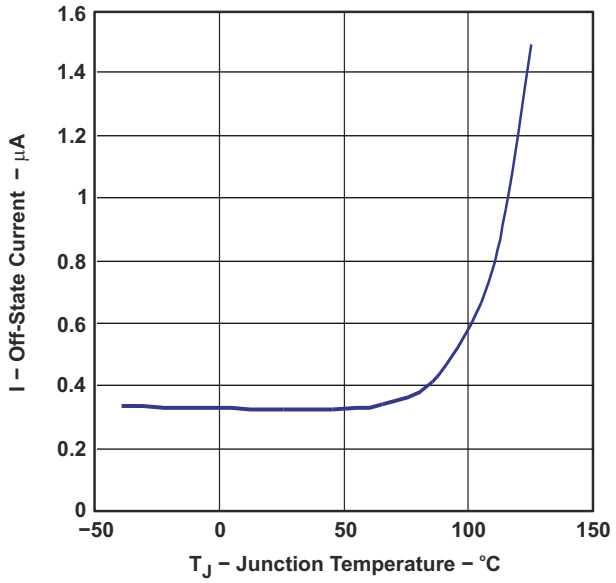


Figure 5-7. TPS2065-1 SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

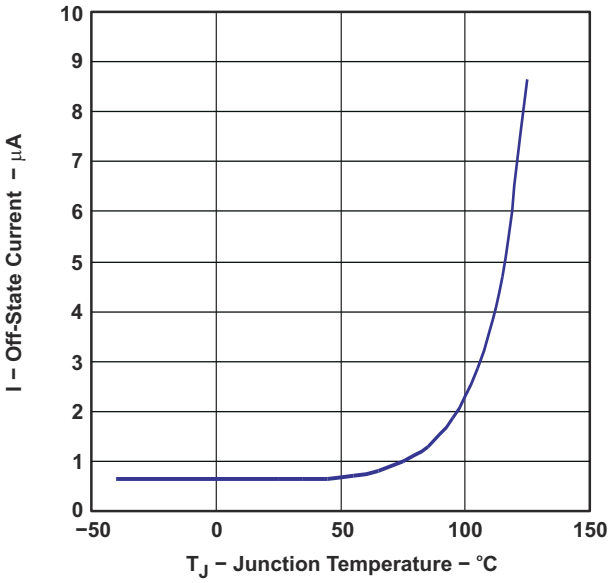


Figure 5-8. TPS2062-1, TPS2066-1 SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

5.5 Typical Characteristics (continued)

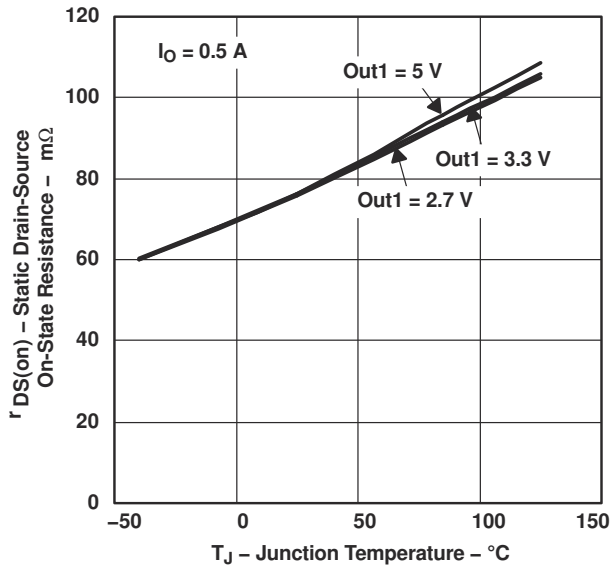


Figure 5-9. STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

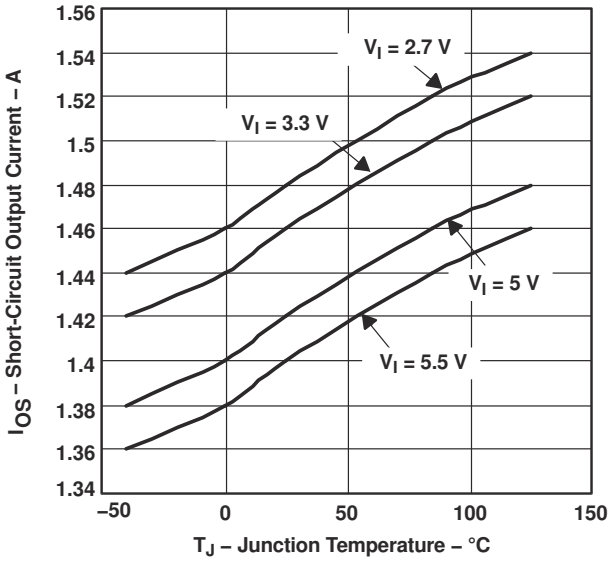


Figure 5-10. SHORT-CIRCUIT OUTPUT CURRENT vsJUNCTION TEMPERATURE

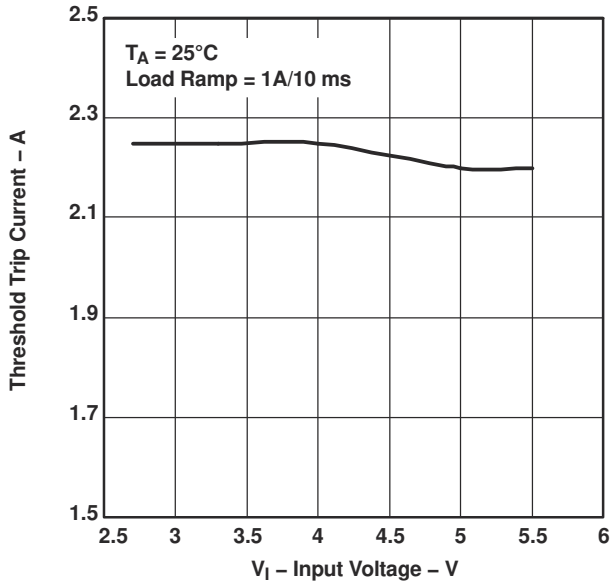


Figure 5-11. THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

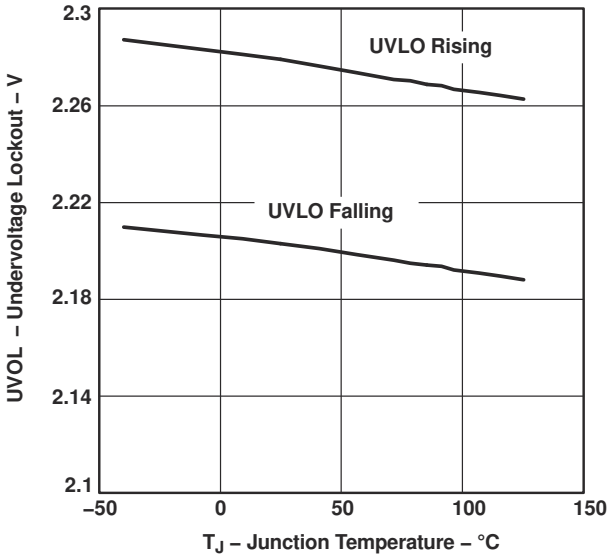


Figure 5-12. UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE

5.5 Typical Characteristics (continued)

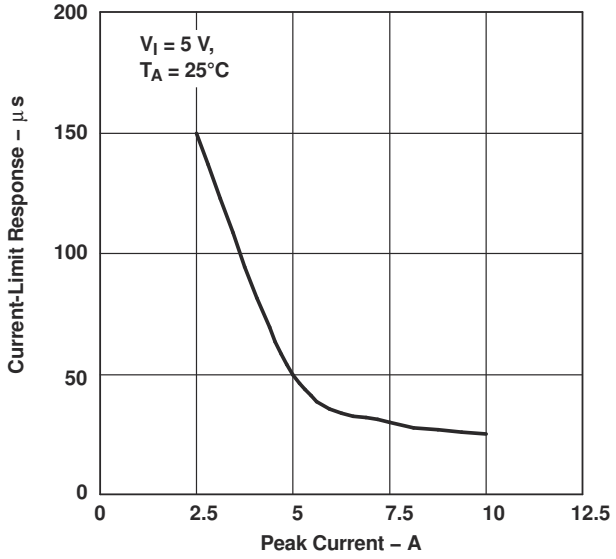


Figure 5-13. CURRENT-LIMIT RESPONSE vs PEAK CURRENT

6 Parameter Measurement Information

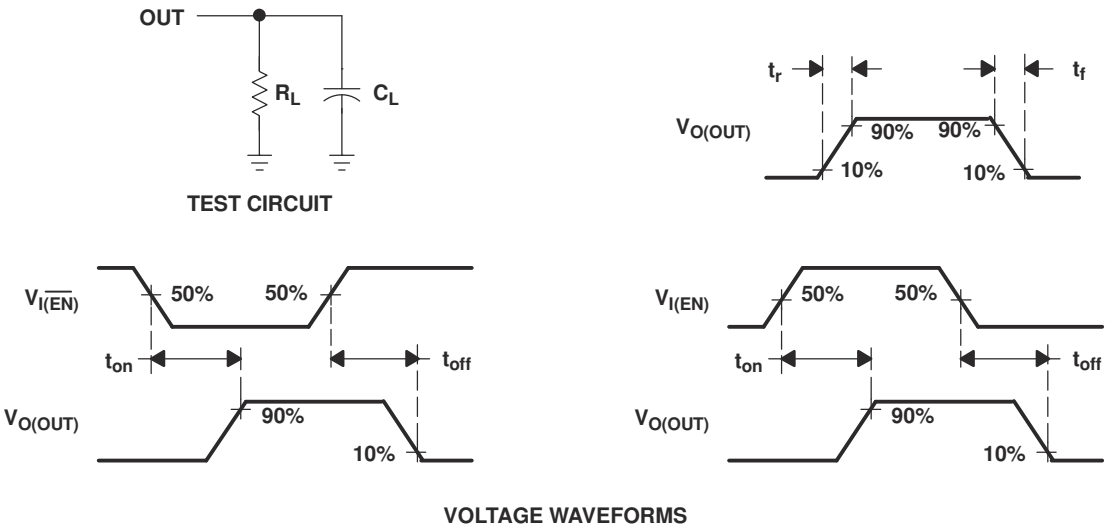


Figure 6-1. Test Circuit and Voltage Waveforms

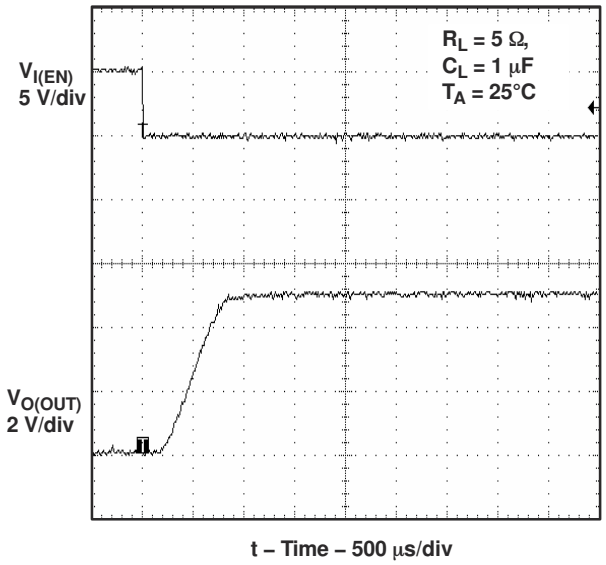


Figure 6-2. Turnon Delay and Rise Time With 1-µF Load

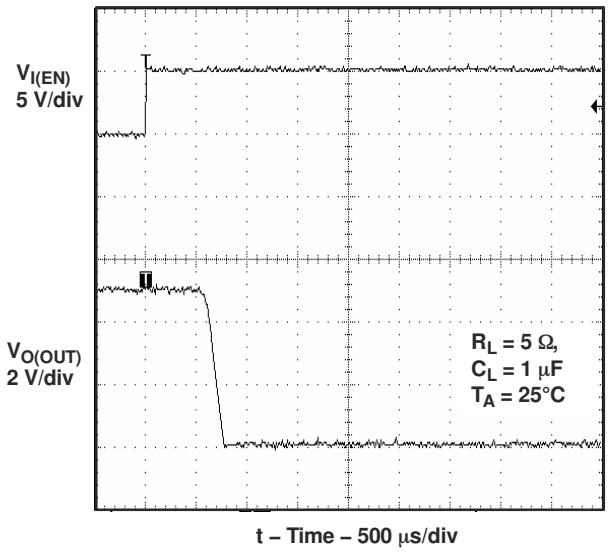


Figure 6-3. Turnoff Delay and Fall Time With 1-µF Load

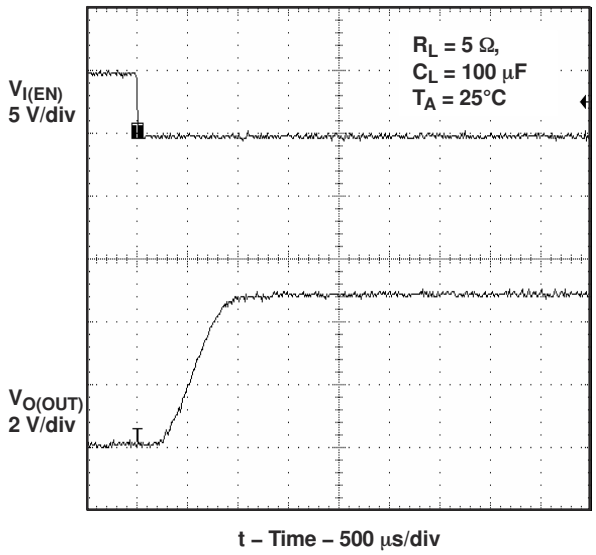


Figure 6-4. Turnon Delay and Rise Time With 100-µF Load

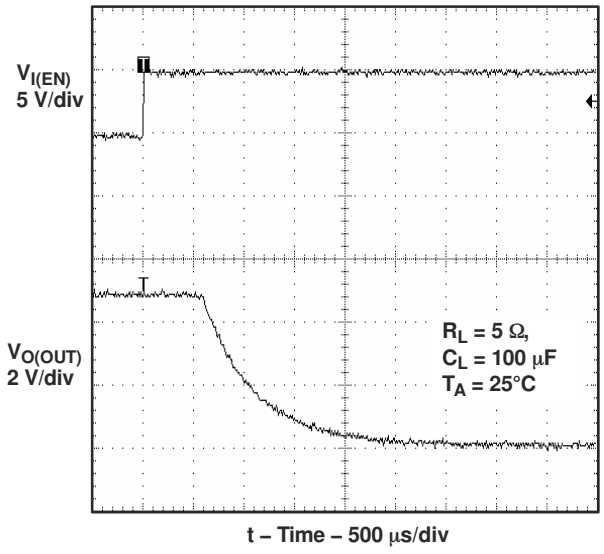


Figure 6-5. Turnoff Delay and Fall Time With 100-µF Load

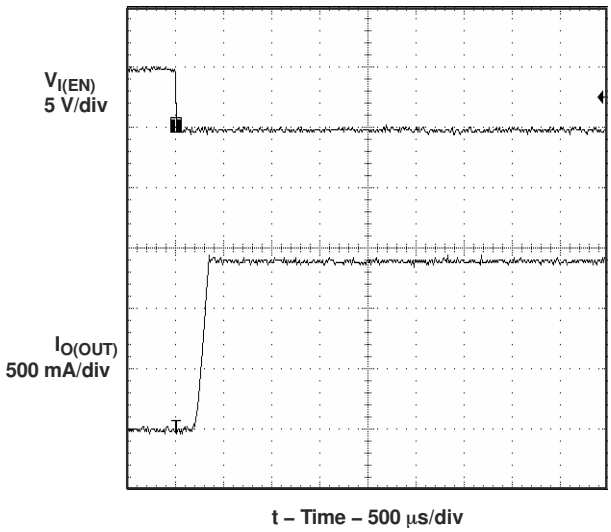


Figure 6-6. Short-Circuit Current, Device Enabled Into Short

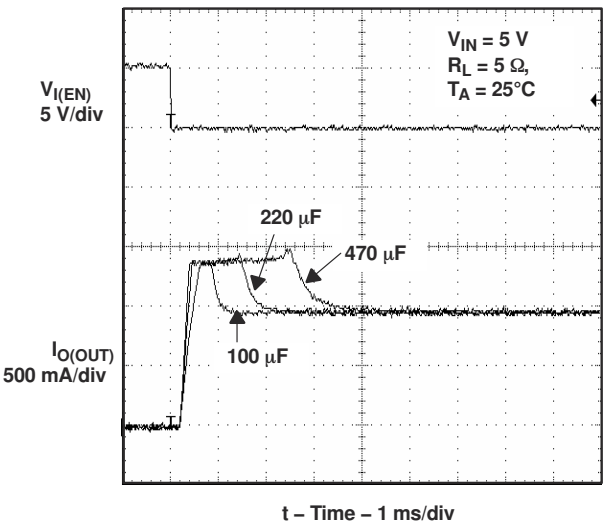


Figure 6-7. Inrush Current With Different Load Capacitance

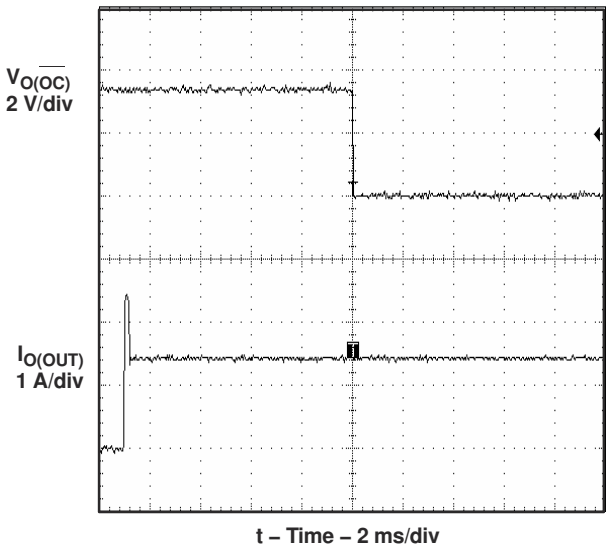


Figure 6-8. 2-Ω Load Connected to Enabled Device

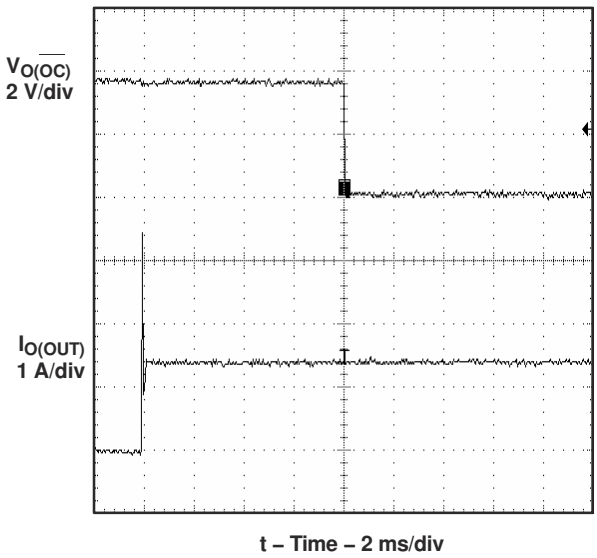
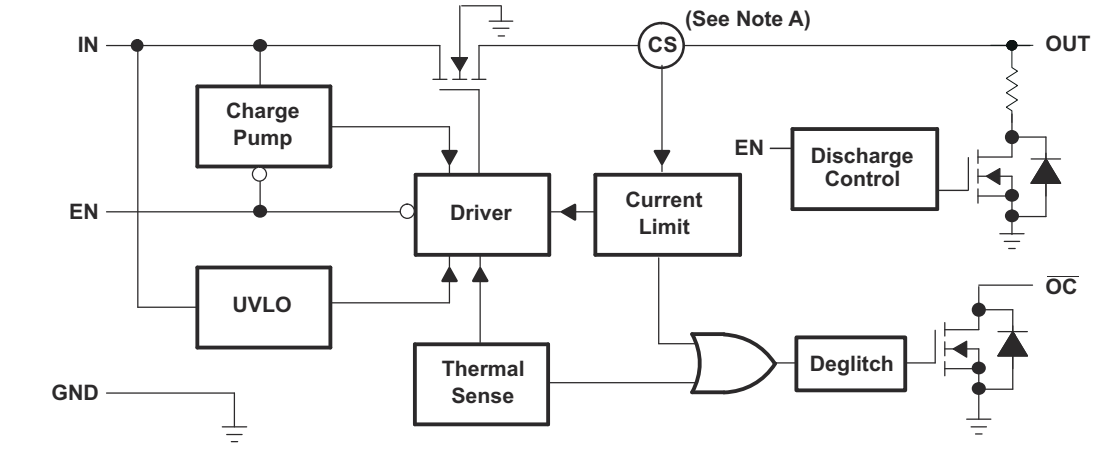


Figure 6-9. 1-Ω Load Connected to Enabled Device

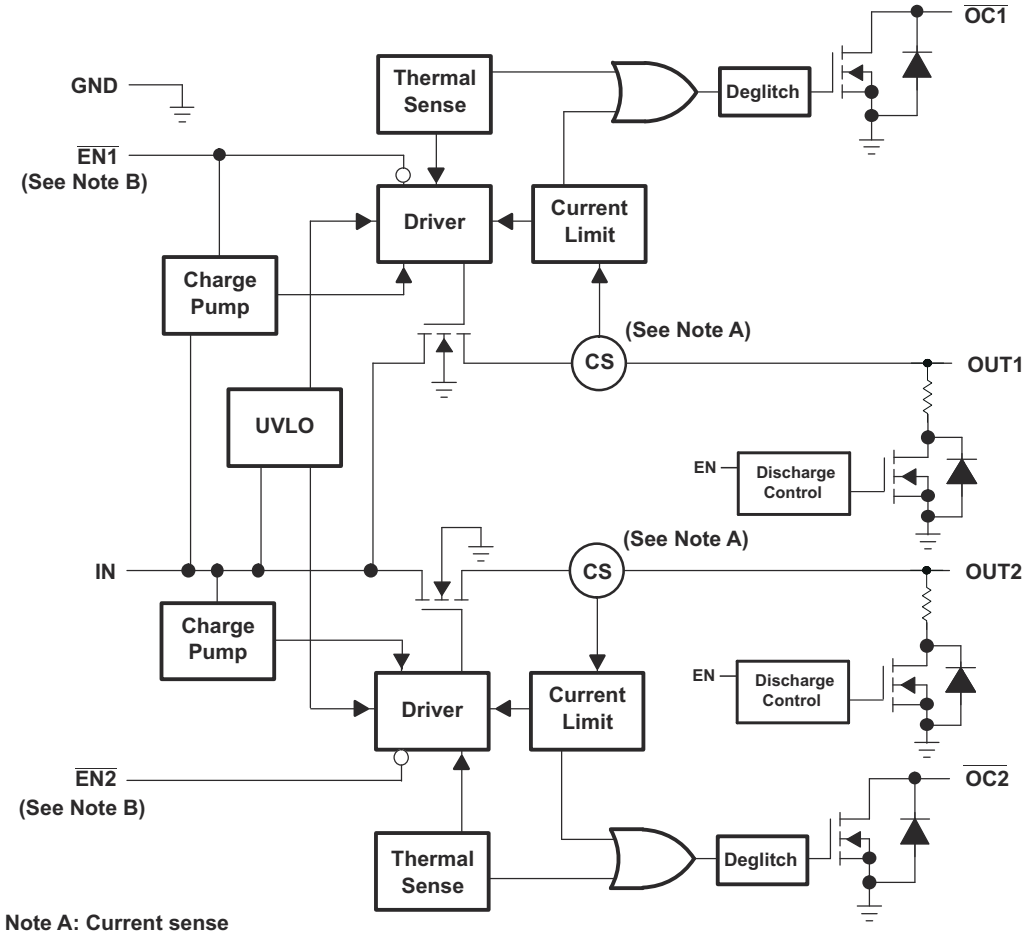
7 Detailed Description

7.1 Functional Block Diagram



Note A: Current sense

Figure 7-1. FUNCTIONAL BLOCK DIAGRAM (TPS2065-1)



Note A: Current sense
Note B: Active low (ENx) for TPS2062. Active high (ENx) for TPS2066

Figure 7-2. FUNCTIONAL BLOCK DIAGRAM (TPS2062-1 and TPS2066-1)

7.2 Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1 A.

7.3 Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

7.4 Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

7.5 Enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{\text{ENx}}$, or when a logic low is present on ENx. A logic zero input on $\overline{\text{ENx}}$, or a logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

7.6 Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

7.7 Overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

There are two kinds of current limit profiles for the TPS206x-1 devices.

The TPS2062-1 and TPS2065-1 have an output I vs V characteristic similar to the plot labeled **Current Limit with Peaking** in Figure 7-3. This type of limiting can be characterized by two parameters, the overcurrent trip threshold (I_{OC}), and the short-circuit output current threshold (I_{OS}).

The TPS2066-1 has an output I vs V characteristic similar to the plot labeled **Flat Current Limit** in Figure 7-3. This type of limiting can be characterized by one parameters, the short circuit current (I_{OS}).

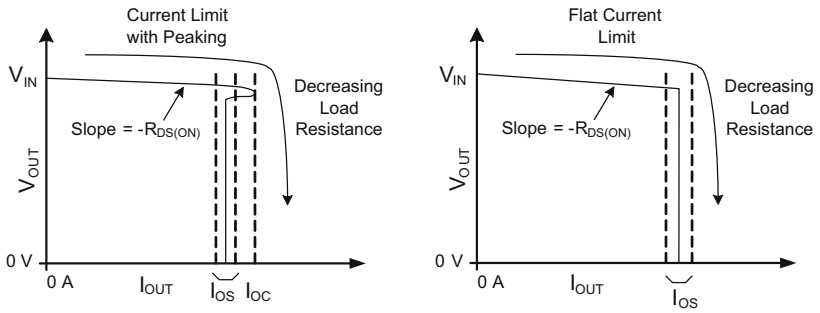


Figure 7-3. Current Limit Profiles

7.7.1 Overcurrent Conditions (TPS2062-1 and TPS2065-1)

Three possible overload conditions can occur for the TPS2062-1 and TPS2065-1. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6-6 through Figure 6-9). The TPS2062-1 and TPS2065-1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold (I_{OC})), the device switches into constant-current mode and current is limited at the short-circuit output current threshold (I_{OS}).

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the overcurrent trip threshold (I_{OC}) is reached or until the thermal limit of the device is exceeded. The TPS2062-1 and TPS2065-1 are capable of delivering current up to the current-limit threshold without damaging the device. Once the overcurrent trip threshold (I_{OC}) has been reached, the device switches into the constant-current mode current is limited at the short-circuit output current threshold (I_{OS}).

7.7.2 Overcurrent Conditions (TPS2066-1)

Three possible overload conditions can occur for the TPS2066-1. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied. The TPS2066-1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the short-circuit output current threshold (I_{OS}) is reached, the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. After the short-circuit output current threshold (I_{OS}) is reached, the device switches into constant-current mode.

7.8 Overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

7.9 Thermal Sense

The TPS206x-1 implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

7.10 Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

7.11 Discharge Function

When the device is disabled (when enable is deasserted or during power-up power-down when V_I < UVLO) the discharge function is active. The discharge function offers a resistive discharge path for the external storage capacitor. The discharge function is suitable only to discharge filter capacitors for limited time and cannot dissipate steady state currents greater than 8 ma.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Power-Supply Considerations

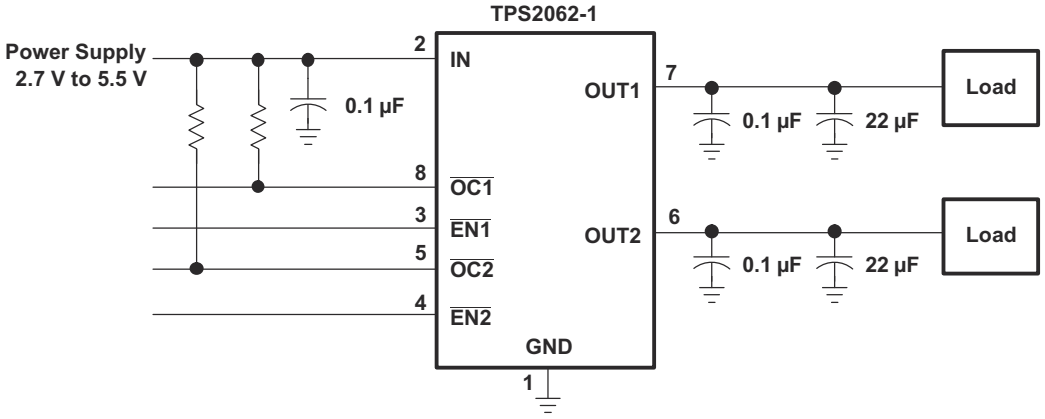


Figure 8-1. Typical Application

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

8.1.2 $\overline{OC}$ Response

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{OCx}$ occurs due to the 10-ms deglitch circuit. The TPS206x-1 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{OCx}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

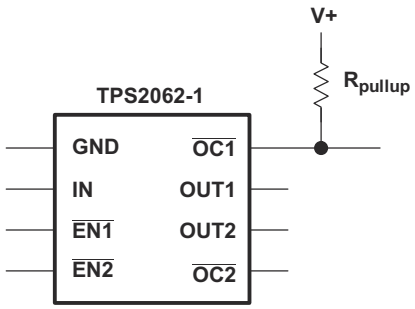


Figure 8-2. Typical Circuit for the $\overline{OC}$ Pin

8.1.3 Power Dissipation and Junction Temperature

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 5-9. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A= Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

8.1.4 Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS206x-1 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

8.1.5 Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. The UVLO facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

8.1.6 Universal Serial Bus (USB) Applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS206x-1 has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

8.1.7 Host/Self-Powered and Bus-Powered Hubs

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see Figure 8-3). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

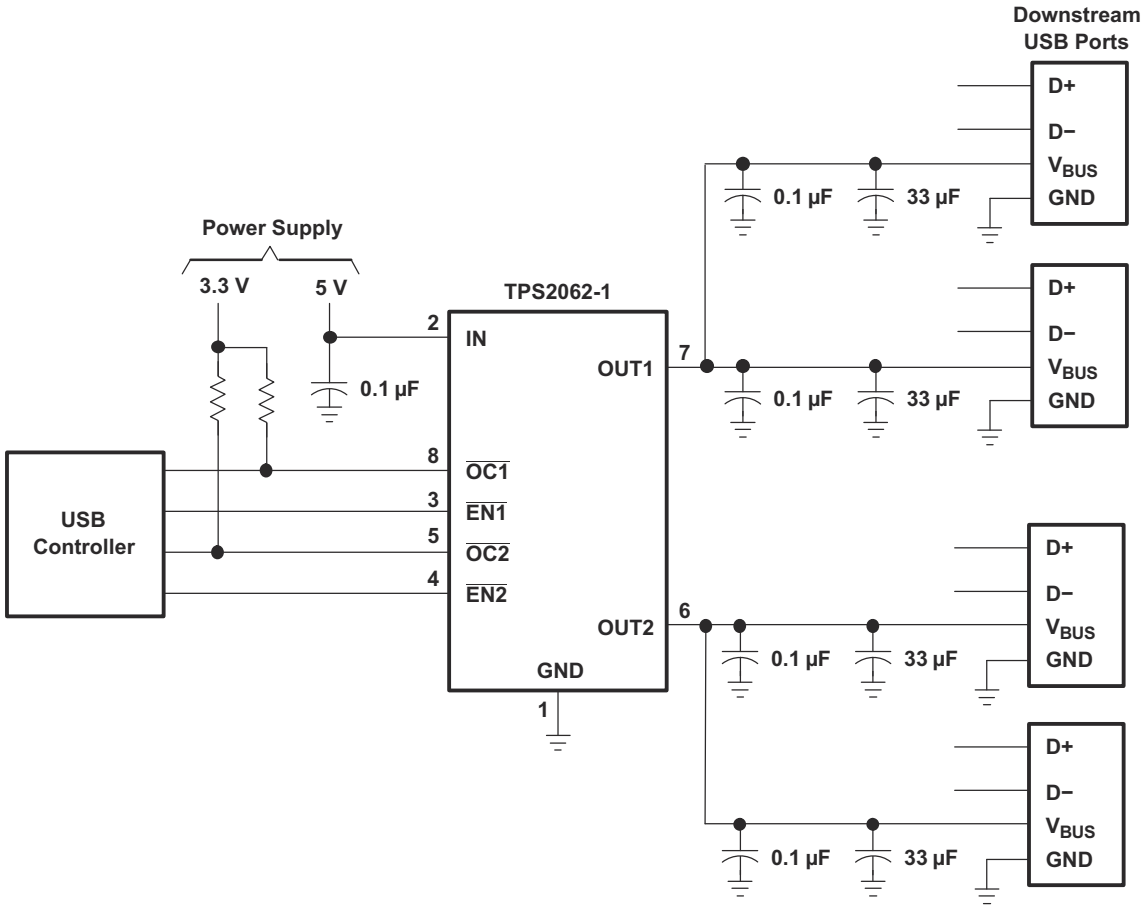


Figure 8-3. Typical Four-Port USB Host / Self-Powered Hub

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the

embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

8.1.8 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 8-4). With TPS206x-1, the internal functions draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.

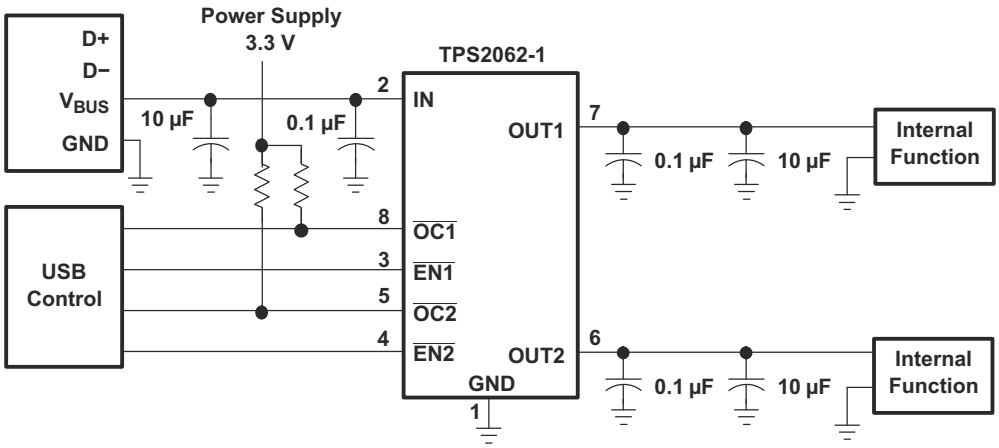


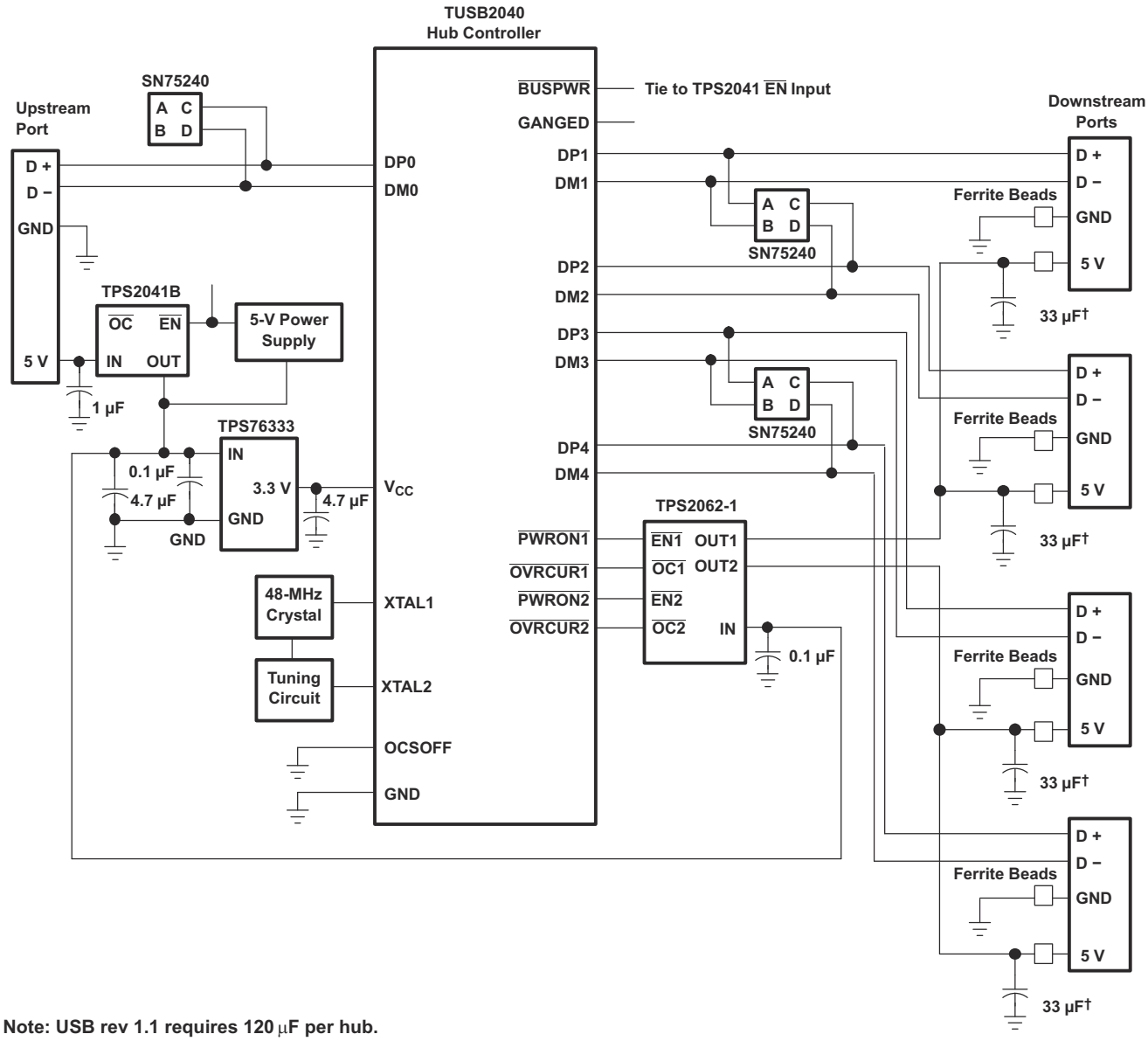
Figure 8-4. High-Power Bus-Powered Function

8.1.9 USB Power-Distribution Requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS206x-1 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 8-5).



Note: USB rev 1.1 requires 120 µF per hub.

Figure 8-5. Hybrid Self / Bus-Powered Hub Implementation

8.1.10 Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS206x-1, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS206x-1 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

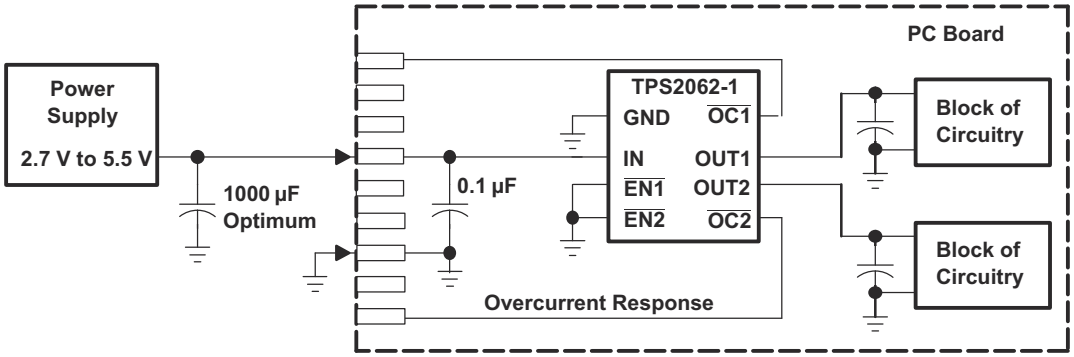


Figure 8-6. Typical Hot-Plug Implementation

By placing the TPS206x-1 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.2 Documentation Support

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2009) to Revision B (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Deleted Dissipation Ratings table	1
• Thermal Information of new needle respin, TPS2066DGNR-1	4
• Added Thermal Information table	4
• Updated max UVLO value for TPS2066-1	4
• Updated max Supply current, high-level output for TPS2066-1	4
• Updated Overcurrent trip threshold to apply only to TPS2062-1 and TPS2065-1	4
• Updated section information	15
• Added Section 7.7.1	16
• Added Section 7.7.2	16

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2062D-1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062-1	Samples
TPS2062DR-1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062-1	Samples
TPS2065DGNR-1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2065 -1	Samples
TPS2066DGN-1	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2066 -1	
TPS2066DGNR-1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066 -1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS2062-1, TPS2065-1, TPS2066-1 :

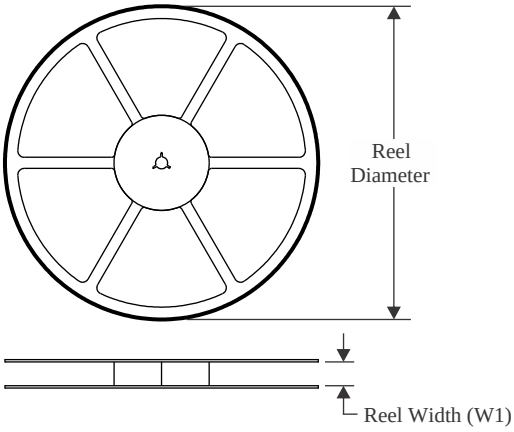
- Automotive : TPS2062-Q1, TPS2065-Q1, TPS2066-Q1

NOTE: Qualified Version Definitions:

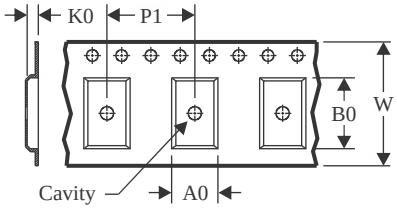
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

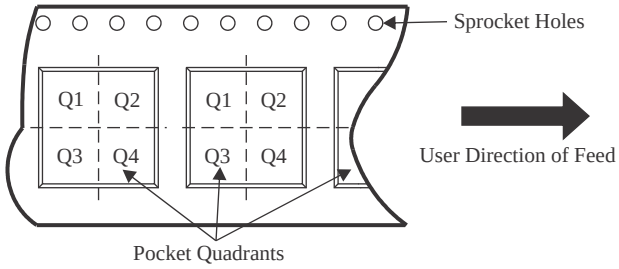


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

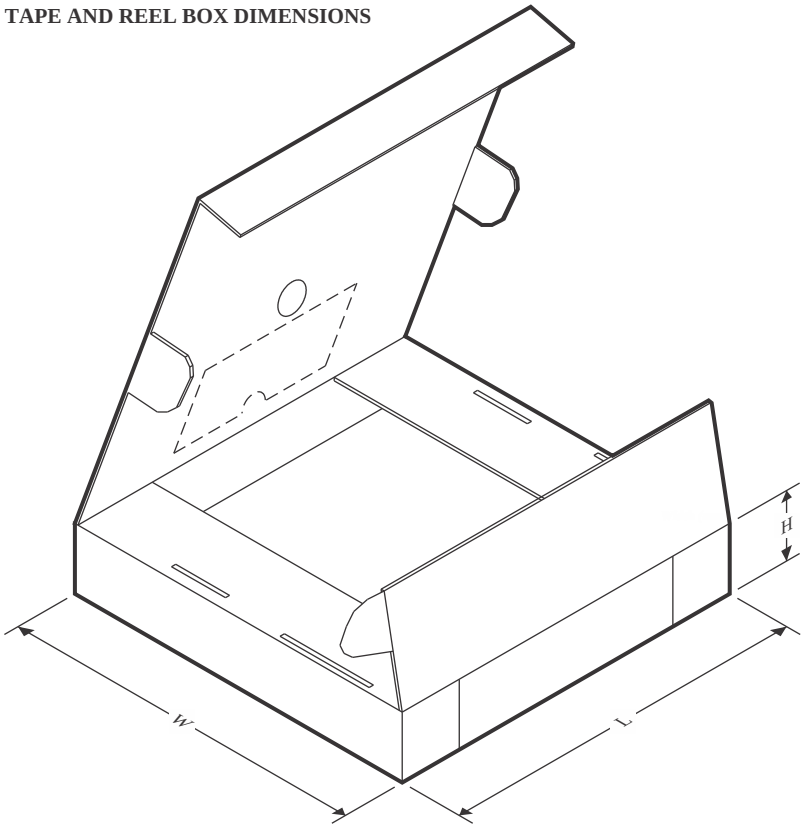
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2062DR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2065DGNR-1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065DGNR-1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS2066DGNR-1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

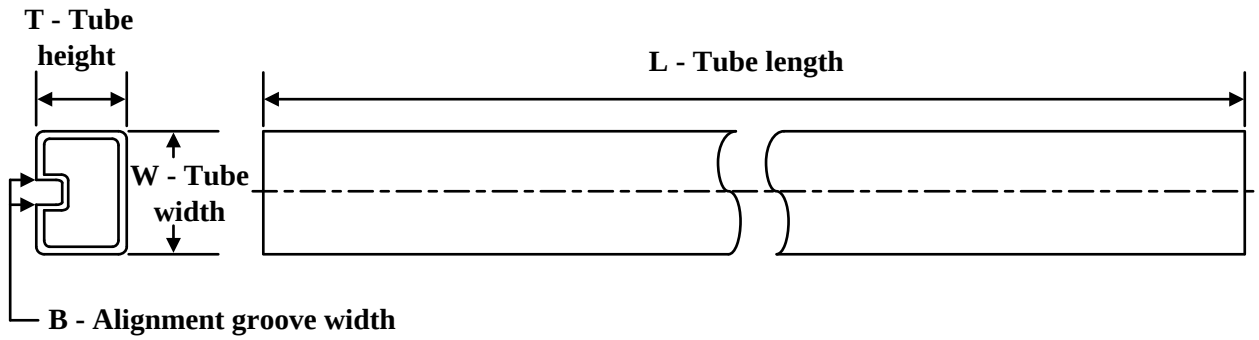
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2062DR-1	SOIC	D	8	2500	340.5	338.1	20.6
TPS2065DGNR-1	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2065DGNR-1	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS2066DGNR-1	HVSSOP	DGN	8	2500	346.0	346.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2062D-1	D	SOIC	8	75	507	8	3940	4.32
TPS2066DGN-1	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066DGN-1	DGN	HVSSOP	8	80	322	6.55	1000	3.01

GENERIC PACKAGE VIEW

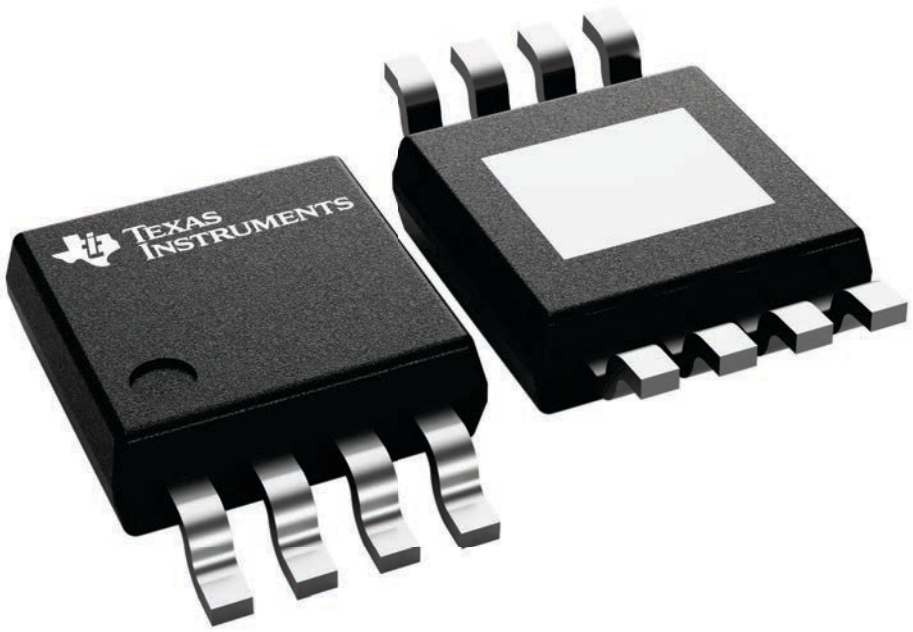
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

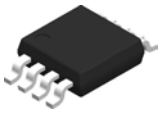
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

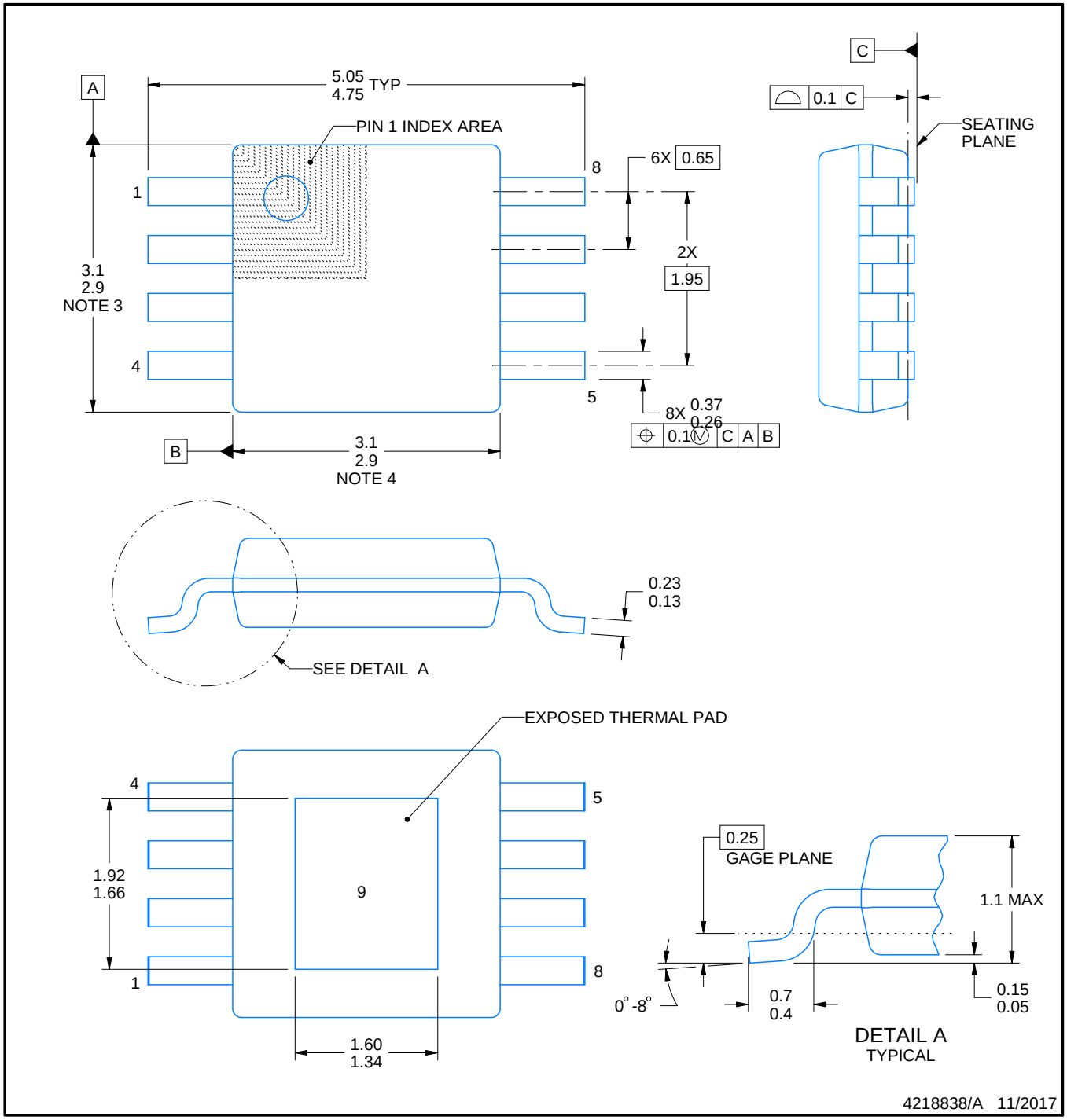
PACKAGE OUTLINE

DGN0008C



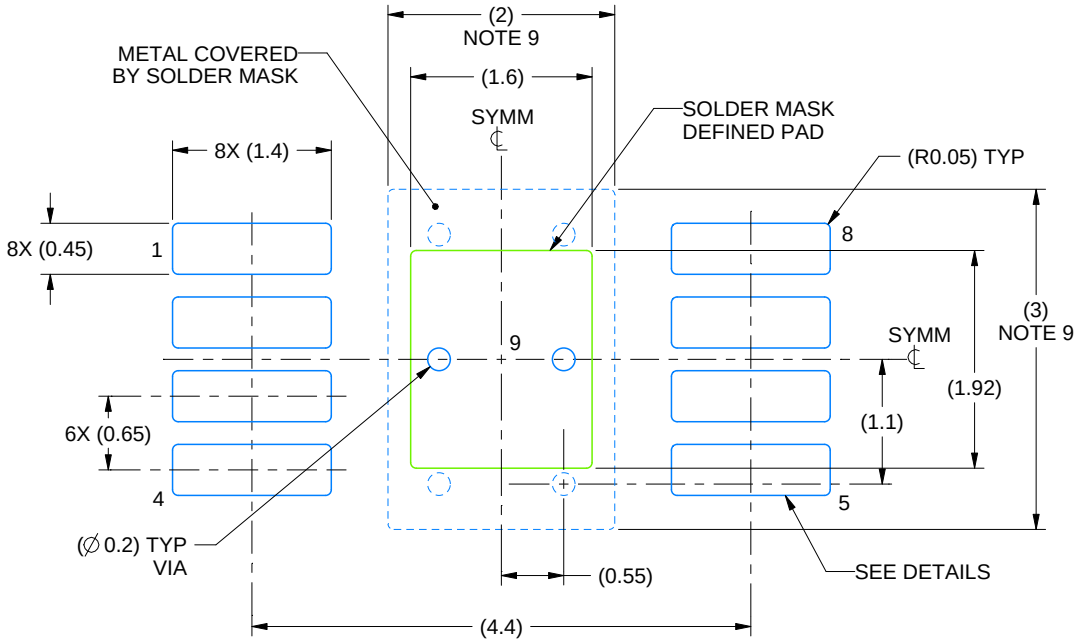
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

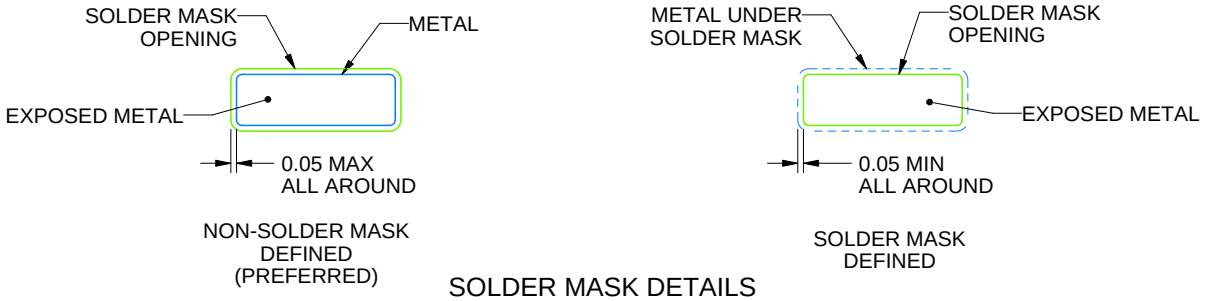


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

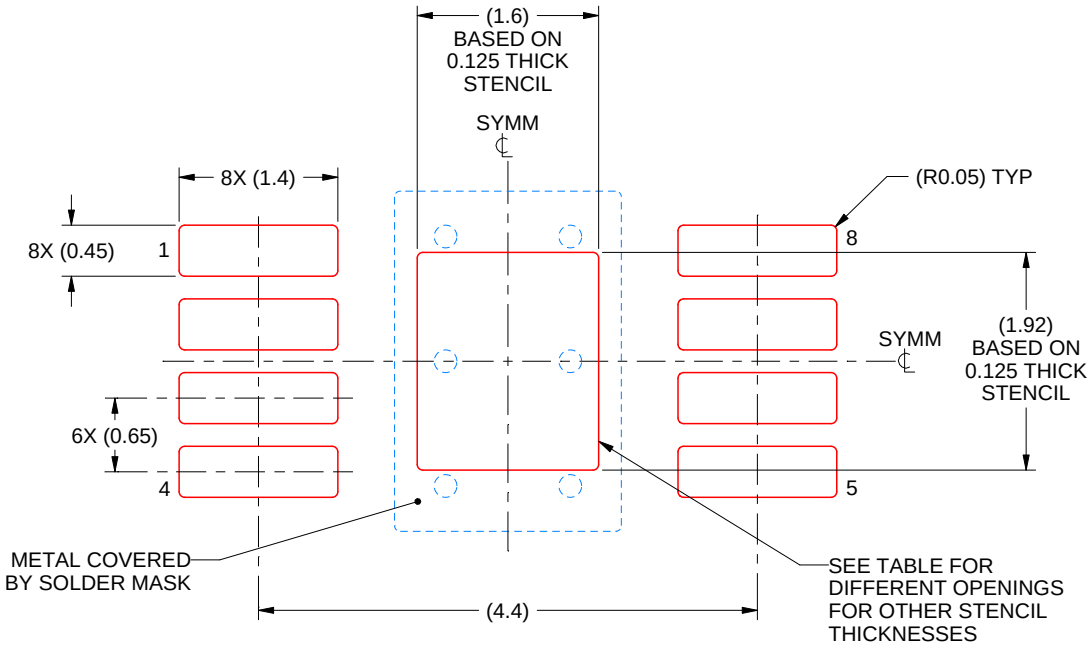


SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

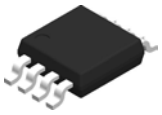
4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

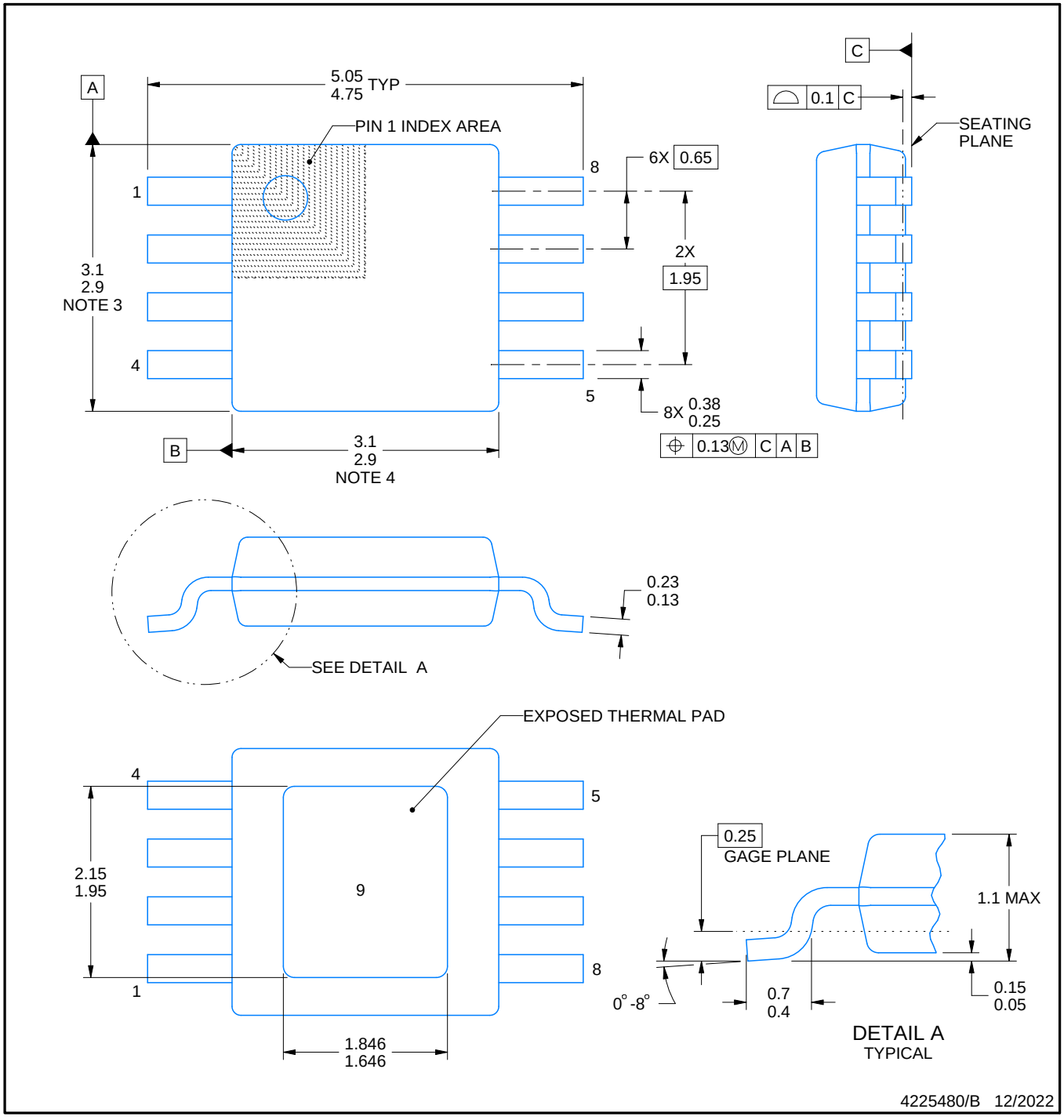
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

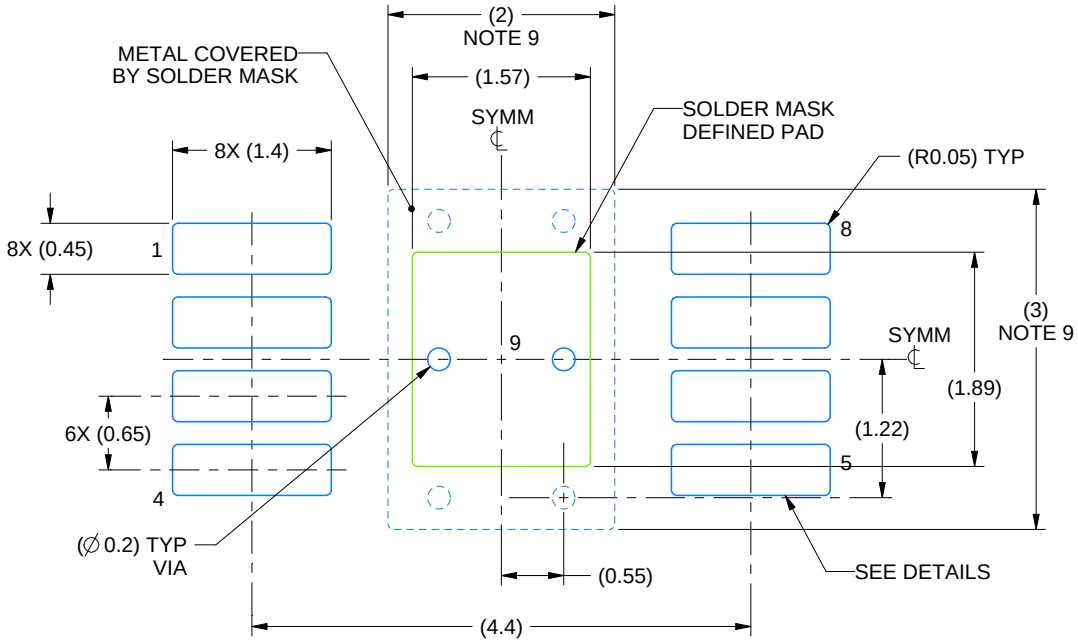
SMALL OUTLINE PACKAGE



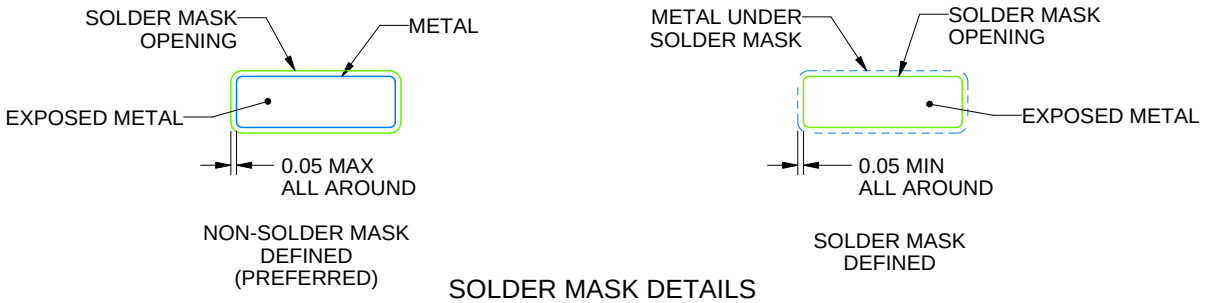
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

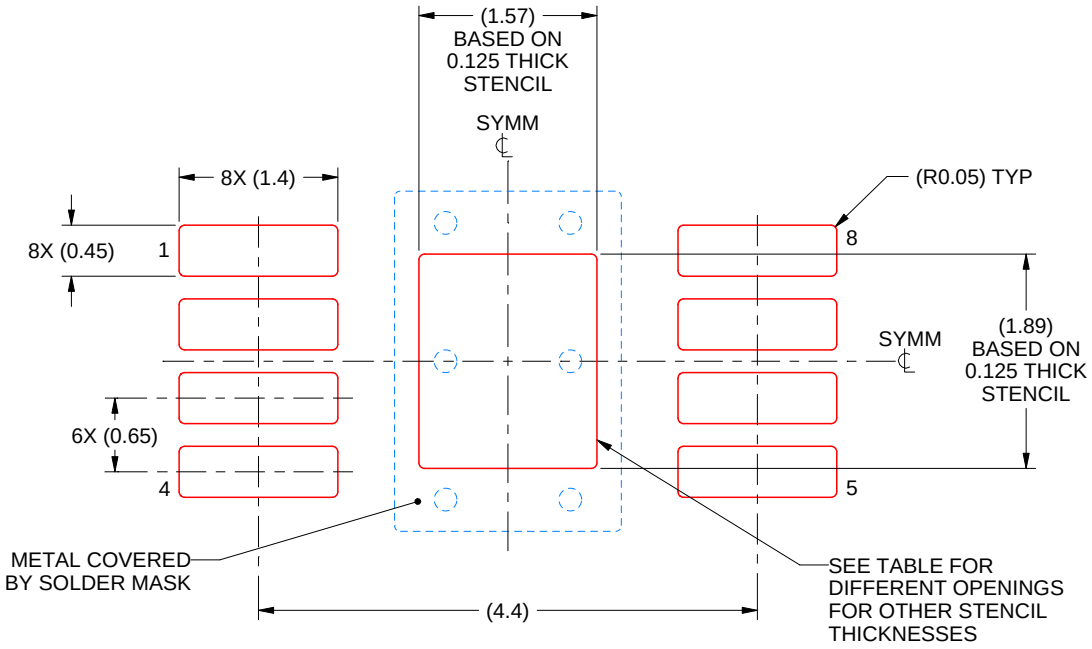


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



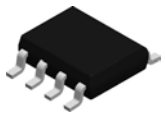
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

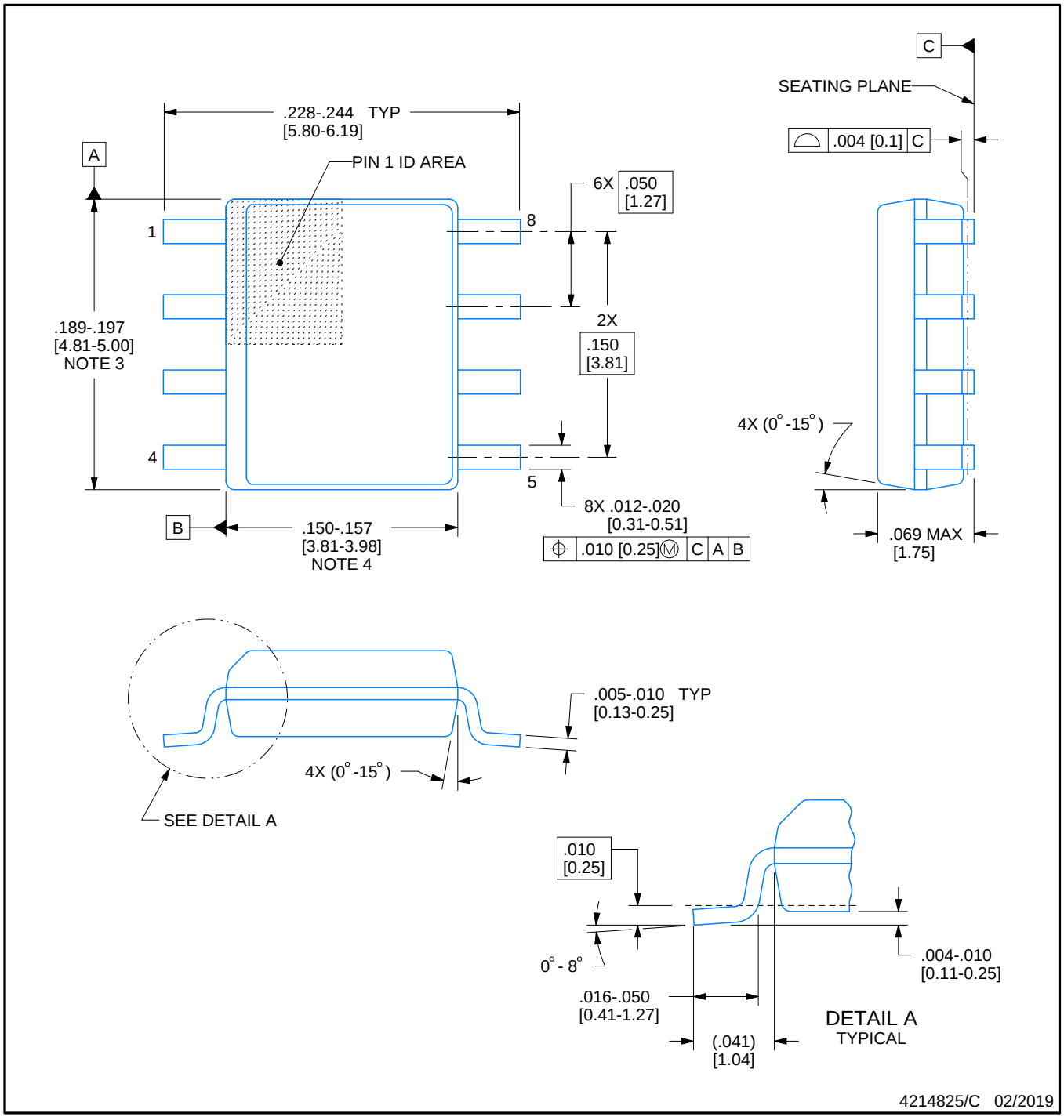


PACKAGE OUTLINE

D0008A

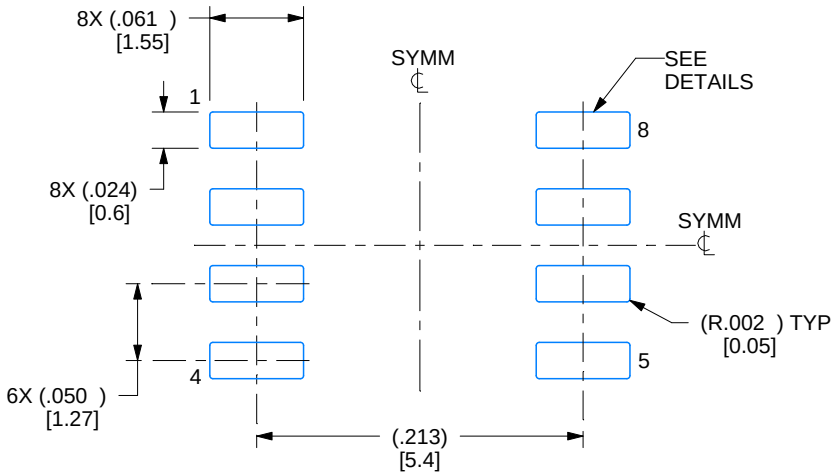
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

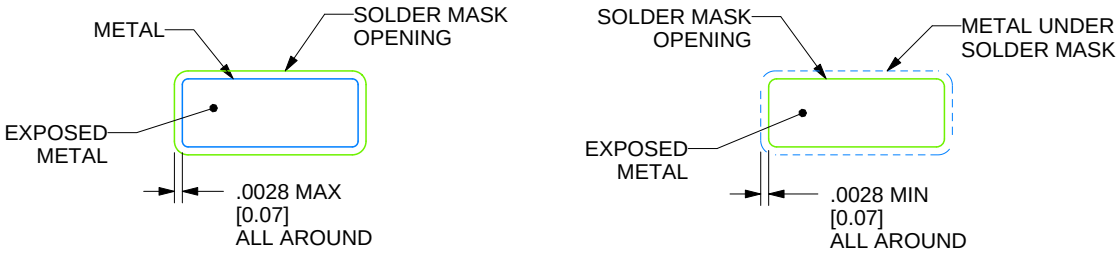


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

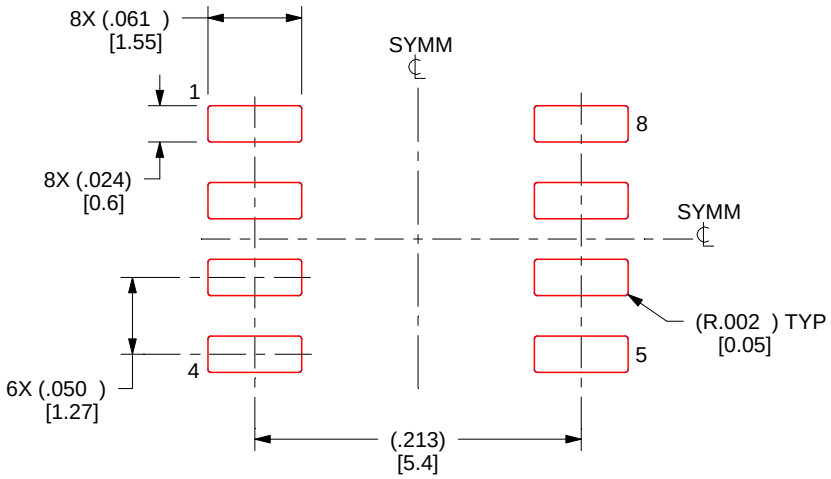
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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