



## Dual, 14-Bit, 125MSPS DIGITAL-TO-ANALOG CONVERTER

Check for Samples: [DAC2904](#)

### FEATURES

- 125MSPS UPDATE RATE
- SINGLE SUPPLY: +3.3V or +5V
- HIGH SFDR: 78dB at  $f_{OUT} = 10\text{MHz}$
- LOW GLITCH: 2pV-s
- LOW POWER: 310mW
- INTERNAL REFERENCE
- POWER-DOWN MODE: 23mW

### DESCRIPTION

The DAC2904 is a monolithic, 14-bit, dual-channel, high-speed Digital-to-Analog Converter (DAC), and is optimized to provide high dynamic performance while dissipating only 310mW.

Operating with high update rates of up to 125MSPS, the DAC2904 offers exceptional dynamic performance, and enables the generation of very-high output frequencies suitable for “Direct IF” applications. The DAC2904 has been optimized for communications applications in which separate I and Q data are processed while maintaining tight-gain and offset matching.

Each DAC has a high-impedance differential-current output, suitable for single-ended or differential analog-output configurations.

### APPLICATIONS

- COMMUNICATIONS:
  - Base Stations, WLL, WLAN
  - Baseband I/Q Modulation
- MEDICAL/TEST INSTRUMENTATION
- ARBITRARY WAVEFORM GENERATORS (ARB)
- DIRECT DIGITAL SYNTHESIS (DDS)

The DAC2904 combines high dynamic performance with a high update rate to create a cost-effective solution for a wide variety of waveform-synthesis applications:

- Pin compatibility between family members provides 10-bit (DAC2900), 12-bit (DAC2902), and 14-bit (DAC2904) resolution.
- Pin compatible to the AD9767 dual DAC.
- Gain matching is typically 0.5% of full-scale, and offset matching is specified at 0.02% max.
- The DAC2904 utilizes an advanced CMOS process; the segmented architecture minimizes output-glitch energy, and maximizes the dynamic performance.
- All digital inputs are +3.3V and +5V logic compatible. The DAC2904 has an internal reference circuit, and allows use in a multiplying configuration.

The DAC2904 is available in a TQFP-48 package, and is specified over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(2)</sup>	TRANSPORT MEDIA, QUANTITY
DAC2904Y	TQFP-48	PFB	-40°C to +85°C	DAC2904Y	DAC2904Y/250	Tape and Reel, 250
					DAC2904Y/1K	Tape and Reel, 1k
					DAC2904IPFB	Tray, 250

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Models with a slash (/) are available only in tape and reel media in the quantities indicated (for example, **1K** indicates 1000 devices per reel). Ordering 1000 pieces of *DAC2904Y/1K* will get a single 1000-piece tape and reel.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

	DAC2904	UNIT
+V <sub>A</sub> to AGND	-0.3 to +6	V
+V <sub>D</sub> to DGND	-0.3 to +6	V
AGND to DGND	-0.3 to +0.3	V
+V <sub>A</sub> to +V <sub>D</sub>	-6 to +6	V
CLK, PD to DGND	-0.3 to V <sub>D</sub> +0.3	V
D0–D9 to DGND	-0.3 to V <sub>D</sub> +0.3	V
I <sub>OUT</sub> , $\overline{I_{OUT}}$ to AGND	-1 to V <sub>A</sub> + 0.3	V
BW, BYP to AGND	-0.3 to V <sub>A</sub> + 0.3	V
REF <sub>IN</sub> , FSA to AGND	-0.3 to V <sub>A</sub> + 0.3	V
$\overline{INT}/EXT$ to AGND	-0.3 to V <sub>A</sub> + 0.3	V
Junction Temperature	+150	°C
Case Temperature	+100	°C
Storage Temperature	+125	°C

- (1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$T_{MIN}$  to  $T_{MAX}$ ,  $+V_A = +5V$ ,  $+V_D = +3.3V$ , differential transformer coupled output, and  $50\Omega$  doubly-terminated, unless otherwise noted. Independent Gain Mode.

PARAMETER	TEST CONDITIONS	DAC2904			UNIT
		MIN	TYP	MAX	
<b>RESOLUTION</b>					
Resolution			14		Bits
Output Update Rate ( $f_{CLOCK}$ )			125		MSPS
<b>STATIC ACCURACY<sup>(1)</sup></b>					
Differential Nonlinearity (DNL)	$T_A = +25^\circ C$		$\pm 4.0$		LSB
Integral Nonlinearity (INL)	$T_A = +25^\circ C$		$\pm 5.0$		LSB
<b>DYNAMIC PERFORMANCE</b>					
Spurious-Free Dynamic Range (SFDR)	To Nyquist				
$f_{OUT} = 1MHz$ , $f_{CLOCK} = 50MSPS$	0dBFS Output	71	82		dBc
	-6dBFS Output		77		dBc
	-12dBFS Output		72		dBc
$f_{OUT} = 1MHz$ , $f_{CLOCK} = 26MSPS$			82		dBc
$f_{OUT} = 2.18MHz$ , $f_{CLOCK} = 52MSPS$			81		dBc
$f_{OUT} = 5.24MHz$ , $f_{CLOCK} = 52MSPS$			81		dBc
$f_{OUT} = 10.4MHz$ , $f_{CLOCK} = 78MSPS$			78		dBc
$f_{OUT} = 15.7MHz$ , $f_{CLOCK} = 78MSPS$			72		dBc
$f_{OUT} = 5.04MHz$ , $f_{CLOCK} = 100MSPS$			80		dBc
$f_{OUT} = 20.2MHz$ , $f_{CLOCK} = 100MSPS$			69		dBc
$f_{OUT} = 20.1MHz$ , $f_{CLOCK} = 125MSPS$			69		dBc
$f_{OUT} = 40.2MHz$ , $f_{CLOCK} = 125MSPS$			64		dBc
Spurious-Free Dynamic Range within a Window					
$f_{OUT} = 1MHz$ , $f_{CLOCK} = 50MSPS$	2MHz span	80	90		dBc
$f_{OUT} = 5.24MHz$ , $f_{CLOCK} = 52MSPS$	10MHz span		88		dBc
$f_{OUT} = 5.26MHz$ , $f_{CLOCK} = 78MSPS$	10MHz span		88		dBc
$f_{OUT} = 5.04MHz$ , $f_{CLOCK} = 125MSPS$	10MHz span		88		dBc
Total Harmonic Distortion (THD)					dBc
$f_{OUT} = 1MHz$ , $f_{CLOCK} = 50MSPS$			-79	-70	dBc
$f_{OUT} = 5.24MHz$ , $f_{CLOCK} = 52MSPS$			-77		dBc
$f_{OUT} = 5.26MHz$ , $f_{CLOCK} = 78MSPS$			-76		dBc
$f_{OUT} = 5.04MHz$ , $f_{CLOCK} = 125MSPS$			-75		dBc
Multitone Power Ratio	Eight tone with 110kHz spacing				
$f_{OUT} = 2.0MHz$ to $2.99MHz$ , $f_{CLOCK} = 65MSPS$	0dBFS output		80		dBc
Signal-to-Noise Ratio (SNR)					
$f_{OUT} = 5.02MHz$ , $f_{CLOCK} = 50MHz$	0dBFS output		68		dBc
Signal-to-Noise and Distortion (SINAD)					
$f_{OUT} = 5.02MHz$ , $f_{CLOCK} = 50MHz$	0dBFS output		67		dBc
Channel Isolation					
$f_{OUT} = 1MHz$ , $f_{CLOCK} = 52MSPS$			85		dBc
$f_{OUT} = 20MHz$ , $f_{CLOCK} = 125MSPS$			77		dBc

(1) At output  $I_{OUT}$ , while driving a virtual ground.

**ELECTRICAL CHARACTERISTICS (continued)**

T<sub>MIN</sub> to T<sub>MAX</sub>, +V<sub>A</sub> = +5V, +V<sub>D</sub> = +3.3V, differential transformer coupled output, and 50Ω doubly-terminated, unless otherwise noted. Independent Gain Mode.

PARAMETER	TEST CONDITIONS	DAC2904			UNIT
		MIN	TYP	MAX	
<b>DYNAMIC PERFORMANCE, continued</b>					
Output Settling Time <sup>(2)</sup>	To 0.1%		30		ns
Output Rise Time <sup>(2)</sup>	10% to 90%		2		ns
Output Fall Time <sup>(2)</sup>	10% to 90%		2		ns
Glitch Impulse			2		pV-s
<b>DC ACCURACY</b>					
Full-Scale Output Range <sup>(3)</sup> (FSR)	All Bits HIGH, I <sub>OUT</sub>	2		20	mA
Output Compliance Range	With internal reference	-1.0		+1.25	V
Gain Error—Full-Scale	With internal reference	-5	±1	+5	%FSR
Gain Error	With internal reference	-2.5	±1	+2.5	%FSR
Gain Matching	With internal reference	-2.0	0.5	+2.0	%FSR
Gain Drift	With internal reference		±50		ppmFSR/°C
Offset Error	With internal reference	-0.02		+0.02	%FSR
Offset Drift	With internal reference		±0.2		ppmFSR/°C
Power-Supply Rejection, +V <sub>A</sub>	+5V, ±10%	-0.2		+0.2	%FSR/V
Power-Supply Rejection, +V <sub>D</sub>	+3.3V, ±10%	-0.025		+0.025	%FSR/V
Output Noise	I <sub>OUT</sub> = 20mA, R <sub>LOAD</sub> = 50Ω		50		pA/√Hz
	I <sub>OUT</sub> = 2mA		30		pA/√Hz
Output Resistance			200		kΩ
Output Capacitance	I <sub>OUT</sub> , I <sub>OUT</sub> to ground		6		pF
<b>REFERENCE/CONTROL AMP</b>					
Reference Voltage		+1.18	+1.25	+1.31	V
Reference Voltage Drift			±50		ppmFSR/°C
Reference Output Current			100		nA
Reference Multiplying Bandwidth			0.3		MHz
Input Compliance Range		+0.5		+1.25	V
<b>DIGITAL INPUTS</b>					
Logic Coding		Straight Binary			
Logic High Voltage, V <sub>IH</sub>	+V <sub>D</sub> = 5V	3.5	5		V
Logic Low Voltage, V <sub>IL</sub>	+V <sub>D</sub> = 5V		0	1.2	V
Logic High Voltage, V <sub>IH</sub>	+V <sub>D</sub> = 3.3V	2	3		V
Logic Low Voltage, V <sub>IL</sub>	+V <sub>D</sub> = 3.3V		0	0.8	V
Logic High Current, I <sub>IH</sub> <sup>(4)</sup>	+V <sub>D</sub> = 3.3V		±10		μA
Logic Low Current	+V <sub>D</sub> = 3.3V		±10		μA
Input Capacitance			5		pF

(2) Measured single-ended into 50Ω load.  
 (3) Nominal full-scale output current is 32 × I<sub>REF</sub>; see Applicationxx section for details.  
 (4) Typically 45μA for the PD pin, which has an internal pull-down resistor.

**ELECTRICAL CHARACTERISTICS (continued)**

$T_{MIN}$  to  $T_{MAX}$ ,  $+V_A = +5V$ ,  $+V_D = +3.3V$ , differential transformer coupled output, and  $50\Omega$  doubly-terminated, unless otherwise noted. Independent Gain Mode.

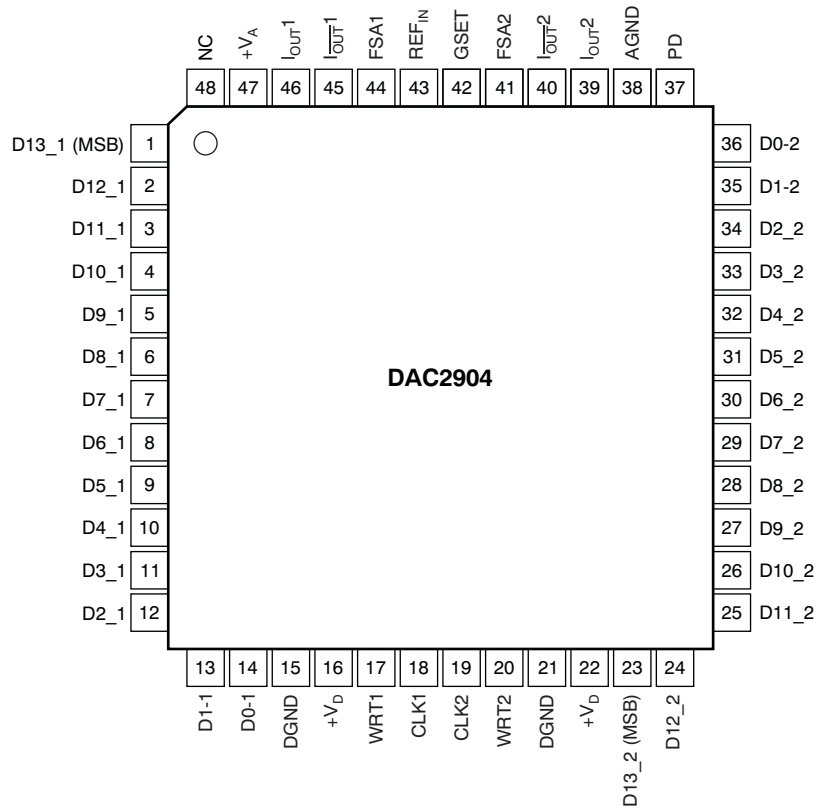
PARAMETER	TEST CONDITIONS	DAC2904			UNIT
		MIN	TYP	MAX	
<b>POWER SUPPLY</b>					
Supply Voltages					
+ $V_A$		+3.0	+5	+5.5	V
+ $V_D$		+3.0	+3.3	+5.5	V
Supply Current					
$I_{VA}$ <sup>(5)</sup>	$+V_A = +5V$ , $I_{OUT} = 20mA$		58	65	mA
$I_{VA}$ <sup>(5)</sup>	Power-Down mode		1.7	3	mA
$I_{VD}$ <sup>(5)</sup>			4.2	7	mA
$I_{VD}$ <sup>(6)</sup>			17	19.5	mA
Power Dissipation <sup>(5)</sup>	$+V_A = +5V$ , $+V_D = 3.3V$ , $I_{OUT} = 20mA$		310	350	mW
Power Dissipation <sup>(6)</sup>	$+V_A = +5V$ , $+V_D = 3.3V$ , $I_{OUT} = 20mA$		348	390	mW
Power Dissipation <sup>(5)</sup>	$+V_A = +5V$ , $+V_D = 3.3V$ , $I_{OUT} = 2mA$		130		mW
Power Dissipation	Power-Down mode		23	38	mW
Thermal Resistance, TQFP-48					
$\theta_{JA}$			60		°C/W
$\theta_{JC}$			13		°C/W
<b>TEMPERATURE RANGE</b>					
Specified	Ambient	-40		+85	°C
Operating	Ambient	-40		+85	°C

(5) Measured at  $f_{CLOCK} = 25MSPS$  and  $f_{OUT} = 1MHz$ .

(6) Measured at  $f_{CLOCK} = 100MSPS$  and  $f_{OUT} = 40MHz$ .

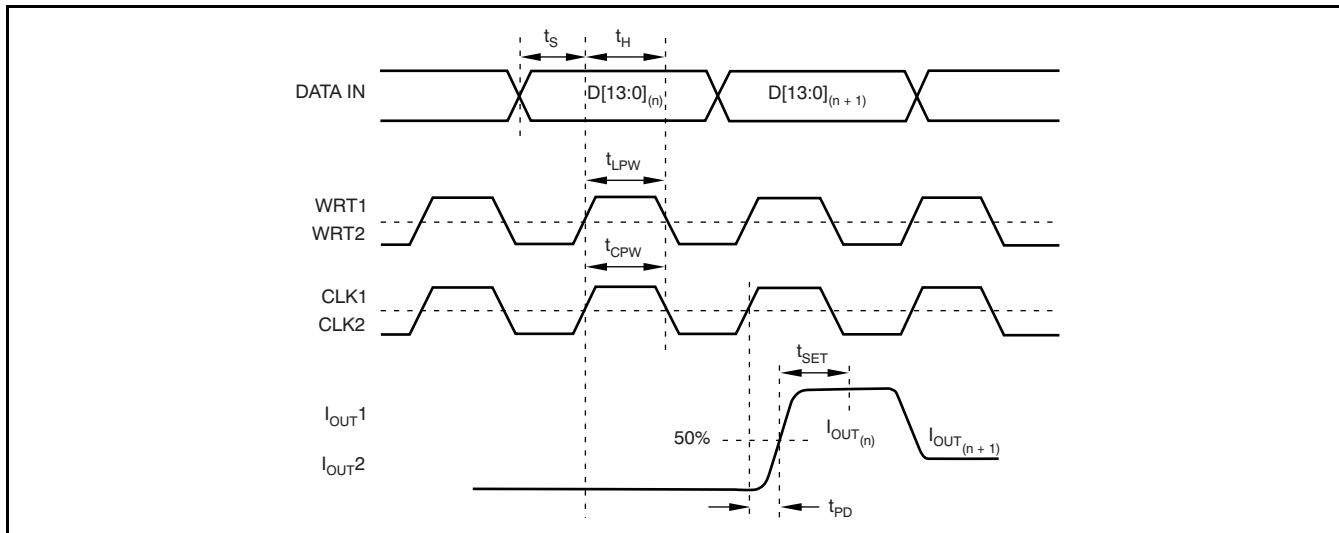
**DEVICE INFORMATION**

**PFB PACKAGE  
TQFP-48  
(TOP VIEW)**



**TERMINAL FUNCTIONS**

TERMINAL		DESCRIPTION
NAME	NO.	
D[13:0]_1	1–14	Data port DAC1, data bit 13 (MSB) to bit 0 (LSB)
DGND	15, 21	Digital ground
+V <sub>D</sub>	16, 22	Digital supply, +3.0V to +5.5V
WRT1	17	DAC1 input latches write signal
CLK1	18	Clock input DAC1
CLK2	19	Clock input DAC2
WRT2	20	DAC2 input latches write signal
D[13:0]_2	23–36	Data port DAC2, data bit 13 (MSB) to bit 0 (LSB).
PD	37	Power-down function control input. <i>H</i> = DAC in power-down mode; <i>L</i> = DAC in normal operation (internal pull-down for default <i>L</i> ).
AGND	38	Analog ground
I <sub>out2</sub>	39	Current output DAC2. Full-scale with all bits of data port 2 high.
I <sub>OUT</sub> 2	40	Complementary current output DAC2. Full-scale with all bits of data port 2 low.
FSA2	41	Full-scale adjust, DAC2. Connect external R <sub>SET</sub> resistor.
GSET	42	Gain-setting mode ( <i>H</i> = one resistor, <i>L</i> = two resistors)
REF <sub>IN</sub>	43	Internal reference voltage output; external reference voltage input. Bypass with 0.1μF capacitor to AGND for internal reference operation.
FSA1	44	Full-scale adjust, DAC1. Connect external R <sub>SET</sub> resistor.
I <sub>OUT</sub> 1	45	Complementary current output DAC1. Full-scale with all bits of data port 1 low.
I <sub>out1</sub>	46	Current output DAC1. Full-scale with all bits of data port 1 high.
+V <sub>A</sub>	47	Analog supply, +3.0V to +5.5V
NC	48	No connection



## TIMING REQUIREMENTS

PARAMETER		MIN	TYP	MAX	UNIT
$t_S$	Input setup time	2			ns
$t_H$	Input hold time	1.5			ns
$t_{LPW}$ , $t_{CPW}$	Latch/Clock pulse width	3.5	4		ns
$t_{CW}$	Delay rising CLK edge to rising WRT edge	0		$t_{PW} - 2$	ns
$t_{PD}$	Propagation delay		1		ns
$t_{SET}$	Settling time (0.1%)		30		ns

## DIGITAL INPUTS AND TIMING

The data input ports of the DAC2904 accept a standard positive coding with data bit D13 being the most significant bit (MSB). The converter outputs support a clock rate of up to 125MSPS. The best performance will typically be achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Also, the set-up and hold times may be chosen within their specified limits.

All digital inputs of the DAC2904 are CMOS compatible. The logic thresholds depend on the applied digital supply voltages, such that they are set to approximately half the supply voltage;  $V_{th} = +V_D/2$  ( $\pm 20\%$  tolerance). The DAC2904 is designed to operate with a digital supply ( $+V_D$ ) of +3.0V to +5.5V.

The two converter channels within the DAC2904 consist of two independent, 14-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRT1, WRT2) and clock (CLK1, CLK2) inputs. Here, the WRT lines control the channel input latches and the CLK lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRT line. This data is presented to the DAC latch on the following falling edge of the WRT signal. On the next rising edge of the CLK line, the DAC is updated with the new data and the analog output signal will change accordingly. The double latch architecture of the DAC2904 results in a defined sequence for the WRT and CLK signals, expressed by parameter  $t_{CW}$ . A correct timing is observed when the rising edge of CLK occurs at the same time, or before, the rising edge of the WRT signal. This condition can simply be met by connecting the WRT and CLK lines together. Note that all specifications were measured with the WRT and CLK lines connected together.

**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $+V_D = +3.3\text{V}$ ,  $+V_A = +5\text{V}$ , differential transformer coupled,  $I_{OUT} = 20\text{mA}$ ,  $50\Omega$  double terminated load, and SFDR up to Nyquist, unless otherwise noted.

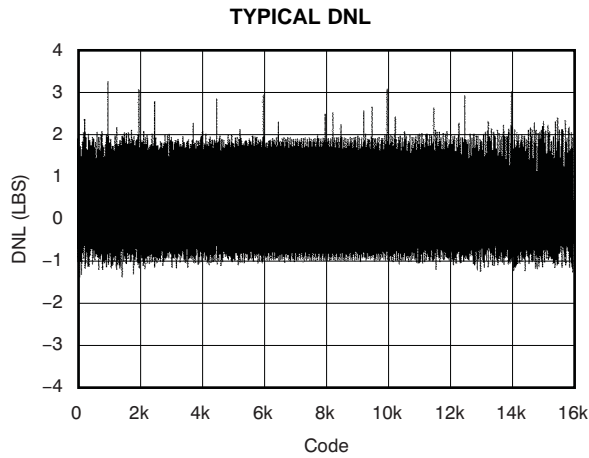


Figure 1.

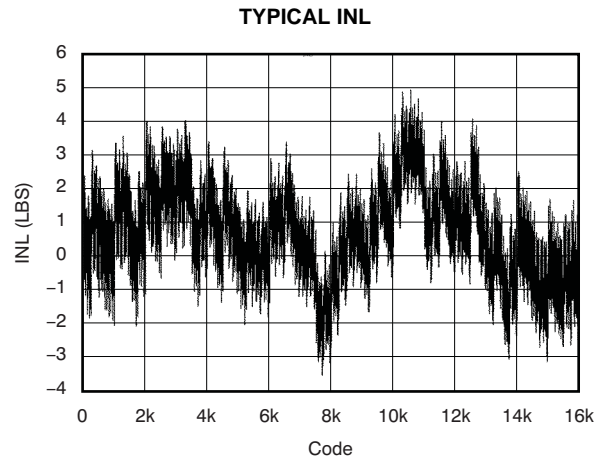


Figure 2.

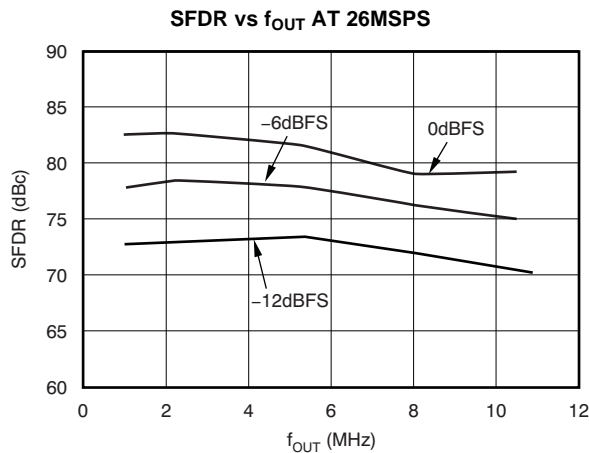


Figure 3.

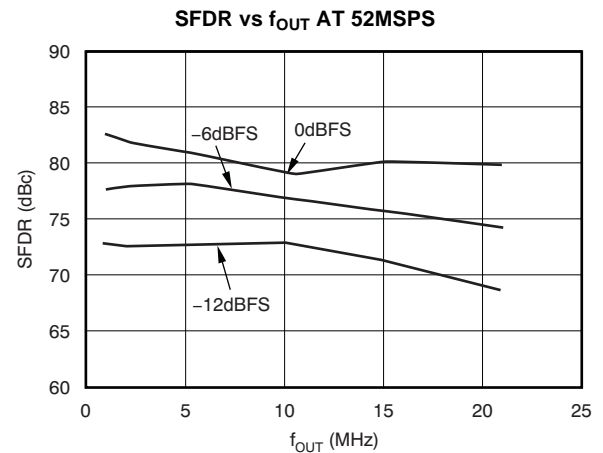


Figure 4.

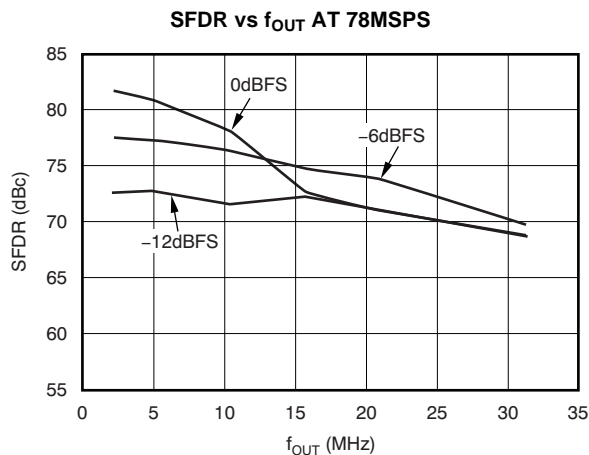


Figure 5.

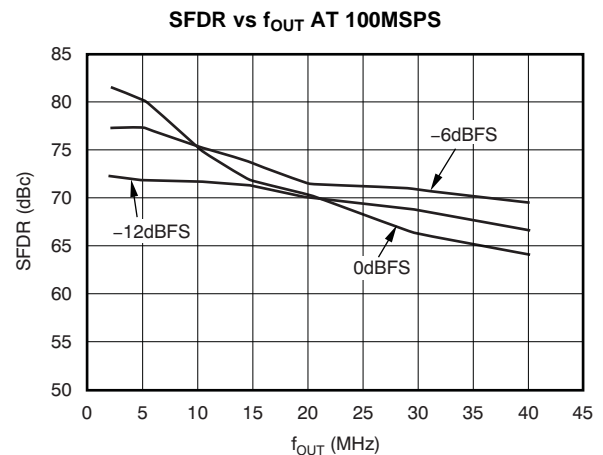


Figure 6.



**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_D = +3.3\text{V}$ ,  $+V_A = +5\text{V}$ , differential transformer coupled,  $I_{OUT} = 20\text{mA}$ ,  $50\Omega$  double terminated load, and SFDR up to Nyquist, unless otherwise noted.

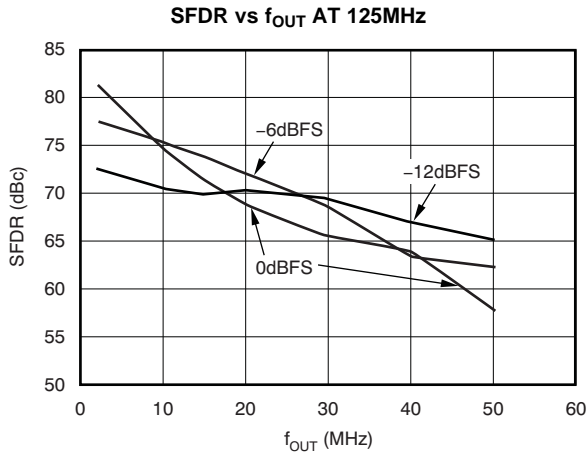


Figure 7.

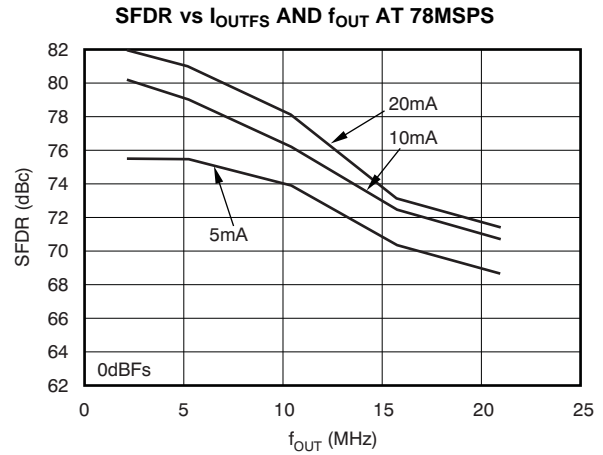


Figure 8.

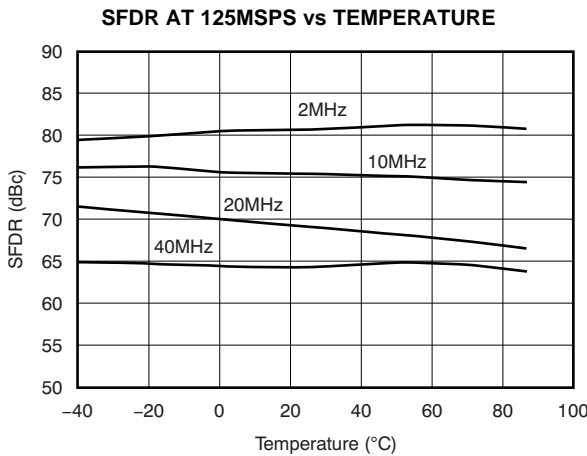


Figure 9.

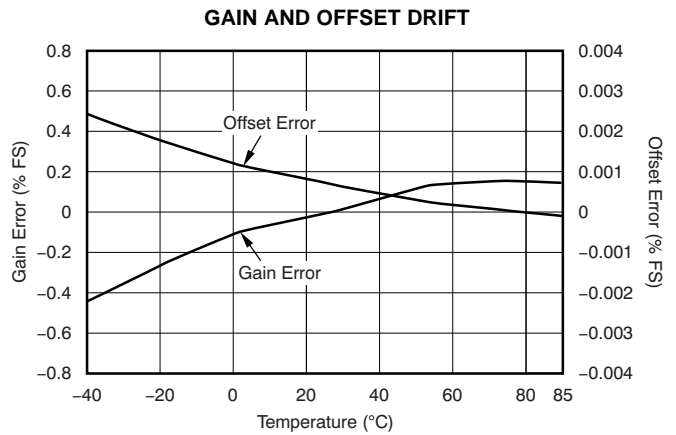


Figure 10.

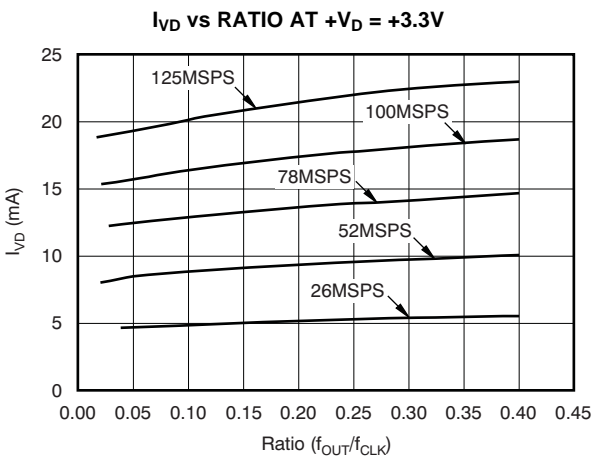


Figure 11.

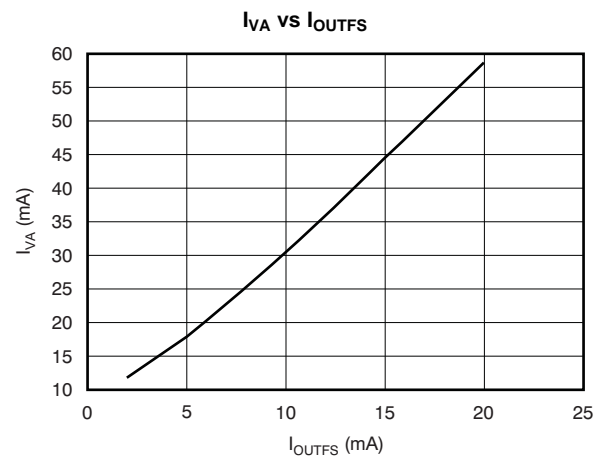


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_D = +3.3\text{V}$ ,  $+V_A = +5\text{V}$ , differential transformer coupled,  $I_{\text{OUT}} = 20\text{mA}$ ,  $50\Omega$  double terminated load, and SFDR up to Nyquist, unless otherwise noted.

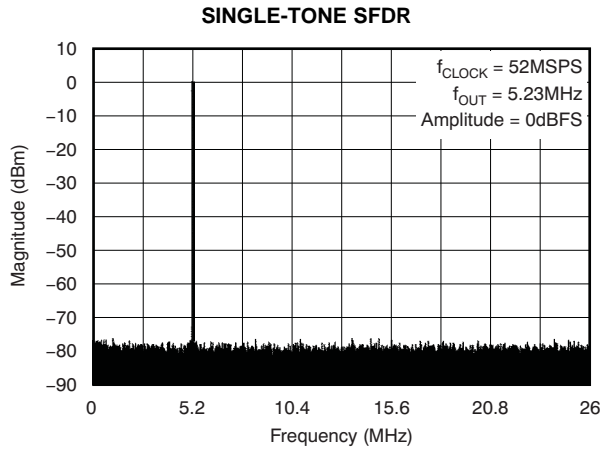


Figure 13.

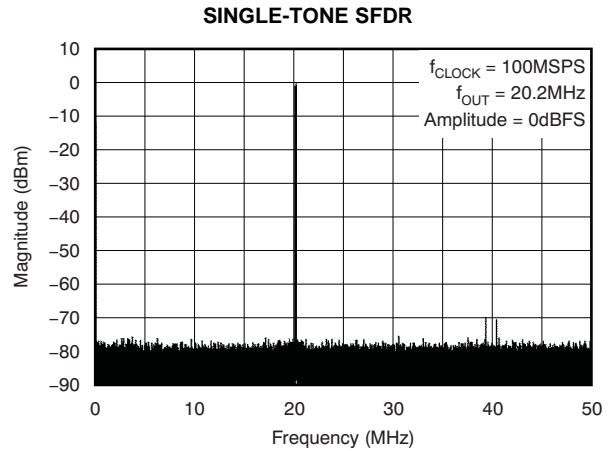


Figure 14.

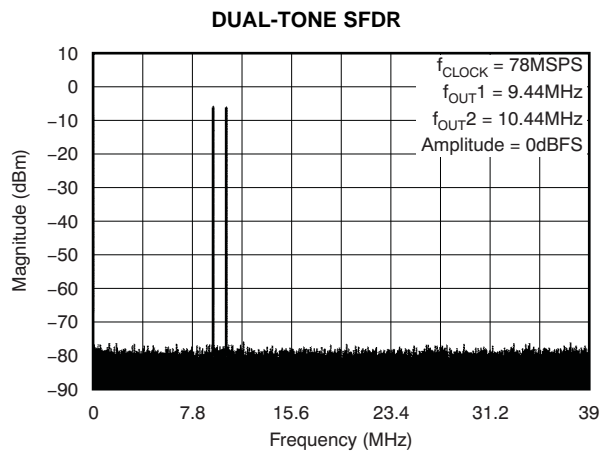


Figure 15.

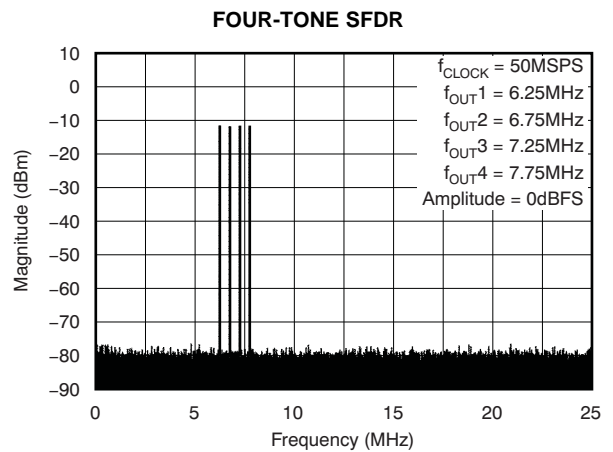
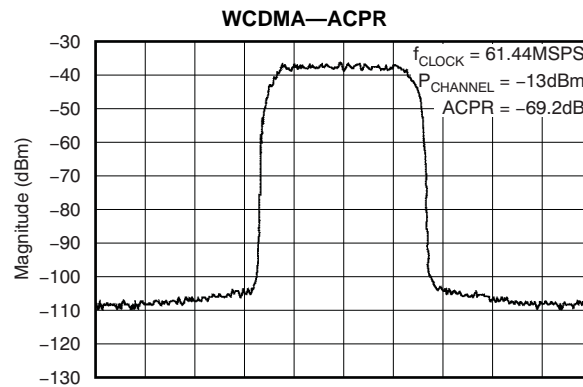


Figure 16.



Center: 15.36MHz; Span: 14MHz

Figure 17.

## APPLICATION INFORMATION

### THEORY OF OPERATION

The architecture of the DAC2904 uses the current steering technique to enable fast switching and a high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20mA, as shown in [Figure 18](#). An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node,  $I_{OUT}$  or  $I_{\overline{OUT}}$ . The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy, improves the dynamic performance (SFDR), and DNL. The current outputs maintain a very high output impedance of greater than 200k $\Omega$ .

The full-scale output current is determined by the ratio of the internal reference voltage (1.25V) and an external resistor,  $R_{SET}$ . The resulting  $I_{REF}$  is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2mA to 20mA, depending on the value of  $R_{SET}$ .

The DAC2904 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises the current source array with its associated switches, and the reference circuitry.

### DAC TRANSFER FUNCTION

Each of the DACs in the DAC2904 has a set of complementary current output,  $I_{OUT}$  and  $I_{\overline{OUT}}$ . The full-scale output current,  $I_{OUTFS}$ , is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT} + I_{\overline{OUT}} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT} = I_{OUTFS} \times \frac{\text{Code}}{16,384} \quad (2)$$

$$I_{\overline{OUT}} = I_{OUTFS} \times \left(16,383 - \frac{\text{Code}}{16,384}\right) \quad (3)$$

where *Code* is the decimal representation of the DAC data input word. Additionally,  $I_{OUTFS}$  is a function of the reference current  $I_{REF}$ , which is determined by the reference voltage and the external setting resistor,  $R_{SET}$ .

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases the complementary outputs will drive resistive loads or a terminated transformer. A signal voltage will develop at each output according to:

$$V_{OUT} = I_{OUT} \times R_{LOAD} \quad (5)$$

$$V_{\overline{OUT}} = I_{\overline{OUT}} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC2904. To maintain specified linearity performance, the voltage for  $I_{OUT}$  and  $I_{\overline{OUT}}$  should not exceed the maximum allowable compliance range.

The two single-ended output voltages can be combined to find the total differential output swing:

$$V_{OUTDIFF} = V_{OUT} - V_{\overline{OUT}} = \frac{(2 \times \text{Code} - 16,383)}{16,384} \times I_{OUTFS} \times R_{LOAD} \quad (7)$$

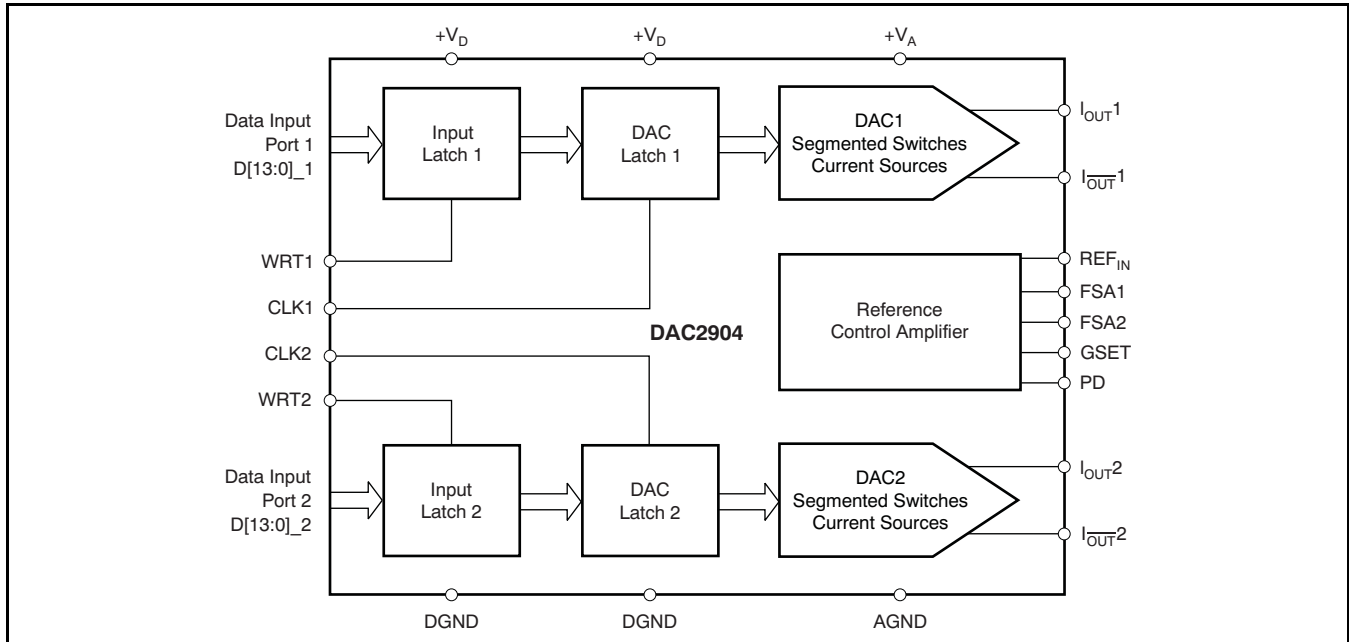


Figure 18. Block Diagram of the DAC2904

**ANALOG OUTPUTS**

The DAC2904 provides two complementary current outputs,  $I_{OUT}$  and  $I_{\overline{OUT}}$ . The simplified circuit of the analog output stage representing the differential topology is shown in Figure 19. The output impedance of  $I_{OUT}$  and  $I_{\overline{OUT}}$  results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

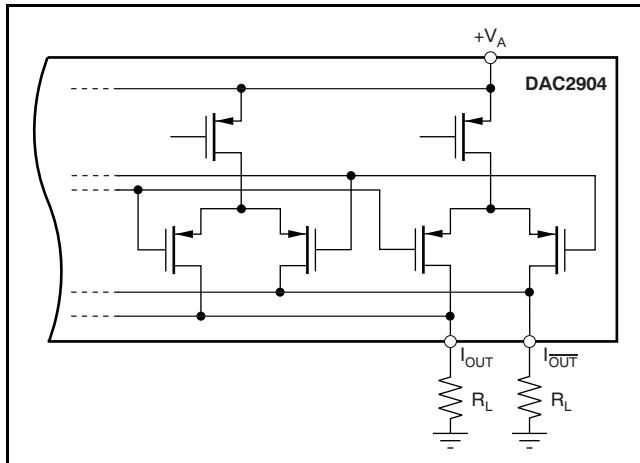


Figure 19. Equivalent Analog Output

The signal voltage swing that may develop at the two outputs,  $I_{OUT}$  and  $I_{\overline{OUT}}$ , is limited by a negative and positive compliance. The negative limit of  $-1V$  is

given by the breakdown voltage of the CMOS process, and exceeding it will compromise the reliability of the DAC2904, or even cause permanent damage. With the full-scale output set to 20mA, the positive compliance equals 1.25V, operating with an analog supply of  $+V_A = 5V$ . Note that the compliance range decreases to about 1V for a selected output current of  $I_{OUTFS} = 2mA$ . Care should be taken that the configuration of DAC2904 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately 0.5V<sub>PP</sub>. This is the case for a 50Ω doubly terminated load and a 20mA full-scale output current. A variety of loads can be adapted to the output of the DAC2904 by selecting a suitable transformer while maintaining optimum voltage levels at  $I_{OUT}$  and  $I_{\overline{OUT}}$ . Furthermore, using the differential output configuration in combination with a transformer will be instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 20mA. A lower full-scale range down to 2mA may be considered for applications that require a low power consumption, but can tolerate a slightly reduced performance level.

## OUTPUT CONFIGURATIONS

The current outputs of the DAC2904 allow for a variety of configurations, some of which are illustrated in Table 1. As mentioned previously, utilizing the converter differential outputs will yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps will be suitable for a dc-coupled configuration.

**Table 1. Input Coding vs Analog Output Current**

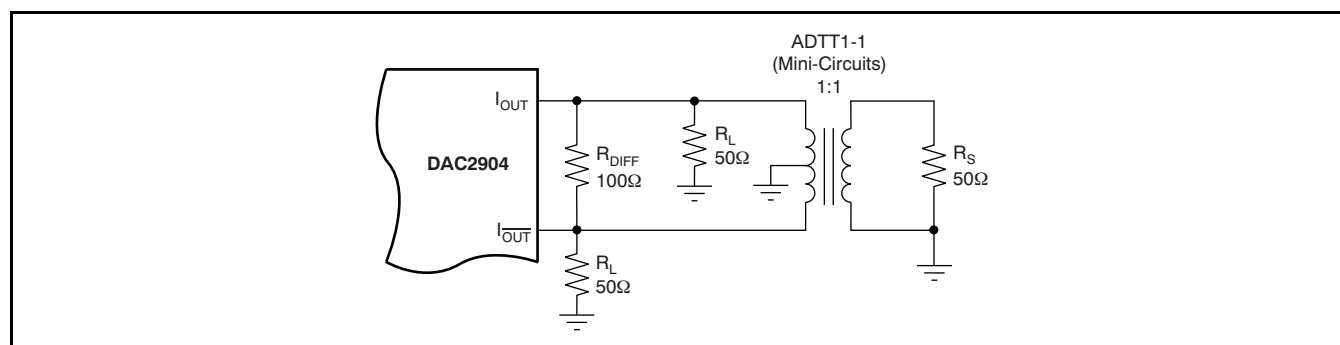
INPUT CODE (D13 - D0)	$I_{OUT}$	$I_{\overline{OUT}}$
11 1111 1111 1111	20mA	0mA
10 0000 0000 0000	10mA	10mA
00 0000 0000 0000	0mA	20mA

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground will convert the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op amp configuration may be considered.

## DIFFERENTIAL WITH TRANSFORMER

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance (see Figure 20). The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements. The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio), the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs. The model shown, ADTT1-1 (by Mini-Circuits), has a 1:1 ratio and may be used to interface the DAC2904 to a 50Ω load. This results in a 25Ω load for each of the outputs,  $I_{OUT}$  and  $I_{\overline{OUT}}$ . The output signals are ac-coupled and inherently isolated because of its magnetic coupling.

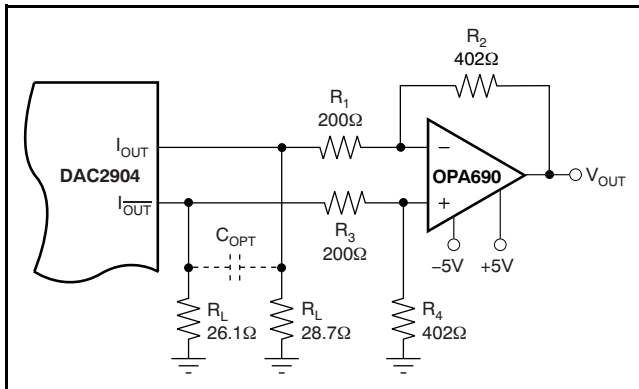
As shown in Figure 20, the transformer center tap is connected to ground. This forces the voltage swing on  $I_{OUT}$  and  $I_{\overline{OUT}}$  to be centered at 0V. In this case the two resistors,  $R_L$ , may be replaced with one,  $R_{DIFF}$ , or omitted altogether. This approach should only be used if all components are close to each other, and if the VSWR is not important. A complete power transfer from the DAC output to the load can be realized, but the output compliance range should be observed. Alternatively, if the center tap is not connected, the signal swing will be centered at  $(R_L \times I_{OUTFS}/2)$ . However, in this case, the two load resistors,  $R_L$ , must be used to enable the necessary dc-current flow for both outputs.



**Figure 20. Differential Output Configuration Using an RF Transformer**

## DIFFERENTIAL CONFIGURATION USING AN OP AMP

If the application requires a dc-coupled output, a difference amplifier may be considered, as shown in Figure 21. Four external resistors are needed to configure the voltage-feedback op amp OPA690 as a difference amplifier performing the differential to single-ended conversion. Under the configuration shown, the DAC2904 generates a differential output signal of  $0.5V_{PP}$  at the load resistors,  $R_L$ . The resistor values shown were selected to result in a symmetric 25 $\Omega$  loading for each of the current outputs since the input impedance of the difference amplifier is in parallel to resistors  $R_L$ , and should be considered.



**Figure 21. Difference Amplifier Provides Differential to Single-Ended Conversion and DC-Coupling**

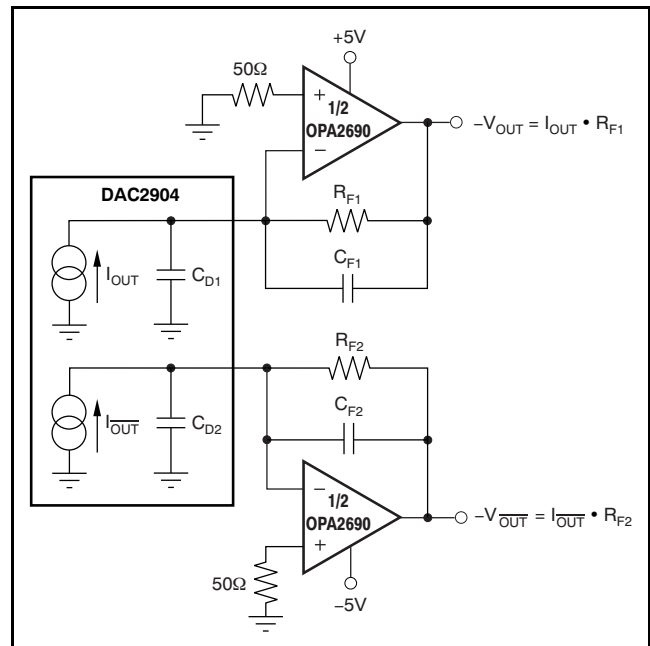
The OPA690 is configured for a gain of two. Therefore, operating the DAC2904 with a 20mA full-scale output will produce a voltage output of  $\pm 1V$ . This requires the amplifier to operate off of a dual power supply ( $\pm 5V$ ). The tolerance of the resistors typically sets the limit for the achievable common-mode rejection. An improvement can be obtained by fine-tuning resistor  $R_4$ .

This configuration typically delivers a lower level of ac performance than the previously discussed transformer solution because the amplifier introduces another source of distortion. Suitable amplifiers should be selected based on the slew rate, harmonic distortion, and output swing capabilities. High-speed amplifiers like the OPA690 or OPA687 may be considered. The ac performance of this circuit may be improved by adding a small capacitor,  $C_{DIFF}$ , between the outputs  $I_{OUT}$  and  $I_{OUT-bar}$  (see Figure 21). This will introduce a real pole to create a low-pass filter in order to slew-limit the DAC fast output signal steps, which otherwise could drive the amplifier into

slew-limitations or into an overload condition; both would cause excessive distortion. The difference amplifier can easily be modified to add a level shift for applications requiring the single-ended output voltage to be unipolar; that is, swing between 0V and +2V.

## DUAL TRANSIMPEDANCE OUTPUT CONFIGURATION

The circuit example of Figure 22 shows the signal output currents connected into the summing junctions of the dual voltage-feedback op amp OPA2690 that is set up as a transimpedance stage, or -to-V converter. With this circuit, the DAC output will be kept at a virtual ground, minimizing the effects of output impedance variations, which results in the best dc linearity (INL). As mentioned previously, care should be taken not to drive the amplifier into slew-rate limitations, and produce unwanted distortion.



**Figure 22. Dual, Voltage-Feedback Amplifier OPA2690 Forms Differential Transimpedance Amplifier**

The dc gain for this circuit is equal to feedback resistor  $R_F$ . At high frequencies, the DAC output impedance ( $C_{D1}$ ,  $C_{D2}$ ) will produce a zero in the noise gain for the OPA2690 that may cause peaking in the closed-loop frequency response.

$C_F$  is added across  $R_F$  to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \frac{\sqrt{GBP}}{4\pi R_F C_D} \quad (8)$$

with  $GBP$  = Gain Bandwidth Product of the OPA

which will give a corner frequency  $f_{-3dB}$  of approximately:

$$f_{-3dB} = \frac{\sqrt{GBP}}{2\pi R_F C_D} \quad (9)$$

The full-scale output voltage is simply defined by the product of  $I_{OUTFS} \times R_F$ , and has a negative unipolar excursion. To improve on the ac performance of this circuit, adjustment of  $R_F$  and/or  $I_{OUTFS}$  should be considered. Further extensions of this application example may include adding a differential filter at the OPA2690 output followed by a transformer, in order to convert to a single-ended signal.

### SINGLE-ENDED CONFIGURATION

Using a single load resistor connected to one of the DAC outputs, a simple current-to-voltage conversion can be accomplished. The circuit in Figure 23 shows a 50Ω resistor connected to  $I_{OUT}$ , providing the termination of the further connected 50Ω cable. Therefore, with a nominal output current of 20mA, the DAC produces a total signal swing of 0V to 0.5V into the 25Ω load.

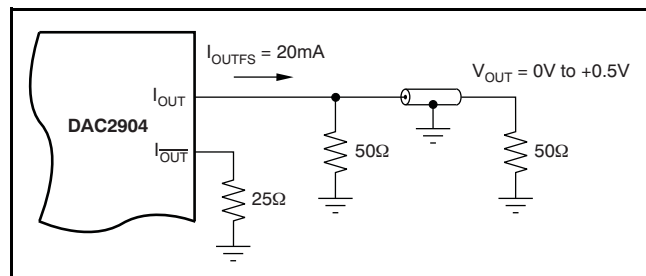


Figure 23. Driving a Doubly-Terminated 50Ω Cable Directly

Different load resistor values may be selected as long as the output compliance range is not exceeded. Additionally, the output current,  $I_{OUTFS}$ , and the load resistor may be mutually adjusted to provide the desired output signal swing and performance.

### INTERFACING ANALOG QUADRATURE MODULATORS

One of the main applications for the dual-channel DAC is baseband I- and Q-channel transmission for digital communications. In this application, the DAC is followed by an analog quadrature modulator, modulating an IF carrier with the baseband data, as shown in Figure 25. Often, the input stages of these quadrature modulators consist of npn-type transistors that require a dc bias (base) voltage greater than 0.8V. The wide output compliance range (–10V to +1.25V) allows for a direct dc-coupling between the DAC2904 and the quadrature modulator.

Figure 24 shows an example of a dc-coupled interface with dc level-shifting, using a precision resistor network. An ac-coupled interface (see Figure 26) has the advantage that the common-mode levels at the input of the modulator can be set independently of those at the output of the DAC. Furthermore, no voltage loss is obtained in this setup.

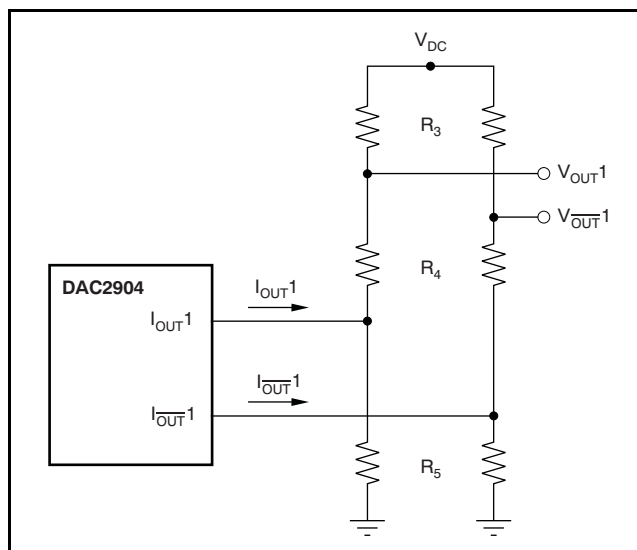
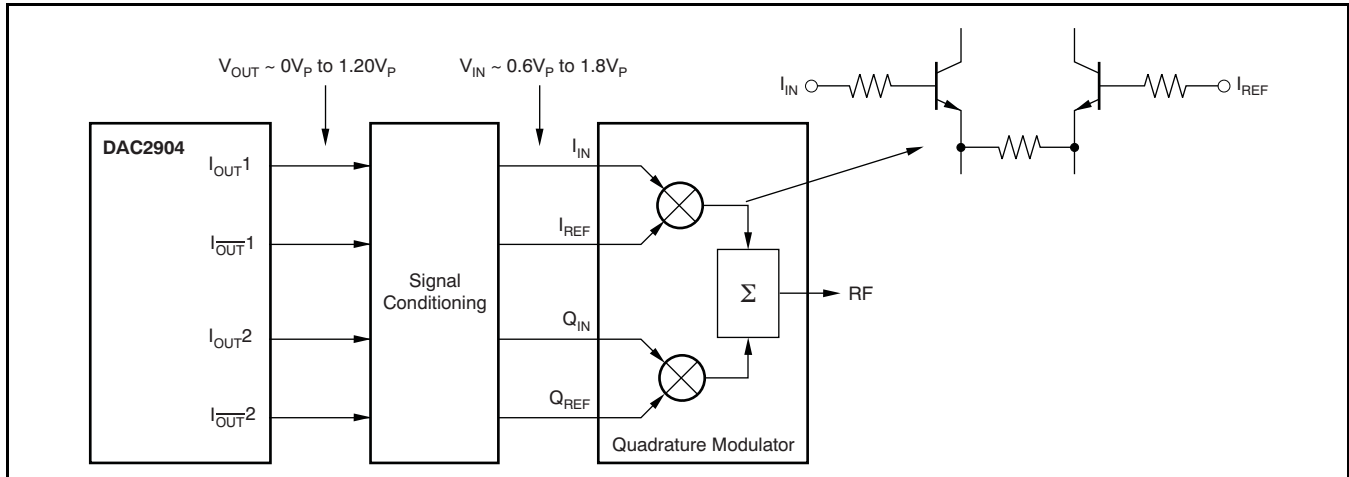


Figure 24. DC-Coupled Interface to Quadrature Modulator Applying Level Shifting



Signal conditioning (level-shifting) may be required to ensure correct dc common-mode levels at the input of the quadrature modulator.

**Figure 25. Generic Interface to a Quadrature Modulator**

**INTERNAL REFERENCE OPERATION**

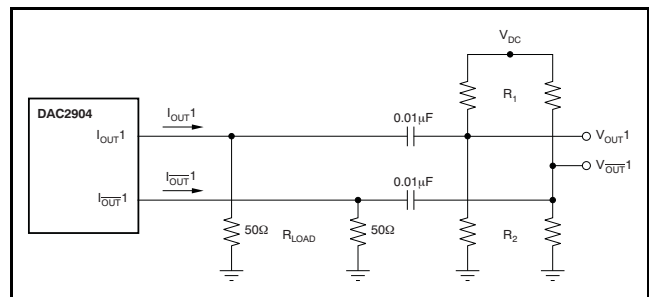
The DAC2904 has an on-chip reference circuit which consists of a 1.25V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current,  $I_{OUTFS}$ , of the DAC2904 is determined by the reference voltage,  $V_{REF}$ , and the value of resistor  $R_{SET}$ .  $I_{OUTFS}$  can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \tag{10}$$

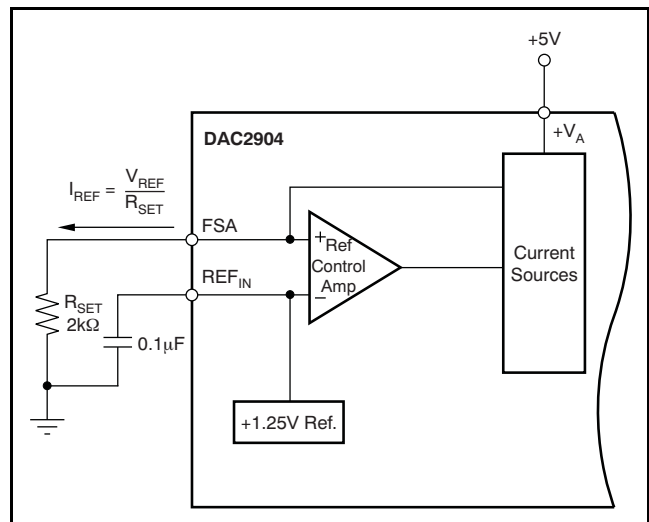
As shown in Figure 27, the external resistor  $R_{SET}$  connects to the FSA pin (Full-Scale Adjust). The reference control amplifier operates as a V-to-I converter producing a reference current,  $I_{REF}$ , which is determined by the ratio of  $V_{REF}$  and  $R_{SET}$  (see Equation 10). The full-scale output current,  $I_{OUTFS}$ , results from multiplying  $I_{REF}$  by a fixed factor of 32.

Using the internal reference, a 2kΩ resistor value results in a full-scale output of approximately 20mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20mA down to 2mA. Operating the DAC2904 at lower than 20mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the  $REF_{IN}$  pin with a ceramic chip capacitor of 0.1μF or more. The control amplifier is internally compensated, and its small-signal bandwidth is approximately 0.3MHz.



**Figure 26. AC-Coupled Interface to Quadrature Modulator Applying Level Shifting**



**Figure 27. Internal Reference Configuration**



## GAIN SETTING OPTIONS

The full-scale output current on the DAC2904 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required—one  $R_{SET}$  connected to the FSA1 pin (pin 44) and the other to the FSA2 pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (that is, connected to  $+V_A$ ), the DAC2904 will switch into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external  $R_{SET}$  resistor connected to the FSA1 pin. The resistor at the FSA2 pin may be removed; however, this is not required because this pin is not functional in this mode and the resistor has no effect on the gain equation. The formula for deriving the correct  $R_{SET}$  remains unchanged; for example,  $R_{SET} = 2k\Omega$  will result in a 20mA output for both DACs.

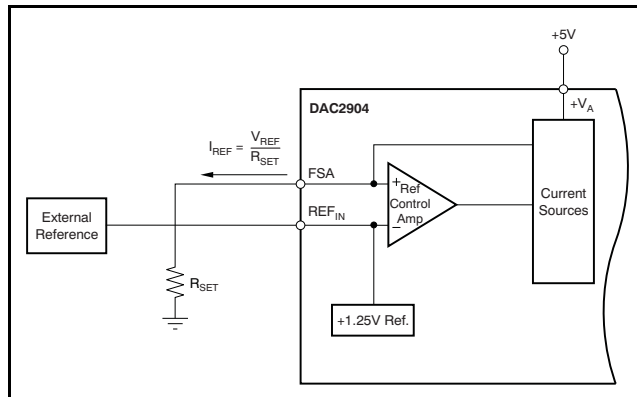
## EXTERNAL REFERENCE OPERATION

The internal reference can be disabled by simply applying an external reference voltage into the  $REF_{IN}$  pin, which in this case functions as an input, as shown in Figure 28. The use of an external reference may be considered for applications that require higher accuracy and drift performance, or to add the ability of dynamic gain control.

While a  $0.1\mu F$  capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input,  $REF_{IN}$ , has a high input impedance ( $1M\Omega$ ) and can easily be driven by various sources. Note that the voltage range of the external reference should stay within the compliance range of the reference input.

## POWER-DOWN MODE

The DAC2904 features a power-down function which can be used to reduce the total supply current to less than 6mA over the specified supply range of 3.0V to 5.5V. Applying a logic high to the PD pin will initiate the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit will enable the normal operation of the converter.



**Figure 28. External Reference Configuration**

## GROUNDING, DECOUPLING AND LAYOUT INFORMATION

Proper grounding and bypassing, short lead lengths, and the use of ground planes are particularly important for high-frequency designs. Multilayer printed circuit boards (PCBs) are recommended for best performance because they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

The DAC2904 uses separate pins for its analog and digital supply and ground connections. The placement of the decoupling capacitor should be such that the analog supply ( $+V_A$ ) is bypassed to the analog ground (AGND), and the digital supply bypassed to the digital ground (DGND). In most cases  $0.1\mu F$  ceramic chip capacitors at each supply pin are adequate to provide a low impedance decoupling path. Keep in mind that the effectiveness of these capacitors largely depends on the proximity to the individual supply and ground pins. Therefore, they should be located as close as physically possible to those device leads. Whenever possible, the capacitors should be located immediately under each pair of supply/ground pins on the reverse side of the PCB. This layout approach will minimize the parasitic inductance of component leads and PCB runs.

Further supply decoupling with surface-mount tantalum capacitors ( $1\mu F$  to  $4.7\mu F$ ) may be added as needed in proximity of the converter.

Low noise is required for all supply and ground connections to the DAC2904. It is recommended to use a multilayer PCB utilizing separate power and ground planes. Mixed signal designs require particular attention to the routing of the different supply currents and signal traces. Generally, analog supply and ground planes should only extend into analog signal areas, such as the DAC output signal and the reference signal. Digital supply and ground

planes must be confined to areas covering digital circuitry, including the digital input lines connecting to the converter, as well as the clock signal. The analog and digital ground planes should be joined together at one point underneath the DAC. This can be realized with a short track of approximately 1/8 inch (3,0 mm).

The power to the DAC2904 should be provided through the use of wide PCB runs or planes. Wide runs will present a lower trace impedance, further optimizing the supply decoupling. The analog and digital supplies for the converter should only be

connected together at the supply connector of the PCB. In the case of only one supply voltage being available to power the DAC, ferrite beads along with bypass capacitors may be used to create an LC filter. This will generate a low-noise analog supply voltage, which can then be connected to the +V<sub>A</sub> supply pin of the DAC2904.

While designing the layout, it is important to keep the analog signal traces separated from any digital line, in order to prevent noise coupling onto the analog signal path.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (November, 2003) to Revision C</b>	<b>Page</b>
• Updated document format to current standards .....	<a href="#">1</a>
• Added DAC2904IPFB orderable to <i>Package/Ordering Information</i> table .....	<a href="#">2</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC2904IPFB	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC2904Y	<a href="#">Samples</a>
DAC2904Y/1K	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC2904Y	<a href="#">Samples</a>
DAC2904Y/250	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC2904Y	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC2904Y/1K	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DAC2904Y/250	TQFP	PFB	48	250	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC2904Y/1K	TQFP	PFB	48	1000	367.0	367.0	38.0
DAC2904Y/250	TQFP	PFB	48	250	367.0	367.0	38.0

**TRAY**

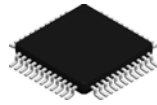

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC2904IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25



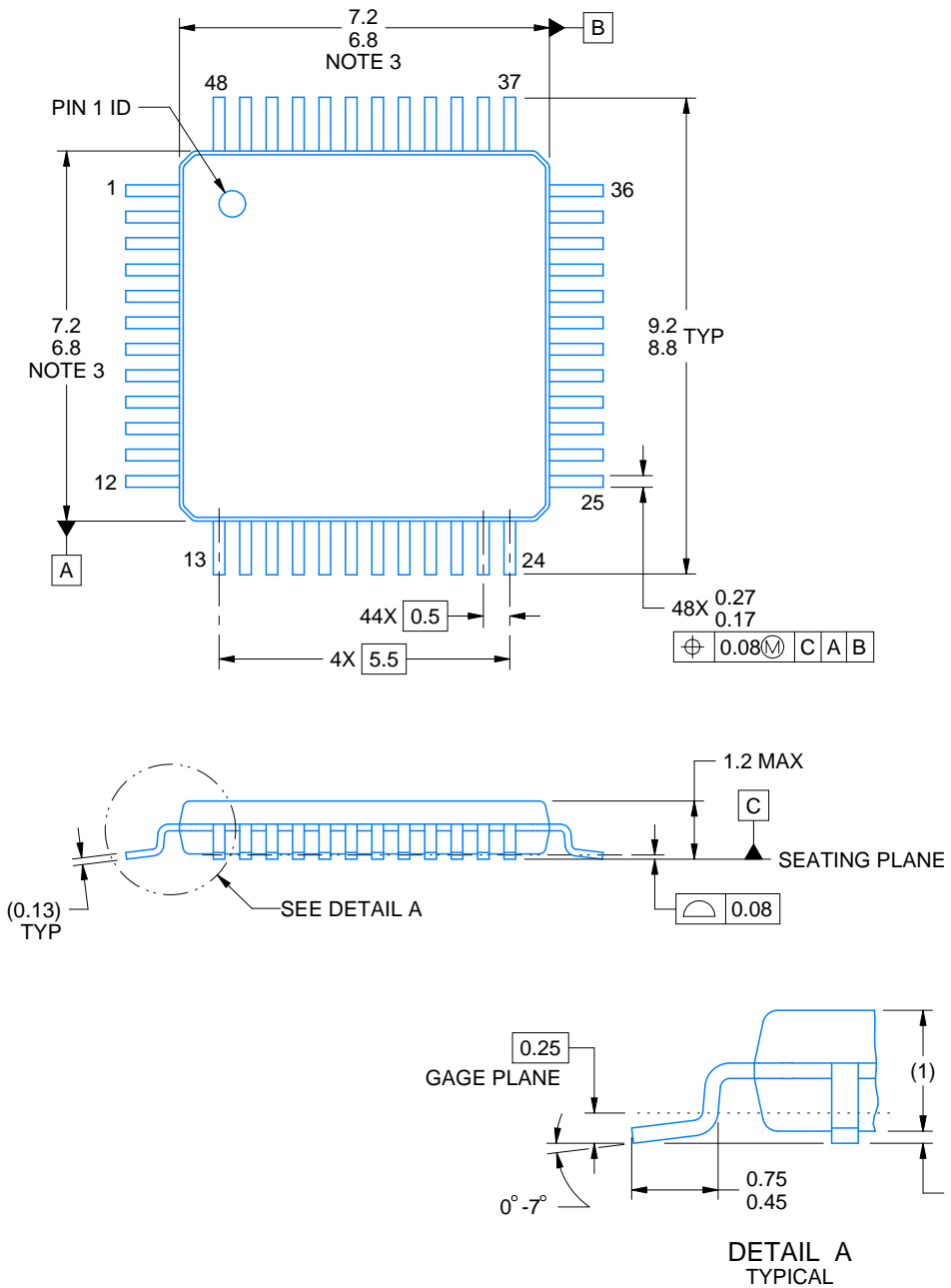
PFB0048A



# PACKAGE OUTLINE

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4215157/A 03/2024

NOTES:

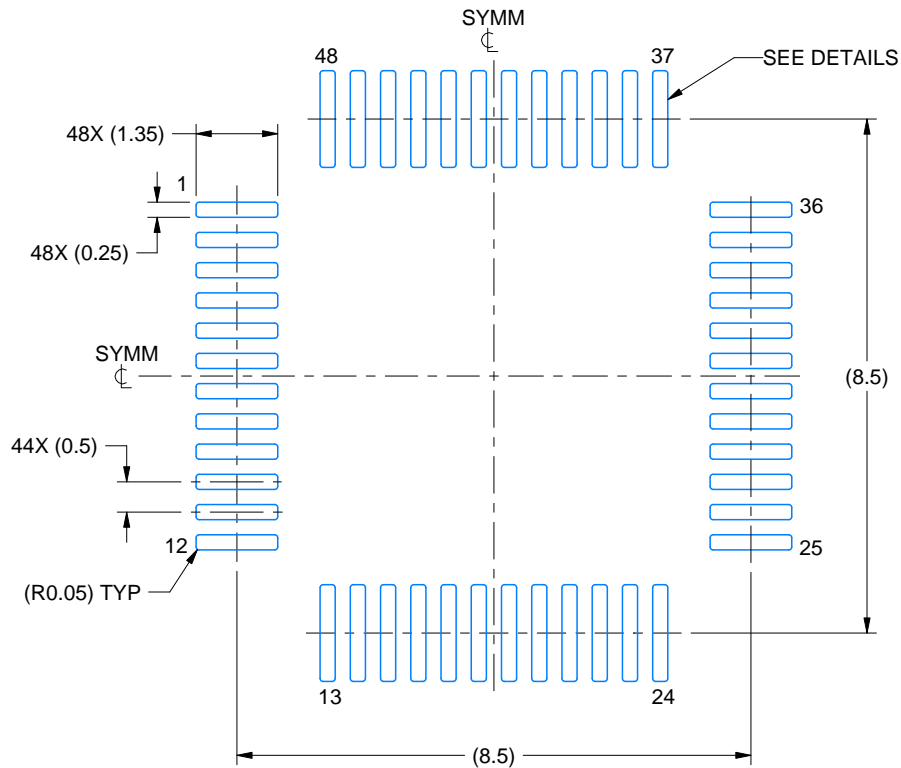
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

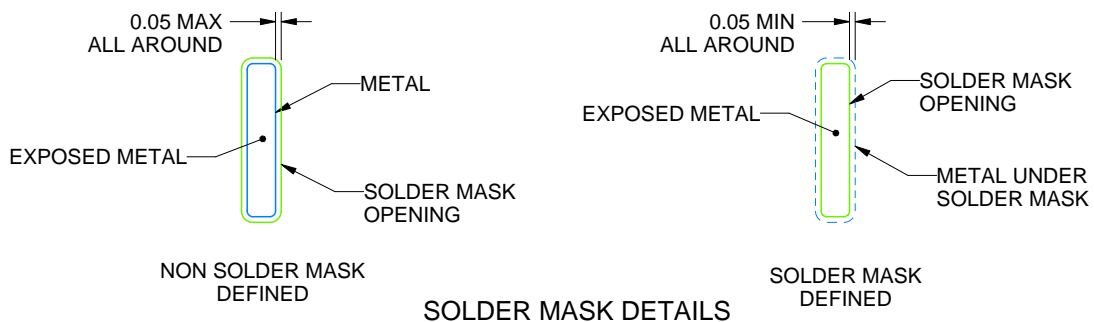
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



4215157/A 03/2024

NOTES: (continued)

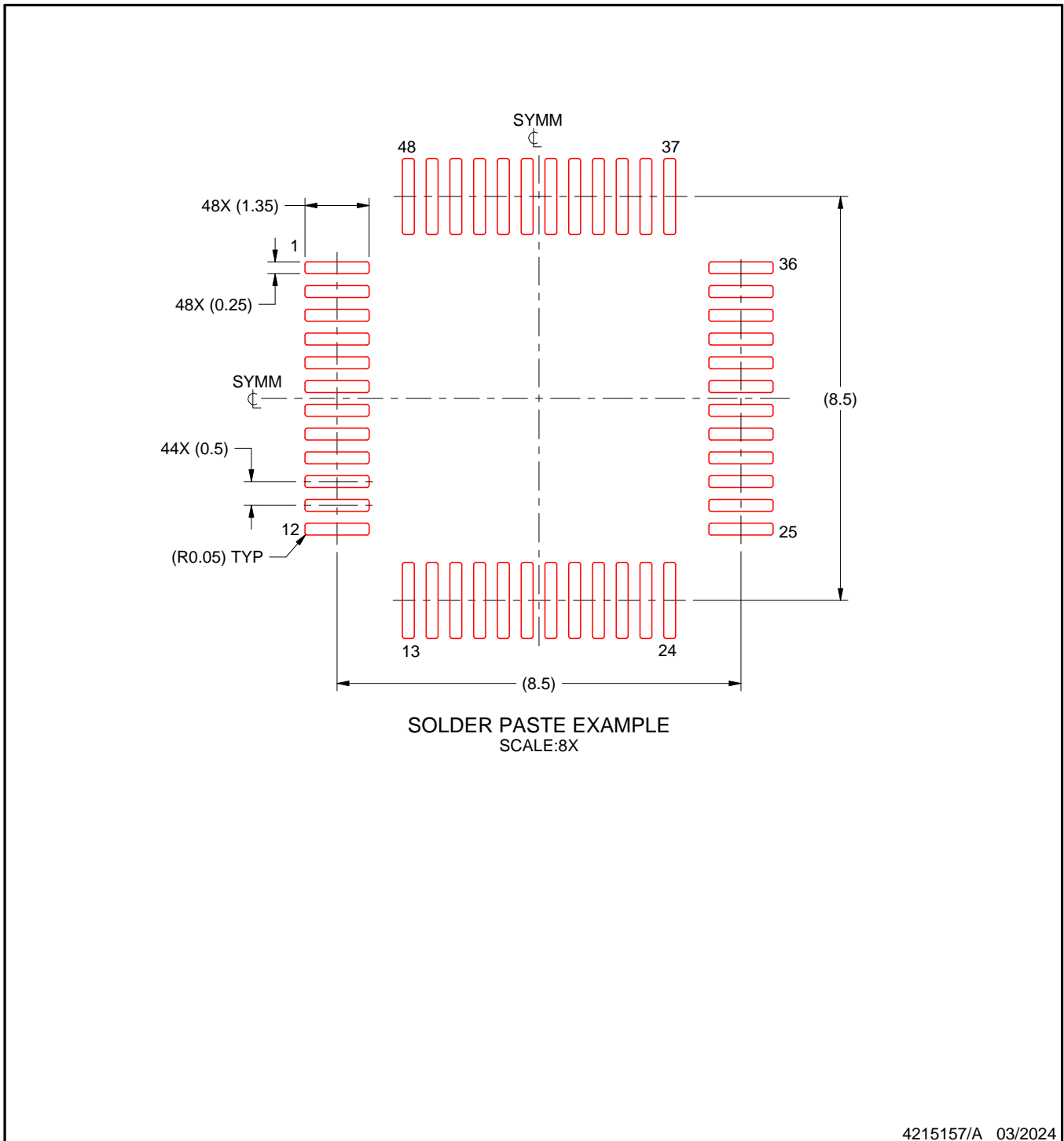
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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