DS90UH927Q-Q1 5-MHz to 85-MHz 24-Bit Color FPD-Link III Serializer with HDCP

1 Features

- Integrated HDCP Cipher Engine with On-Chip Key Storage
- Bidirectional Control Channel Interface with I^2C Compatible Serial Control Bus
- Low EMI FPD-Link Video Input
- Supports High Definition (720p) Digital Video Format
- 5-MHz to 85-MHz PCLK Supported
- RGB888 + VS, HS, DE and I^2S Audio Supported
- Up to 4 I^2S Digital Audio Inputs for Surround Sound Applications
- 4 Bidirectional GPIO Channels with 2 Dedicated Pins
- Single 3.3-V Supply with 1.8-V or 3.3-V Compatible LVCMOS I/O Interface
- AC-Coupled STP Interconnect up to 10 Meters
- DC-Balanced & Scrambled Data with Embedded Clock
- Supports HDCP Repeater Application
- Internal Pattern Generation
- Low Power Modes Minimize Power Dissipation
- Automotive Grade Product: AEC-Q100 Grade 2 Qualified
- > 8-kV HBM and ISO 10605 ESD Rating
- Backward Compatible Modes

2 Applications

- Automotive Displays for Navigation
- Rear Seat Entertainment Systems

3 Description

The DS90UH927Q-Q1 serializer, in conjunction with a DS90UH928Q-Q1 or DS90UH926Q-Q1 deserializer, provides a solution for secure distribution of content-protected digital video within automotive entertainment systems. This chipset translates a FPD-Link video interface into a single-pair high-speed serialized interface. The digital video data is protected using the industry standard High-Bandwidth Digital Content Protection (HDCP) copy protection scheme. The FPD-Link III serial bus scheme supports full duplex, high speed forward channel data transmission and low-speed back channel communication over a single differential link. Consolidation of audio, video, and control data over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

The DS90UH927Q-Q1 serializer embeds the clock, content protects the data payload, and level shifts the signals to high-speed differential signaling. Up to 24 RGB data bits are serialized along with three video control signals, and up to four I^2S data inputs.

The FPD-Link data interface allows for easy interfacing with data sources while also minimizing EMI and bus width. EMI on the high-speed FPD-Link III bus is minimized using low voltage differential signaling, data scrambling and randomization, and dc-balancing.

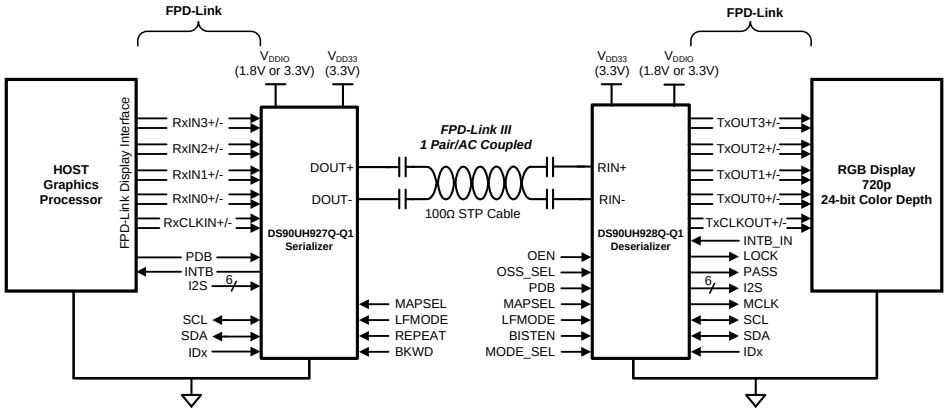
The HDCP cipher engine is implemented in both the serializer and deserializer. HDCP keys are stored in on-chip memory.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UH927Q-Q1	WQFN (40)	6.00 mm x 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



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4 Revision History

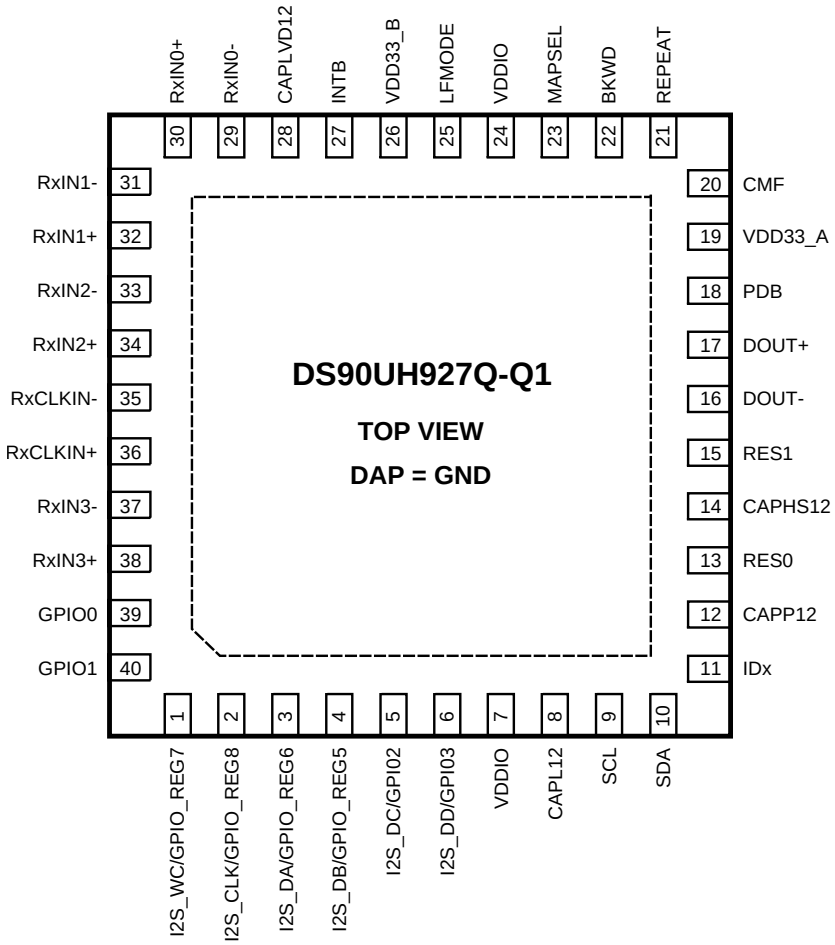
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2013) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision A (November 2012) to Revision B	Page
• Changed layout of National data sheet to TI format	56

5 Pin Configuration and Functions

RTA Package
40-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
FPD-LINK INPUT INTERFACE			
RxCLKIN-	35	I, LVDS	Inverting LVDS Clock Input The pair requires external 100-Ω differential termination for standard LVDS levels
RxCLKIN+	36	I, LVDS	True LVDS Clock Input The pair requires external 100-Ω differential termination for standard LVDS levels
RxIN[3:0]-	37, 33, 31, 29	I, LVDS	Inverting LVDS Data Inputs Each pair requires external 100-Ω differential termination for standard LVDS levels
RxIN[3:0]+	38, 34, 32, 30	I, LVDS	True LVDS Data Inputs Each pair requires external 100-Ω differential termination for standard LVDS levels
LVCMOS PARALLEL INTERFACE			
BKWD	22	I, LVCMOS w/ pull down	Backward Compatible Mode Select BKWD = 0, interfacing to DS90UH926/8Q-Q1 (Default) BKWD = 1, interfacing to DS90UR906/8Q-Q1, DS90UR916Q Requires a 10-kΩ pullup if set HIGH
GPIO[1:0]	40, 39	I/O, LVCMOS w/ pull down	General Purpose I/O See Table 1

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
I2S_DA I2S_DB I2S_DC I2S_DD	3 4 5 6	I, LVCMOS w/ pull down	Digital Audio Interface I^2S Data Inputs Shared with GPIO_REG6, GPIO_REG5, GPIO2, GPIO3
I2S_WC I2S_CLK	1 2	I, LVCMOS w/ pull down	Digital Audio Interface I^2S Word Clock and I^2S Bit Clock Inputs Shared with GPIO_REG7 and GPIO_REG8 Table 3
LFMODE	25	I, LVCMOS w/ pull down	Low Frequency Mode Select LFMODE = 0, 15 MHz ≤ RxCLKIN ≤ 85 MHz (Default) LFMODE = 1, 5 MHz ≤ RxCLKIN < 15 MHz Requires a 10-kΩ pullup if set HIGH
MAPSEL	23	I, LVCMOS w/ pull down	FPD-Link Input Map Select MAPSEL = 0, LSBs on RxIN3± (Default) MAPSEL = 1, MSBs on RxIN3± See Figure 19 and Figure 20 Requires a 10-kΩ pullup if set HIGH
REPEAT	21	I, LVCMOS w/ pull down	Repeater Mode Select REPEAT = 0, Repeater Mode disabled (Default) REPEAT = 1, Repeater Mode enabled Requires a 10-kΩ pullup if set HIGH
OPTIONAL PARALLEL INTERFACE			
GPIO[3:2]	6, 5	I/O, LVCMOS w/ pull down	General Purpose I/O Shared with I2S_DD and I2S_DC See Table 1
GPIO_REG[8:5]	2, 1, 3, 4	I/O, LVCMOS w/ pull down	Register-Only General Purpose I/O Shared with I2S_CLK, I2S_WC, I2S_DA, I2S_DB See Table 2
CONTROL AND CONFIGURATION			
IDx	11	I, Analog	I^2C Address Select External pullup to V_{DD33} is required under all conditions. **DO NOT FLOAT.** Connect to external pullup to V_{DD33} and pulldown to GND to create a voltage divider. See Figure 25 and Table 4
PDB	18	I, LVCMOS w/ pulldown	Power-down Mode Input Pin Must be driven or pulled up to V_{DD33}. Refer to *Power Supply Recommendations*. PDB = H, device is enabled (normal operation) PDB = L, device is powered down. When the device is in the powered down state, the Driver Outputs are both HIGH, the PLL is shutdown, and I_{DD} is minimized. Control Registers are **RESET**.
SCL	9	I/O, LVCMOS Open Drain	I^2C Clock Input / Output Interface Must have an external pullup to V_{DD33}. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
SDA	10	I/O, LVCMOS Open Drain	I^2C Data Input / Output Interface Must have an external pullup to V_{DD33}. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
STATUS			
INTB	27	O, LVCMOS Open Drain	HDCP Interrupt INTB = H, normal INTB = L, Interrupt request Recommended pullup: 4.7 kΩ to V_{DDIO}. **DO NOT FLOAT.**
FPD-LINK III SERIAL INTERFACE			
CMF	20	Analog	Common Mode Filter. Connect 0.1 µF to GND (required)
DOUT-	16	I/O, LVDS	Inverting Output The output must be AC-coupled with a 0.1-µF capacitor.
DOUT+	17	I/O, LVDS	True Output The output must be AC-coupled with a 0.1-µF capacitor.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
POWER AND GROUND(1)			
GND	DAP	Ground	Large metal contact at the bottom center of the device package **Connect to the ground plane (GND) with at least 9 vias.**
VDD33_A VDD33_B	19 26	Power	Power to on-chip regulator **3.0 V - 3.6 V**. Each pin requires a 4.7 µF capacitor to GND
VDDIO	7, 24	Power	LVCMOS I/O Power **1.8 V ±5% OR 3.0 V - 3.6 V**. Each pin requires 4.7 µF capacitor to GND
REGULATOR CAPACITOR			
CAPP12 CAPHS12 CAPLVD12	12 14 28	CAP	Decoupling capacitor connection for on-chip regulator Each requires a 4.7-µF decoupling capacitor to GND.
CAPL12	8	CAP	Decoupling capacitor connection for on-chip regulator Requires two 4.7-µF decoupling capacitors to GND
OTHER			
RES[1:0]	15, 13	GND	Reserved Connect to GND.

(1) The V_{DD} (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)(3)

	MIN	MAX	UNIT
Supply Voltage – V_{DD33}(4)	−0.3	4.0	V
Supply Voltage – V_{DDIO}(4)	−0.3	4.0	V
LVCMOS I/O Voltage	−0.3	(V_{DDIO} + 0.3)	V
Serializer Output Voltage	−0.3	2.75	V
Junction Temperature		150	°C
Storage Temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and www.ti.com/lit/an/snoa549c/snoa549c.pdf.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The DS90UH927Q-Q1 V_{DD33} and V_{DDIO} voltages require a specific ramp rate during power up. The power supply ramp time must be less than 1.5 ms with a monotonic rise

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±8000	V
		Charged device model (CDM), per AEC Q100-011		±1250	
		Machine model (MM)		±250	
		(IEC 61000-4-2, powered-up only) R_D = 330 Ω, C_S = 150 pF	Air Discharge (Pin 16 and 17)	±15000	V
			Contact Discharge (Pin 16 and 17)	±8000	
		(ISO 10605) R_D = 330 Ω, C_S = 150 pF/330 pF R_D = 2 kΩ, C_S = 150 pF/330 pF	Air Discharge (Pin 16 and 17)	±15000	
			Contact Discharge (Pin 16 and 17)	±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD33})		3	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO})(1)	Connect V_{DDIO} to 3.3 V and use 3.3-V IOs	3	3.3	3.6	V
	Connect V_{DDIO} to 1.8 V and use 1.8-V IOs	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)		−40	+25	+105	°C
PCLK Frequency		5		85	MHz
Supply Noise(2)				100	mV_{P-P}

(1) $V_{DDIO} < V_{DD33} + 0.3$ V
(2) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DD33} and V_{DDIO}supplies with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 50 MHz. The Des on the other hand shows no error when the noise frequency is less than 50 MHz.

6.4 Thermal Information

THERMAL METRIC(1)		DS90UH927Q-Q1 RTA (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
LVCMOS I/O								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 V to 3.6 V (4)		PDB	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 V to 3.6 V (4)			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{DDIO} = 3.0 V to 3.6 V (4)			−15	±1	+15	µA
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 V to 3.6 V		GPIO[1:0] I2S_CLK I2S_WC I2S_D [A,B,C,D] LFMODE MAPSEL BKWD REPEAT	2.0		V_{DDIO}	V
		V_{DDIO} = 1.71 V to 1.89 V			0.65× V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 V to 3.6 V			GND		0.8	V
		V_{DDIO} = 1.71 V to 1.89 V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{DDIO}	V_{DDIO} = 3.0 V to 3.6 V		−15	±1	+15	µA
			V_{DDIO} = 1.71 V to 1.89 V		−15	±1	+15	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	V_{DDIO} = 3.0 V to 3.6 V	GPIO[3:0], GPO_REG [8:5]	2.4		V_{DDIO}	V
			V_{DDIO} = 1.71 V to 1.89 V		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA	V_{DDIO} = 3.0 V to 3.6 V		GND		0.4	V
			V_{DDIO} = 1.71 V to 1.89 V		GND		0.45	V
I_{OS}	Output Short Circuit Current (5)	V_{OUT} = 0 V				−55		mA
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L,			−15		+15	µA
FPD-LINK LVDS RECEIVER								
V_{TH}	Threshold High Voltage	V_{CM} = 1.2 V		RxCLKIN± RxIN[3:0]±			+100	mV
V_{TL}	Threshold Low Voltage				−100			mV
$\|V_{ID}\|$	Differential Input Voltage Swing				200		600	mV
V_{CM}	Common Mode Voltage				0	1.2	2.4	V
I_{IN}	Input Current				−10		+10	µA

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages. Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50 MHz.
(4) PDB is specified to 3.3-V LVCMOS only and must be driven or pulled up to V_{DD33} or to $V_{DDIO} \geq$ 3.0 V
(5) I_{OS} is not specified for an indefinite period of time. Do not hold in short circuit for more than 500 ms or part damage may result

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III CML DRIVER							
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)	R_L = 100 Ω	DOUT±	800	1000	1200	mV_{p-p}
ΔV_{OD}	Output Voltage Unbalance				1	50	mV
V_{OS}	Offset Voltage – Single-ended	R_L = 100 Ω			2.5-0.25* V_{ODp-p} (TYP)		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended				1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, PDB = L or H					mA
R_T	Internal Termination Resistance - Differential			80	100	120	Ω
SUPPLY CURRENT							
I_{DD1}	Supply Current R_L = 100Ω, PCLK = 85MHz	Checkerboard Pattern	V_{DD33}= 3.6 V		135	160	mA
I_{DDIO1}			V_{DDIO} = 3.6 V		100	500	µA
			V_{DDIO} = 1.89 V		200	600	µA
I_{DD2}		Random Pattern PRBS7	V_{DD33}= 3.6 V		133		mA
I_{DDIO2}			V_{DDIO} = 3.6 V		100		µA
			V_{DDIO} = 1.89 V		100		µA
I_{DDS}	Supply Current — Remote Auto Power Down	reg_0x01[7]=1, Back channel Idle	V_{DD33} = 3.6 V		1.2	2.4	mA
I_{DDIOS}			V_{DDIO} = 3.6 V		4	30	µA
			V_{DDIO} = 1.89 V		5	30	µA
I_{DDZ}	Supply Current — Power Down	PDB = 0 V, All other LVCMOS inputs = 0 V	V_{DD33} = 3.6 V		1	2.2	mA
I_{DDIOZ}			V_{DDIO} = 3.6 V		8	20	µA
			V_{DDIO} = 1.89 V		4	20	µA

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK LVDS INPUT							
t_{RSP}	Receiver Strobe Position	See Figure 4	RxCLKIN±, RXIN[3:0]±	0.25	0.5	0.75	UI
FPD-LINK III CML I/O							
t_{LHT}	CML Output Low-to-High Transition Time	See Figure 3	DOUT+, DOUT-		100	140	ps
t_{HLT}	CML Output High-to-Low Transition Time				100	140	ps
t_{PLD}	Serializer PLL Lock Time	See Figure 5, (4)	PCLK = 5 MHz to 85 MHz			5	ms
t_{SD}	Delay — Latency	See Figure 6			146*T		ns
t_{TJIT}	Output Total Jitter, Bit Error Rate ≤1E-9, see Figure 7, (5) (6) (7) (8)(9)	Checkerboard Pattern PCLK=5 MHz, see Figure 8	RxCLKIN±		0.17	0.2	UI
		Checkerboard Pattern PCLK=85 MHz, see Figure 8			0.26	0.29	UI
t_{IJIT}	Input Jitter Tolerance, Bit Error Rate ≤1E-9 (8) (10)	f/40 < Jitter Freq < f/20, DES = DS90UH926Q-Q1	RxCLKIN±, f = 78 MHz		0.6		UI
		f/40 < Jitter Freq < f/20, DES = DS90UH928Q-Q1			0.5		UI
I^2S RECEIVER							
T_{I2S}	I^2S Clock Period, see Figure 10, (7) (11)	RxCLKIN± f=5 MHz to 85 MHz	I2S_CLK, PCLK = 5 MHz to 85 MHz		>4 / PCLK or >77		ns
T_{HC}	I^2S Clock High Time, see Figure 10, (11)		I2S_CLK	0.35			T_{I2S}
T_{LC}	I^2S Clock Low Time, see Figure 10, (11)		I2S_CLK	0.35			T_{I2S}
t_{sr}	I^2S Set-up Time		I2S_WC I2S_D[A,B,C,D]	0.2			T_{I2S}
t_{htr}	I^2S Hold Time		I2S_WC I2S_D[A,B,C,D]	0.2			T_{I2S}
OTHER I/O							
$t_{GPIO,FC}$	GPIO Pulse Width, Forward Channel		GPIO[3:0], PCLK = 5 MHz to 85 MHz	>2/PCLK			s
$t_{GPIO,BC}$	GPIO Pulse Width, Back Channel		GPIO[3:0]	20			µs

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages. Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50 MHz.
(4) t_{PLD} is the time required by the device to obtain lock when exiting power-down state with an active PCLK.
(5) Output jitter specs are dependent upon the input clock jitter at the SER.
(6) UI – Unit Interval is equivalent to one ideal serialized bit width. The UI scales with PCLK frequency.
(7) Specification is ensured by design and is not tested in production.
(8) Specification is ensured by characterization and is not tested in production.
(9) t_{TJIT} (@BER of 1E-9) specifies the allowable jitter on RxCLKIN±.
(10) Jitter Frequency is specified in conjunction with DS90UH928Q-Q1 PLL bandwidth.
(11) I^2S specifications for t_{LC} and t_{HC} pulses must each be greater than 2 PCLK periods to ensure sampling and supersedes the 0.35*T_{I2S_CLK} requirement. t_{LC} and t_{HC} must be longer than the greater of either 0.35*T_{I2S_CLK} or 2*PCLK.

6.7 DC and AC Serial Control Bus Characteristics

Over 3.3-V supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DDIO}		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DD33}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA or SCL, IOL = 1.25 mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-10		+10	µA
C_{in}	Input Capacitance	SDA or SCL		<5		pF

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(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages. Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50 MHz.

6.8 Recommended Timing Requirements for the Serial Control Bus

Over 3.3-V supply and temperature ranges unless otherwise specified.(1)(2)(3)

			MIN	NOM	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition, see Figure 9	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU;STA}$	Set Up time for a start or a repeated start condition, see Figure 9	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data Hold Time, see Figure 9	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU;DAT}$	Data Set Up Time, see Figure 9	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, see Figure 9	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START, see Figure 9	Standard Mode	4.7			µs
		Fast Mode	1.3			µs

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3V, V_{DDIO} = 1.8V or 3.3V, T_A = 25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages. Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the supply pins with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the serializer and output of the deserializer with 10 meter cable shows no error when the noise frequency is less than 50 MHz.

Recommended Timing Requirements for the Serial Control Bus (continued)

Over 3.3-V supply and temperature ranges unless otherwise specified.(1)(2)(3)

			MIN	NOM	MAX	UNIT
t_r	SCL & SDA Rise Time, see Figure 9	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, see Figure 9	Standard Mode			300	ns
		Fast mode			300	ns

6.9 Timing Requirements

			MIN	NOM	MAX	UNIT
t_R	SDA RiseTime – READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF, see Figure 9		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time — READ	See Figure 9		560		ns
$t_{HD;DAT}$	Hold Up Time — READ	See Figure 9		615		ns
t_{SP}	Input Filter			50		ns

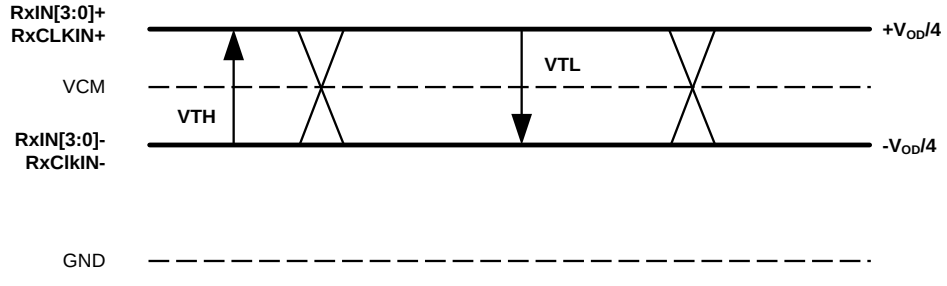


Figure 1. FPD-Link DC V_{TH}/V_{TL} Definition

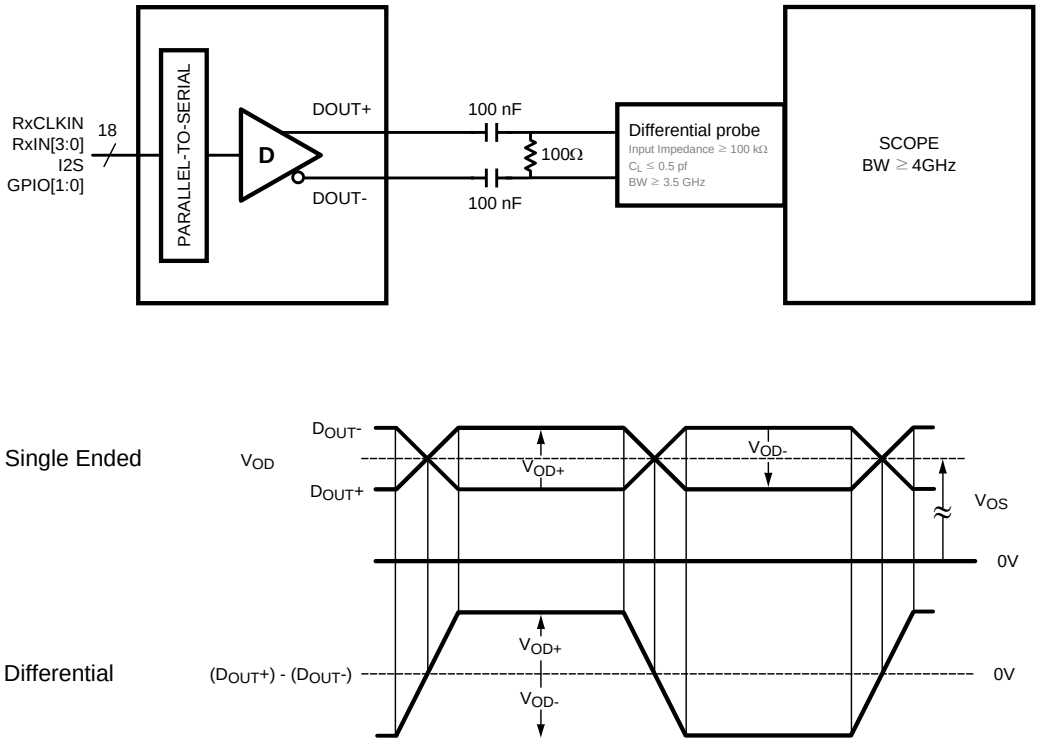


Figure 2. Serializer V_{OD} DC Output

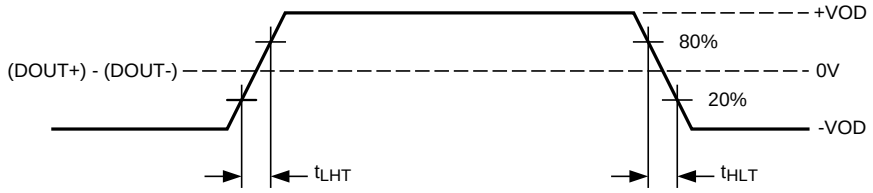


Figure 3. Output Transition Times

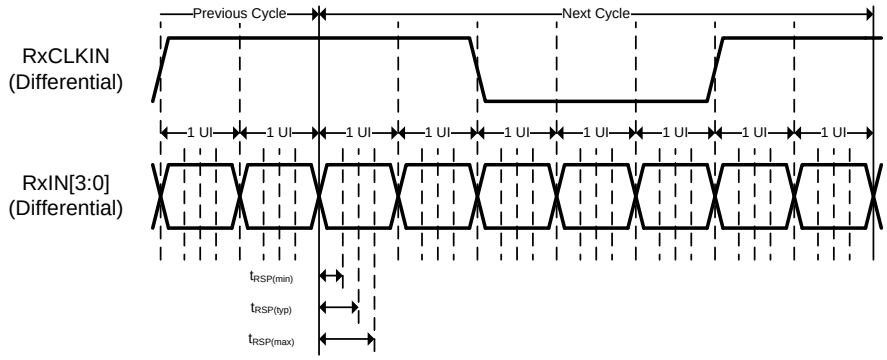


Figure 4. FPD-Link Input Strobe Position

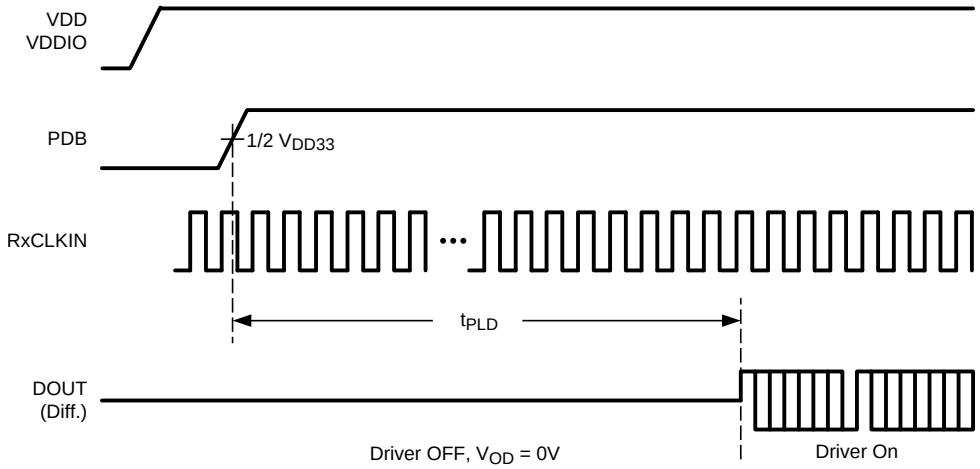


Figure 5. Serializer Lock Time

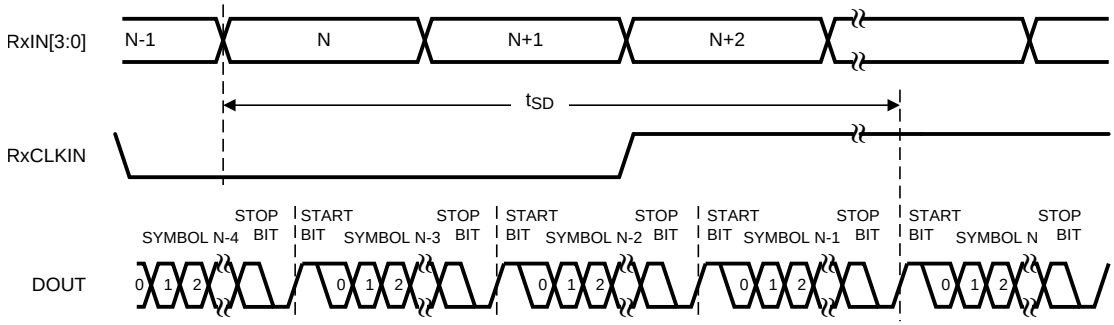


Figure 6. Latency Delay

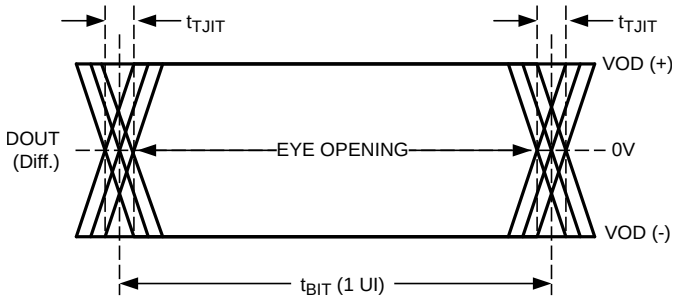


Figure 7. CML Serializer Output Jitter

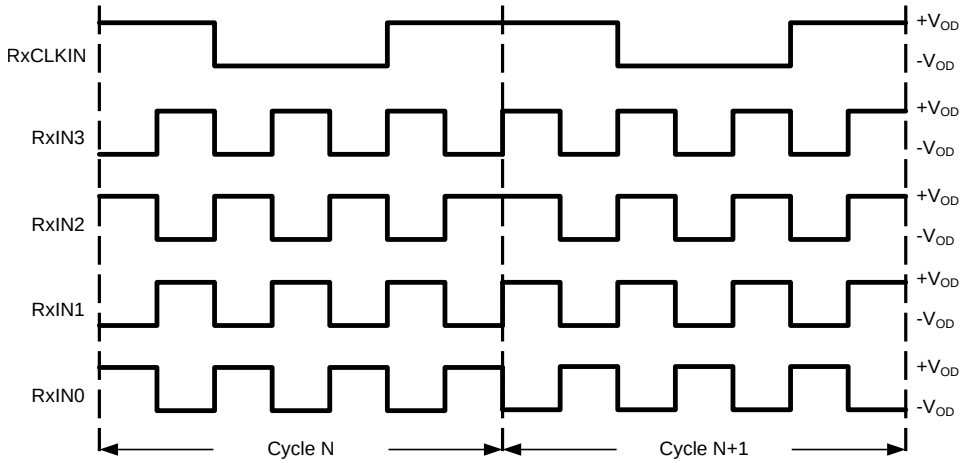


Figure 8. Checkerboard Data Pattern

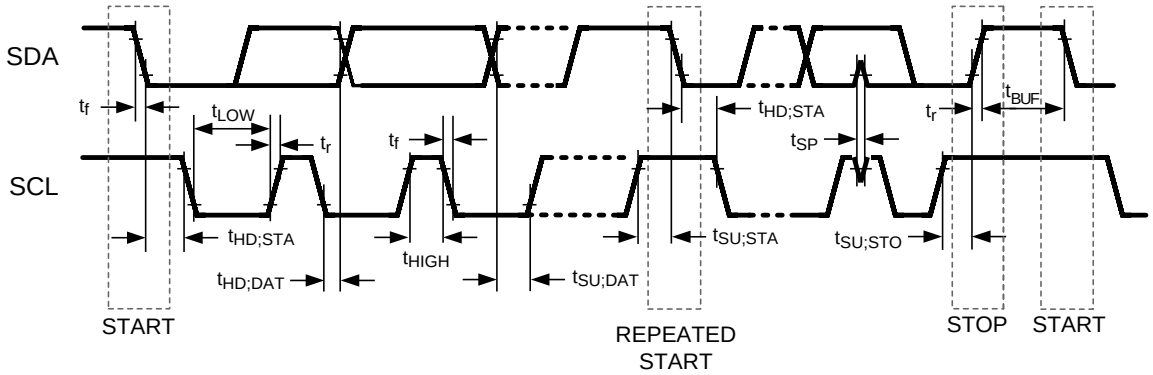


Figure 9. Serial Control Bus Timing Diagram

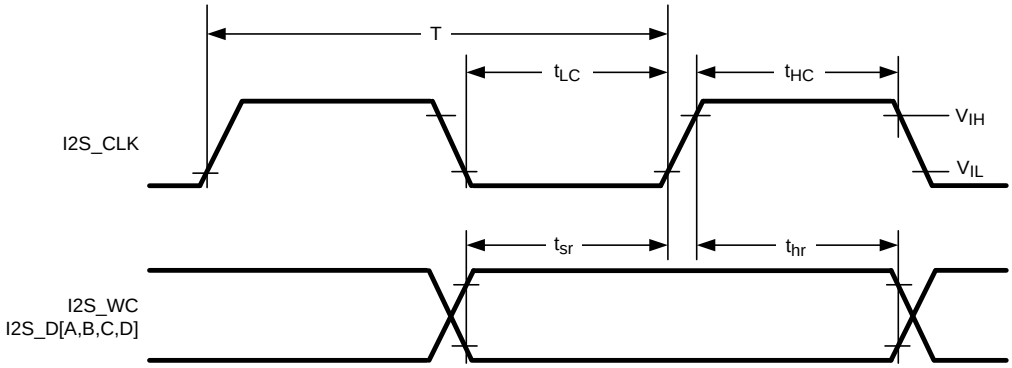


Figure 10. I²S Timing Diagram

6.10 Typical Characteristics

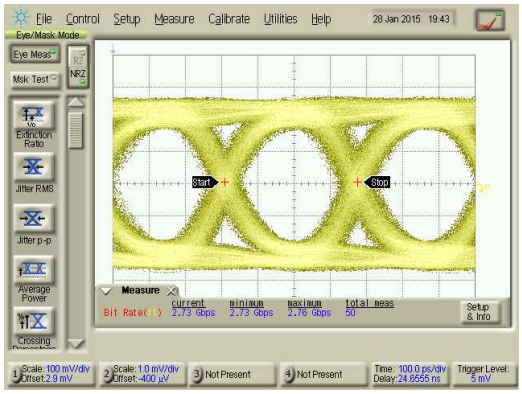


Figure 11. Serializer Eye with 78-MHz Input Clock

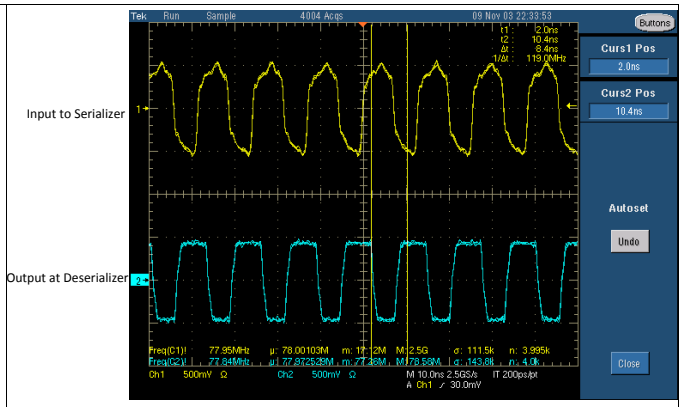


Figure 12. 78-MHz Clock at Serializer and Deserializer

7 Detailed Description

7.1 Overview

The DS90UH927Q-Q1 converts a FPD-Link interface (4 LVDS data channels + 1 LVDS Clock) to a FPD-Link III interface. This device transmits a 35-bit symbol over a single serial pair operating at up to a 2.975-Gbps line rate. The serial stream contains an embedded clock, video control signals, RGB video data, and audio data. The payload is DC-balanced to enhance signal quality and support AC coupling.

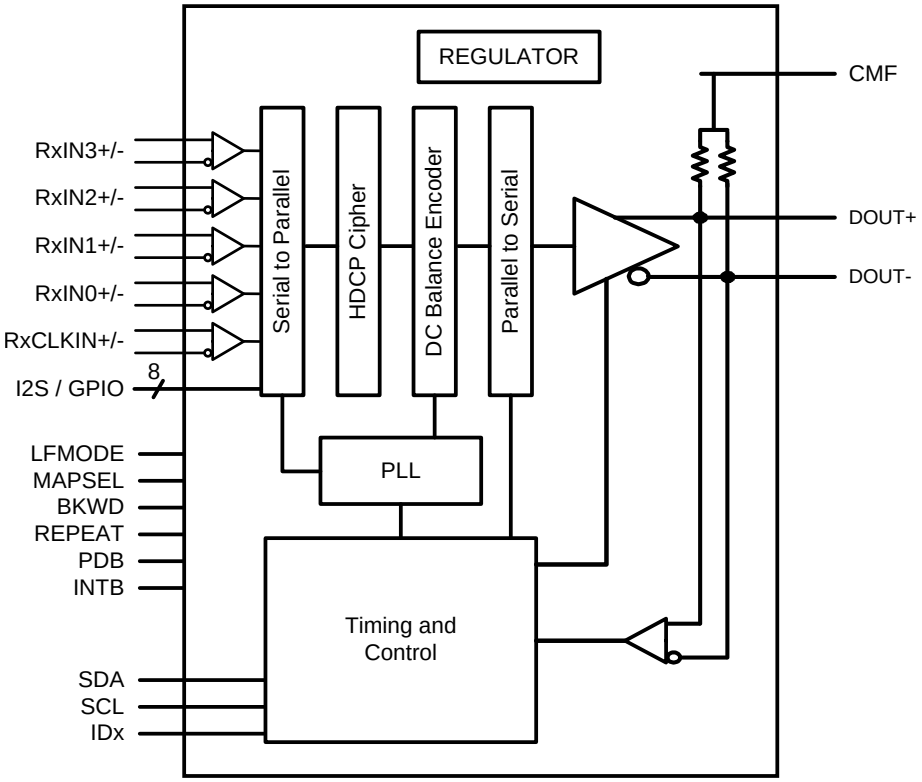
The DS90UH927Q-Q1 applies encryption to the video data using a High-Bandwidth Digital Content Protection (HDCP) Cipher, and transmits the encrypted data out through the FPD-Link III interface. Audio encryption is supported. On chip non-volatile memory stores the HDCP keys. All key exchanges are conducted over the FPD-Link III bidirectional control interface.

The DS90UH927Q-Q1 serializer is intended for use with a DS90UH928Q-Q1 or DS90UH926Q-Q1 deserializer, but is also backward compatible with DS90UR906Q, DS90UR908Q, DS90UR910Q, and DS90UR916Q FPD-Link II deserializers.

The DS90UH927Q-Q1 serializer and DS90UH928Q-Q1 or DS90UH926Q-Q1 deserializer incorporate an I^2C compatible interface. The I^2C compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I^2C slave devices.

The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I^2C transactions across the serial link from one I^2C bus to another. The implementation allows for arbitration with other I^2C compatible masters at either side of the serial link.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel is composed of a 35-bit frame containing RGB data, sync signals, HDCP, I^2C, and I^2S audio transmitted from Serializer to Deserializer. Figure 13 illustrates the serial stream generated per PCLK cycle into RxCLKIN±. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, DC-balanced and scrambled.

Figure 13. FPD-Link III Serial Stream

The device supports pixel clock ranges of 5 MHz to 15 MHz (LFMODE=1) and 15 MHz to 85 MHz (LFMODE=0). This corresponds to an application payload rate range of 155 Mbps to 2.635 Gbps, with an actual line rate range of 525 Mbps to 2.975 Gbps.

7.3.2 Low-Speed Back Channel Data Transfer

The Low-Speed Back Channel of the DS90UH927Q-Q1 provides bidirectional communication between the display and host processor. Data is transferred simultaneously over the same physical link as the high-speed forward channel data. The back channel transports I^2C, HDCP, CRC, and 4 bits of standard GPIO information with a 10 Mbps line rate.

7.3.3 Common Mode Filter Pin (CMF)

The serializer provides access to the center tap of the internal CML termination. A 0.1-µF capacitor must be connected from this pin to GND for additional common-mode filtering of the differential pair (Figure 29). This increases noise rejection capability in high-noise environments.

7.3.4 Video Control Signals

The video control signal bits embedded in the high-speed FPD-Link LVDS are subject to certain limitations relative to the video pixel clock period (PCLK). By default, the DS90UH927Q-Q1 applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

- Horizontal Sync (HS): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 5. HS can have at most two transitions per 130 PCLKs.
- Vertical Sync (VS): The video control signal pulse is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
- Data Enable Input (DE): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 5. DE can have at most two transitions per 130 PCLKs.

7.3.5 EMI Reduction Features

7.3.5.1 LVCMOS V_{DDIO} Option

The 1.8-V or 3.3-V LVCMOS inputs and outputs are powered from separate VDDIO supply pins to offer compatibility with external system interface signals. Note: When configuring the V_{DDIO} power supplies, all the single-ended control input pins for device need to scale together with the same operating V_{DDIO} levels. If V_{DDIO} is selected to operate in the 3.0 V to 3.6 V range, V_{DDIO} must be operated within 300 mV of V_{DD33}.

7.3.6 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

Feature Description (continued)

7.3.6.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK status is valid throughout the entire duration of BIST.

See Figure 14 for the BIST mode flow diagram.

Sample BIST Sequence

Step 1: For the DS90UH927Q-Q1 paired with a FPD-Link III Deserializer, BIST Mode is enabled via the BISTEN pin of Deserializer. The desired clock source is selected through the deserializer BISTC pin.

Step 2: The DS90UH927Q-Q1 serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. Figure 15 shows the waveform diagram of a typical BIST for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission, and so forth), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

Feature Description (continued)

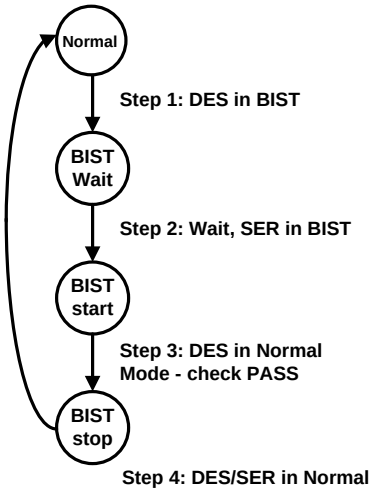


Figure 14. BIST Mode Flow Diagram

7.3.7 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, and so forth, and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 5). CRC errors are recorded in an 8-bit register in the serializer. The register is cleared when the serializer enters the BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of the last BIST run until cleared or the serializer enters BIST mode again.

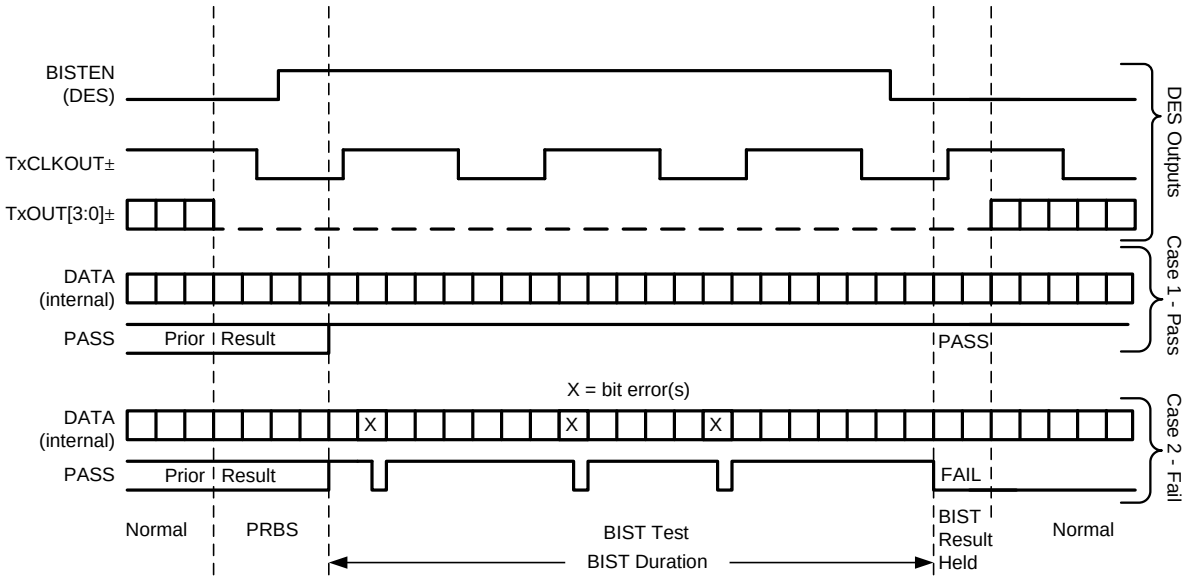


Figure 15. BIST Waveforms

Feature Description (continued)

7.3.8 Internal Pattern Generation

The DS90UH927Q-Q1 serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132).

7.3.8.1 Pattern Options

The DS90UH927Q-Q1 serializer pattern generator is capable of generating 17 default patterns for use in basic testing and debugging of panels. Each pattern can be inverted using register bits (Table 5). The 17 default patterns are listed as follows:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White
8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color (or its inversion) configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

Additionally, the Pattern Generator incorporates one user-configurable full-screen 24-bit color, which is controlled by the PGRS, PGGS, and PGBS registers. This is pattern #14. One of the pattern options is statically selected in the PGCTL register when Auto-Scrolling is disabled. The PGTSC and PGTSO1-8 registers control the pattern selection and order when Auto-Scrolling is enabled.

7.3.8.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (Table 5). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0.

7.3.8.3 Video Timing Modes

The Pattern Generator has two video timing modes – external and internal. In external timing mode, the Pattern Generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the Pattern Generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the Pattern Generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or Internal timing with External Clock are enabled by the control registers (Table 5).

Feature Description (continued)

7.3.8.4 External Timing

In external timing mode, the Pattern Generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two pixel clock delay. It extracts the active frame dimensions from the incoming signals in order to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the Pattern Generator determines the Vertical Blank time by detecting a long period of pixel clocks without DE asserted.

7.3.8.5 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

7.3.8.6 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

7.3.9 Remote Auto Power Down Mode

The DS90UH927Q-Q1 serializer features a Remote Auto Power Down mode. This feature is enabled and disabled through the register bit 0x01[7] (Table 5). When the back channel is not detected, either due to an idle or powered-down deserializer, the serializer enters remote auto power down mode. Power dissipation of the serializer is significantly reduced in this mode. The serializer automatically attempts to resume normal operation upon detection of an active back channel from the deserializer. To complete the wake-up process and reactivate forward channel operation, the remote power-down feature must be disabled by either a local I^2C host, or by an auto-ACK I^2C transaction from a remote I^2C host located at the deserializer. The Remote Auto Power Down Sleep/Wake cycle is shown below in Figure 16:

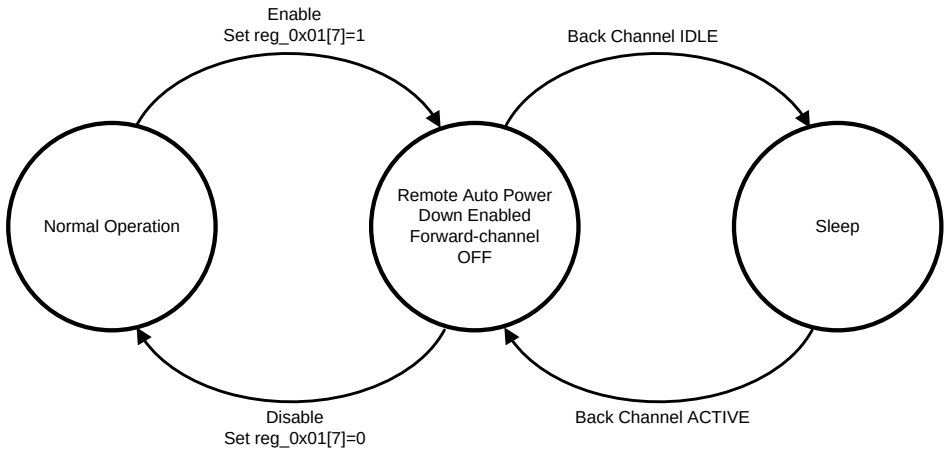


Figure 16. Remote Auto Power Down Sleep/Wake Cycle

To resume normal operation, the Remote Auto Power Down feature must be disabled in the device control register. This may be accomplished from a local I^2C controller by writing reg_0x01[7]=0 (Table 5). To disable from a remote I^2C controller located at the deserializer, perform the following procedure to complete the wake-up process:

1. Power up remote deserializer (back channel must be active)
2. Enable I^2C PASS-THROUGH ALL by setting deserializer register reg_0x05[7]=1
3. Enable I^2C AUTO ACK by setting deserializer register reg_0x03[2]=1
4. Disable Remote Auto Power Down by setting serializer register reg_0x01[7]=0
5. Disable I^2C AUTO ACK by setting deserializer register reg_0x03[2]=0

Feature Description (continued)

6. Disable I^2C PASS-THROUGH ALL by setting deserializer register reg_0x05[7]=0

7.3.10 Input RxCLKIN Loss Detect

The serializer can be programmed to enter a low power SLEEP state when the input clock (PCLK) is lost. A clock loss condition is detected when PCLK drops below approximately 1MHz. When a PCLK is detected again, the serializer will then lock to the incoming RxCLKIN±. Note: when RxCLKIN± is lost, the optional Serial Bus Control Registers values are still retained. See (Table 5) for more information.

7.3.11 Serial Link Fault Detect

The DS90UH927Q-Q1 can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Table 5). The DS90UH927Q-Q1 will detect any of the following conditions:

1. Cable open
2. + to - short
3. + to GND short
4. - to GND short
5. + to battery short
6. - to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

NOTE

The device will detect any of the above conditions, but does not report specifically which one has occurred.

7.3.12 INTERRUPT Pin (INTB)

1. On the DS90UH927Q-Q1 serializer, set register reg_0xC6[5] = 1 and 0xC6[0] = 1 (Table 5) to configure the interrupt.
2. On the serializer, read from HDCP_ISR register 0xC7 to arm the interrupt for the first time.
3. When INTB_IN on the deserializer (DS90UH926Q-Q1 or DS90UH928Q-Q1) is set LOW, the INTB pin on the serializer also pulls low, indicating an interrupt condition.
4. The external controller detects INTB = LOW and reads the HDCP_ISR register (Table 5) to determine the interrupt source. Reading this register also clears and resets the interrupt.

7.3.13 General-Purpose I/O

7.3.13.1 GPIO[3:0]

In normal operation, GPIO[3:0] may be used as general purpose IOs in either forward channel (inputs) or back channel (outputs) applications. GPIO modes may be configured from the registers (Table 5). GPIO[1:0] are dedicated pins and GPIO[3:2] are shared with I2S_DC and I2S_DD respectively. Note: if the DS90UH927Q-Q1 is paired with a DS90UH926Q-Q1 deserializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the DS90UH927 serializer. To enable 18-bit mode, set serializer register reg_0x12[2] = 1. 18-bit mode will be auto-loaded into the deserializer from the serializer. See Table 1 for GPIO enable and configuration.

Table 1. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3	DS90UH927Q-Q1	0x0F = 0x03	0x0F = 0x05
	DS90UH926/8Q-Q1	0x1F = 0x05	0x1F = 0x03
GPIO2	DS90UH927Q-Q1	0x0E = 0x30	0x0E = 0x50
	DS90UH926/8Q-Q1	0x1E = 0x50	0x1E = 0x30

Feature Description (continued)

Table 1. GPIO Enable and Configuration (continued)

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO1	DS90UH927Q-Q1	0x0E = 0x03	0x0E = 0x05
	DS90UH926/8Q-Q1	0x1E = 0x05	0x1E = 0x03
GPIO0	DS90UH927Q-Q1	0x0D = 0x03	0x0D = 0x05
	DS90UH926/8Q-Q1	0x1D = 0x05	0x1D = 0x03

The input value present on GPIO[3:0] may also be read from register, or configured to local output mode (Table 5).

7.3.13.2 GPIO[8:5]

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I^2S pins and will override I^2S input if enabled into REG_GPIO mode. See Table 2 for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Low-Speed Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 2. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG8	0x11 = 0x01	Output, L
	0x11 = 0x09	Output, H
	0x11 = 0x03	Input, Read: 0x1D[0]
GPIO_REG7	0x10 = 0x01	Output, L
	0x10 = 0x09	Output, H
	0x10 = 0x03	Input, Read: 0x1C[7]
GPIO_REG6	0x10 = 0x01	Output, L
	0x10 = 0x09	Output, H
	0x10 = 0x03	Input, Read: 0x1C[6]
GPIO_REG5	0x0F = 0x01	Output, L
	0x0F = 0x09	Output, H
	0x0F = 0x03	Input, Read: 0x1C[5]
GPIO3	0x0F = 0x01	Output, L
	0x0F = 0x09	Output, H
	0x0F = 0x03	Input, Read: 0x1C[3]
GPIO2	0x0E = 0x01	Output, L
	0x0E = 0x09	Output, H
	0x0E = 0x03	Input, Read: 0x1C[2]
GPIO1	0x0E = 0x01	Output, L
	0x0E = 0x09	Output, H
	0x0E = 0x03	Input, Read: 0x1C[1]
GPIO0	0x0D = 0x01	Output, L
	0x0D = 0x09	Output, H
	0x0D = 0x03	Input, Read: 0x1C[0]

7.3.14 I²S Audio Interface

The DS90UH927Q-Q1 serializer features six I²S input pins that, when paired with a DS90UH928Q-Q1 deserializer, supports surround sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the smaller of <PCLK/2 or <13 MHz. Four I²S data inputs transport two channels of I²S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input. I²S audio transport is not available in Backwards Compatibility Mode (BKWD = 1).

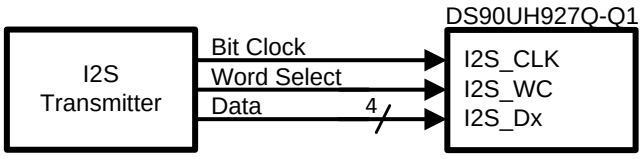


Figure 17. I²S Connection Diagram

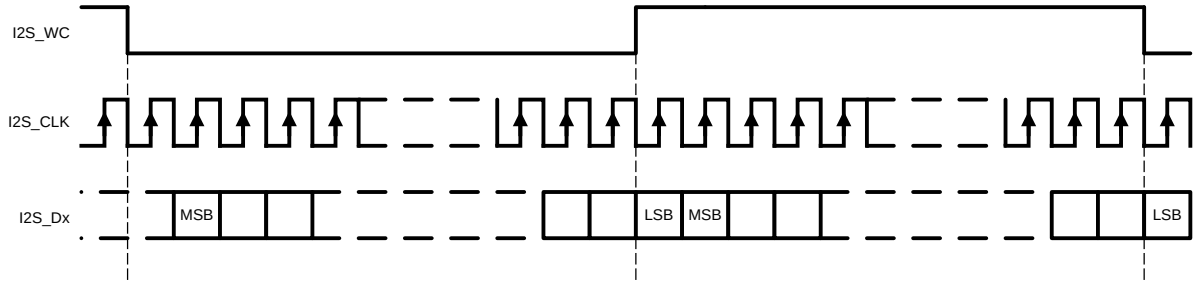


Figure 18. I²S Frame Timing Diagram

When paired with a DS90UH926Q-Q1, the DS90UH927Q-Q1 I²S interface supports a single I²S data input through I2S_DA (24-bit video mode), or two I²S data inputs through I2S_DA and I2S_DB (18-bit video mode).

Table 3 covers several common I²S sample rates:

Table 3. Audio Interface Frequencies

Sample Rate (kHz)	I2S Data Word Size (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

7.3.14.1 I^2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames may be disabled from control registers if Forward Channel Frame Transport of I^2S data is desired. In this mode, only I2S_DA is transmitted to the DS90UH928Q-Q1 deserializer. If connected to a DS90UH926Q-Q1 deserializer, I2S_DA and I2S_DB are transmitted. Surround Sound Mode, which transmits all four I^2S data inputs (I2S_D[A..D]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UH928Q-Q1 deserializer.

7.3.14.2 I^2S Repeater

I^2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated via Data Island Transport on the FPD-Link interface during the video blanking periods. If frame transport is desired, then the I^2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level deserializer automatically configures downstream DS90UH927Q-Q1 serializers and DS90UH928Q-Q1 deserializers for surround sound transport utilizing Data Island Transport. If 4-channel operation utilizing I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (Table 5).

A DS90UH927Q-Q1 serializer configured in repeater mode may also regenerate I^2S audio from its I^2S input pins in lieu of Data Island frames. See the HDCP Repeater Connection Diagram (Figure 23) and the I^2C Control Registers (Table 5) for additional details.

7.3.15 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. It consists of the Pattern Generator Indirect Address (PGIA reg_0x66 — Table 5) and the Pattern Generator Indirect Data (PGID reg_0x67 — Table 5). See Application Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132).

7.4 Device Functional Modes

7.4.1 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}, where V_{DDIO} = 3.0 V to 3.6 V or V_{DD33}. To save power, disable the link when the display is not needed (PDB = LOW). Ensure that this pin is not driven HIGH before V_{DD33} and V_{DDIO} have reached final levels. When PDB is driven low, ensure that the pin is driven to 0 V for at least 1.5 ms before releasing or driving high. In the case where PDB is pulled up to V_{DDIO} = 3.0 V to 3.6 V or V_{DD33} directly, a 10-kΩ pullup resistor and a >10-µF capacitor to ground are required (See Figure 29).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held low for a minimum period of time. See *AC Electrical Characteristics* for more information.

7.4.2 Backward Compatible Mode

The DS90UH927Q-Q1 is also backward compatible to DS90UR906Q, DS90UR908Q FPD, and DS90UR916Q FPD-Link II deserializers for PCLK frequencies ranging from 5 MHz to 65 MHz. It is also backward compatible with the DS90UR910Q for PCLK frequencies ranging from 5 MHz to 75 MHz. The serializer transmits 28-bits of data over a single serial FPD-Link II pair operating at a payload rate of 120 Mbps to 1.8 Gbps, corresponding to a line rate of 140 Mbps to 2.1 Gbps. The Backward Compatibility configuration can be selected through the BKWD pin or programmed through the configuration register (Table 5). The bidirectional control channel, HDCP, bidirectional GPIOs, I^2S, and interrupt (INTB) are not active in this mode. However, local I^2C access to the serializer is still available. Note: PCLK frequency range in this mode is 15 MHz to 75 MHz for LFMODE=0 and 5 MHZ to <15 MHz for LFMODE=1.

Device Functional Modes (continued)

7.4.3 Low Frequency Optimization (LFMODE)

The LFMODE is set via register (Table 5) or LFMODE Pin. This mode optimizes device operation for lower input data clock ranges supported by the serializer. If LFMODE is Low (LFMODE = 0, default), the RxCLKIN± frequency is between 15 MHz and 85 MHz. If LFMODE is High (LFMODE = 1), the RxCLKIN± frequency is between 5 MHz and <15 MHz. Note: when the device LFMODE is changed, a PDB reset is required. When LFMODE is high (LFMODE=1), the line rate relative to the input data rate is multiplied by four. Thus, for the operating range of 5 MHz to <15 MHz, the line rate is 700 Mbps to <2.1 Gbps with an effective data payload of 175 Mbps to 525 Mbps. Note: for Backwards Compatibility Mode (BKWD=1), the line rate relative to the input data rate remains the same.

7.4.4 FPD-Link Input Frame and Color Bit Mapping Select

The DS90UH927Q-Q1 can be configured to accept 24-bit color (8-bit RGB) with 2 different mapping schemes: LSBs on RxIN[3]±, shown in Figure 19, or MSBs on RxIN[3], shown in Figure 20. Each frame corresponds to a single pixel clock (PCLK) cycle. The LVDS clock input to RxCLKIN± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by MAPSEL pin or by Register (Table 5).

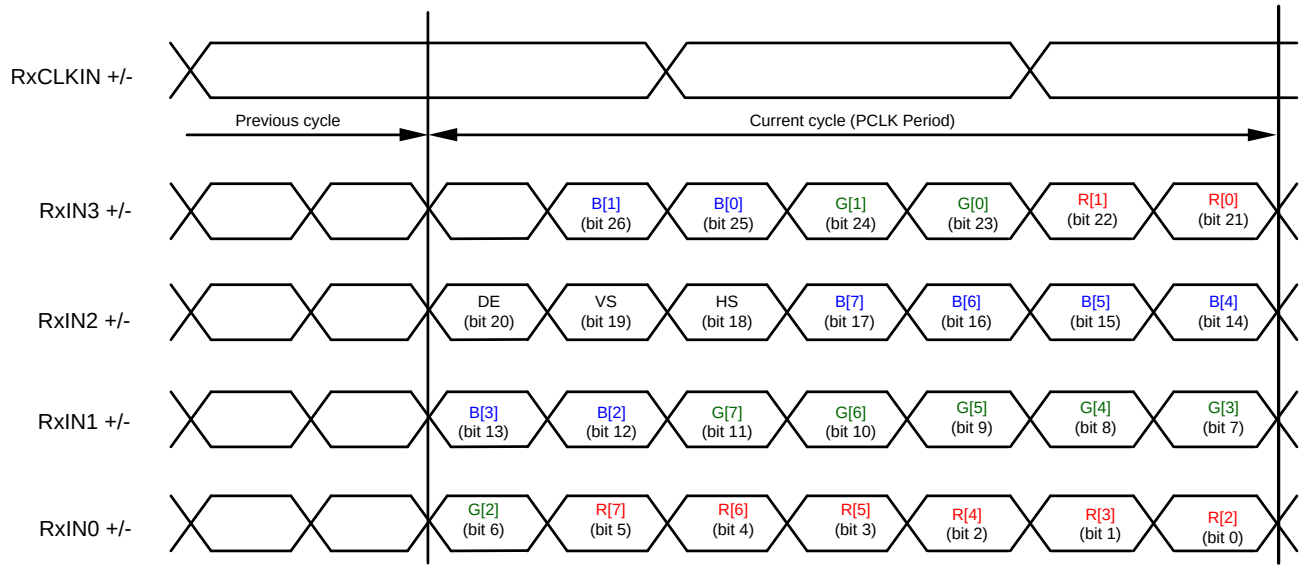


Figure 19. FPD-Link Mapping: LSBs on RxIN3 (MAPSEL=L)

Device Functional Modes (continued)

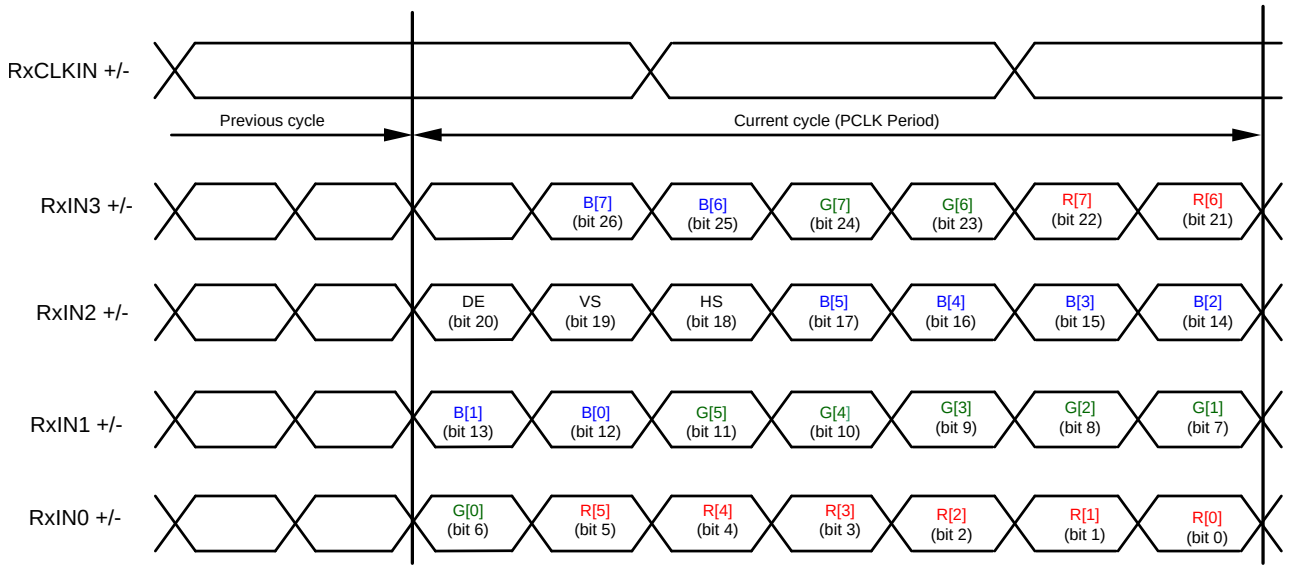


Figure 20. FPD-Link Mapping: MSBs on RxIN3 (MAPSEL=H)

7.4.5 HDCP

The Cipher function is implemented in the serializer per HDCP v1.3 specification. The DS90UH927Q-Q1 provides HDCP encryption of audiovisual content when connected to an HDCP capable FPD-Link III deserializer. HDCP authentication and shared key generation is performed using the HDCP Control Channel which is embedded in the forward and backward channels of the serial link. On-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

The DS90UH927Q-Q1 uses the Cipher engine to encrypt the data as per HDCP v1.3. The encrypted data is sent through the FPD-Link III interface.

7.4.5.1 HDCP Repeater

The supported HDCP Repeater application provides a mechanism to extend HDCP transmission over multiple links to multiple display devices. It authenticates all HDCP Receivers in the system and distributes protected content to the HDCP Receivers using the encryption mechanisms provided in the HDCP specification.

7.4.5.2 HDCP I^2S Audio Encryption

When HDCP is active, packetized Data Island Transport audio is also encrypted along with the video data per HDCP v.1.3. I^2S audio transmitted in Forward Channel Frame Transport mode is not encrypted. Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

7.4.5.3 Repeater Configuration

In HDCP repeater application, this document refers to the DS90UH927Q-Q1 as the HDCP Transmitter (TX), and refers to the DS90UH928Q-Q1 as the HDCP Receiver (RX). Figure 21 shows the maximum configuration supported for HDCP Repeater implementations using the DS90UH925/7Q-Q1 (TX), and DS90UH926/8Q-Q1 (RX). Two levels of HDCP Repeaters are supported with a maximum of three HDCP Transmitters per HDCP Receiver. To ensure parallel video interface compatibility, repeater nodes should feature either the DS90UH926Q-Q1/DS90UH925Q (RX/TX) chipset or the DS90UH927Q-Q1/DS90UH928Q-Q1 (TX/RX) chipset.

Device Functional Modes (continued)

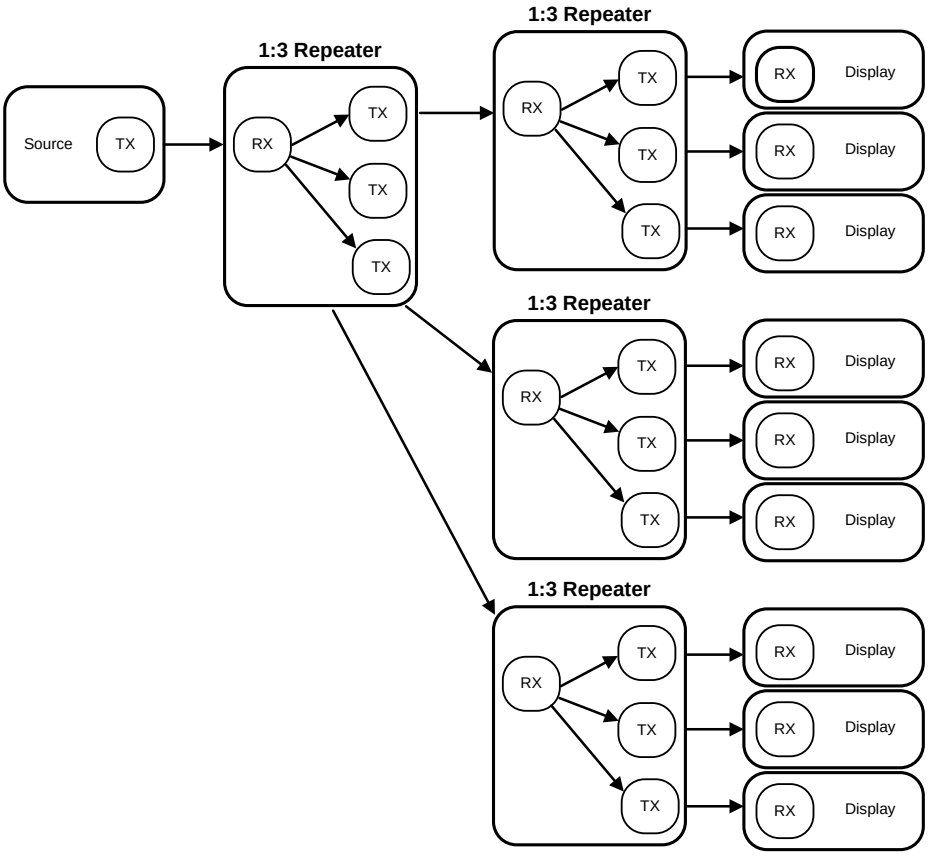


Figure 21. HDCP Maximum Repeater Application

In a repeater application, the I^2C interface at each TX and RX may be configured to transparently pass I^2C communications upstream or downstream to any I^2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

To support HDCP Repeater operation, the RX includes the ability to control the downstream authentication process, assemble the KSV list for downstream HDCP Receivers, and pass the KSV list to the upstream HDCP Transmitter. An I^2C master within the RX communicates with the I^2C slave within the TX. The TX handles authenticating with a downstream HDCP Receiver and makes status available through the I^2C interface. The RX monitors the transmit port status for each TX and reads downstream KSV and KSV list values from the TX.

In addition to the I^2C interface used to control the authentication process, the HDCP Repeater implementation includes two other interfaces. The FPD-Link LVDS interface provides the unencrypted video data in 24-bit RGB format and includes the DE/VS/HS control signals. In addition to providing the RGB video data, the LVDS interface communicates control information and packetized audio data during video blanking intervals. A separate I^2S audio interface may optionally be used to send I^2S audio data between the HDCP Receiver and HDCP Transmitter in place of using the packetized audio. All audio and video data is decrypted at the output of the HDCP Receiver and is re-encrypted by the HDCP Transmitter. Figure 22 provides more detailed block diagram of a 1:2 HDCP repeater configuration.

If video data is output to a local display, White Balancing and Hi-FRC dithering functions should not be used as they will block encrypted I^2S audio.

Device Functional Modes (continued)

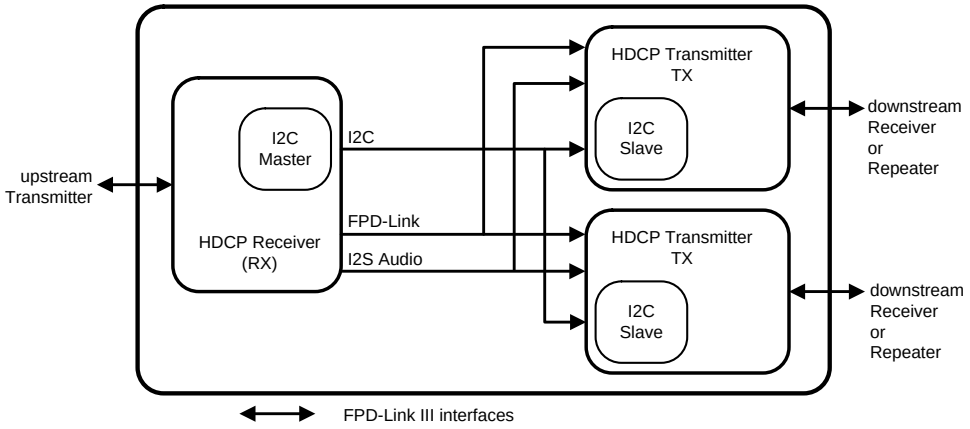


Figure 22. HDCP 1:2 Repeater Configuration

Device Functional Modes (continued)

7.4.5.4 Repeater Connections

The HDCP Repeater requires the following connections between the HDCP Receiver and each HDCP Transmitter Figure 23.

1. Video Data – Connect all FPD-Link data and clock pairs
2. I^2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} or V_{DDIO} = 3.0 V to 3.6 V with 4.7-kΩ resistors.
3. Audio (optional) – Connect I2S_CLK, I2S_WC, and I2S_Dx signals.
4. IDx pin – Each HDCP Transmitter and Receiver must have a unique I^2C address.
5. REPEAT pin — All HDCP Transmitters and Receivers must be set into Repeater Mode.
6. Interrupt pin – Connect DS90UH928Q-Q1 INTB_IN pin to DS90UH927Q-Q1 INTB pin. The signal must be pulled up to V_{DDIO}.

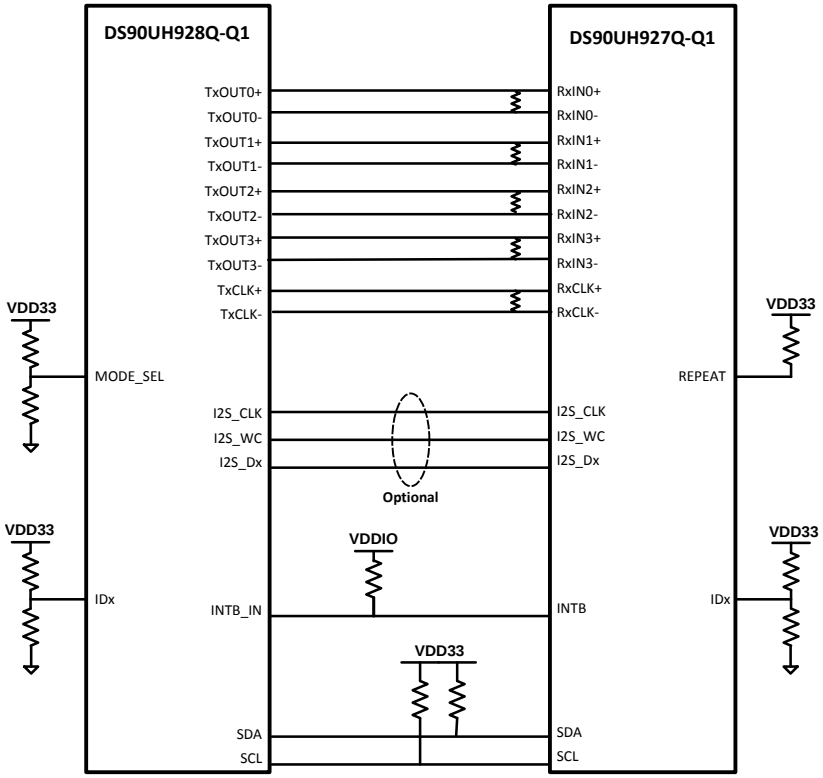


Figure 23. HDCP Repeater Connection Diagram

7.4.5.4.1 Repeater Fan-Out Electrical Requirements

Repeater applications requiring fan-out from one DS90UH928Q-Q1 deserializer to up to three DS90UH927Q-Q1 serializers requires special considerations for routing and termination of the FPD-Link differential traces. Figure 24 details the requirements that must be met for each signal pair:

Device Functional Modes (continued)

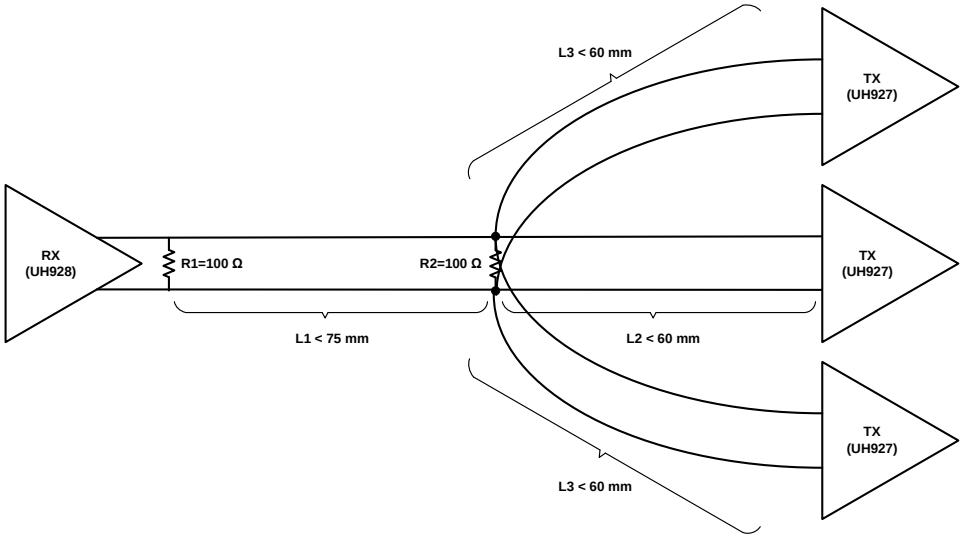


Figure 24. FPD-Link Fan-Out Electrical Requirements

7.5 Programming

7.5.1 Serial Control Bus

The DS90UH927Q-Q1 may also be configured by the use of an I^2C compatible serial control bus. Multiple devices may share the serial control bus (up to 10 device addresses supported). The device address is set via a resistor divider (R1 and R2 — see Figure 25) connected to the IDx pin.

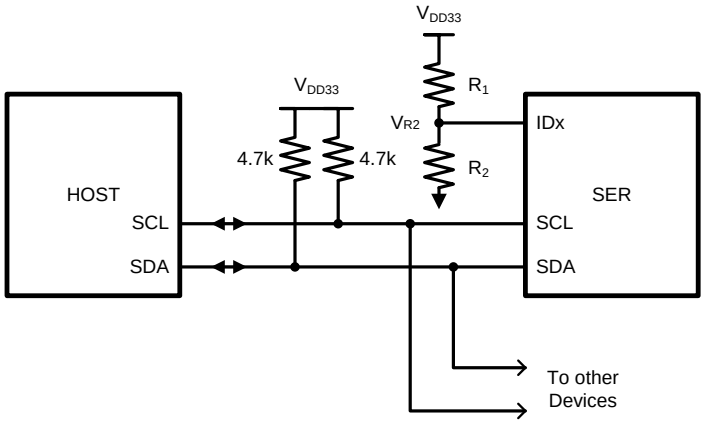


Figure 25. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pullup resistor to V_{DD33} or V_{DDIO} = 3.0 V to 3.6 V. For most applications, a 4.7-kΩ pullup resistor to V_{DD33} is recommended. However, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 10 possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{R2}) and V_{DD33}, each ratio corresponding to a specific device address. See Table 5.

Programming (continued)

Table 4. Serial Control Bus Addresses for IDx

#	Ideal Ratio V_{R2} / V_{DD33}	Ideal V_{R2} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Address 7'b	Address 8'b
1	0	0	Open	40.2 or >10	0x0C	0x18
2	0.306	1.011	221	97.6	0x13	0x26
3	0.350	1.154	210	113	0x14	0x28
4	0.393	1.298	196	127	0x15	0x2A
5	0.440	1.452	182	143	0x16	0x2C
6	0.483	1.594	169	158	0x17	0x2E
7	0.529	1.745	147	165	0x18	0x30
8	0.572	1.887	143	191	0x19	0x32
9	0.618	2.040	121	196	0x1A	0x34
10	0.768	2.535	90.9	301	0x1B	0x36

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 26.

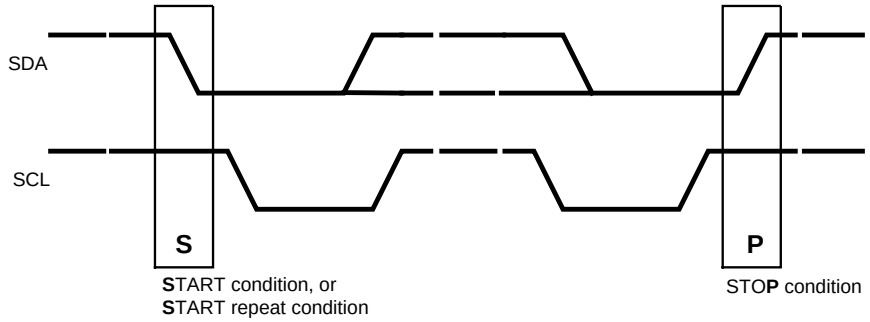


Figure 26. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 27 and a WRITE is shown in Figure 28.

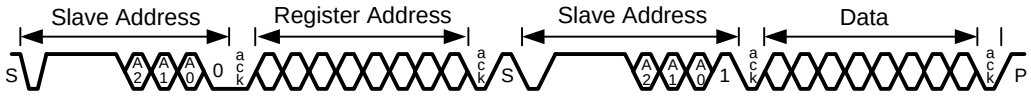


Figure 27. Serial Control Bus — READ

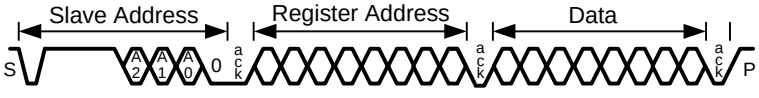


Figure 28. Serial Control Bus — WRITE

The I²C Master located at the DS90UH927Q-Q1 serializer must support I²C clock stretching. For more information on I²C interface requirements and throughput considerations, please refer to *I2C Communication Over FPD-Link III with Bidirectional Control Channel* (SNLA131).

7.6 Register Maps

Table 5. Serial Control Bus Registers

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
0	0x00	I²C Device ID	7:1	RW	IDx	Device ID	7–bit address of Serializer Note: Read-only unless bit 0 is set
			0	RW		ID Setting	I²C ID Setting 0: Device ID is from IDx pin 1: Register I²C Device ID overrides IDx pin
1	0x01	Reset	7	RW	0x00	Remote Auto Power Down	Remote Auto Power Down 0: Do not power down when no Bidirectional Control Channel link is detected (default) 1: Enable power down when no Bidirectional Control Channel link is detected
			6:2				***Reserved***.
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 0: Normal operation (default) 1: Reset
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 0: Normal operation (default) 1: Reset
3	0x03	General Configuration	7	RW	0xD2	Back channel CRC Checker Enable	Back Channel Check Enable 0: Disable 1: Enable (default)
			6				***Reserved***.
			5	RW		I²C Remote Write Auto Acknowledge	Automatically Acknowledge I²C Remote Write When enabled, I²C writes to the Deserializer (or any remote I²C Slave, if I²C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I²C bus. Note: this mode will prevent any NACK or read/write error indication from a remote device from reaching the I²C master. 0: Disable (default) 1: Enable
			4	RW		Filter Enable	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 0: Filtering disable 1: Filtering enable (default)
			3	RW		I²C Pass-through	I²C Pass-Through Mode Read/Write transactions matching any entry in the DeviceAlias registers will be passed through to the remote deserializer I²C interface. 0: Pass-Through Disabled (default) 1: Pass-Through Enabled
			2				***Reserved***
			1	RW		PCLK Auto	Switch over to internal OSC in the absence of PCLK 0: Disable auto-switch 1: Enable auto-switch (default)
			0	RW		TRFB	***Reserved***

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
4	0x04	Mode Select	7	RW	0x80	Failsafe State	Input Failsafe State 0: Failsafe to High 1: Failsafe to Low (default)
			6				***Reserved***
			5	RW		CRC Error Reset	Clear back channel CRC Error Counters This bit is NOT self-clearing 0: Normal Operation (default) 1: Clear Counters
			4				***Reserved***
			3	RW		BKWD ModeOverride	Backward Compatible mode set by BKWD pin or register 0: BC mode is set by BKWD pin (default) 1: BC mode is set by register bit
			2	RW		BKWD	Backward compatibility mode, device to pair with DS90UR906Q, DS90UR908Q, or DS90UR916Q 0: Normal HDCP device (default) 1: Compatible with 906/908/916
			1	RW		LFMODE Override	Frequency mode set by LFMODE pin or register 0: Frequency mode is set by LFMODE pin (default) 1: Frequency mode is set by register bit
			0	RW		LFMODE	Frequency mode select 0: High frequency mode (15 MHz ≤ RxCLKIN ≤ 85 MHz) (default) 1: Low frequency mode (5 MHz ≤ RxCLKIN < 15 MHz)
5	0x05	I^2C Control	7:5		0x00		***Reserved***
			4:3	RW		SDA Output Delay	SDA output delay Configures output delay on the SDA output. Setting this value will increase output delay in units of 40 ns. Nominal output delay values for SCL to SDA are: 00: 240 ns (default) 01: 280 ns 10: 320 ns 11: 360 ns
			2	RW		Local Write Disable	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I^2C master attached to the Deserializer. Setting this bit does not affect remote access to I^2C slaves at the Serializer. 0: Enable (default) 1: Disable
			1	RW		I^2C Bus Timer Speedup	Speed up I^2C Bus Watchdog Timer 0: Watchdog Timer expires after ~1 s (default) 1: Watchdog Timer expires after ~50 µs
			0	RW		I^2C Bus timer Disable	Disable I^2C Bus Watchdog Timer When the I^2C Watchdog Timer may be used to detect when the I^2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1s, the I^2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL 0: Enable (default) 1: Disable

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
6	0x06	DES ID	7:1	RW	0x00	DES Device ID	7-bit Deserializer Device ID Configures the I^2C Slave ID of the remote Deserializer. A value of 0 in this field disables I^2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
			0				***Reserved***
7	0x07	Slave ID 0	7:1	RW	0X00	Slave Device ID 0	7-bit Remote Slave Device ID 0 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Device Alias ID 0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
8	0x08	Slave Alias 0	7:1	RW	0x00	Slave Device Alias ID 0	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 0 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB	Number of Back Channel CRC errors – 8 least significant bits. Cleared by 0x04[5]
11	0x0B		7:0	R	0x00	CRC Error MSB	Number of Back Channel CRC errors – 8 most significant bits. Cleared by 0x04[5]
12	0x0C	General Status	7:4		0x00		***Reserved***
			3	R		BIST CRC Error	Back Channel CRC error during BIST communication with Deserializer. This bit is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04. 0: No CRC errors detected during BIST (default) 1: CRC Errors detected during BIST
			2	R		PCLK Detect	Pixel Clock Status 0: Valid PCLK not detected (default) 1: Valid PCLK detected
			1	R		DES Error	CRC error during BIST communication with Deserializer. This bit is cleared upon loss of link or assertion of 0x04[5] 0: No CRC errors detected (default) 1: CRC errors detected
			0	R		LINK Detect	LINK Detect Status 0: Cable link not detected (default) 1: Cable link detected

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
13	0x0D	GPIO0 Configuration	7:4	R	0x20	Revision ID	Revision ID: 0010: Production Device
			3	RW		GPIO0 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO0 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			1	RW		GPIO0 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPIO0 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
14	0x0E	GPIO1 and GPIO2 Configuration	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			6	RW		GPIO2 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			5	RW		GPIO2 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO2 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO1 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO1 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
15	0x0F	GPIO3 Configuration	7:4		0x00		***Reserved***
			3	RW		GPIO3 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO3 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote Deserializer (default) 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer.
			1	RW		GPIO3 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPIO3 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
16	0x10	GPIO_REG5 and GPIO_REG6 Configuration	7	RW	0x00	GPIO_REG 6 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			6				***Reserved***
			5	RW		GPIO_REG 6 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO_REG 6 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO_REG 5 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			2				***Reserved***
			1	RW		GPIO_REG 5 Direction	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			0	RW		GPIO_REG 5 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
17	0x11	GPIO_REG7 and GPIO_REG8 Configuration	7	RW	0x00	GPIO_REG 8 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			6				***Reserved***
			5	RW		GPIO_REG 8 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO_REG 8 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO_REG 7 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			2				***Reserved***
			1	RW		GPIO_REG 7 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPO_REG 7 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
18	0x12	Data Path Control	7		0x00		***Reserved***
			6	RW		Pass RGB	Pass RGB on DE Setting this bit causes RGB data to be sent independent of DE in DS90UH927, which can be used to allow DS90UH927 to interoperate with DS90UB926, DS90UB928, and DS90UR906. However, setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in Backward Compatibility mode. 0: Normal operation (default) 1: Pass RGB independent of DE
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low) (default) 1: DE is inverted (active low, idle high)
			4	RW		I^2S Repeater Regen	Regenerate I^2S Data From Repeater I^2S Pins 0: Repeater pass through I^2S from video pins (default) 1: Repeater regenerate I^2S from I^2S pins
			3	RW		I^2S Channel B Enable Override	I^2S Channel B Override 0: Set I^2S Channel B Disabled (default) 1: Set I^2S Channel B Enable from reg_12[0]
			2	RW		18-bit Video Select	Video Color Depth Mode 0: Select 24-bit video mode (default) 1: Select 18-bit video mode
			1	RW		I^2S Transport Select	Select I^2S Transport Mode 0: Enable I^2S Data Island Transport (default) 1: Enable I^2S Data Forward Channel Frame Transport
			0	RW		I^2S Channel B Enable	I^2S Channel B Enable 0: I^2S Channel B disabled (default) 1: Enable I^2S Channel B

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
19	0x13	General Purpose Control	7	R	0x10	MAPSEL Mode	Returns Map Select Mode (MAPSEL) pin status
			6	RW		MAPSEL Override	FPD-Link Map Select (MAPSEL) set by input pin or register 0: Map Select is set by input pin (default) 1: Map Select is set by register bit 0x13[5]
			5	RW		MAPSEL Value	FPD-Link Map Select (MAPSEL) value when 0x13[6] is set 0: LSBs on RxIN3± (default) 1: MSBs on RxIN3±
			4				***Reserved***
			3	R		LFMODE Status	Low Frequency Mode (LFMODE) pin status 0: 15 ≤ RxCLKIN ≤ 85 MHz (default) 1: 5 ≤ RxCLKIN < 15 MHz
			2	R		REPEAT Status	Repeater Mode (REPEAT) pin Status 0: Non-repeater (default) 1: Repeater
			1	R		BKWD Status	Backward Compatible Mode (BKWD) Status 0: Compatible to DS90UB926/8Q-Q1 (default) 1: Backward compatible to DS90UR906/8Q-Q1
			0	R		I2S_DB Status	I^2S Channel B Mode (I2S_DB) Status 0: I2S_DB inactive (default) 1: I2S_DB active
20	0x14	BIST Control	7:3		0x00		***Reserved***
			2:1	RW		OSC Clock Source	Internal OSC clock select for Functional Mode or BIST. Functional Mode when PCLK is not present and 0x03[1]=1. 00: 33-MHz Oscillator (default) 01: 33-MHz Oscillator Clock Source in BIST mode 00: External Pixel Clock (default) 01: 33-MHz Oscillator Note: In LFMODE=1, the internal oscillator is 12.5 MHz
			0	R		BIST Enable	BIST Control 0: Disabled (default) 1: Enabled
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
			0	RW		Timer Control	Disable BCC Watchdog Timer 0: Enable BCC Watchdog Timer operation (default) 1: Disable BCC Watchdog Timer operation

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
23	0x17	I^2C Control	7	RW	0x1E	I^2C Pass All	Pass All 0: Enable Forward Control Channel pass-through only of I^2C accesses to I^2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID. (default) 1: Enable Forward Control Channel pass-through of all I^2C accesses to I^2C Slave IDs that do not match the Serializer I^2C Slave ID.
			6:4	RW		SDA Hold Time	Internal SDA Hold Time Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
			3:0	RW		I^2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.
24	0x18	SCL High Time	7:0	RW	0xA1	SCL HIGH Time	I^2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I^2C bus. Units are 40 ns for the nominal oscillator clock frequency.
25	0x19	SCL Low Time	7:0	RW	0xA5	SCL LOW Time	I^2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I^2C bus. This value is also used as the SDA setup time by the I^2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency.
26	0x1A	Data Path Control 2	7	RW	0x00	Block I^2S Auto Config	Block automatic I^2S mode configuration (repeater only) 0: I^2S mode (2-channel, 4-channel, or surround) is detected from the in-band audio signaling 1: Disable automatic detection of I^2S mode
			6:1				***Reserved***
			0	RW		I^2S Surround	Enable 5.1- or 7.1-channel I^2S audio transport 0: 2-channel or 4-channel I^2S audio is enabled as configured in register 0x12 bits 3 and 0 (default) 1: 5.1- or 7.1-channel audio is enabled Note that I^2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I^2S mode detection.
27	0x1B	BIST BC Error Count	7:0	R	0x00	BIST BC Errorr	BIST Back Channel CRC Error Counter This register stores the back-channel CRC error count during BIST Mode (saturates at 255 errors). Clears when a new BIST is initiated or by 0x04[5]

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
28	0x1C	GPIO Pin Status 1	7	R	0x00	GPIO_REG 7 Pin Status	GPIO_REG7 Input Pin Status Status valid only if set to GPI (input) mode
			6	R		GPIO_REG 6 Pin Status	GPIO_REG6 Input Pin Status Status valid only if set to GPI (input) mode
			5	R		GPIO_REG 5 Pin Status	GPIO_REG5 Input Pin Status Status valid only if set to GPI (input) mode
			4				***Reserved***
			3	R		GPIO3 Pin Status	GPIO3 Input Pin Status Status valid only if set to GPI (input) mode
			2	R		GPIO2 Pin Status	GPIO2 Input Pin Status Status valid only if set to GPI (input) mode
			1	R		GPIO1 Pin Status	GPIO1 Input Pin Status Status valid only if set to GPI (input) mode
			0	R		GPIO0 Pin Status	GPIO0 Input Pin Status Status valid only if set to GPI (input) mode
29	0x1D	GPIO Pin Status 2	7:1		0x00		***Reserved***
			0	R		GPIO_REG 8 Pin Status	GPIO_REG8 Input Pin Status Status valid only if set to GPI (input) mode
30	0x1F	Frequency Counter	7:0	RW	0x00	Frequency Counter	Frequency Counter Control Write: Measure number of pixel clock periods in written interval (40ns units) Read: Return number of pixel clock periods counted
32	0x20	Deserializer Capabilities	7	RW	0x00	Freeze DES CAP	Freeze Deserializer Capabilities Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x20 and 0x21. 0: Normal operation (default) 1: Freeze
			6:2				***Reserved***
			1	RW		HD Audio	Deserializer supports 24-bit video concurrently with HD audio This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. 0: Normal operation (default) 1: Freeze
			0	RW		FC GPIO	Deserializer supports GPIO in the Forward Channel Frame This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel. 0: Normal operation (default) 1: Freeze

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted 0000: Checkerboard 0001: White/Black (default) 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontal Black-White/White-Black 0111: Horizontal Black-Red/White-Cyan 1000: Horizontal Black-Green/White-Magenta 1001: Horizontal Black-Blue/White-Yellow 1010: Vertical Black-White/White— Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertical Black-Green/White-Magenta 1101: Vertical Black-Blue/White-Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: VCOM See TI App Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132).
			3				***Reserved***
			2	RW		Color Bars Pattern	Enable Color Bars 0: Color Bars disabled (default) 1: Color Bars enabled Overrides the selection from reg_0x64[7:4]
			1	RW		VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern 0: Color sequence from top left is (YCBR) (default) 1: Color sequence from top left is (RBCY)
			0	RW		Pattern Generator Enable	Pattern Generator Enable 0: Disable Pattern Generator (default) 1: Enable Pattern Generator

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
101	0x65	Pattern Generator Configuration	7		0x00		***Reserved***
			6	RW		Checkerboard Scale	Scale Checkered Patterns: 0: Normal operation (each square is 1x1 pixel) (default) 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels) Setting this bit gives better visibility of the checkered patterns.
			5	RW		Custom Checkerboard	Use Custom Checkerboard Color 0: Use white and black in the Checkerboard pattern (default) 1: Use the Custom Color and black in the Checkerboard pattern
			4	RW		PG 18–bit Mode	18-bit Mode Select: 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. (default) 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.
			3	RW		External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default) 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Timing Select	Timing Select Control: 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. (default) 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. See TI App Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132).
			1	RW		Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output. (default) 1: Invert the color output. See TI App Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132).
			0	RW		Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern. (default) 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See TI App Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132).
102	0x66	PGIA	7:0	RW	0x00	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132)

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
103	0x67	PGID	7:0	RW	0x00	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See TI App Note *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p* (SNLA132)
112	0x70	Slave ID[1]	7:1	RW	0x00	Slave ID 1	7-bit Remote Slave Device ID 1 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
113	0x71	Slave ID[2]	7:1	RW	0x00	Slave ID 2	7-bit Remote Slave Device ID 2 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
114	0x72	Slave ID[3]	7:1	RW	0x00	Slave ID 3	7-bit Remote Slave Device ID 3 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
115	0x73	Slave ID[4]	7:1	RW	0x00	Slave ID 4	7-bit Remote Slave Device ID 4 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
116	0x74	Slave ID[5]	7:1	RW	0x00	Slave ID 5	7-bit Remote Slave Device ID 5 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
117	0x75	Slave ID[6]	7:1	RW	0x00	Slave ID 6	7-bit Remote Slave Device ID 6 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
118	0x76	Slave ID[7]	7:1	RW	0x00	Slave ID 7	7-bit Remote Slave Device ID 7 Configures the physical I^2C address of the remote I^2C Slave device attached to the remote Deserializer. If an I^2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer.
			0				***Reserved***
119	0x77	Slave Alias[1]	7:1	RW	0x00	Slave Alias ID 1	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
120	0x78	Slave Alias[2]	7:1	RW	0x00	Slave Alias ID 2	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
121	0x79	Slave Alias[3]	7:1	RW	0x00	Slave Alias ID 3	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
122	0x7A	Slave Alias[4]	7:1	RW	0x00	Slave Alias ID 4	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
123	0x7B	Slave Alias[5]	7:1	RW	0x00	Slave Alias ID 5	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
124	0x7C	Slave Alias[6]	7:1	RW	0x00	Slave Alias ID 6	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
125	0x7D	Slave Alias[7]	7:1	RW	0x00	Slave Alias ID 7	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I^2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I^2C Slave.
			0				***Reserved***
128	0x80	RX_BKSV0	7:0	R	0x00	RX BKSV0	BKSV0: Value of byte 0 of the Deserializer KSV
129	0x81	RX_BKSV1	7:0	R	0x00	RX BKSV1	BKSV1: Value of byte 1 of the Deserializer KSV
130	0x82	RX_BKSV2	7:0	R	0x00	RX BKSV2	BKSV2: Value of byte 2 of the Deserializer KSV
131	0x83	RX_BKSV3	7:0	R	0x00	RX BKSV3	BKSV3: Value of byte 3 of the Deserializer KSV.
132	0x84	RX_BKSV4	7:0	R	0x00	RX BKSV4	BKSV4: Value of byte 4 of the Deserializer KSV.
144	0x90	TX_KSV0	7:0	R	0x00	TX KSV0	KSV0: Value of byte 0 of the Serializer KSV.
145	0x91	TX_KSV1	7:0	R	0x00	TX KSV1	KSV1: Value of byte 1 of the Serializer KSV.
146	0x92	TX_KSV2	7:0	R	0x00	TX KSV2	KSV2: Value of byte 2 of the Serializer KSV.
147	0x93	TX_KSV3	7:0	R	0x00	TX KSV3	KSV3: Value of byte 3 of the Serializer KSV.
148	0x94	TX_KSV4	7:0	R	0x00	TX KSV4	KSV4: Value of byte 4 of the Serializer KSV.
152	0x98	TX_AN0	7:0	R	0x00	TX AN0	TX_AN0: Value of byte 0 of the Serializer AN Value
153	0x99	TX_AN1	7:0	R	0x00	TX AN1	TX_AN1: Value of byte 1 of the Serializer AN Value
154	0x9A	TX_AN2	7:0	R	0x00	TX AN2	TX_AN2: Value of byte 2 of the Serializer AN Value
155	0x9B	TX_AN3	7:0	R	0x00	TX AN3	TX_AN3: Value of byte 3 of the Serializer AN Value
156	0x9C	TX_AN4	7:0	R	0x00	TX AN4	TX_AN4: Value of byte 4 of the Serializer AN Value
157	0x9D	TX_AN5	7:0	R	0x00	TX AN5	TX_AN5: Value of byte 5 of the Serializer AN Value
158	0x9E	TX_AN6	7:0	R	0x00	TX AN6	TX_AN6: Value of byte 6 of the Serializer AN Value
159	0x9F	TX_AN7	7:0	R	0x00	TX AN7	TX_AN7: Value of byte 7 of the Serializer AN Value
160	0xA0	RX BCAPS	7		0x00		***Reserved***
			6	R		Repeater	Indicates if the attached Receiver supports downstream connections. This bit is valid once the Bksv is ready as indicated by the BKSV_RDY bit in the HDCP
			5	R		KSV FIFO	KSV FIFO Ready Indicates the receiver has built the list of attached KSVs and computed the verification value
			4:2				***Reserved***
			1	R		Features	HDCP v1.1_Features The HDCP Receiver supports the Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options.
			0	R		Fast Re-auth	The HDCP Receiver is capable of receiving (unencrypted) video signal during the session re-authentication.
161	0xA1	RX BSTATUS0	7	R	0x00	Max Devices	Maximum Devices Exceeded: Indicates a topology error was detected. Indicates the number of downstream devices has exceeded the depth of the Repeater's KSV FIFO.
			6:0	R		Device Count	Total number of attached downstream device. For a Repeater, this will indicate the number of downstream devices, not including the Repeater. For an HDCP Receiver that is not also a Repeater, this field will be 0.

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
162	0xA2	RX BSTATUS1	7:4		0x00		***Reserved***
			3	R		Max Cascade	Maximum Cascade Exceeded: Indicates a topology error was detected — more than seven levels of repeaters have been cascaded together.
			2:0	R		Cascade Depth	Indicates the number of attached levels of devices for the Repeater.
163	0xA3	KSV FIFO	7:0	R	0x00	KSV FIFO	KSV FIFO Each read of the KSV FIFO returns one byte of the KSV FIFO list composed by the downstream Receiver.
192	0xC0	HDCP DBG	7:4		0x00		***Reserved***
			3	RW		RGB CHKSUM	Enable RGB video line checksum Enables sending of ones-complement checksum for each 8-bit RGB data channel following end of each video data line.
			2	RW		Fast LV	Fast Link Verification HDCP periodically verifies that the HDCP Receiver is correctly synchronized. Setting this bit will increase the rate at which synchronization is verified. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames.
			1	RW		TMR Speed Up	Timer Speedup Speed up HDCP authentication timers.
			0	RW		HDCP I2C Fast	HDCP I^2C Fast Mode Enable Setting this bit to a 1 will enable the HDCP I^2C Master in the HDCP Receiver to operate with Fast mode timing. If set to a 0, the I^2C Master will operate with Standard mode timing. This bit is mirrored in the IND_STS register.

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
194	0xC2	HDCP CFG	7	RW	0x80	ENH LV	Enable Enhanced Link Verification Allows checking of the encryption Pj value on every 16th frame. 0: Enhanced Link Verification disabled 1: Enhanced Link Verification enabled (default)
			6	RW		HDCP EESS	Enables Enhanced Encryption Status Signaling (EESS) instead of the Original Encryption Status Signaling (OESS). 0: OESS mode enabled (default) 1: EESS mode enabled
			5	RW		TX RPTR	Transmit Repeater Enable Enables the transmitter to act as a repeater. In this mode, the HDCP Transmitter incorporates the additional authentication steps required of an HDCP Repeater. 0: Transmit Repeater mode disabled (default) 1: Transmit Repeater mode enabled
			4:3	RW		ENC Mode	Encryption Control Mode Determines mode for controlling whether encryption is required for video frames. 00: Enc_Authenticated (default) 01: Enc_Reg_Control 10: Enc_Always 11: Enc_InBand_Control (per frame) If the Repeater strap option is set at power-up, Enc_InBand_Control (ENC_MODE == 11) will be selected. Otherwise, the default will be Enc_Authenticated mode (ENC_MODE == 00).
			2	RW		Wait	Enable 100 ms Wait: The HDCP 1.3 specification allows for a 100 ms wait to allow the HDCP Receiver to compute the initial encryption values. The FPD-Link III implementation ensures that the Receiver will complete the computations before the HDCP Transmitter. Thus the timer is unnecessary. 0: 100 ms timer disabled (default) 1: 100 ms timer enabled
			1	RW		RX DET SEL	RX Detect Select: Controls assertion of the Receiver Detect Interrupt. 0: The Receiver Detect Interrupt will be asserted on detection of an FPD-Link III Receiver. (default) 1: the Receiver Detect Interrupt will also require a receive lock indication from the receiver.
			0	RW		HDCP AV MUTE	Enable AVMUTE This bit may only be set if the HDCP_EESS bit is also set. 0: Resume normal operation (default) 1: Initiate AVMUTE operation. The transmitter will ignore encryption status controls while in this state.

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
195	0xC3	HDCP CTL	7	RW	0x00	HDCP RST	HDCP Reset Setting this bit will reset the HDCP transmitter and disable HDCP authentication. This bit is self-clearing.
			6				***Reserved***
			5	RW		KSV List Valid	The controller sets this bit after validating the Repeater's KSV List against the Key revocation list. This allows completion of the Authentication process. This bit is self-clearing.
			4	RW		KSV Valid	The controller sets this bit after validating the Receiver's KSV against the Key revocation list. This allows continuation of the Authentication process. This bit will be cleared upon assertion of the KSV_RDY flag in the HDCP_STS register. Setting this bit to a 0 will have no effect.
			3	RW		HDCP ENC DIS	HDCP Encrypt Disable Disables HDCP encryption. Setting this bit to a 1 will cause video data to be sent without encryption. Authentication status will be maintained. This bit is self-clearing.
			2	RW		HDCP ENC EN	HDCP Encrypt Enable Enables HDCP encryption. When set, if the device is authenticated, encrypted data will be sent. If device is not authenticated, a blue screen will be sent. Encryption should always be enabled when video data requiring content protection is being supplied to the transmitter. When this bit is not set, video data will be sent without encryption. Note that when CFG_ENC_MODE is set to Enc_Always, this bit will be read only with a value of 1.
			1	RW		HDCP DIS	HDCP Disable Disables HDCP authentication. Setting this bit to a 1 will disable the HDCP authentication. This bit is self-clearing.
			0	RW		HDCP EN	HDCP Enable/Restart Enables HDCP authentication. If HDCP is already enabled, setting this bit to a 1 will restart authentication. Setting this bit to a 0 will have no effect. A register read will return the current HDCP enabled status.

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
196	0xC4	HDCP STS	7	R	0x00	I2C ERR DET	HDCP I^2C Error Detected This bit indicates an error was detected on the embedded communications channel with the HDCP Receiver. Setting of this bit might indicate that a problem exists on the link between the HDCP Transmitter and HDCP Receiver. This bit will be cleared on read.
			6	R		RX INT	RX Interrupt Status of the RX Interrupt signal. The signal is received from the attached HDCP Receiver and is the status on the INTB_IN pin of the HDCP Receiver. The signal is active low, a 0 indicates an interrupt condition.
			5	R		RX Lock DET	Receiver Lock Detect This bit indicates that the downstream Receiver has indicated Receive Lock to incoming serial data.
			4	R		DOWN HPD	Downstream Hot Plug Detect This bit indicates the local device or a downstream repeater has reported a Hot Plug event, indicating addition of a new receiver. This bit will be cleared on read.
			3	R		RX DET	Receiver Detect This bit indicates that a downstream Receiver has been detected.
			2	R		KSV LIST RDY	HDCP Repeater KSV List Ready This bit indicates that the Receiver KSV list has been read and is available in the KSV_FIFO registers. The device will wait for the controller to set the KSV_LIST_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_LIST_VALID bit.
			1	R		KSV RDY	HDCP Receiver KSV Ready This bit indicates that the Receiver KSV has been read and is available in the HDCP_ BKSV registers. If the device is not a Repeater, it will wait for the controller to set the KSV_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_VALID bit.. The bit will also be cleared if authentication fails.
			0	R		AUTHED	HDCP Authenticated Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication.

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
198	0xC6	HDCP ICR	7	RW	0x00	IE IND ACC	Interrupt on Indirect Access Complete Enables interrupt on completion of Indirect Register Access.
			6	RW		IE RXDET INT	Interrupt on Receiver Detect Enables interrupt on detection of a downstream Receiver. If HDCP_CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	RW		IS_RX_INT	Interrupt on Receiver Interrupt Enables interrupt on indication from the HDCP Receiver. Allows propagation of interrupts from downstream devices.
			4	RW		IE LIST RDY	Interrupt on KSV List Ready Enables interrupt on KSV List Ready.
			3	RW		IE KSV RDY	Interrupt on KSV Ready Enables interrupt on KSV Ready.
			2	RW		IE AUTH FAIL	Interrupt on Authentication Failure Enables interrupt on authentication failure or loss of authentication.
			1	RW		IE AUTH PASS	Interrupt on Authentication Pass Enables interrupt on successful completion of authentication.
			0	RW		INT Enable	Global Interrupt Enable Enables interrupt on the interrupt signal to the controller.
199	0xC7	HDCP ISR	7	R	0x00	IS IND ACC	Interrupt on Indirect Access Complete Indirect Register Access has completed.
			6	R		INT Detect	Interrupt on Receiver Detect interrupt A downstream receiver has been detected.
			5	R		IS RX INT	Interrupt on Receiver interrupt Receiver has indicated an interrupt request from downstream device.
			4	R		IS LIST RDY	Interrupt on KSV List Ready The KSV list is ready for reading by the controller.
			3	R		IS KSV RDY	Interrupt on KSV Ready The Receiver KSV is ready for reading by the controller.
			2	R		IS AUTH FAIL	Interrupt on Authentication Failure Authentication failure or loss of authentication has occurred.
			1	R		IS AUTH PASS	Interrupt on Authentication Pass Authentication has completed successfully.
			0	R		INT	Global Interrupt Set if any enabled interrupt is indicated.

Register Maps (continued)

Table 5. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
208	0xD0	IND STS	7	RW	0x00	IA Reset	Indirect Access Reset Setting this bit to a 1 will reset the I^2C Master in the HDCP Receiver. As this may leave the I^2C bus in an indeterminate state, it should only be done if the Indirect Access mechanism is not able to complete due to an error on the destination I^2C bus.
			6				***Reserved***
			5	RW		I2C TO DIS	I^2C Timeout Disable Setting this bit to a 1 will disable the bus timeout function in the I^2C master. When enabled, the bus timeout function allows the I^2C master to assume the bus is free if no signaling occurs for more than 1 second.
			4	RW		I2C Fast	I^2C Fast mode Enable Setting this bit to a 1 will enable the I^2C Master in the HDCP Receiver to operation with Fast mode timing. If set to a 0 (default), the I^2C Master will operate with Standard mode timing.
			3:2				***Reserved***
			1	R		IA ACK	Indirect Access Acknowledge The acknowledge bit indicates that a valid acknowledge was received upon completion of the I^2C read or write to the slave. A value of 0 (default) indicates the read/write did not complete successfully.
			0	R		IA DONE	Indirect Access Done Set to a 1 to indicate completion of Indirect Register Access. This bit will be cleared or read or by start of a new Indirect Register Access.
209	0xD1	IND SAR	7:1	RW	0x00	IA SADDR	Indirect Access Slave Address This field should be programmed with the slave address for the I^2C slave to be accessed.
			0	RW		IA RW	Indirect Access Read/Write 0: Write (default) 1: Read
210	0xD2	IND OAR	7:0	RW	0x00	IA Offset	Indirect Access Offset It is programmed with the register address for the I^2C indirect access.
211	0xD3	IND DATA	7:0	RW	0x00	IA Data	Indirect Access Data For an indirect write, It is written with the write data. For an indirect read, it contains the result of a successful read.
240	0xF0	HDCP TX ID	7:0	R	0x5F	ID0	First byte ID code, '_'
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code, 'U'
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code. 'H'
243	0xF3		7:0	R	0x39	ID3	Forth byte of ID code: '9'
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: "2"
245	0xF5		7:0	R	0x37	ID5	Sixth byte of ID code: "7"

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UH927Q-Q1, in conjunction with the DS90UH928Q-Q1 or DS90UH926Q-Q1, is intended for interface between a HDCP compliant host (graphics processor) and a display supporting 24-bit color depth (RGB888) and high definition (720p) digital video format. It can receive an 8-bit RGB stream with a pixel clock rate up to 85 MHz together with three control bits (VS, HS and DE) and four I^2S audio streams. The included HDCP 1.3 compliant cipher block allows the authentication of the HDCP Deserializer, which decrypts both video and audio contents. The HDCP keys are pre-loaded by TI into Non-Volatile Memory (NVM) for maximum security.

8.2 Typical Application

Figure 29 shows a typical application of the DS90UH927Q-Q1 serializer for an 85 MHz 24-bit Color Display Application. The 5 LVDS input pairs require external 100Ω terminations. The CML outputs must have an external 0.1-µF AC coupling capacitor on the high speed serial lines. The serializer has internal CML termination on its high speed outputs.

Bypass capacitors should be placed near the power supply pins. At a minimum, four (4) 4.7-µF capacitors should be used for local device bypassing. Ferrite beads are placed on the two sets of supply pins (VDD33 and VDDIO) for effective noise suppression. The interface to the graphics source is LVDS. The VDDIO pins may be connected to 3.3 V or 1.8 V. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable.

Typical Application (continued)

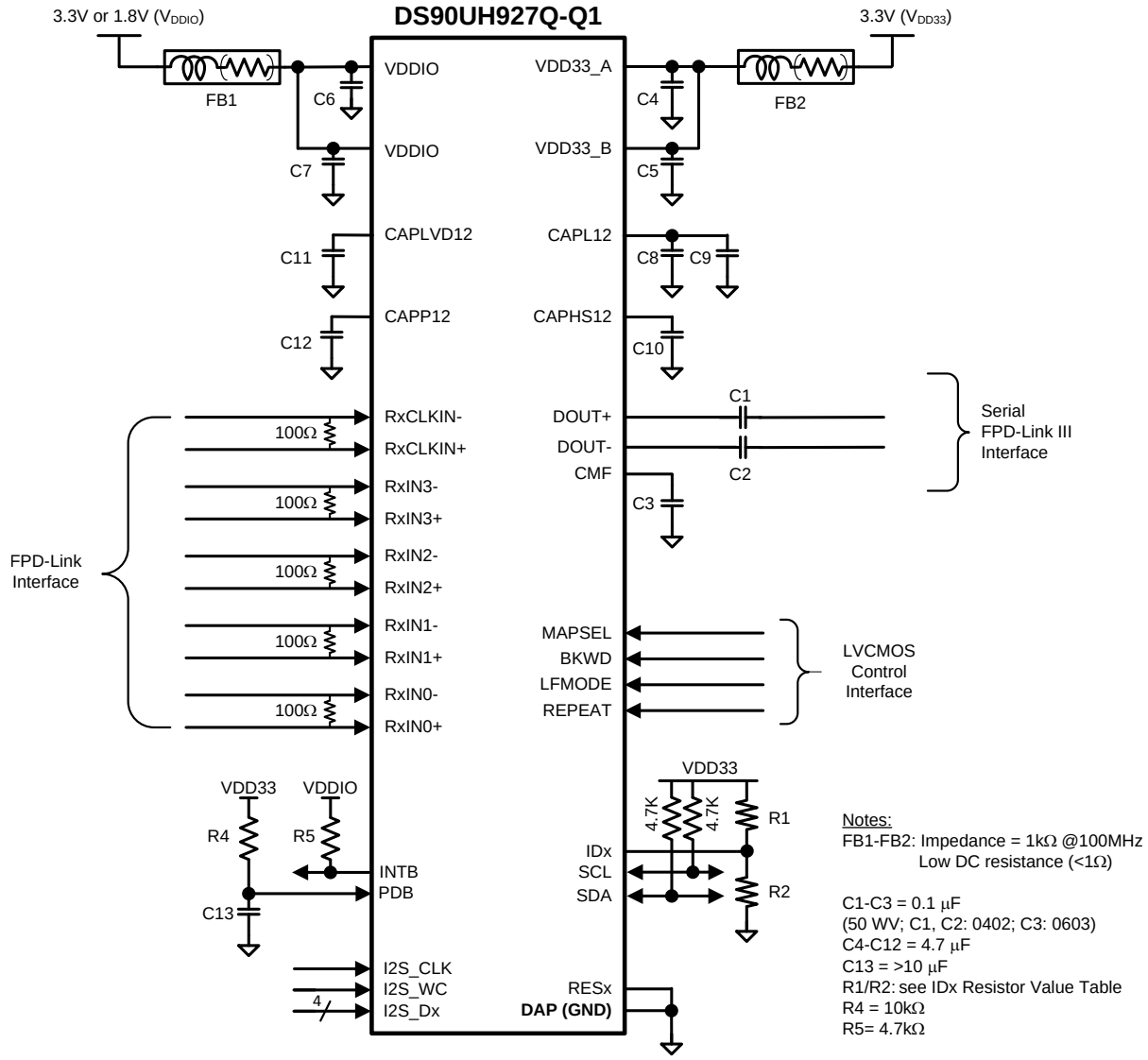


Figure 29. Typical Connection Diagram

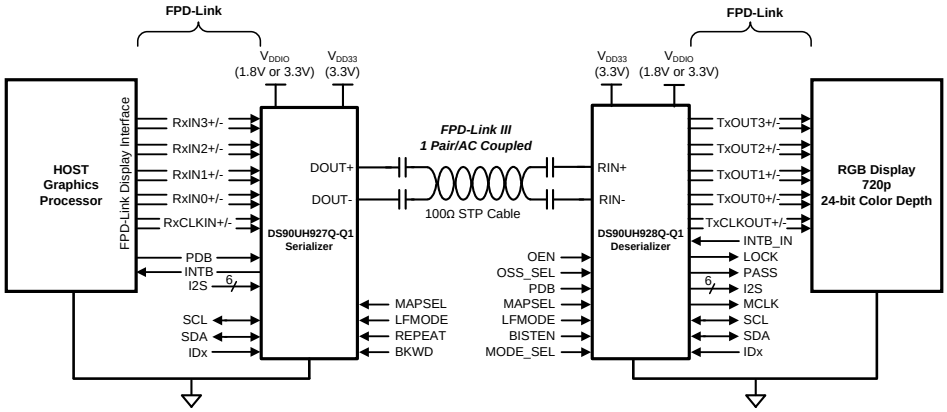


Figure 30. Display Application

Typical Application (continued)

8.2.1 Design Requirements

For the typical design application, use the following as input parameters.

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD33	3.3 V
AC Coupling Capacitor for DOUT±	100 nF
PCLK Frequency	85 MHz

8.2.2 Detailed Design Procedure

Figure 29 shows a typical application of the DS90UH927Q-Q1 serializer for an 85-MHz 24-bit Color Display Application. The CML outputs must have an external 0.1-µF AC coupling capacitor on the high speed serial lines. Bypass capacitors are placed near the power supply pins. At a minimum, six (6) 4.7-µF capacitors and two (2) additional 1-µF capacitors should be used for local device bypassing. Ferrite beads are placed on the two (2) VDDs (VDD33 and VDDIO) for effective noise suppression. An RC delay is placed on the PDB signal to delay the enabling of the device until power is stable.

8.2.3 Application Curves

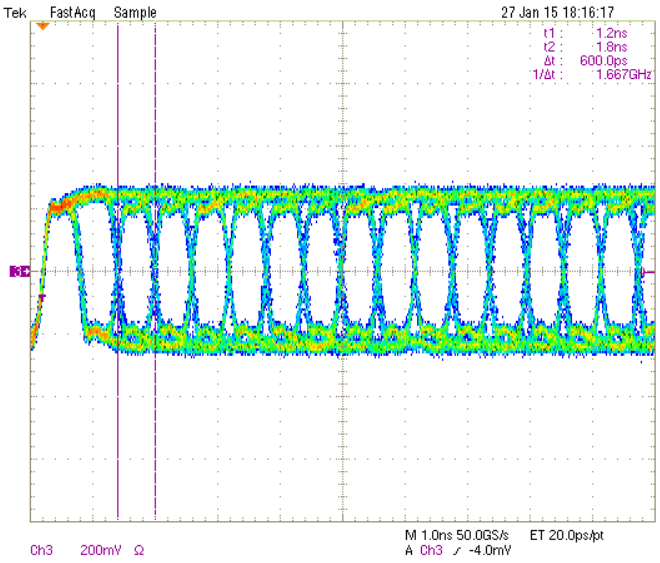


Figure 31. Serializer Output Stream with 48-MHz Input Clock

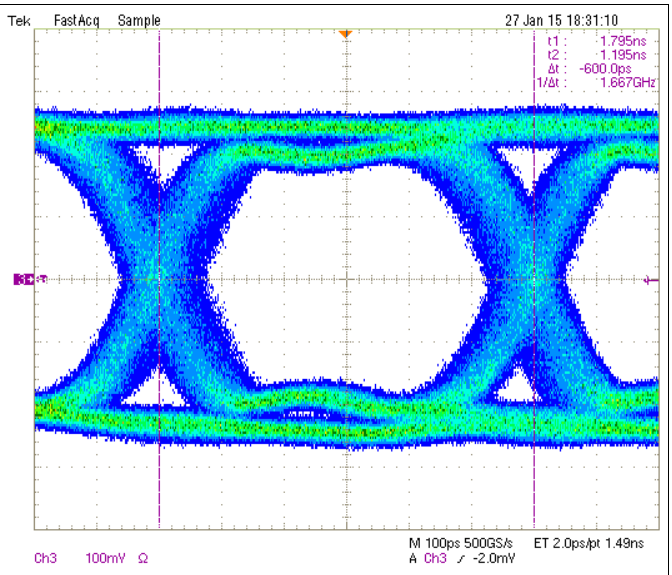


Figure 32. Serializer Eye with 48-MHz Input Clock

9 Power Supply Recommendations

The power supply ramp (V_{DD33} and V_{DDIO}) should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V_{DD33}, a 10-kΩ pullup and a > 10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both V_{DD33} and V_{DDIO} has reached steady state. Pins VDD33_A and VDD33_B should both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 10 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 µF to 100 µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs. For DS90UH927Q-Q1, only one common ground plane is required to connect all device related ground pins.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the WQFN style package, including PCB design and manufacturing requirements, is provided in TI Application Note: *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

Layout Guidelines (continued)

10.1.1 CML Interconnect Guidelines

See SNLA008 and SNLA035 for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible.

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: http://www.ti.com/lit/ml/snla187/snla187.pdf

10.2 Layout Example

Notes:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271.
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Layout Example (continued)

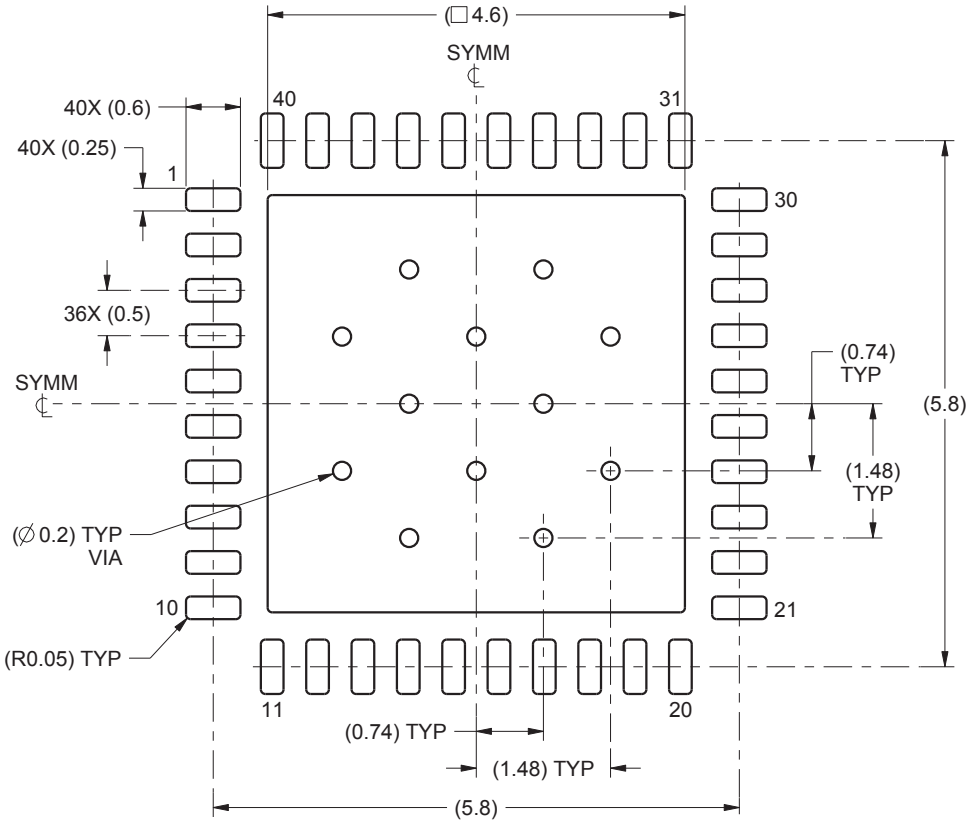


Figure 33. Land Pattern Example and Solder Mask Details

Layout Example (continued)

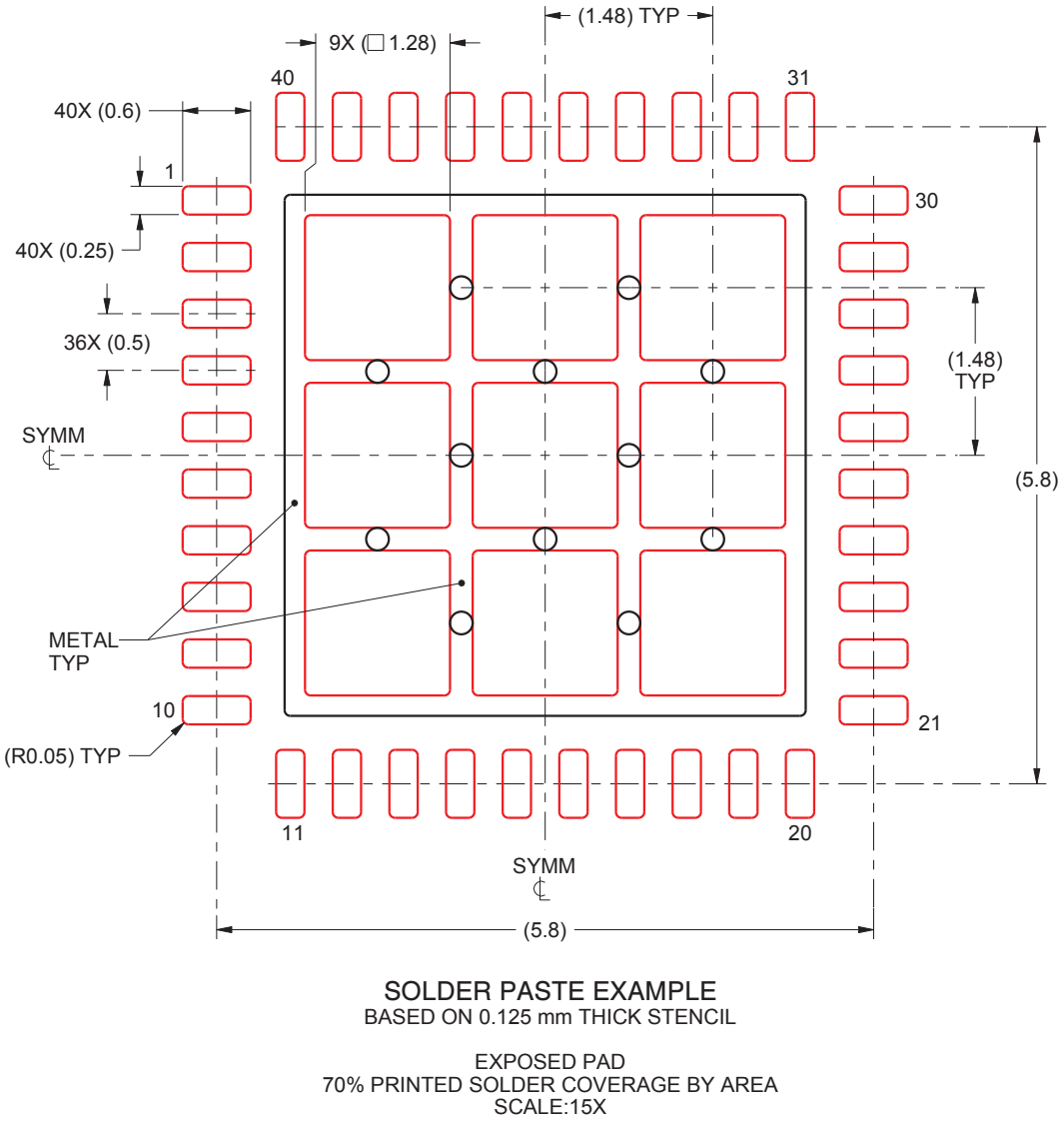


Figure 34. Solder Paste Example

Figure 35 PCB layout example is derived from the layout design of the DS90UH927Q-Q1 Evaluation Board. The graphic and layout description are used to determine both proper routing and proper solder techniques when designing the Serializer board.

Layout Example (continued)

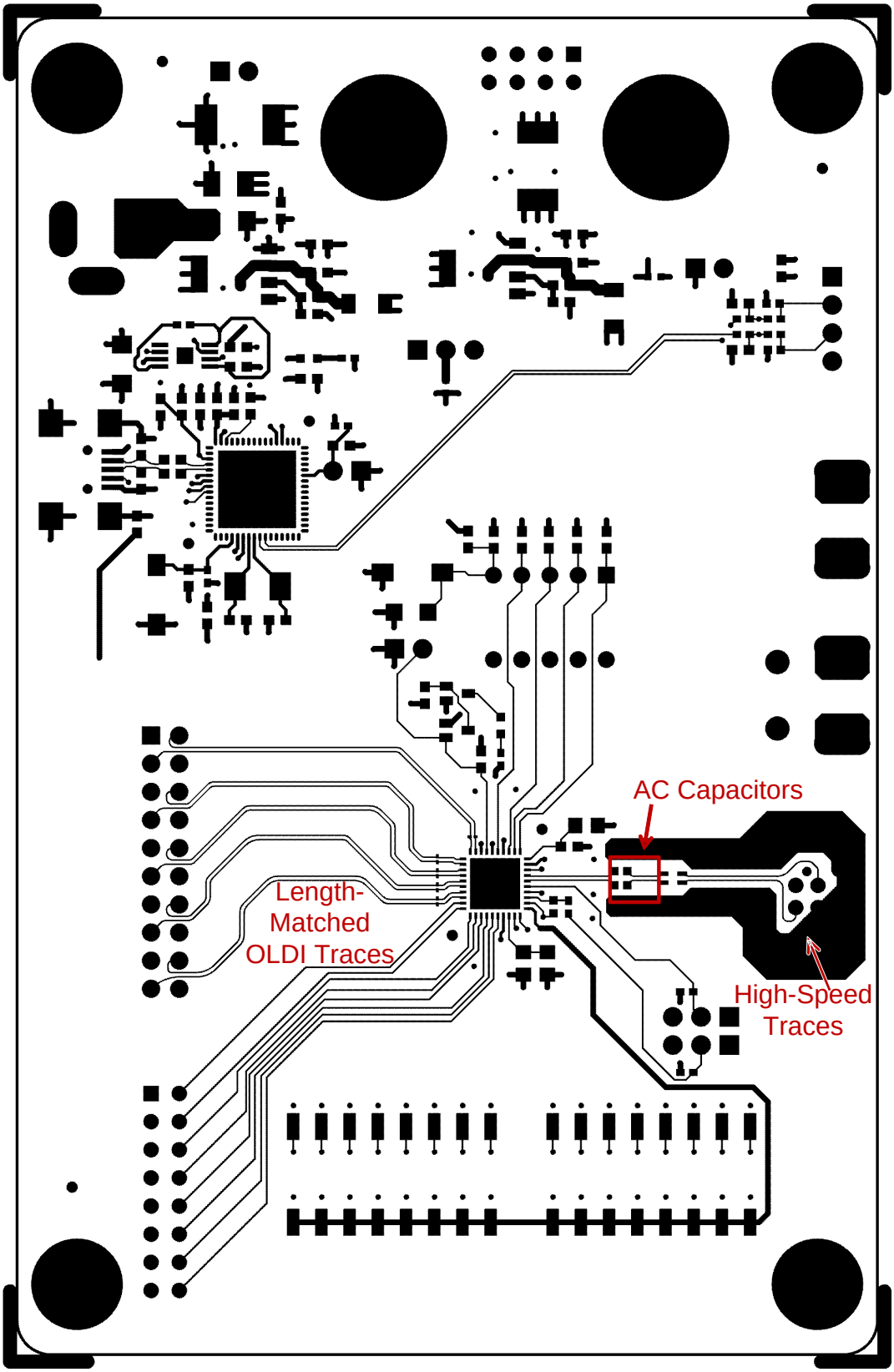


Figure 35. DS90UH927Q-Q1 Serializer Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p*, SNLA132
- *I2C Communication Over FPD-Link III with Bidirectional Control Channel*, SNLA131
- *AN-1187 Leadless Leadframe Package (LLP)*, SNOA401
- *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines*, SNLA008
- *AN-905 Transmission Line RAPIDESIGNER Operation and Applications Guide*, SNLA035
- *LVDS Owner's Manual*, SNLA187
- *QFN/SON PCB Attachment*, SLUA271

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UH927QSQ/NOPB	ACTIVE	WQFN	RTA	40	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UH927QSQ	Samples
DS90UH927QSQE/NOPB	ACTIVE	WQFN	RTA	40	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UH927QSQ	Samples
DS90UH927QSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UH927QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

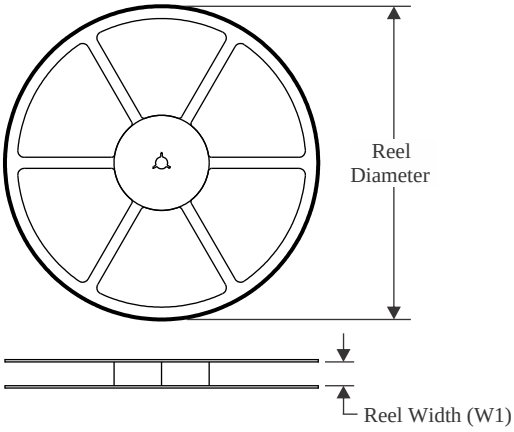
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

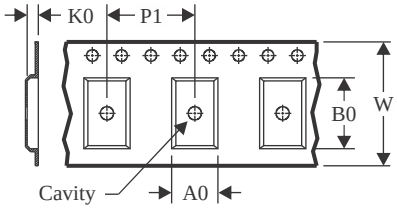
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

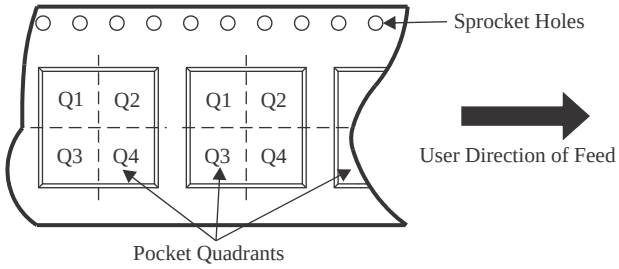


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

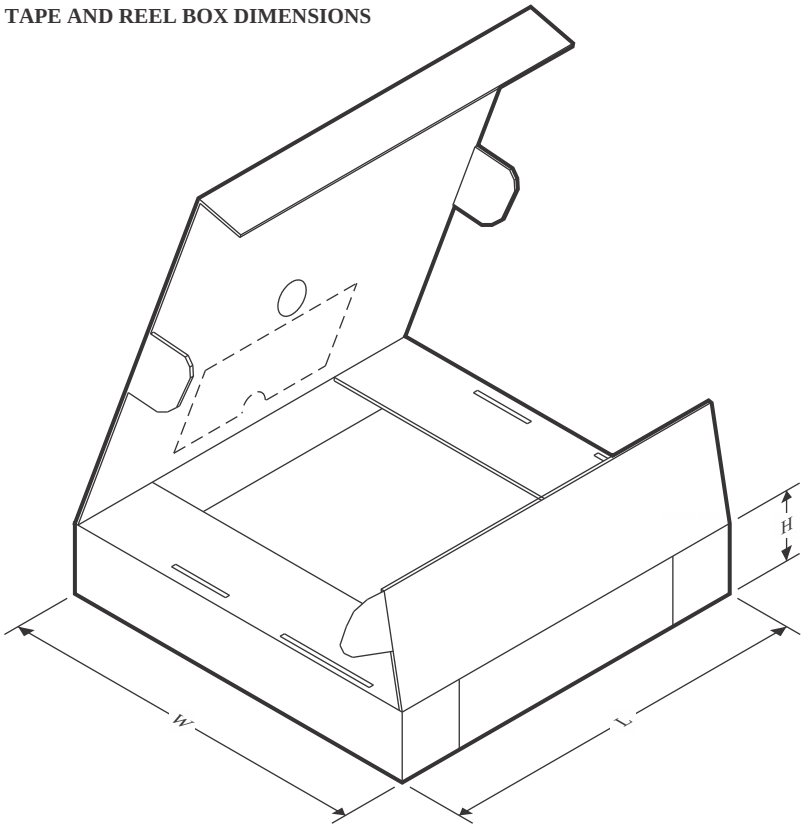
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH927QSQ/NOPB	WQFN	RTA	40	1000	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UH927QSQE/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS90UH927QSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

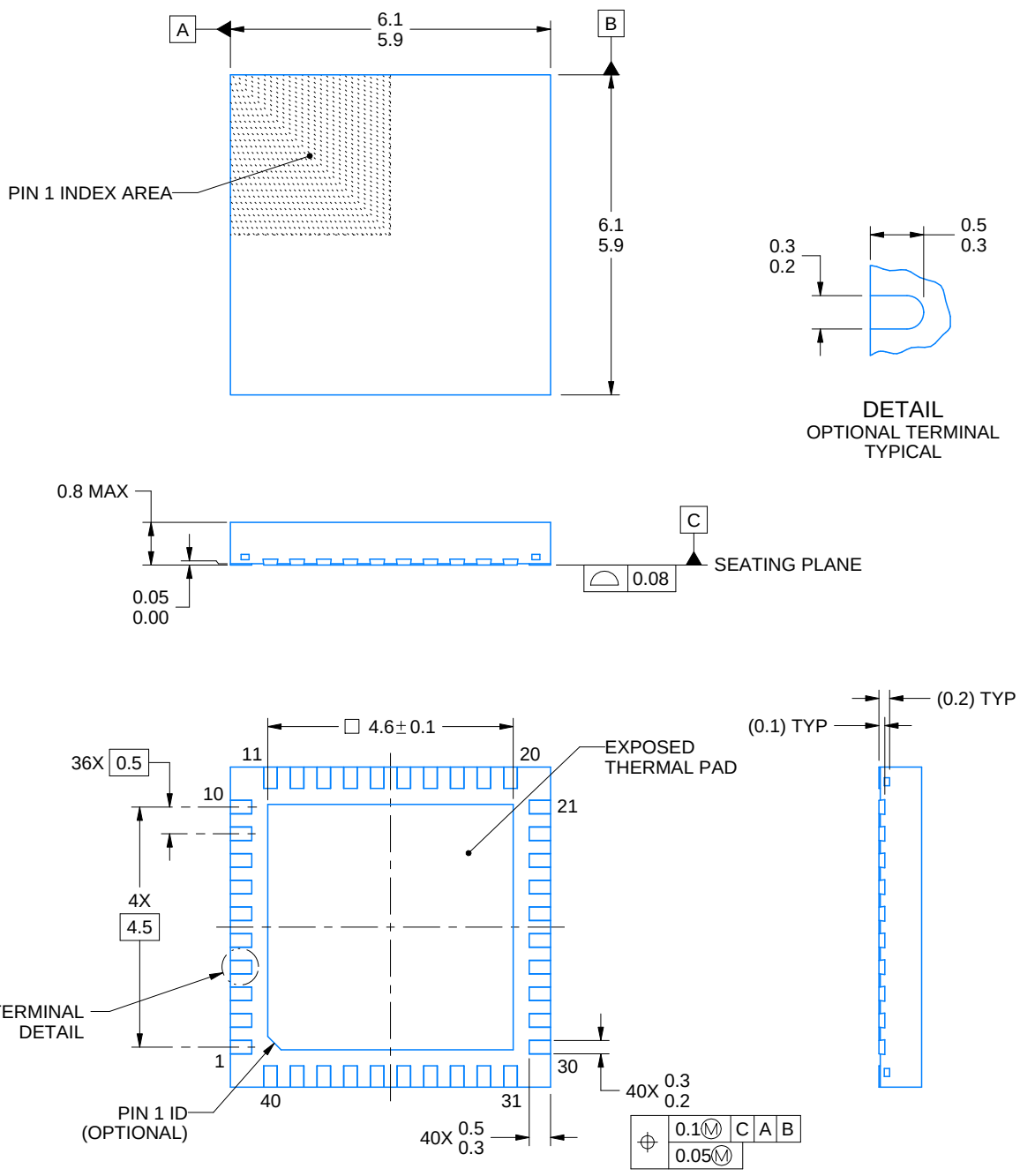
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH927QSQ/NOPB	WQFN	RTA	40	1000	356.0	356.0	36.0
DS90UH927QSQE/NOPB	WQFN	RTA	40	250	208.0	191.0	35.0
DS90UH927QSQX/NOPB	WQFN	RTA	40	2500	356.0	356.0	36.0

PACKAGE OUTLINE

RTA0040A

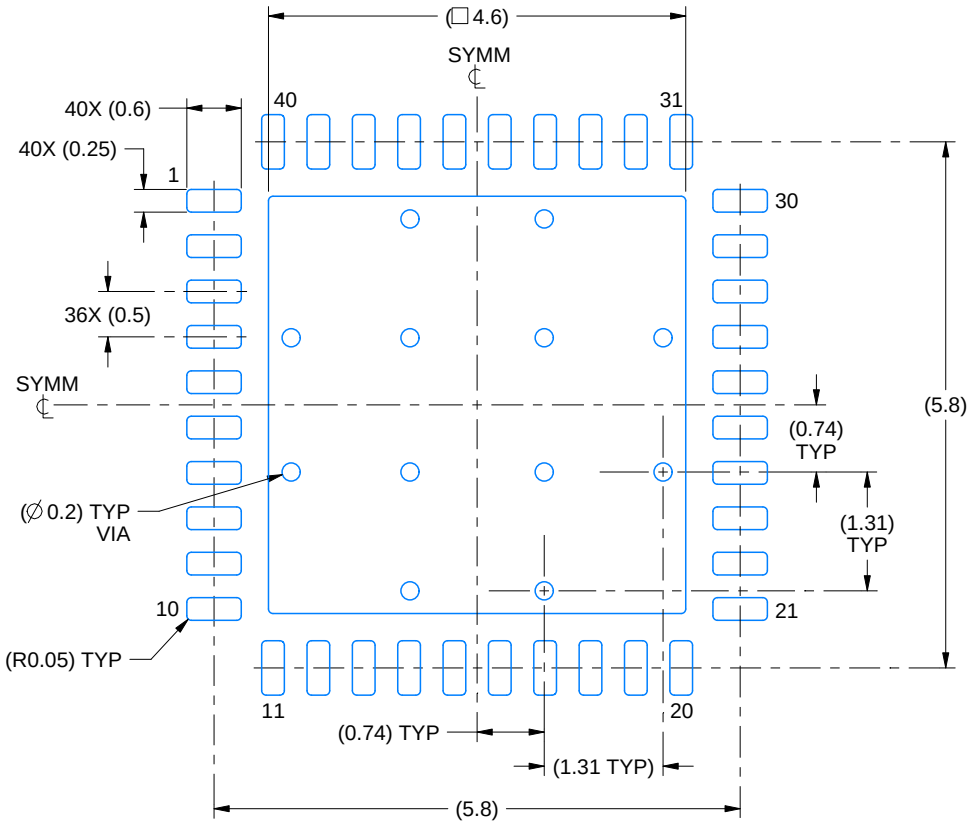
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

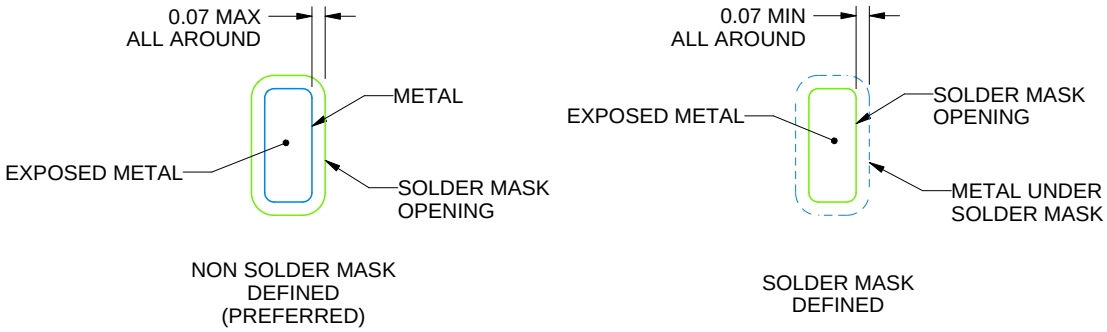


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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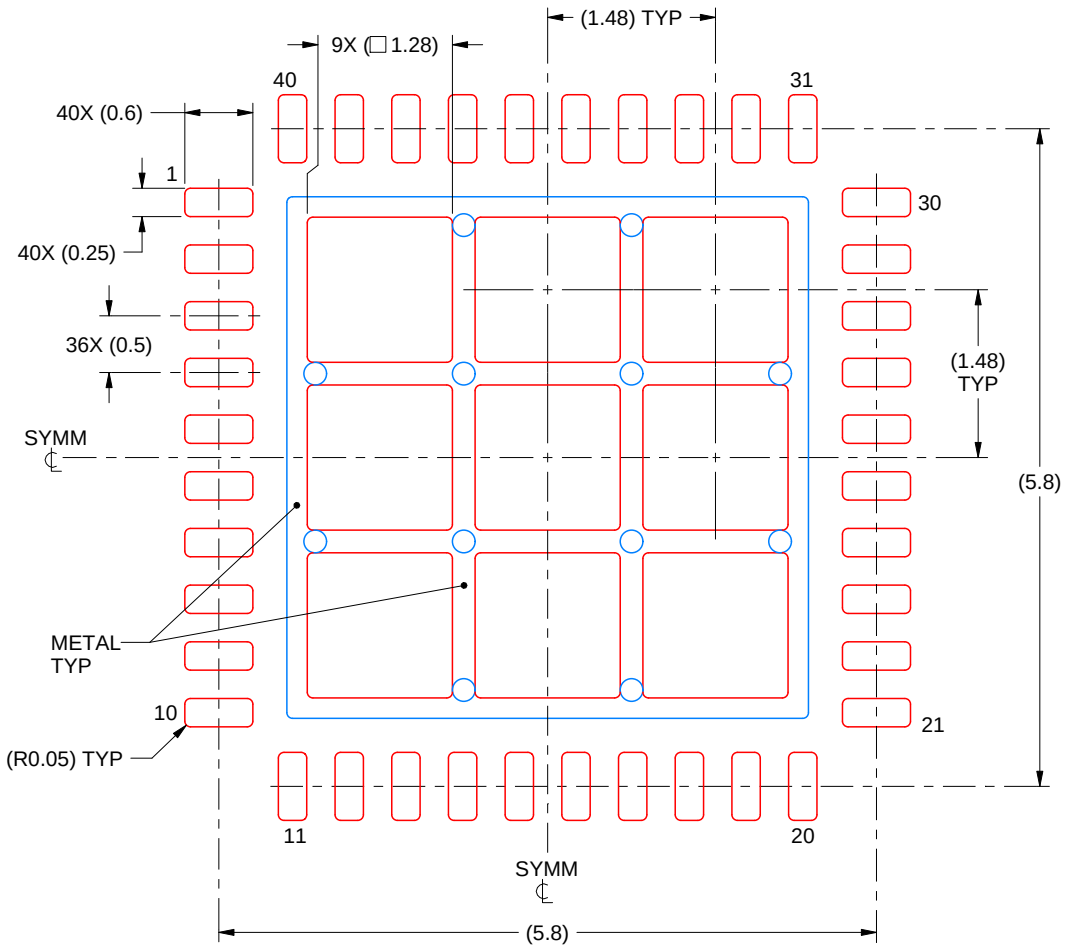
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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