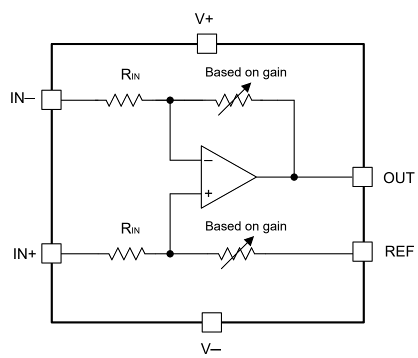
INA500 Cost and Size Optimized, Low Power, 1.7V to 5.5V Difference Amplifier with >1MΩ Input Impedance

1 Features

- Optimized for small-size, low-power, and low-cost
- >1MΩ Ultra-high input impedance
- Three gain options (G = 1, 0.50, and 0.25)
- Good precision for 8-bit to 12-bit systems
  - CMRR: 87dB (typical)
  - Gain error: ±0.01% (typical)
  - Offset voltage: ±0.70mV (typical)
- Space saving 0.8mm^2 X2SON package
- Bandwidth: 125kHz (typical)
- Drives 200pF with <20% overshoot (typical)
- Low quiescent current: 13.5μA (typical)
- Supply range: 1.7V (±0.85V) to 5.5V (±2.75V)
- Specified temperature range: –40°C to 125°C

2 Applications

- Battery cell formation and test equipment
- String inverter
- EV charging station power module
- Battery energy storage system
- Power tools
- Industrial AC-DC
- Wearable fitness and activity monitor



NOTE: The input resistors (R_{IN}) values are 1.08MΩ for INA500A, 1.44MΩ for INA500B, and 1.68MΩ for INA500C.

INA500 Simplified Internal Schematic

3 Description

The INA500 is a difference amplifier with integrated op-amp and matched resistors that offers three gain options. The INA500A version offers gain option of 1, while the INA500B and INA500C versions offer gain options of 0.50 and 0.25 respectively.

These are voltage sensing INAs in difference amplifier configuration with high input impedance of >1MΩ and low quiescent current of 13.5μA. The device achieves 75dB of minimum CMRR and an accurate ±0.05% of maximum gain error, along with 3.5mV of maximum offset (referred to output) in G = 1 configuration. The device can handle up to 27.5V (±13.75V) of input common-mode voltage in G = 0.25 with 5.5V (±2.75V) of supply voltage. The combination of specifications noted above are designed for a variety of level translation and battery monitoring applications.

The precision matched integrated resistors of the INA500 saves BOM costs and board space by removing the need for precise and low tolerance external resistors. The INA500 can interface directly to low-speed, 8-bit to 12-bit, analog-to-digital converters (ADC) and is an excellent choice for replacing discrete implementation of difference amplifiers built with commodity amplifiers and discrete resistors. The INA500 is offered in standard 6-pin packages such as SOT-23 and SC70 as well as the space saving, X2SON package.

Package Information

PART NUMBER(1)	VERSION	PACKAGE(2)	PACKAGE SIZE(4)
INA500	A	DCK (SC70, 6)	2.1mm × 1.25mm
		DBV (SOT-23, 6)	2.9mm × 2.8mm
		DTQ (X2SON, 6) (3)	1mm × 0.8mm
	B	DCK (SC70, 6)	2.1mm × 1.25mm
		DBV (SOT-23, 6)	2.9mm × 2.8mm
		DTQ (X2SON, 6) (3)	1mm × 0.8mm
	C	DCK (SC70, 6)	2.1mm × 1.25mm
		DBV (SOT-23, 6)	2.9mm × 2.8mm
		DTQ (X2SON, 6) (3)	1mm × 0.8mm

(1) See Device Comparison
(2) For more information, see Section 11
(3) This package is preview only.
(4) The package size (length × width) is a nominal value and includes pins, where applicable

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4 Device Comparison Table

DEVICE	VERSION	NO. OF CHANNELS	PACKAGE LEADS		
			SOT-23 DBV	SC70 DCK	X2SON DTQ(1)
INA500	A	1	6	6	6
	B	1	6	6	6
	C	1	6	6	6

(1) Package is preview only.

5 Pin Configuration and Functions

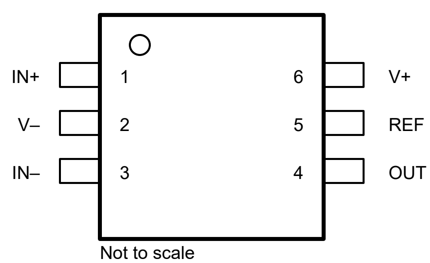


Figure 5-1. INA500 DCK Package, 6-Pin SC70 (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	SC70		
IN–	3	I	Negative (inverting) input
IN+	1	I	Positive (non-inverting) input
OUT	4	O	Output
REF	5	I	Reference input
V–	2	—	Negative supply
V+	6	—	Positive supply

(1) I = input, O = output

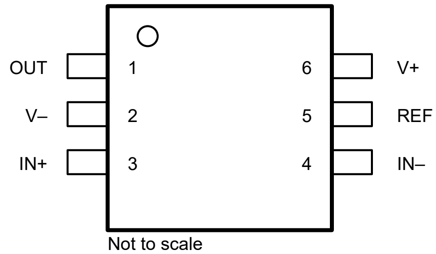


Figure 5-2. INA500 DBV Package, 6-Pin SOT-23 (Top View)

Table 5-2. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	SOT-23		
IN–	4	I	Negative (inverting) input
IN+	3	I	Positive (noninverting) input
OUT	1	O	Output
REF	5	I	Reference input
V–	2	—	Negative supply
V+	6	—	Positive supply

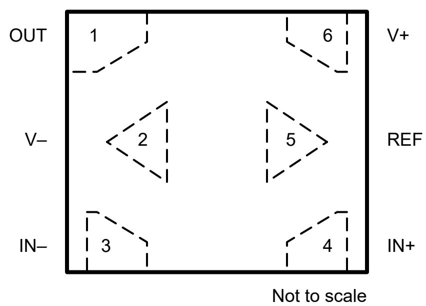


Figure 5-3. INA500 DTQ Package, 6-Pin X2SON (Top View)

Table 5-3. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	X2SON		
IN–	3	I	Negative (inverting) input
IN+	4	I	Positive (noninverting) input
OUT	1	O	Output
REF	5	I	Reference input
V–	2	—	Negative supply
V+	6	—	Positive supply

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single Supply		6	V
	Dual Supply		±3	V
Signal input pins	Current	–10	10	mA
Output short-circuit[2]		Continuous		
Operating Temperature, T_A		–55	150	°C
Junction Temperature, T_J			150	°C
Storage Temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage V_S = (V+) – (V–)	Single-supply	1.7	5.5	V
	Dual-supply	±0.85	±2.75	
C_{BYP}	Bypass capacitor on the power supply pins [1]	0.1		µF
Specified temperature	Specified temperature	–40	125	°C

(1) For C_{BYP}, use low-ESR ceramic capacitors between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Ensure that C_{BYP} is placed as close to the device as possible and the supply trace routes through C_{BYP} before reaching the supply pin.

6.4 Thermal Information

THERMAL METRIC[1]		INA500			UNIT
		DCK (SC70)	DBV (SOT-23)	DTQ (X2SON)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	200.2	195.9	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.6	115.5	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	77.1	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	42.6	52.2	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.4	76.8	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics - INA500A

For V_S = (V+) – (V–) = 1.7V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1, R_L = 100kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET							
V_{OSO}	Offset voltage, RTO[3]	V_S = 5.5V	T_A = 25°C		±0.70	±3.5	mV
V_{OSO}	Offset voltage over T, RTO[3]	V_S = 5.5V	T_A = –40°C to 125°C			±3.6	mV
V_{OSO}	Offset temp drift, RTO[3] [1]	V_S = 5.5V	T_A = –40°C to 125°C		±1.8	8.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.7V to 5.5V	T_A = 25°C		40	175	µV/V
INPUT IMPEDANCE							
$R_{IN\text{-}DM}$	Differential Resistance				2160		kΩ
$R_{IN\text{-}CM}$	Common-mode Resistance				1080		kΩ
INPUT VOLTAGE							
V_{CM}	Input common-mode Range	V_{REF} = V_S / 2		2*(V–) – V_{REF}		2*(V+) – V_{REF}	V
CMRR DC	Common-mode rejection ratio, RTO[3]	V_{CM} = [2*(V–) – V_{REF}] to [2*(V+) – V_{REF} – 1.4V], High CMRR region	V_S = 5.5V, V_{REF} = V_S / 2	75	87		dB
CMRR DC	Common-mode rejection ratio, RTO[3]	V_{CM} = [2*(V–) – V_{REF}] to [2*(V+) – V_{REF}], Rail-to-Rail CMRR region	V_S = 5.5V, V_{REF} = V_S / 2	62	77		dB
NOISE VOLTAGE							
e_{NI}	Output voltage noise density		f = 1kHz		310		nV/√Hz
			f = 10kHz		308		nV/√Hz
E_{NI}	Output voltage noise	f_B = 0.1Hz to 10Hz			8		μV_{PP}
GAIN							
GE	Gain error[2]	V_{REF} = V_S / 2	V_O = (V–) + 0.1V to (V+) – 0.1V		±0.01	±0.05	%
	Gain drift vs temperature[2]		T_A = –40°C to 125°C			±1	ppm/°C
OUTPUT							
V_{OH}	Positive rail headroom	R_L = 10kΩ to V_S / 2			10.5	15	mV
V_{OL}	Negative rail headroom	R_L = 10kΩ to V_S / 2			8.5	15	mV
C_L Drive	Load capacitance drive	V_O = 100mV step, Overshoot < 20%			200		pF
Z_O	Closed-loop output impedance	f = 10kHz			200		Ω
I_{SC}	Short-circuit current	V_S = 5.5V			±33		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	V_{IN} = 10$mV_{pk\text{-}pk}$			125		kHz
THD + N	Total harmonic distortion + noise	V_S = 5.5V, V_{CM} = 2.75V, V_O = 1V_{RMS}, R_L = 100kΩ *f* = 1kHz, 80kHz measurement BW			0.02		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV			100		dB
SR	Slew rate	V_S = 5V, V_O = 2V step			0.20		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{STEP} = 2V, C_L = 10pF			18		µs
t_S	Settling time	To 0.01%, V_S = 5.5V, V_{STEP} = 2V, C_L = 10pF			33		µs
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{OUT_STEP} = 4V, C_L = 10pF			26		µs
t_S	Settling time	To 0.01%, V_S = 5.5V, V_{OUT_STEP} = 4V, C_L = 10pF			43		µs
	Overload recovery	V_{STEP} = V_S / G			23.2		µs
REFERENCE INPUT							
REF - V_{IN}	Input voltage range	V_S = 5.5V		(V–)		(V+)	V
REF - G	Reference gain to output				1		V/V

6.5 Electrical Characteristics - INA500A (continued)

For V_S = (V+) – (V–) = 1.7V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, V_{REF} = V_S / 2, G = 1, R_L = 100kΩ connected to V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REF - GE	Reference gain error[(2)]	V_S = 5.5V			±0.005	±0.02	%
POWER SUPPLY							
V_S	Power-supply voltage	Dual-supply		±0.85		±2.75	V
I_Q	Quiescent current	V_S = 1.7V			14.5		µA
		V_S = 5.5V			13.5	18.5	µA
		V_S = 5.5V	T_A = –40°C to 125°C			19.5	

(1) Offset drifts are uncorrelated.
(2) Minimum and maximum values are specified by characterization.
(3) RTO stands for Referred to Output

6.6 Electrical Characteristics - INA500B

For V_S = (V+) – (V–) = 1.7V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, V_{MID} = [(V+) + (V–)] / 2, G = 0.5, V_{REF} = V_{MID}, R_L = 100kΩ connected to V_{MID}, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_{MID}, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0V and V_{OUT} = V_{MID} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET							
V_{OSO}	Offset voltage, RTO	V_S = 5.5V	T_A = 25°C		±0.50	±2.6	mV
	Offset voltage over T, RTO	V_S = 5.5V	T_A = –40°C to 125°C			±2.7	mV
	Offset temp drift, RTO(1)	V_S = 5.5V	T_A = –40°C to 125°C		±1.4	6.6	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.7V to 5.5V	T_A = 25°C		40	150	µV/V
INPUT IMPEDANCE							
$R_{IN\text{-}DM}$	Differential Resistance				2880		kΩ
$R_{IN\text{-}CM}$	Common-mode Resistance				1080		kΩ
INPUT VOLTAGE							
V_{CM}	Input common-mode Range	V_{REF} = V_{MID}		3*(V–) – 2*(V_{REF})		3*(V+) – 2*(V_{REF})	V
CMRR DC	Common-mode rejection ratio, RTO	V_{CM} = [3*(V–) – 2*(V_{REF})] to [3*(V+) – 2*(V_{REF}) – 2.1]	V_S = 5.5V, V_{REF} = V_{MID}	77	89		dB
CMRR DC	Common-mode rejection ratio, RTO	V_{CM} = [3*(V–) – 2*(V_{REF})] to [3*(V+) – 2*(V_{REF})]	V_S = 5.5V, V_{REF} = V_{MID}	62	79		dB
NOISE VOLTAGE							
e_{NI}	Output voltage noise density		f = 1kHz		200		nV/√Hz
			f = 10kHz		190		nV/√Hz
E_{NI}	Output voltage noise	f_B = 0.1Hz to 10Hz			7.5		$µV_{PP}$
GAIN							
GE	Gain error(2)	V_{REF} = V_{MID}	V_O = (V–) + 0.1V to (V+) – 0.1V		±0.003	±0.075	%
	Gain drift vs temperature(2)	G = 0.5	T_A = –40°C to 125°C			±1	ppm/°C
OUTPUT							
V_{OH}	Positive rail headroom	R_L = 10kΩ to V_{MID}			10	25	mV
V_{OL}	Negative rail headroom	R_L = 10kΩ to V_{MID}			8	20	mV
C_L Drive	Load capacitance drive	V_O = 100mV step, Overshoot < 20%			120		pF
Z_O	Closed-loop output impedance	f = 10kHz			165		Ω
I_{SC}	Short-circuit current	V_S = 5.5V			±35		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB		V_{IN} = 10$mV_{pk\text{-}pk}$		135		kHz
THD + N	Total harmonic distortion + noise	V_S = 5.5V, V_{CM} = 2.75V, V_O = 1V_{RMS}, R_L = 100kΩ *f* = 1kHz, 80kHz measurement BW			0.017		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV			95		dB
SR	Slew rate	V_S = 5V, V_O = 2V step			0.18		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{STEP} = 2V, C_L = 10pF			21		µs
		To 0.01%, V_S = 5.5V, V_{STEP} = 2V, C_L = 10pF			34		µs
	Settling time	To 0.1%, V_S = 5.5V, V_{OUT_STEP} = 4V, C_L = 10pF			30		µs
		To 0.01%, V_S = 5.5V, V_{OUT_STEP} = 4V, C_L = 10pF			45		µs
	Overload recovery	V_{STEP} = V_S / G			24		µs
REFERENCE INPUT							
REF - V_{IN}	Input voltage range	V_S = 5.5V		(V–)		(V+)	V
REF - G	Reference gain to output				1		V/V

For V_S = (V+) – (V–) = 1.7V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, V_{MID} = [(V+) + (V–)] / 2, G = 0.5, V_{REF} = V_{MID}, R_L = 100kΩ connected to V_{MID}, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_{MID}, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0V and V_{OUT} = V_{MID} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REF - GE	Reference gain error[(2)]	V_S = 5.5V			±0.002	±0.025	%
POWER SUPPLY							
V_S	Power-supply voltage	Dual-supply		±0.85		±2.75	V
I_Q	Quiescent current	V_S = 1.7V			15		µA
I_Q	Quiescent current	V_S = 5.5V			14	19	µA
		V_S = 5.5V	T_A = –40°C to 125°C			20	

(1) Offset drifts are uncorrelated.
(2) Minimum and maximum values are specified by characterization.

6.7 Electrical Characteristics - INA500C

For V_S = (V+) – (V–) = 1.7V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, V_{MID} = [(V+) + (V–)] / 2, G = 0.25, V_{REF} = V_{MID}, R_L = 100kΩ connected to V_{MID}, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_{MID}, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0V and V_{OUT} = V_{MID} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET							
V_{OSO}	Offset voltage, RTO	V_S = 5.5V	T_A = 25°C		±0.40	±2.2	mV
	Offset voltage over T, RTO	V_S = 5.5V	T_A = –40°C to 125°C			±2.3	mV
	Offset temp drift, RTO(1)	V_S = 5.5V	T_A = –40°C to 125°C		±1.1	5.5	µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.7V to 5.5V	T_A = 25°C		40	130	µV/V
INPUT IMPEDANCE							
R_{IN-DM}	Differential Resistance				3360		kΩ
R_{IN-CM}	Common-mode Resistance				1050		kΩ
INPUT VOLTAGE							
V_{CM}	Input common-mode Range	V_{REF} = V_{MID}		5*(V–) – 4*(V_{REF})		5*(V+) – 4*(V_{REF})	V
CMRR DC	Common-mode rejection ratio, RTO	V_{CM} = [5*(V–) – 4*(V_{REF})] to [5*(V+) – 4*(V_{REF}) – 3.5]	V_S = 5.5V, V_{REF} = V_{MID}	77.7	85		dB
CMRR DC	Common-mode rejection ratio, RTO	V_{CM} = [5*(V–) – 4*(V_{REF})] to [5*(V+) – 4*(V_{REF})]	V_S = 5.5V, V_{REF} = V_{MID}	70			dB
NOISE VOLTAGE							
e_{NI}	Output voltage noise density		f = 1kHz		150		nV/√Hz
			f = 10kHz		140		nV/√Hz
E_{NI}	Output voltage noise	f_B = 0.1Hz to 10Hz			7.5		µV_{PP}
GAIN							
GE	Gain error(2)	V_{REF} = V_{MID}	V_O = (V–) + 0.1 V to (V+) – 0.1V		±0.003	±0.1	%
	Gain drift vs temperature(2)	G = 0.5	T_A = –40°C to 125°C			±1	ppm/°C
OUTPUT							
V_{OH}	Positive rail headroom	R_L = 10kΩ to V_{MID}			15	25	mV
V_{OL}	Negative rail headroom	R_L = 10kΩ to V_{MID}			15	20	mV
C_L Drive	Load capacitance drive	V_O = 100mV step, Overshoot < 20%			100		pF
Z_O	Closed-loop output impedance	f = 10kHz			180		Ω
I_{SC}	Short-circuit current	V_S = 5.5V			±30		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB		V_{IN} = 10mV_{pk-pk}		160		kHz
THD + N	Total harmonic distortion + noise	V_S = 5.5V, V_{CM} = 2.75V, V_O = 1V_{RMS}, R_L = 100kΩ f = 1kHz, 80kHz measurement BW			0.017		%
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV			105		dB
SR	Slew rate	V_S = 5V, V_O = 2V step			0.19		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{STEP} = 2V, C_L = 10pF			20		µs
		To 0.01%, V_S = 5.5V, V_{STEP} = 2V, C_L = 10pF			32		µs
	Settling time	To 0.1%, V_S = 5.5V, V_{OUT_STEP} = 4V, C_L = 10pF			26		µs
		To 0.01%, V_S = 5.5V, V_{OUT_STEP} = 4V, C_L = 10pF			40		µs
	Overload recovery	V_{STEP} = V_S / G			23.2		µs
REFERENCE INPUT							
REF - V_{IN}	Input voltage range	V_S = 5.5V, V_{REF} = V_{MID}		(V–)		(V+)	V
REF - G	Reference gain to output				1		V/V

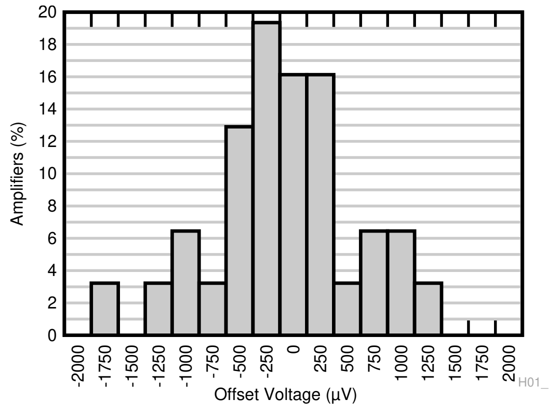
For V_S = (V+) – (V–) = 1.7V to 5.5V (±0.85V to ±2.75V) at T_A = 25°C, V_{MID} = [(V+) + (V–)] / 2, G = 0.25, V_{REF} = V_{MID}, R_L = 100kΩ connected to V_{MID}, V_{CM} = [(V_{IN+}) + ($V_{IN–}$)] / 2 = V_{MID}, V_{IN} = (V_{IN+}) – ($V_{IN–}$) = 0V and V_{OUT} = V_{MID} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REF - GE	Reference gain error[(2)]	V_S = 5.5V			±0.002	±0.02	%
POWER SUPPLY							
V_S	Power-supply voltage	Dual-supply		±0.85		±2.75	V
I_Q	Quiescent current	V_S = 1.7V			15		μA
I_Q	Quiescent current	V_S = 5.5V			14	19	μA
		V_S = 5.5V	T_A = –40°C to 125°C			20	

(1) Offset drifts are uncorrelated.
(2) Minimum and maximum values are specified by characterization.

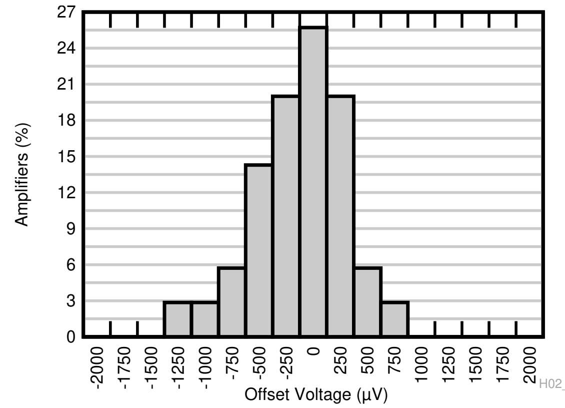
6.8 Typical Characteristics

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



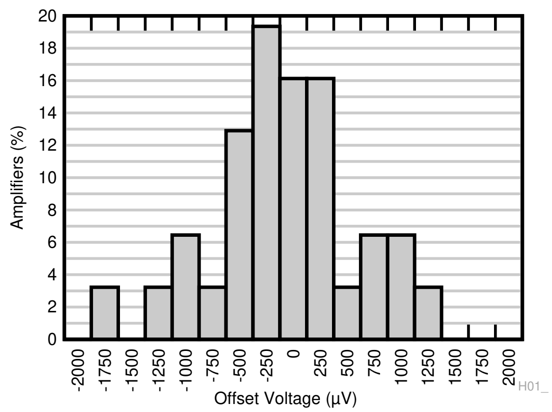
G = 1 N = 31 µ = –5.78µV σ = 0.670mV

Figure 6-1. Typical Distribution of Output Referred Offset Voltage



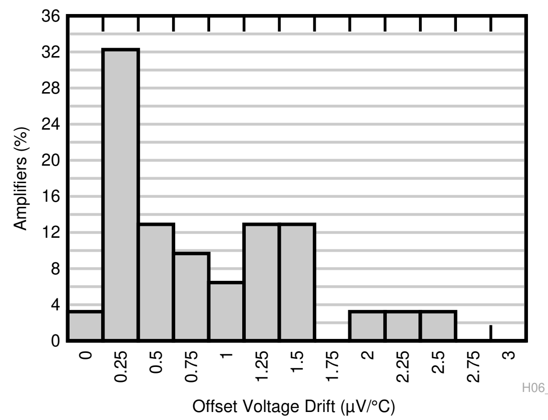
G = 0.5 N = 35 µ = –6.43µV σ = 0.430mV

Figure 6-2. Typical Distribution of Output Referred Offset Voltage



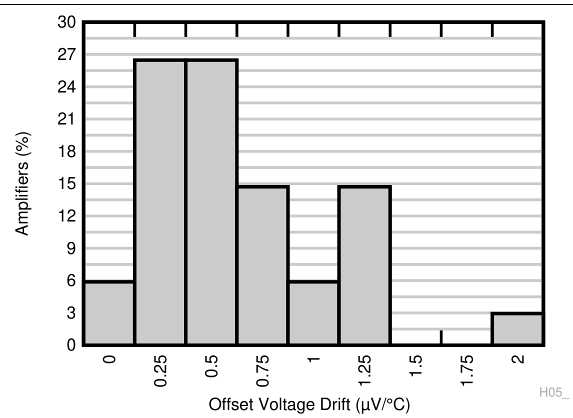
G = 0.25 N = 35 µ = 42.74µV σ = 0.336mV

Figure 6-3. Typical Distribution of Output Referred Offset Voltage



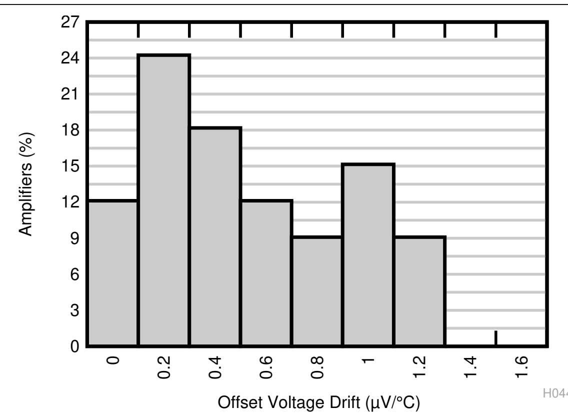
G = 1 N = 31 µ = 0.95µV/°C σ = 0.60µV/°C

Figure 6-4. Typical Distribution of Output Referred Offset Drift



G = 0.5 N = 35 µ = 0.72µV/°C σ = 0.43µV/°C

Figure 6-5. Typical Distribution of Output Referred Offset Drift

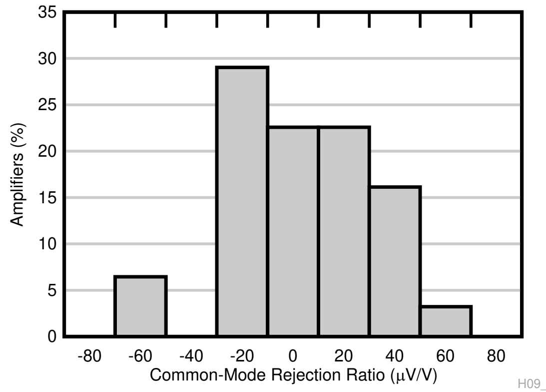


G = 0.25 N = 35 µ = 0.70µV/°C σ = 0.45µV/°C

Figure 6-6. Typical Distribution of Output Referred Offset Drift

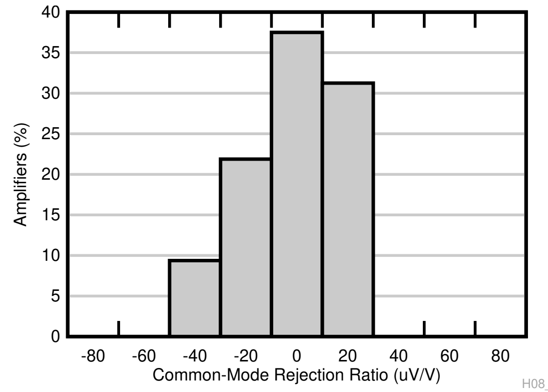
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



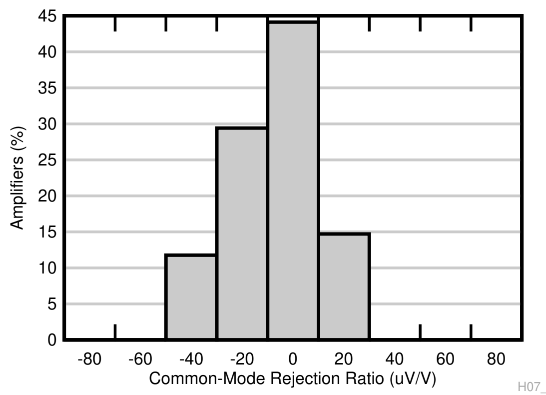
G = 1 N = 31 μ = 13.30μV/V σ = 28.25μV/V

Figure 6-7. Typical Distribution of Output Referred CMRR



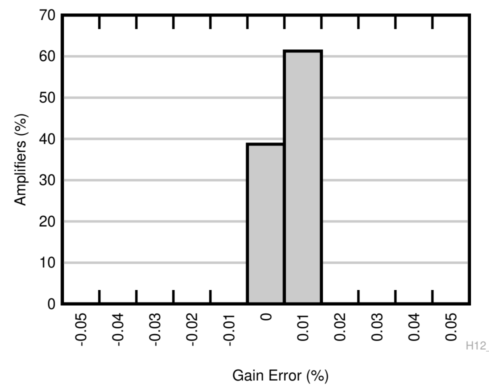
G = 0.5 N = 35 μ = 9.90μV/V σ = 16.30μV/V

Figure 6-8. Typical Distribution of Output Referred CMRR



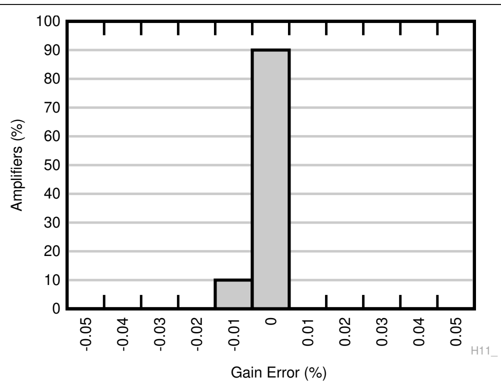
G = 0.25 N = 35 μ = 3.49μV/V σ = 15.46μV/V

Figure 6-9. Typical Distribution of Output Referred CMRR



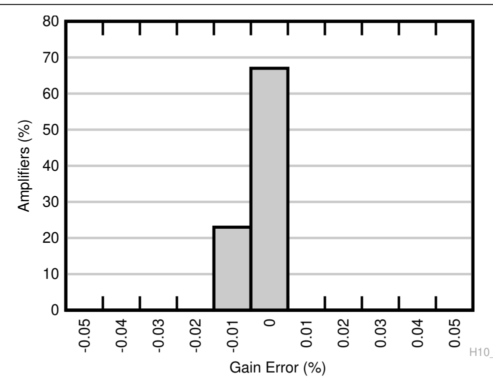
G = 1 N = 31 μ = 0.01% σ = 0.003%

Figure 6-10. Typical Distribution of Gain Error



G = 0.5 N = 35 μ = 0.028% σ = 0.019%

Figure 6-11. Typical Distribution of Gain Error



G = 0.25 N = 35 μ = 0.025% σ = 0.021%

Figure 6-12. Typical Distribution of Gain Error

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)

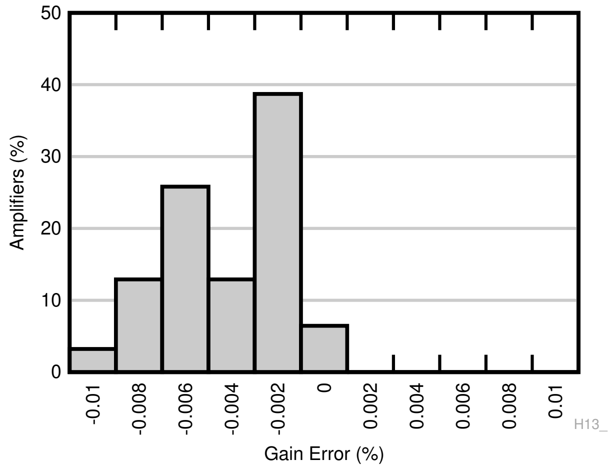


Figure 6-13. Typical Distribution of Reference Gain Error

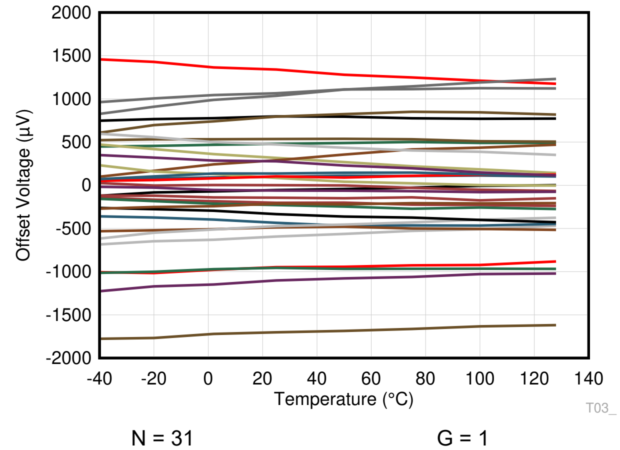


Figure 6-14. Output Referred Offset Voltage vs Temperature

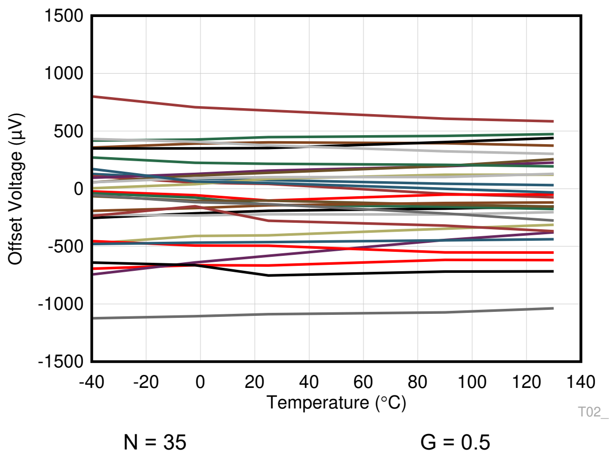


Figure 6-15. Output Referred Offset Voltage vs Temperature

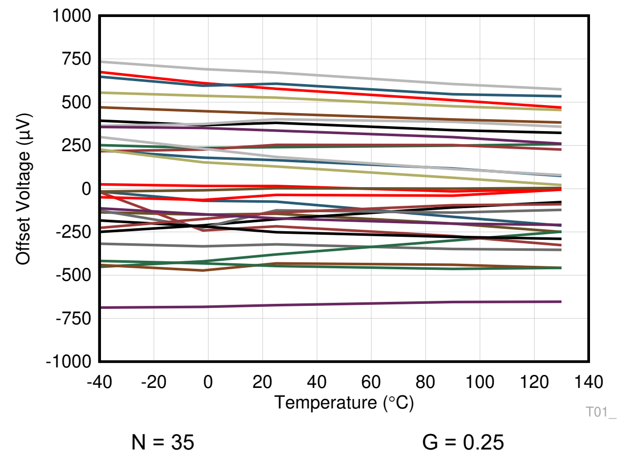


Figure 6-16. Output Referred Offset Voltage vs Temperature

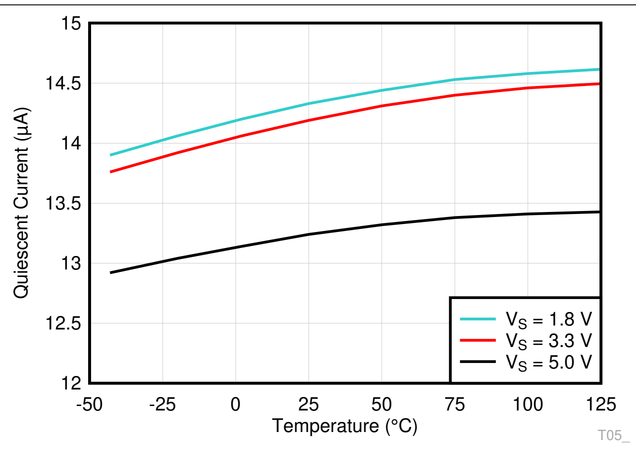


Figure 6-17. Quiescent Current vs Temperature

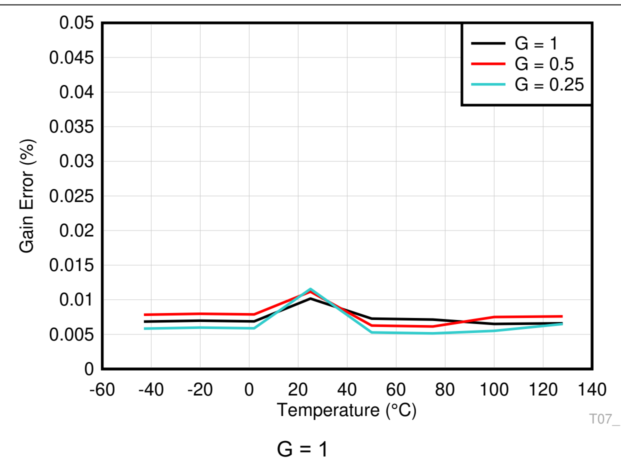
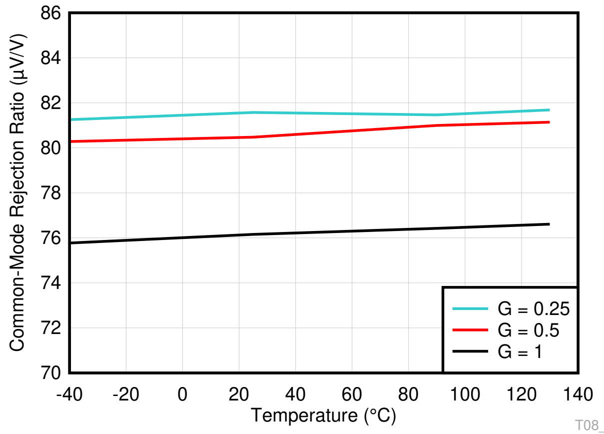


Figure 6-18. Gain Error vs Temperature

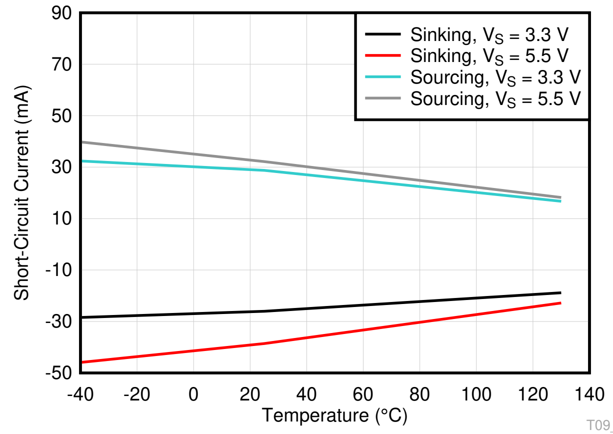
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



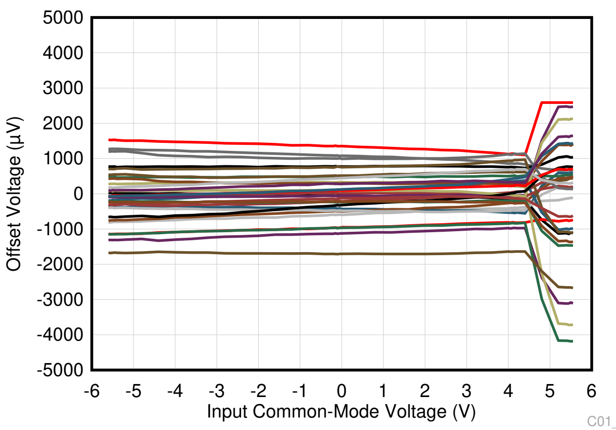
G = 1

Figure 6-19. Output Referred CMRR vs Temperature



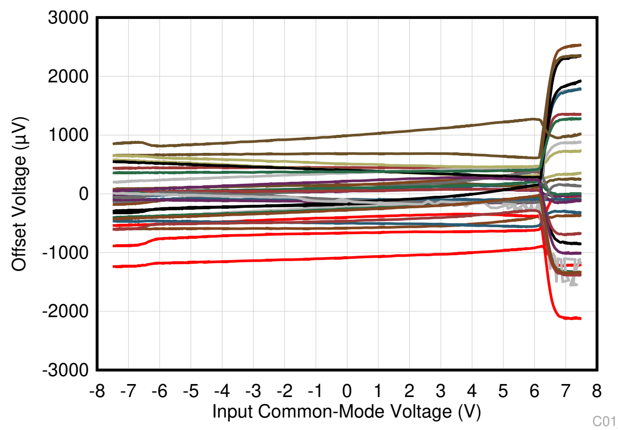
V+ = 2.75V and V– = –2.75V

Figure 6-20. Short-Circuit Current vs Temperature



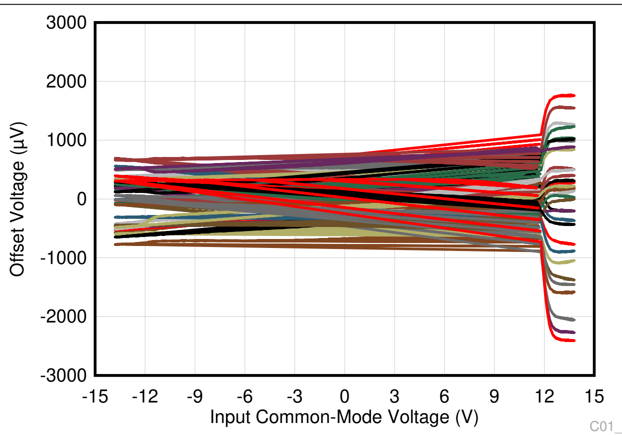
G = 1 V+ = 2.75V and V– = –2.75V N = 31

Figure 6-21. Output Referred Offset Voltage vs Input Common-Mode Voltage



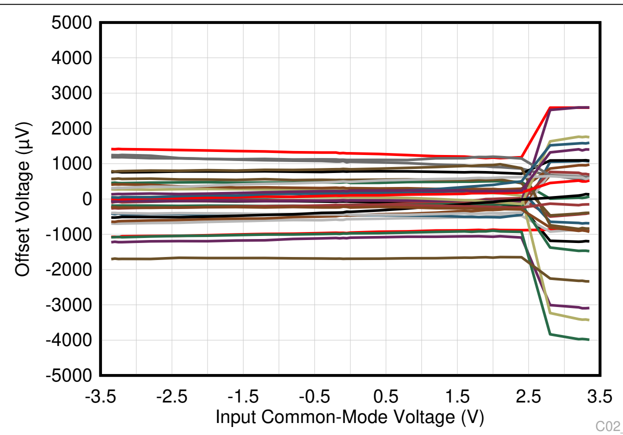
G = 0.5 V+ = 2.75V and V– = –2.75V N = 35

Figure 6-22. Output Referred Offset Voltage vs Input Common-Mode Voltage



G = 0.25 V+ = 2.75V and V– = –2.75V N = 35

Figure 6-23. Output Referred Offset Voltage vs Input Common-Mode Voltage

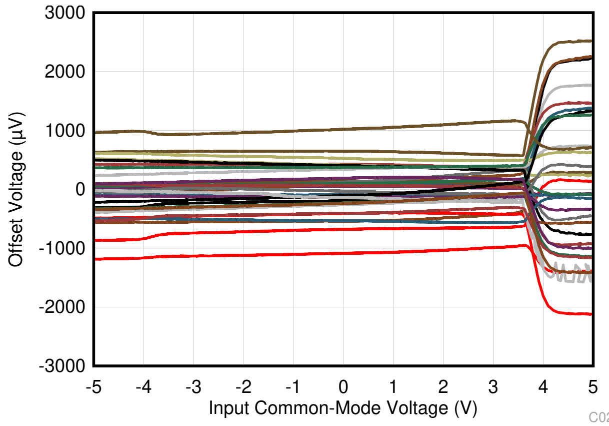


G = 1 V+ = 1.65V and V– = –1.65V N = 31

Figure 6-24. Output Referred Offset Voltage vs Input Common-Mode Voltage

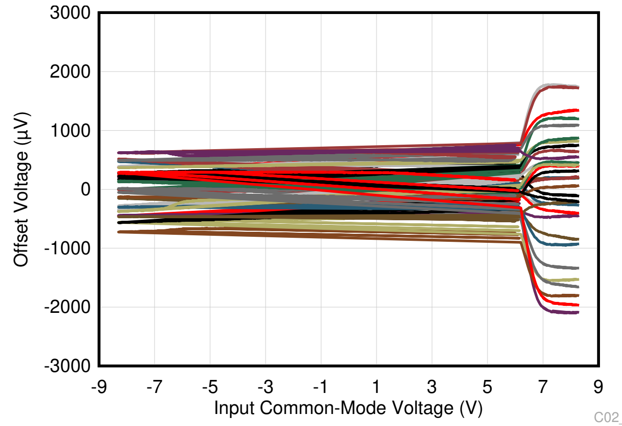
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



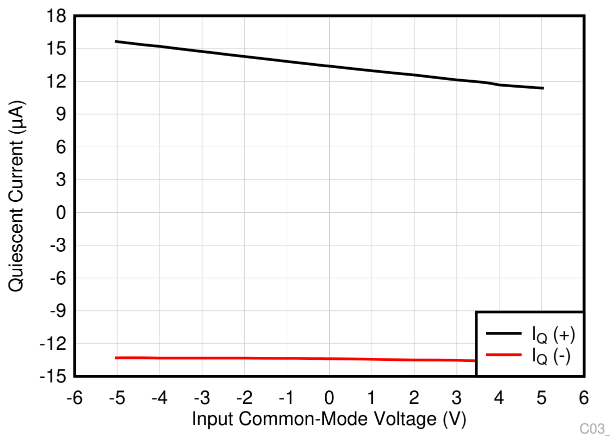
G = 0.5 V+ = 1.65V and V– = –1.65V N = 35

Figure 6-25. Output Referred Offset Voltage vs Input Common-Mode Voltage



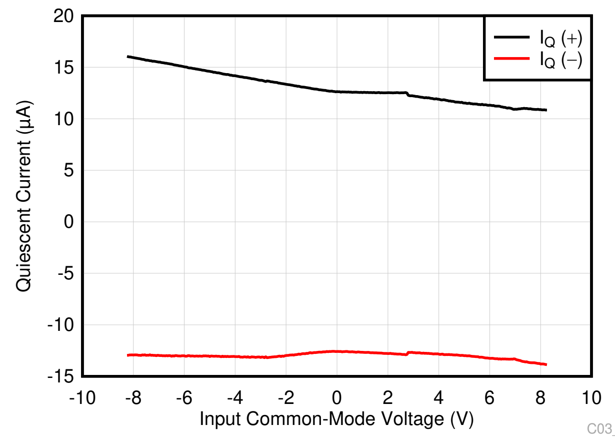
G = 0.25 V+ = 1.65V and V– = –1.65V N = 35

Figure 6-26. Output Referred Offset Voltage vs Input Common-Mode Voltage



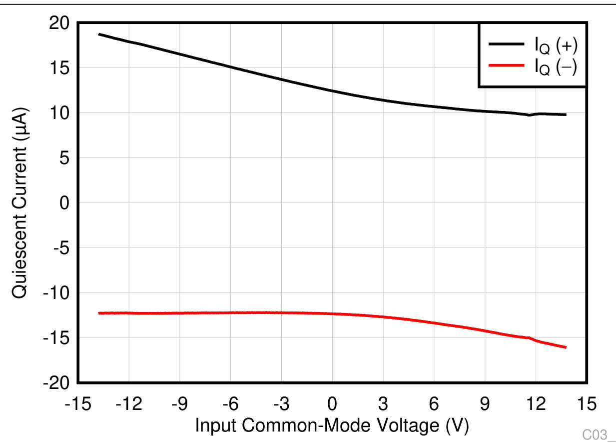
G = 1 V+ = 2.75V and V– = –2.75V

Figure 6-27. Quiescent Current vs Input Common-Mode Voltage



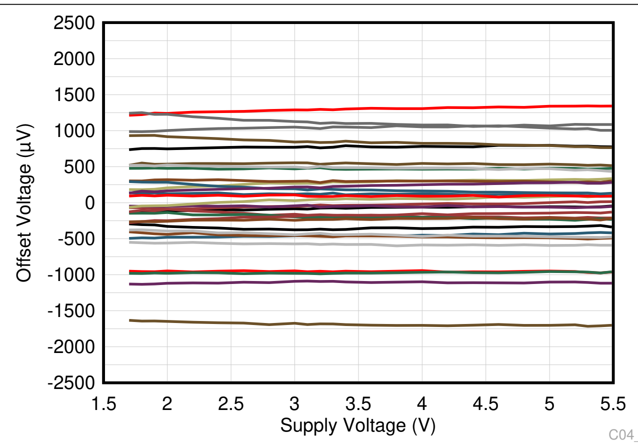
G = 0.5 V+ = 2.75V and V– = –2.75V

Figure 6-28. Quiescent Current vs Input Common-Mode Voltage



G = 0.25 V+ = 2.75V and V– = –2.75V

Figure 6-29. Quiescent Current vs Input Common-Mode Voltage

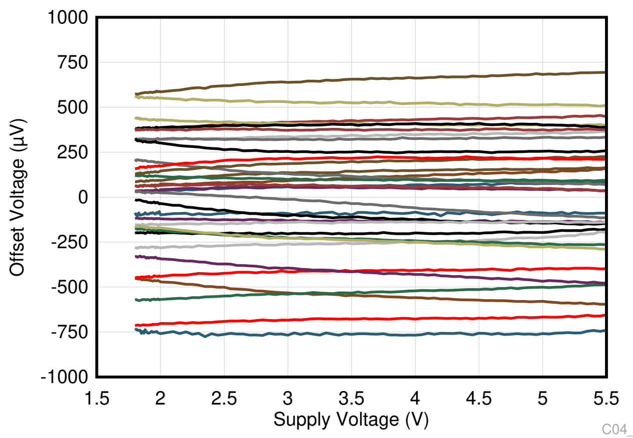


N = 31 G = 1

Figure 6-30. Output Referred Offset Voltage vs Supply Voltage

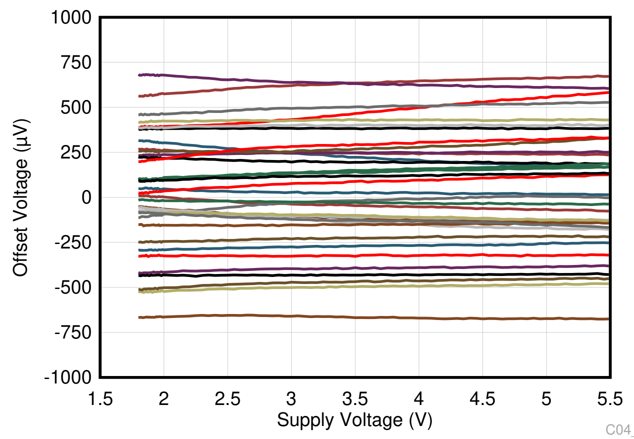
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



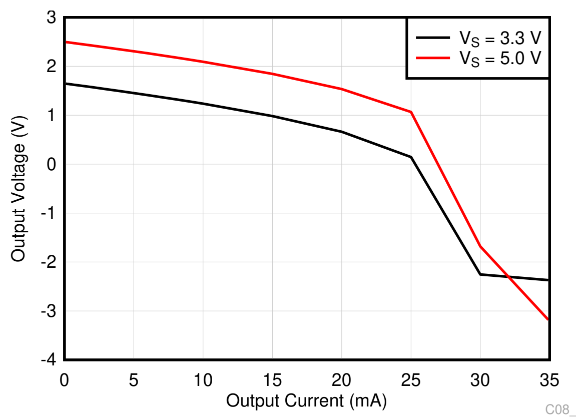
N = 32 G = 0.5

Figure 6-31. Output Referred Offset Voltage vs Supply Voltage



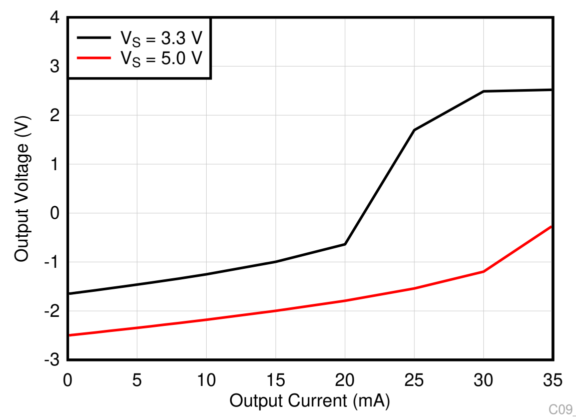
N = 32 G = 0.25

Figure 6-32. Output Referred Offset Voltage vs Supply Voltage



V+ = 2.5V and V– = –2.5V V+ = 1.65V and V– = –1.65V

Figure 6-33. Output Voltage vs Output Current (Sourcing)



V+ = 2.5V and V– = –2.5V V+ = 1.65V and V– = –1.65V

Figure 6-34. Output Voltage vs Output Current (Sinking)

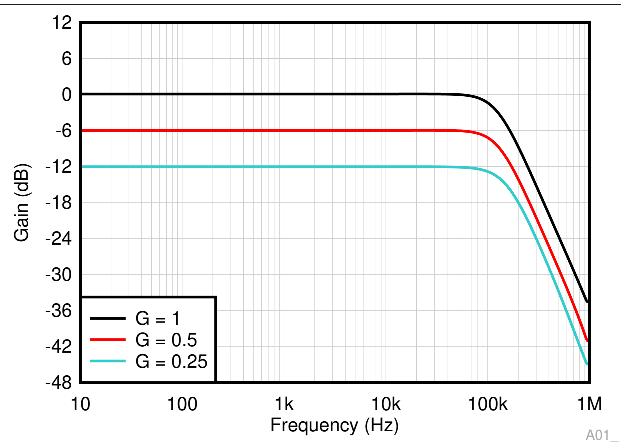


Figure 6-35. Closed-Loop Gain vs Frequency

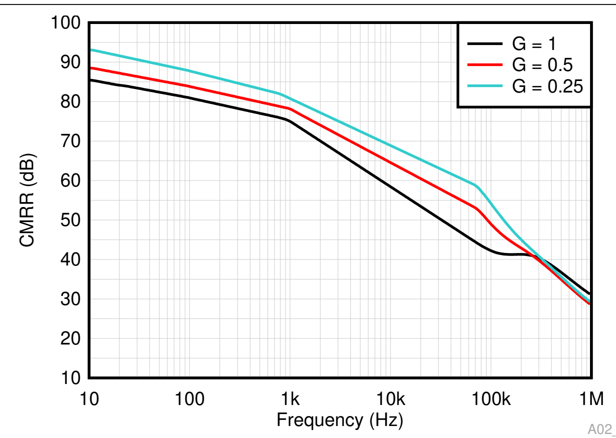


Figure 6-36. CMRR (Referred to Output) vs Frequency

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)

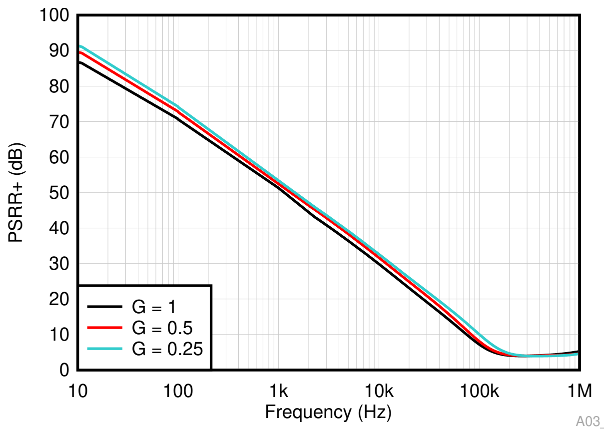


Figure 6-37. PSRR+ (Referred to Output) vs Frequency

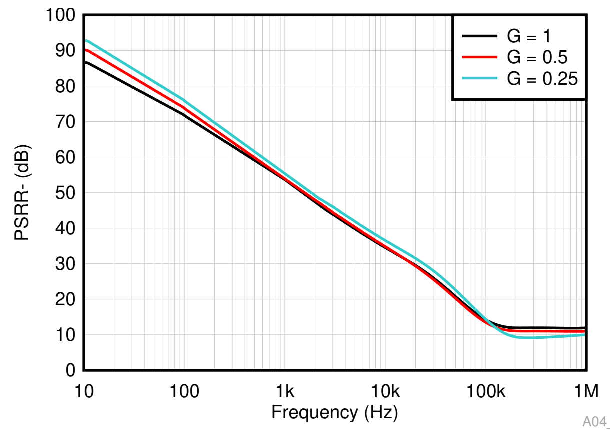


Figure 6-38. PSRR– (Referred to Output) Vs Frequency

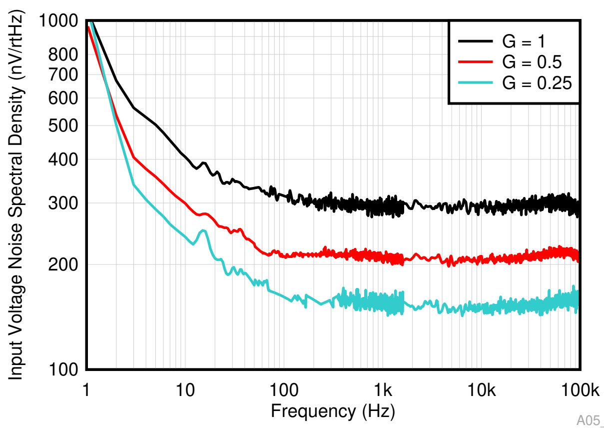


Figure 6-39. Output Referred Voltage Noise Spectral Density

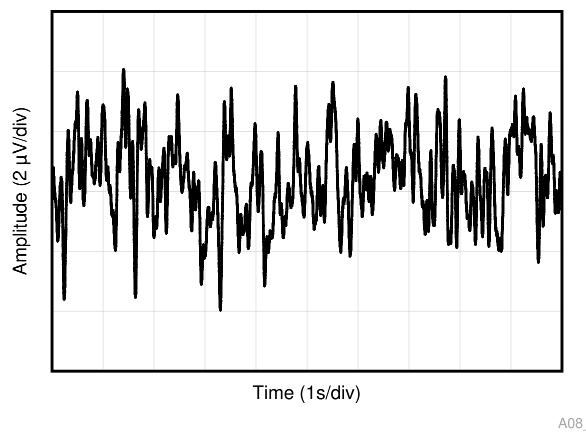


Figure 6-40. Output Referred 0.1 Hz to 10 Hz Voltage Noise in Time Domain

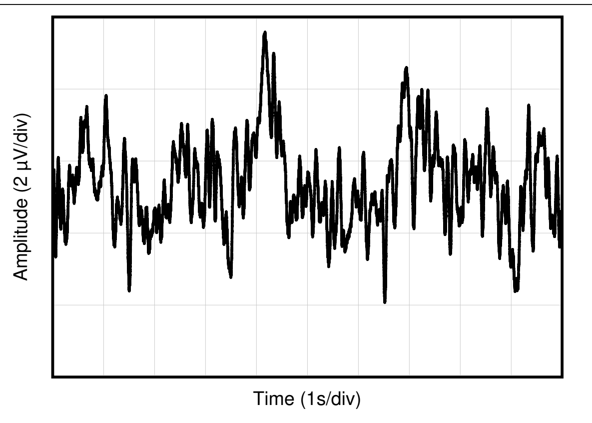


Figure 6-41. Output Referred 0.1 Hz to 10 Hz Voltage Noise in Time Domain

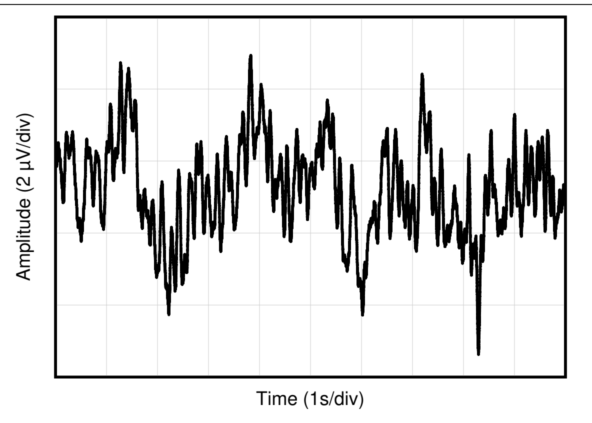


Figure 6-42. Output Referred 0.1 Hz to 10 Hz Voltage Noise in Time Domain

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)

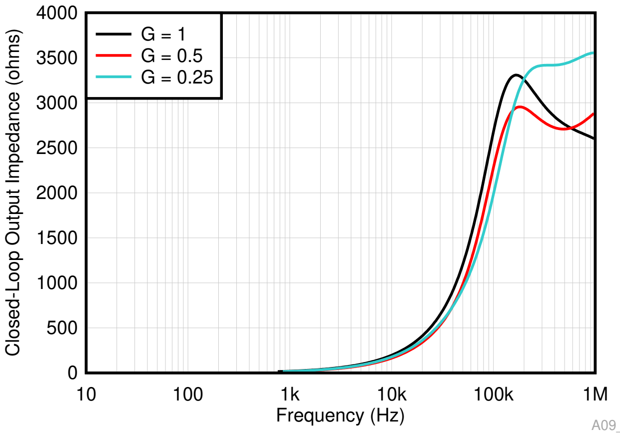


Figure 6-43. Closed-Loop Output Impedance vs Frequency

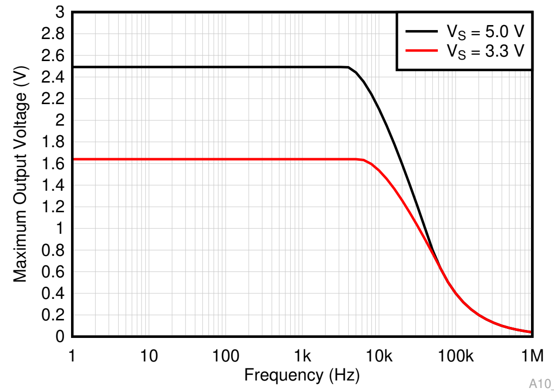
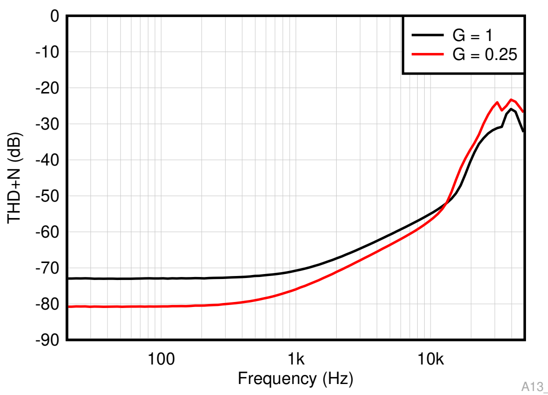
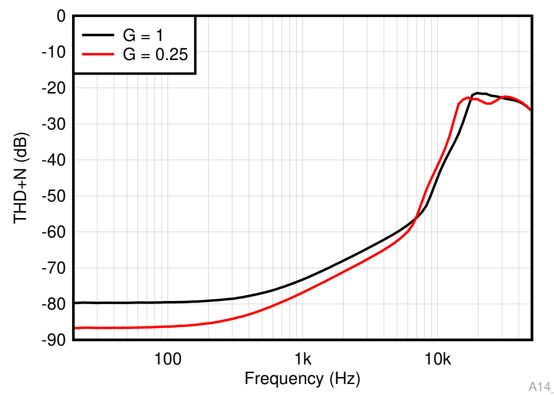


Figure 6-44. Maximum Output Voltage vs Frequency



V_S = 5.5V BW = 80kHz V_{CM} = 2.75V
R_L = 10kΩ V_{OUT} = 0.5V_{RMS} G = 1

Figure 6-45. THD + N Frequency



V_S = 5.5V BW = 80kHz V_{CM} = 2.75V
R_L = 100kΩ V_{OUT} = 1V_{RMS} G = 1

Figure 6-46. THD + N Frequency

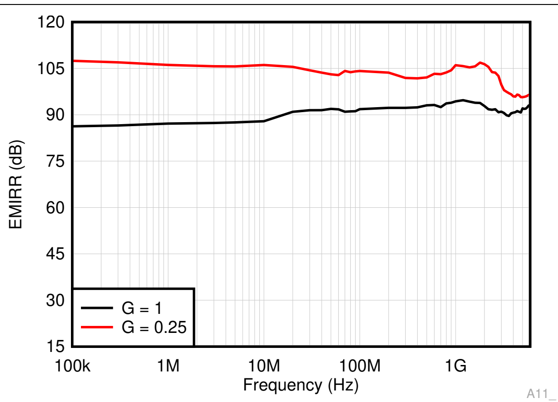


Figure 6-47. Electromagnetic Interference Rejection Ratio Referred to Output vs Frequency (Differential Input)

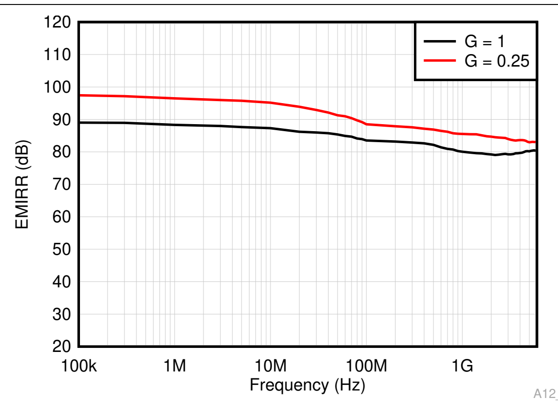
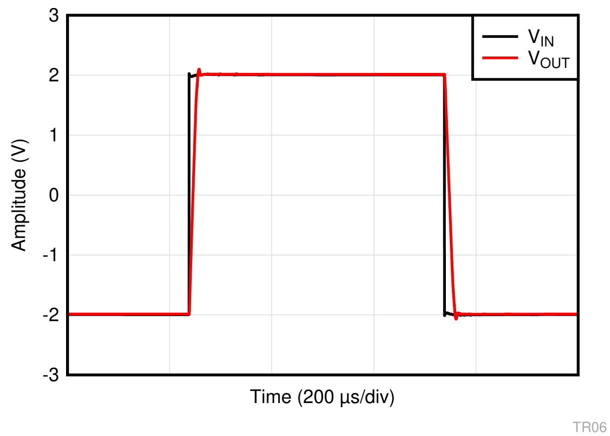


Figure 6-48. Electromagnetic Interference Rejection Ratio Referred to Output vs Frequency (Common-Mode Input)

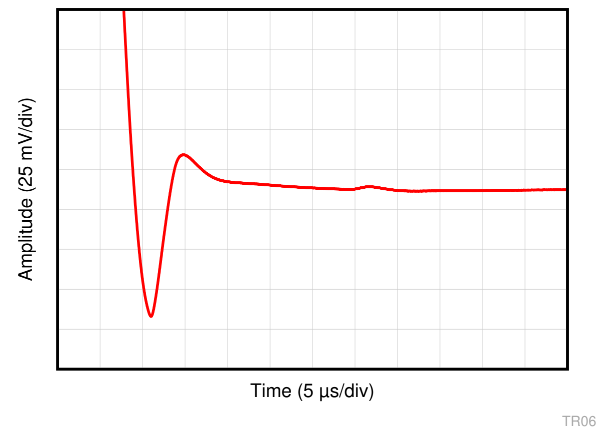
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



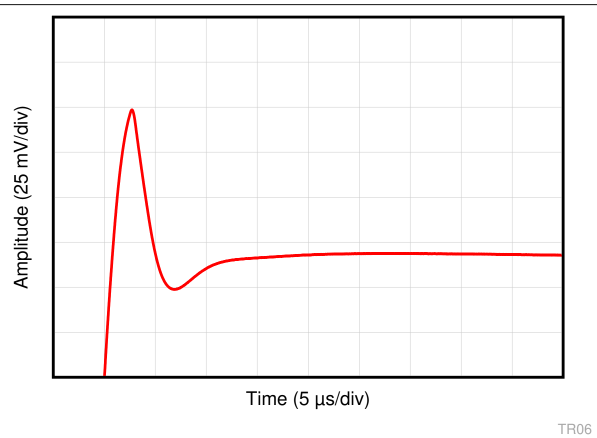
V+ = 2.75V V– = –2.75V G = 1 V_{OUT} = $4V_{PP}$

Figure 6-49. Large Signal Step Response



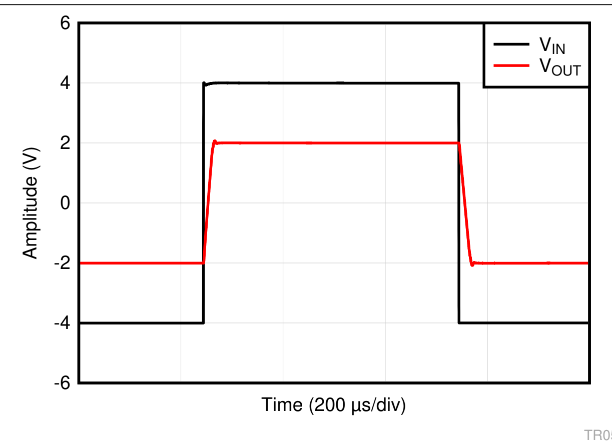
V+ = 2.75V V– = –2.75V G = 1 V_{OUT} = $4V_{PP}$

Figure 6-50. Large Signal Settling Time (Falling Edge)



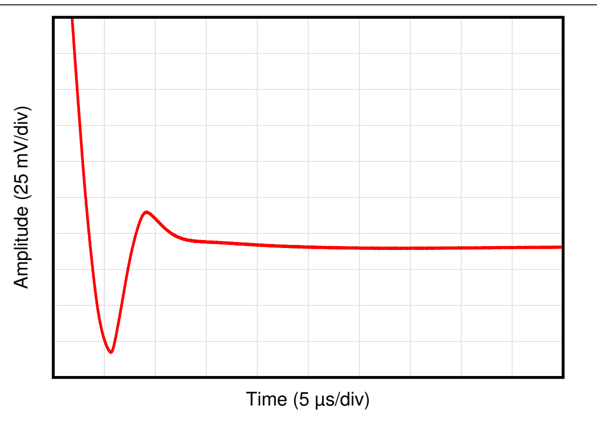
V+ = 2.75V V– = –2.75V G = 1 V_{OUT} = $4V_{PP}$

Figure 6-51. Large Signal Settling Time (Rising Edge)



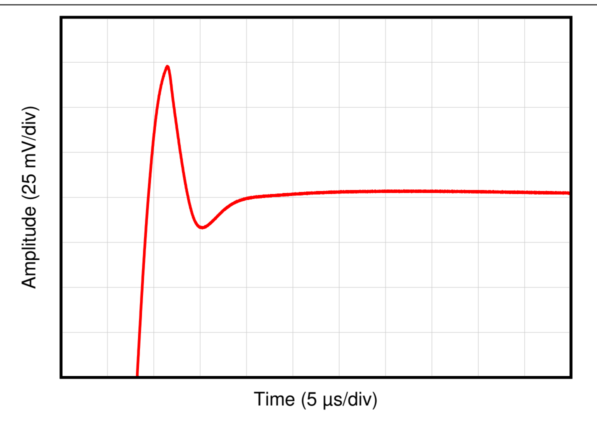
V+ = 2.75V V– = –2.75V G = 0.5 V_{OUT} = $4V_{PP}$

Figure 6-52. Large Signal Step Response



V+ = 2.75V V– = –2.75V G = 0.5 V_{OUT} = $4V_{PP}$

Figure 6-53. Large Signal Settling Time (Falling Edge)

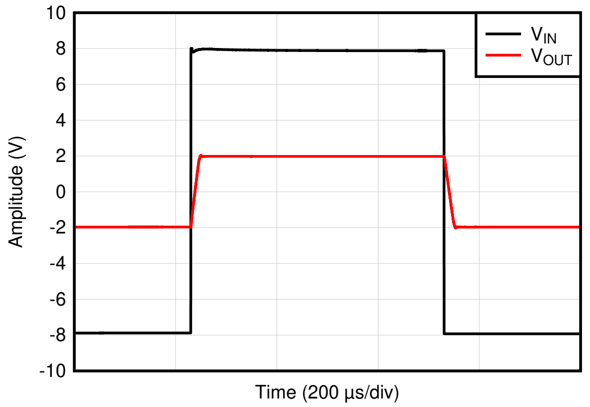


V+ = 2.75V V– = –2.75V G = 0.5 V_{OUT} = $4V_{PP}$

Figure 6-54. Large Signal Settling Time (Rising Edge)

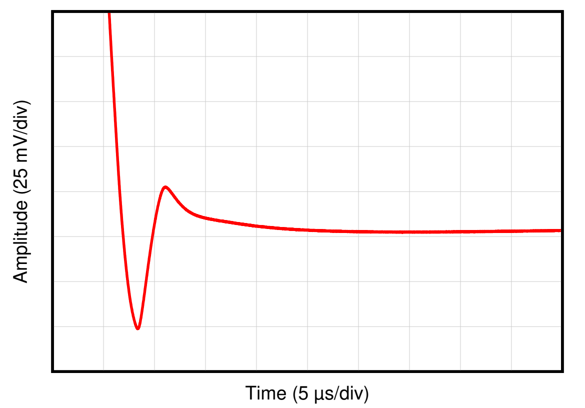
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



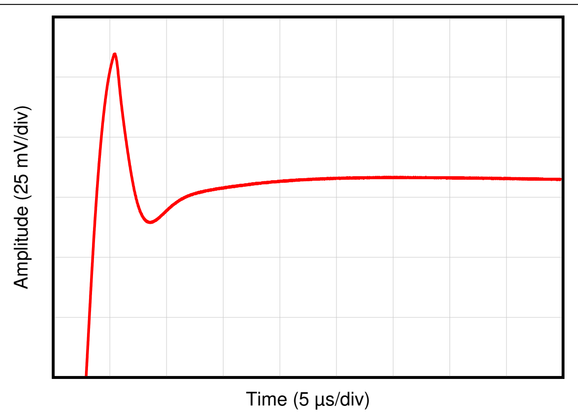
V+ = 2.75V V– = –2.75V G = 0.25 V_{OUT} = $4V_{PP}$

Figure 6-55. Large Signal Step Response



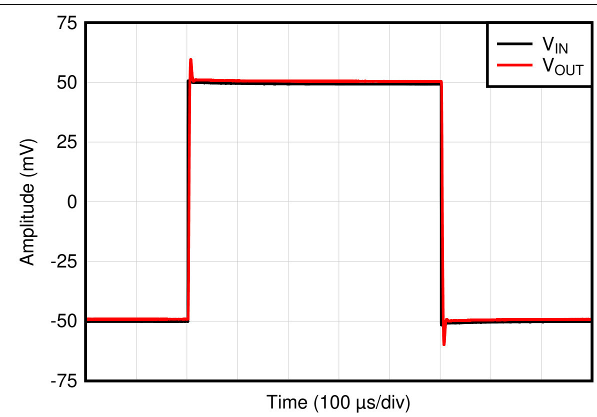
V+ = 2.75V V– = –2.75V G = 0.25 V_{OUT} = $4V_{PP}$

Figure 6-56. Large Signal Settling Time (Falling Edge)



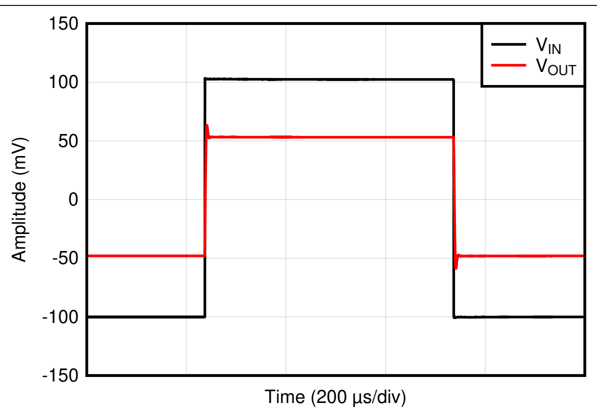
V+ = 2.75V V– = –2.75V G = 0.25 V_{OUT} = $4V_{PP}$

Figure 6-57. Large Signal Settling Time (Rising Edge)



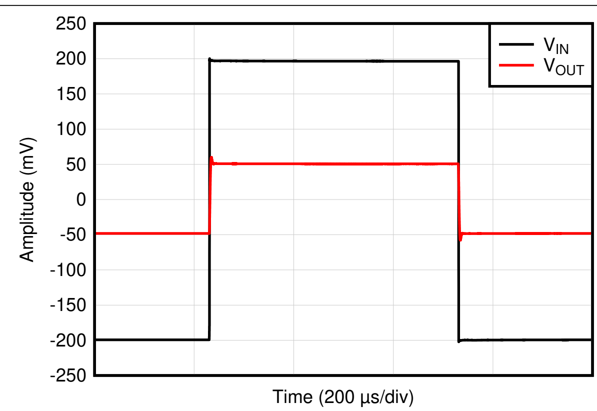
V+ = 2.75V V– = –2.75V G = 1 V_{OUT} = $100mV_{PP}$

Figure 6-58. Small-Signal Step Response



V+ = 2.75V V– = –2.75V G = 0.5 V_{OUT} = $100mV_{PP}$

Figure 6-59. Small-Signal Step Response

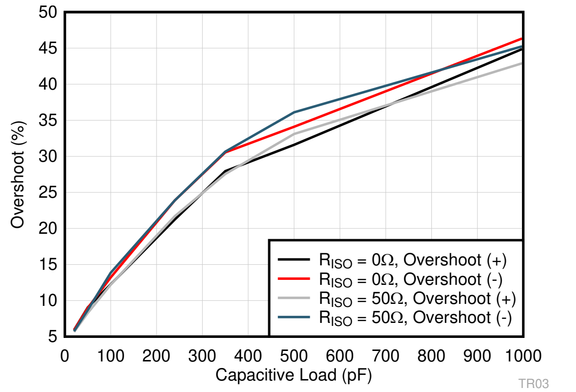


V+ = 2.75V V– = –2.75V G = 0.25 V_{OUT} = $100mV_{PP}$

Figure 6-60. Small-Signal Step Response

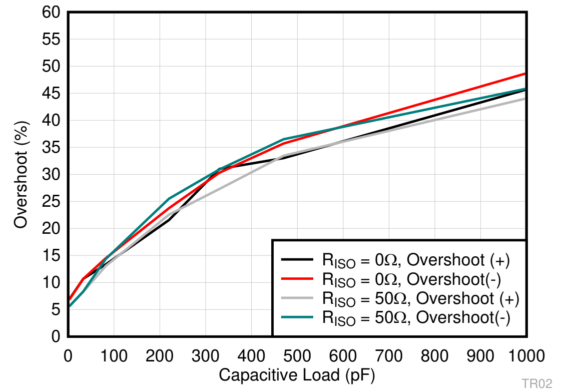
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



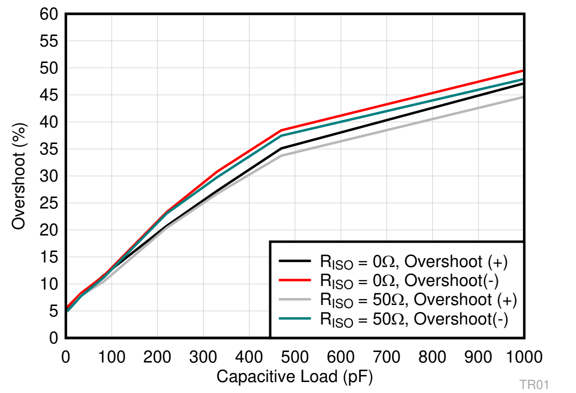
V_S = 5.5V G = 1 V_{OUT} = 100mV_{PP}

Figure 6-61. Small-Signal Overshoot vs Capacitive Load



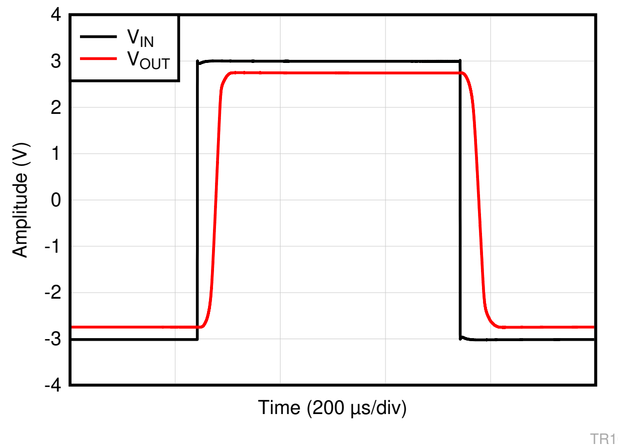
V_S = 5.5V G = 0.5 V_{OUT} = 100mV_{PP}

Figure 6-62. Small-Signal Overshoot vs Capacitive Load



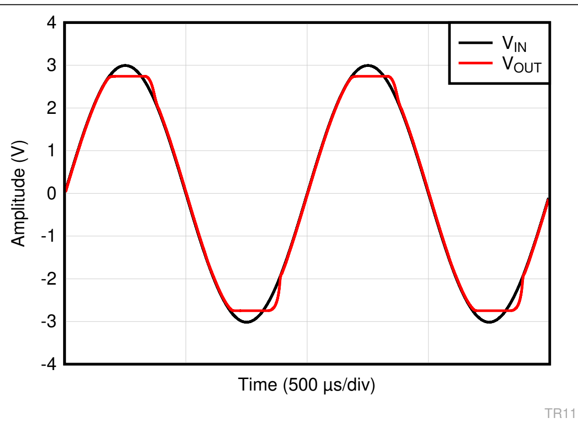
V_S = 5.5V G = 0.25 V_{OUT} = 100mV_{PP}

Figure 6-63. Small-Signal Overshoot vs Capacitive Load



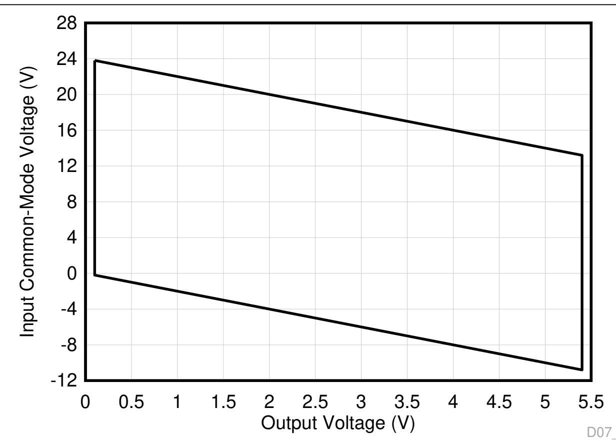
V+ = 2.75V V– = –2.75V G = 1 V_{IN} = 6V_{PP}

Figure 6-64. Over-Load Recovery



V+ = 2.75V V– = –2.75V G = 1 V_{IN} = 6V_{PP}

Figure 6-65. No Phase Reversal

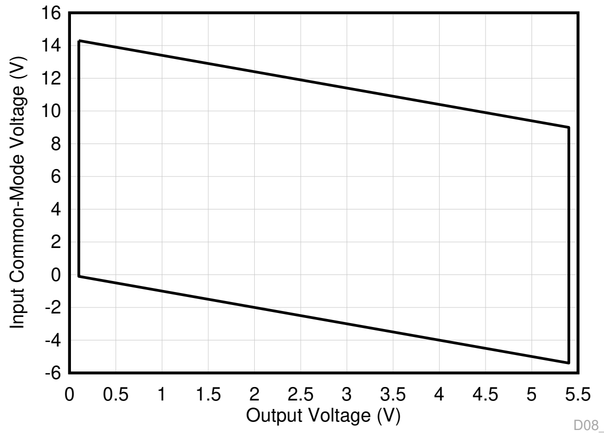


V+ = 5.5V V– = 0V G = 0.25 V_{REF} = 0V

Figure 6-66. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

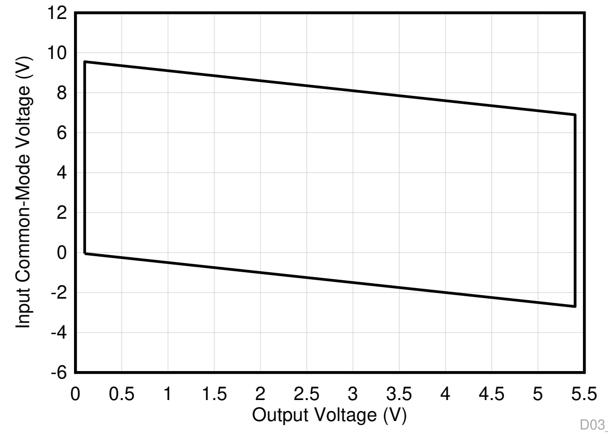
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



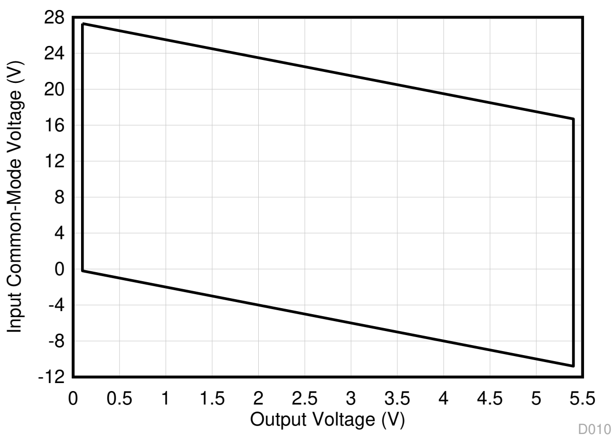
V+ = 5.5V V– = 0V G = 0.5 V_{REF} = 0V

Figure 6-67. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



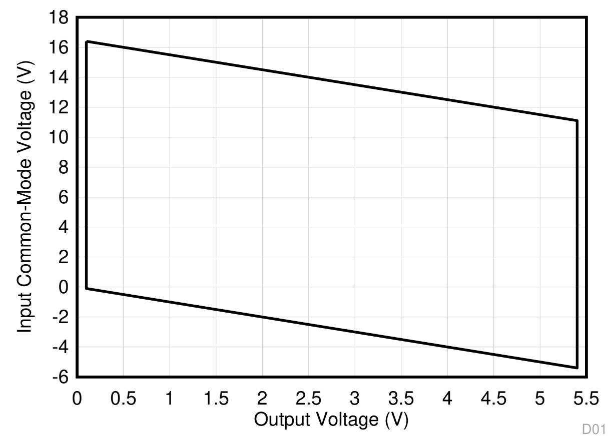
V+ = 5.5V V– = 0V G = 1 V_{REF} = 0V

Figure 6-68. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V+ = 5.5V V– = 0V G = 0.25 V_{REF} = 0V

Figure 6-69. Input Common-Mode Voltage vs Output Voltage (Rail-to-Rail CMRR Region)

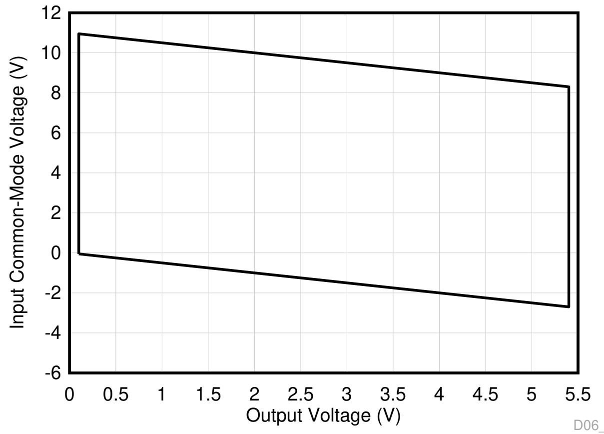


V+ = 5.5V V– = 0V G = 0.5 V_{REF} = 0V

Figure 6-70. Input Common-Mode Voltage vs Output Voltage (Rail-to-Rail CMRR Region)

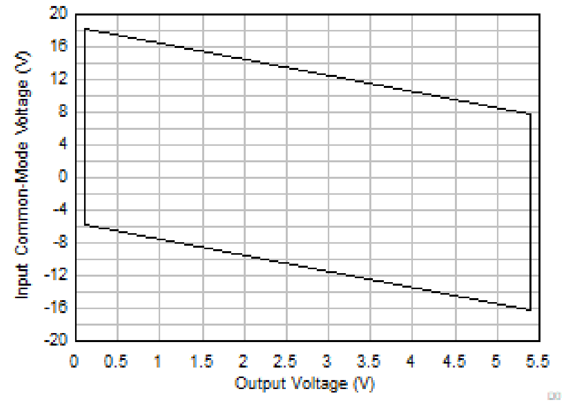
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



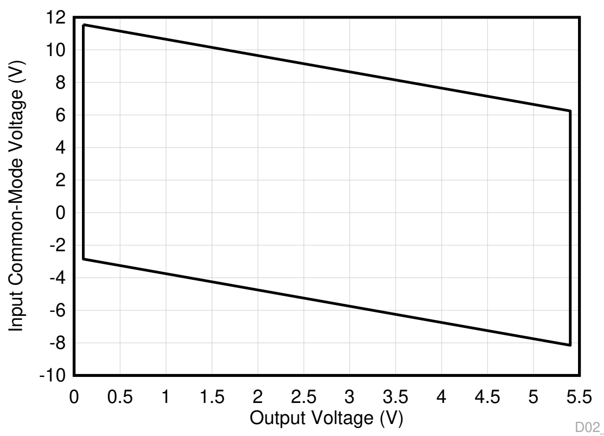
V+ = 5.5V V– = 0V G = 1 V_{REF} = 0V

Figure 6-71. Input Common-Mode Voltage vs Output Voltage (Rail-to-Rail CMRR Region)



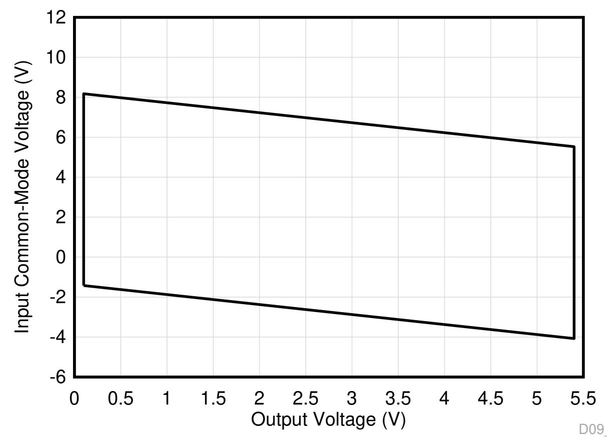
V+ = 5.5V V– = 0V G = 0.25 V_{REF} = 2.75V

Figure 6-72. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V+ = 5.5V V– = 0V G = 0.5 V_{REF} = 2.75V

Figure 6-73. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

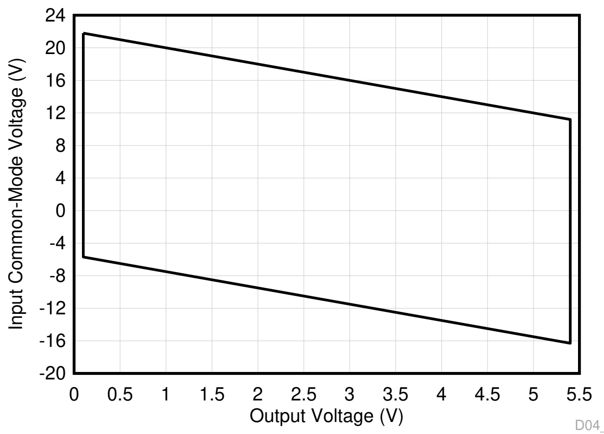


V+ = 5.5V V– = 0V G = 1 V_{REF} = 2.75V

Figure 6-74. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)

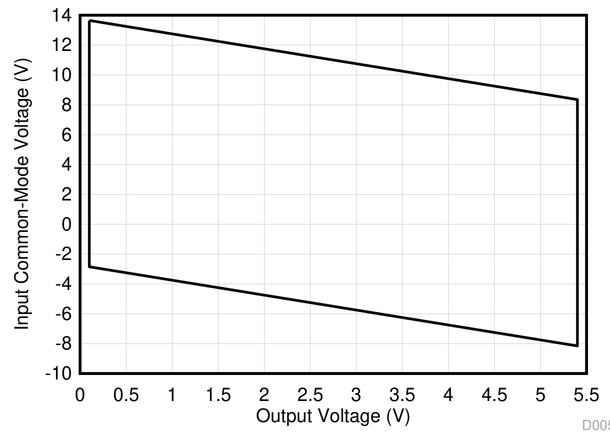
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = (V+) – (V–) = 5.5V, V_{IN} = (V_{IN+} – $V_{IN–}$) = 0V, R_L = 10kΩ, C_L = 10pF, V_{REF} = V_S / 2, V_{CM} = (V_{IN+} + $V_{IN–}$) / 2 = V_S / 2, V_{OUT} = V_S / 2 and G = 1 (unless otherwise noted)



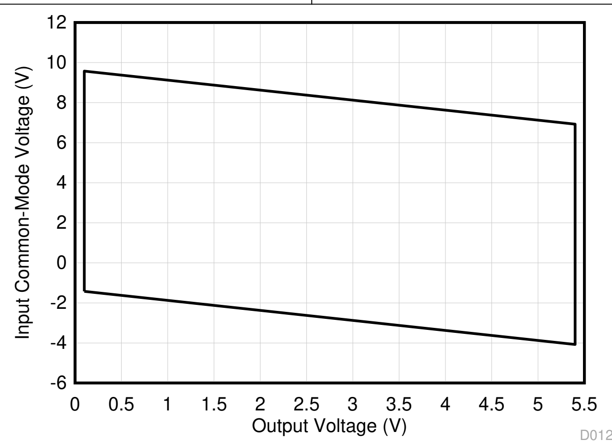
V+ = 5.5V V– = 0V G = 0.25 V_{REF} = 2.75V

Figure 6-75. Input Common-Mode Voltage vs Output Voltage (Rail-to-Rail CMRR Region)



V+ = 5.5V V– = 0V G = 0.5 V_{REF} = 2.75V

Figure 6-76. Input Common-Mode Voltage vs Output Voltage (Rail-to-Rail CMRR Region)



V+ = 5.5V V– = 0V G = 1 V_{REF} = 2.75V

Figure 6-77. Input Common-Mode Voltage vs Output Voltage (Rail-to-Rail CMRR Region)

7 Detailed Description

7.1 Overview

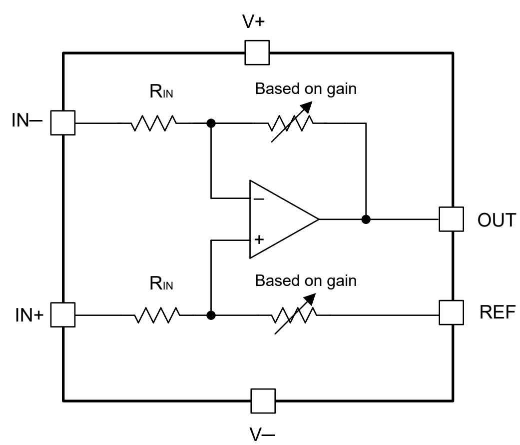
The INA500 is a cost-effective, integrated difference amplifier designed to provide better performance, and smaller solution size for applications employing discrete implementation of difference amplifiers using commodity amplifiers and discrete resistors. The device incorporates one low power operational amplifier and four precision matched integrated resistors. INA500 can be used in 8-bit system without any calibration. Further calibration of offset and gain error at a system level can improve system resolution and accuracy, enabling use in 10-bit and 12-bit systems.

The INA500 is offered in three gain options across three variants. The INA500A version offers gain option of 1, while the INA500B and INA500C versions offer gain options of 0.50 and 0.25 respectively. Optimized for voltage sensing applications, the INA500 offers 75dB of minimum common-mode rejection ratio (CMRR) and ±0.05% of maximum gain error. A high input impedance of >1MΩ along with just 13.5μA of quiescent current is one of the key features of the INA500, which is very useful in single cell battery monitoring applications. All of the errors including offset, offset drift, CMRR and so forth are referred to the output so as to enable easy calculation of signal-to-noise ratio (SNR) and effective number of bits (ENOB) close to the analog-to-digital converter (ADC).

The INA500 gain options are designed for level translation applications that interface with a wide variety of differential (±12V, ±10V, ±5V, and so forth) and single-ended (0V to 12V, 0V to 10V, 0V to 5V, and so forth) high voltage signals into low voltage (0V to 5V, 0V to 3V, 0V to 2.5V, and so forth) ADCs. This would be useful in a variety of end equipments such as Battery testers, Solar string inverters, Power tools, Analog input modules, Battery energy storage systems and so forth where multiple high voltage signals and supply domains are required to be monitored. When routing signals differentially for common-mode noise immunity, the INA500 in G = 1 would be useful in converting the differential signal back to single-ended signal for easy interface to single-ended ADCs while rejecting the common-mode noise. The device also has enough bandwidth of 125kHz to directly drive low-speed (≤10ksps) ADCs.

The INA500 is an excellent choice for use in space-constrained applications such as wearable fitness and activity monitors, cell phones, and so forth as it is offered in ultra-small, 0.8mm^2 X2SON package. For easy use in industrial applications, it is also available in industry standard packages including SOT-23 and SC70.

7.2 Functional Block Diagram



Note: Input resistors (R_{IN}) values are 1.08MΩ for INA500A, 1.44MΩ for INA500B, and 1.68MΩ for INA500C

Figure 7-1. INA500A Simplified Internal Schematic

7.3 Feature Description

7.3.1 Gain Options and Resistors

The gain value of the INA500 is given by the ratio of feedback resistor and input resistor. The gain options are offered across different device variants as provided in Table 7-1. While the typical value of input and feedback resistors are shown in the following table, it is important to note that these values can vary together by about ±15% while maintaining tighter gain error (tolerance) numbers as specified in the *Electrical Characteristics* table.

Table 7-1. Gain Selection Table

DEVICE	INPUT RESISTOR	FEEDBACK RESISTOR	GAIN
INA500A	1.08MΩ	1.08MΩ	1
INA500B	1.44MΩ	0.72MΩ	0.50
INA500C	1.68MΩ	0.42MΩ	0.25

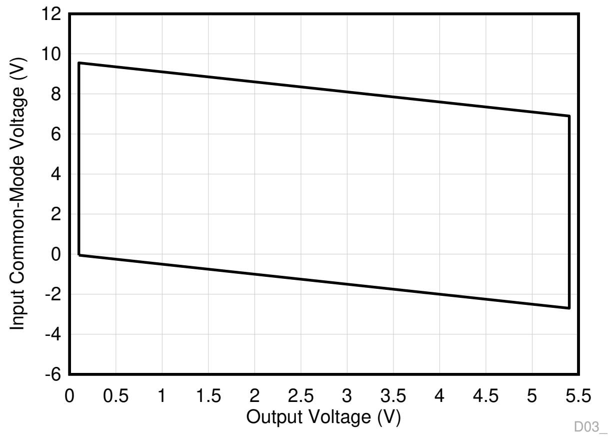
7.3.1.1 Gain Error and Drift

Gain error in the INA500 is limited by the mismatch of the integrated precision resistors and is specified based on characterization results. Maximum gain error of ±0.05% can be expected for all gains of 1, 0.50, and 0.25. Gain drift in the INA500 is limited by the slight mismatch of the temperature coefficient of the integrated resistors. Since these integrated resistors are precision matched with low temperature coefficient resistors to begin with, the overall gain drift is much better in comparison to discrete implementation of the difference amplifiers built using external resistors. Maximum gain error of ±0.02% can be expected for inputs from the reference pin that sets output common-mode voltage.

7.3.2 Input Common-Mode Voltage Range

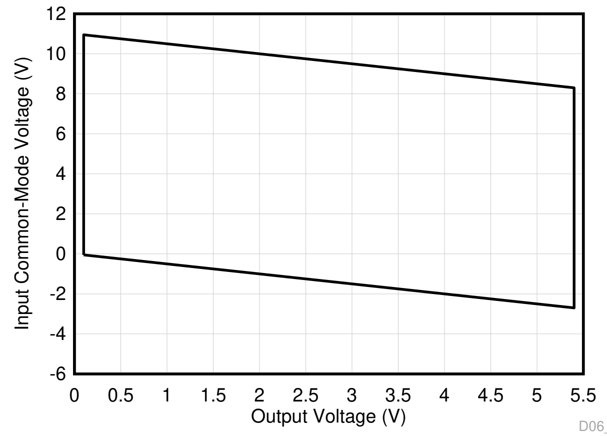
The INA500 difference-amplifier rejects the input common mode. The rejection capability is based on the matching of the internal resistors. The input voltage range of the INA500 is primarily dictated by the signal swing at the op-amp inputs. The INA500 input common-mode voltage range can extend well beyond the supply rails and is a major function of the gain configuration. To maximize performance, it is critical to keep the op-amp inside the INA500 within the linear range for a given combination of gain, reference voltage, and input common-mode voltage for a particular input differential voltage and output swing.

Input common-mode voltage (V_{CM}) vs output voltage graphs (V_{OUT}) in this section outlines the linear performance region of the INA500 for a particular combination of gain and reference voltage values. A good common-mode rejection can be expected when operating with in the limits of the V_{CM} versus V_{OUT} graph. The common-mode range for the INA500 in equation form is outlined in the *Electrical Characteristics* for each gain. The most common operating conditions are outlined graphically in the *Typical Characteristics* section. Figure 7-2 shows the region of operation where a minimum of 75dB CMRR can be achieved. This is referred as the high CMRR region. Figure 7-3 has much wider region of operation with a lower CMRR of 62dB minimum. This is because the input signal crosses over the transition region of the input pairs to achieve rail-to-rail operation.



V+ = 5.5V V– = 0V G = 1 V_{REF} = 0V

Figure 7-2. Input Common-Mode Voltage vs Output Voltage (High CMRR Region)



V+ = 5.5V V– = 0V G = 1 V_{REF} = 0V

Figure 7-3. Input Common-Mode Voltage vs Output Voltage

7.3.3 EMI Rejection

The INA500 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the INA500 benefits from these design improvements. Texas Instruments has the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 7-4 shows the results of this testing on the INA500 for differential EMI interference and Figure 7-5 shows the results of this testing on the INA500 for common-mode EMI interference. Table 7-2 provides the EMIRR IN+ values for the INA500 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

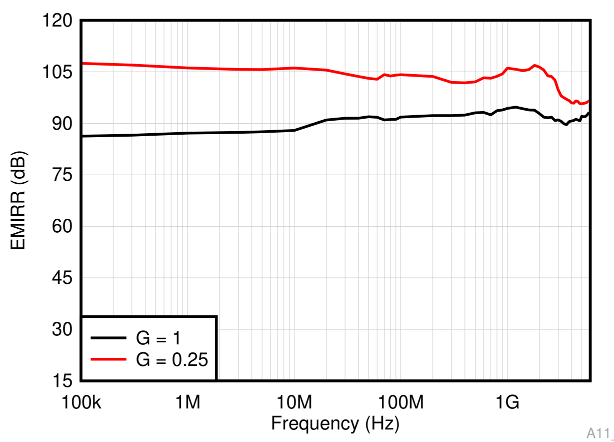


Figure 7-4. Electromagnetic Interference Rejection Ratio Referred to Output vs Frequency (Differential Input)

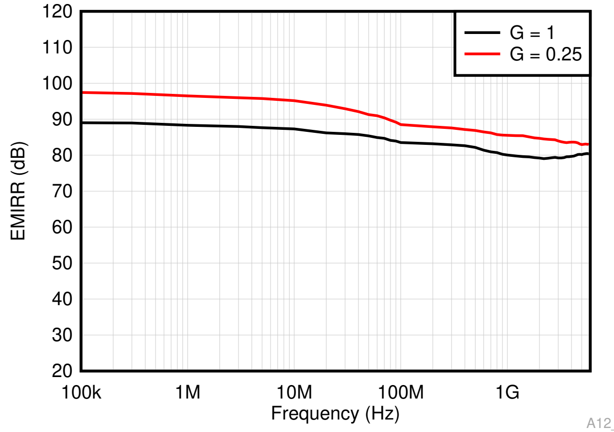


Figure 7-5. Electromagnetic Interference Rejection Ratio Referred to Output vs Frequency (Common-Mode Input)

Table 7-2. INA500 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR DIFFERNTIAL	EMIRR COMMON-MODE
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	91dB	83dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	98dB	82dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	101dB	80dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	95dB	78dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88dB	79dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	94dB	80dB

7.3.4 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, like an amplifier's offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guard band their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

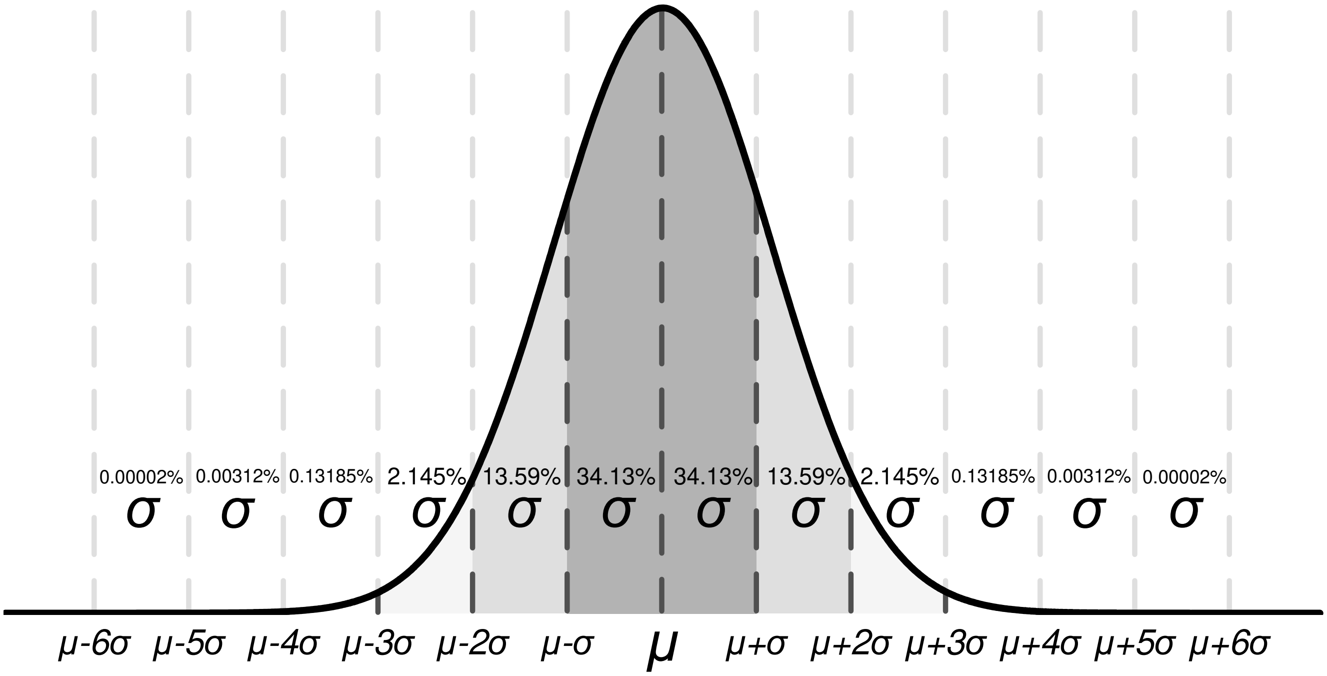


Figure 7-6. Ideal Gaussian Distribution

Figure 7-6 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

This chart can be used to calculate approximate probability of a specification in a unit; for example, the INA500A typical offset voltage is 700μV, so 68.2% of all INA500A devices are expected to have an offset from –700μV to +700μV. At 4 *σ* (±2800μV), 99.9937% of the distribution has an offset voltage less than ±2800μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are verified by TI, and units outside these limits are removed from production material. For example, the INA500A family has a maximum offset voltage of ±3.5mV at 25°C, and even though this corresponds to 5σ (equals approximately 1 in 3.5 million units), which is extremely unlikely, TI verifies that any unit with larger offset than ±3.5mV are removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for the application, and design worst-case conditions using this value. A 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guard band to design a system around. Histograms for some of the important specifications like offset, offset drift, CMRR, gain error are shown in the *Typical Characteristics* section.

In the case of gain error, the INA500 family does not specify a maximum value based on final test but based on characterization as mentioned in the *Electrical Characteristics* table. The corresponding distribution mentioned in Figure 6-10 has a mean of 0.01% and sigma of 0.003%. Hence, the mean plus 6σ value for gain error can be calculated to be approximately 0.03%. When designing for system conditions with 6σ guardband, this method and value can be used to estimate the worst possible gain error.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column that is specified based on final test, TI cannot verify the performance of a device. Hence, the maximum gain error spec in the *Electrical Characteristics* table is relaxed beyond 6σ guardband to be ±0.05%.

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 7-7 shows the ESD circuits contained in the INA500 devices. On the input pins, the ESD protection circuitry involves local high impedance diode structures and do not route the ESD current to power supply ESD cell. On the output pin, there are reverse biased diodes to both the power supply rails. These diode structures route the ESD current back to the internal power supply lines, where there is an absorption power supply ESD cell internal to the difference amplifier. On the reference pin, the ESD protection is local and does not route current to the power supply ESD cell.

All of the ESD protection circuitry is intended to remain inactive during normal circuit operation.

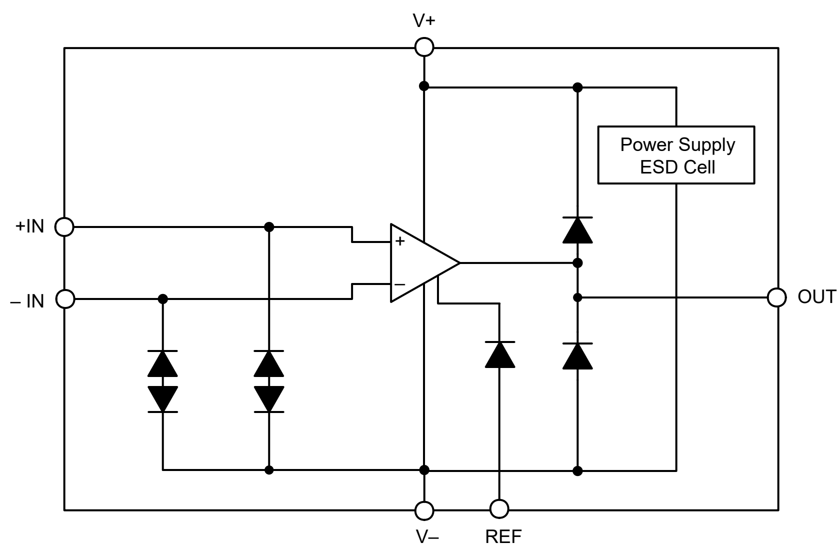


Figure 7-7. Equivalent Internal ESD Circuitry

7.4 Device Functional Modes

The INA500 has only one functional mode. The device powers on, starts drawing quiescent current and is functional as long as the power supply voltages are in the recommended operating voltage range of 1.7V (±0.85V) to 5.5V (±2.75V). Operational temperature range of INA500 is from –40°C to 125°C.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Reference Pin

The output voltage of the INA500 is developed with respect to the voltage on the reference pin (REF). Often in dual-supply operation, REF pin connects to the system ground. However, in single-supply operation, offsetting the output signal to a precise mid-supply level is useful and required (for example, 2.5V in a 5.0V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA can drive a single-supply ADC. This is accomplished using an external reference buffer configured in unity gain, voltage follower configuration as shown in Figure 8-1.

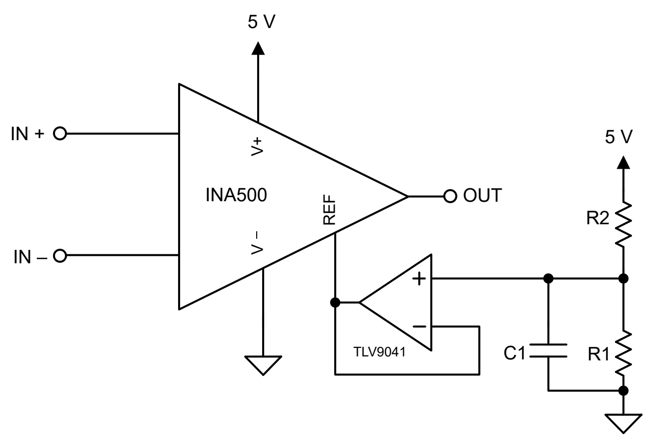


Figure 8-1. INA500 with External Reference Buffer

8.2 Typical Applications

8.2.1 Battery Monitoring using Difference Amplifier

The INA500 is an integrated difference amplifier that processes large differential voltages while simultaneously rejecting larger common-mode voltages. The device offers a low power consumption of 13.5µA (typical) and has a smaller form factor.

With the specifications above, the device is a good fit for portable applications that are powered with single cell or coin-cell batteries. Often, these systems do not need sophisticated battery management technology but a solution that is rather simple and small-size. In a few other systems, battery monitoring ICs are preferred to perform sophisticated functions including cell balancing, protection, voltage and current sensing and so forth but these systems still need a secondary level of protection or redundancy with a simpler and reliable solution for system integrity. It is in these scenarios, the amplifier based battery monitoring application shown below could be quite useful.

Figure 8-2 shows an example circuit that monitors a 12V battery voltage and interfaces it to an ADC that is powered using a 3V power supply. The main advantage for using difference amplifiers in this application is the elimination of ground bounce, which is a common-mode signal, when measuring the battery voltage. These ground bounce signals, when not rejected, are capable of causing errors in the range of few milli-volts to tens or hundreds of milli-volts.

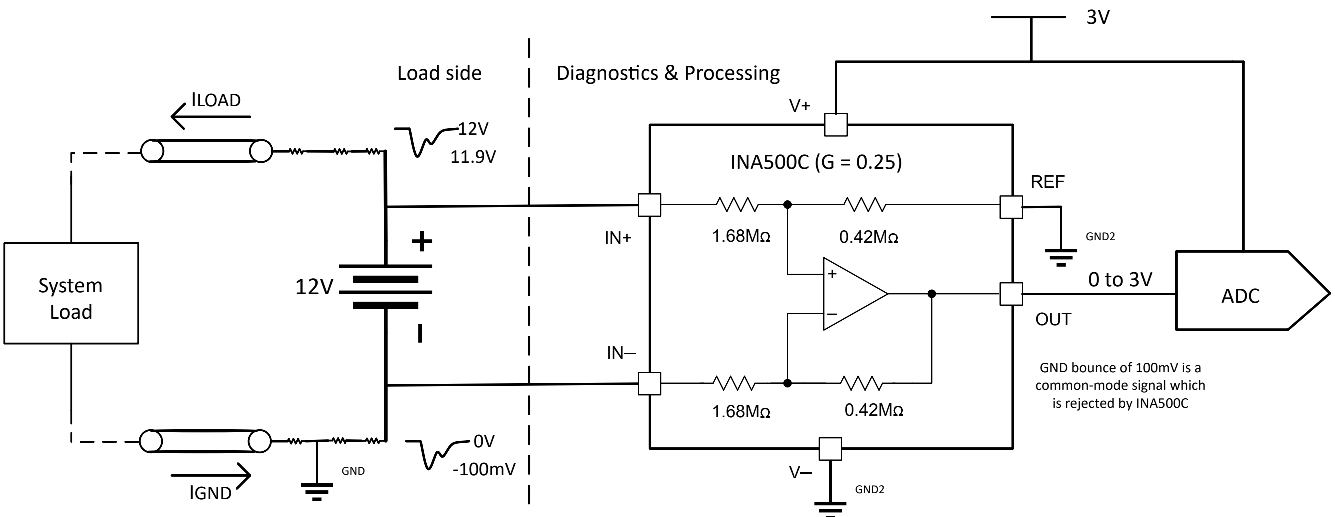


Figure 8-2. Battery Monitoring Circuitry

8.2.1.1 Design Requirements

For this application, the design requirements are as provided in Table 8-1.

Table 8-1. Design Requirements

DESCRIPTION	VALUE
Battery voltage	V_{BAT} = 12V
Supply voltage	V_S = 3V
Full-scale range of ADC	$V_{ADC(fs)}$ = V_{OUT} = 3V
Quiescent current	30µA
Accuracy	8 bits
Common-mode rejection ratio	60dB or a factor of 1000

8.2.1.2 Detailed Design Procedure

This section provides basic calculations for the INA500C difference amplifier with respect to the given design requirements.

Firstly, the 12V battery voltage needs to be attenuated and interfaced to ADC reference voltage of 3V. This requires a G = ¼ or 0.25V/V and hence INA500C is chosen for the application.

$$\text{Gain} = \frac{V_{BAT}}{V_{ADC}} = \frac{12}{3} = \frac{1}{4} = 0.25 \quad (1)$$

The maximum common-mode range of INA500 in a gain of 0.25 is given by,

$$V_{CM\_MAX} = 5*(V+) - 4*V_{REF} = 5*3 - 4*0 = 15V \quad (2)$$

This is well within the requirements for sensing 12V battery voltage and the common-mode rejection ratio (CMRR) referred to output is a minimum of 62dB as per *Electrical Characteristics* table. This corresponds to a attenuation factor of $\frac{1}{1250}$. This helps attenuate the 100mV common-mode error shown in the Figure 8-2 to just 80µV.

$$CM_{Err\_RTO} = \frac{100mV}{1250} = 80\mu V, \text{ when referred to INA500C's output.} \quad (3)$$

Next, INA500C has input impedance of 1.68MΩ as per the *Electrical Characteristics* table. Assuming a full battery voltage of 12V, the input current through the resistor is calculated as,

$$I_{R_{IN}} = \frac{V_{BAT}}{R_{IN}} = \frac{12}{1.68M} = 7.2\mu A \quad (4)$$

This input current through the resistor adds to the amplifier quiescent current of 13.5µA resulting in a total current consumption of 20.7µA, which meets the design requirement of 30µA.

$$I_{total} = I_{R_{IN}} + I_Q \quad (5)$$

The next step is to calculate the other error sources in the application. Maximum gain error and offset error as per *Electrical Characteristics* table are 0.05% and 2.5mV for the Gain = 0.25V/V.

$$\text{Total Error} = \sqrt{(0.0005*12)^2 + 0.0025^2} = 6.5mV \quad (6)$$

For an 8 bit, 3V ADC, V_{LSB} is calculated as,

$$V_{LSB} = \frac{3}{2^8} = 11.7mV \quad (7)$$

The total error of 6.5mV that was calculated is approximately 0.5LSB of ADC full scale voltage of 3V and hence meets the 8-bit accuracy requirement.

Note, that the errors across temperature are not calculated here but can be easily included in the error analysis based on the drift specifications provided in the *Electrical Characteristics* table as per the application's temperature requirements. These drift errors and noise often do not heavily affect the performance at 8 bit accuracy levels. Finally, calibration of offset and gain error can improve the accuracy beyond 10 to 12 bits as these factors can be the major sources of error in the application.

8.2.1.3 Application Curves

The following typical characteristic curve is for the circuit in Figure 8-2.

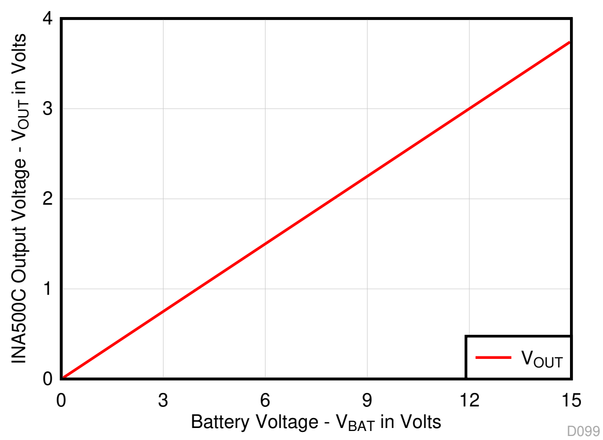


Figure 8-3. Battery Input Voltage vs INA500C Output Voltage

8.3 Power Supply Recommendations

The nominal performance of the INA500 is specified with a supply voltage of ±2.75V and midsupply reference voltage. The device also operates using power supplies from ±0.85V (1.7V) to ±2.75V (5.5V) and non-midsupply reference voltages with good performance. Many specifications apply from –40°C to 125°C. *Electrical Characteristics* presents parameters that can exhibit significant variance due to operating voltage or temperature.

TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Please ensure the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals. For more information, see *Layout Guidelines*.

Parameters can vary with operating voltage and reference voltage. *Typical Characteristics* section can be used to estimate the performance outside of the *Electrical Characteristics* section.

8.4 Layout

8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use the following PCB layout practices:

- Ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Route the input traces as far away from the supply or output traces as possible to reduce parasitic coupling. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

8.4.2 Layout Example

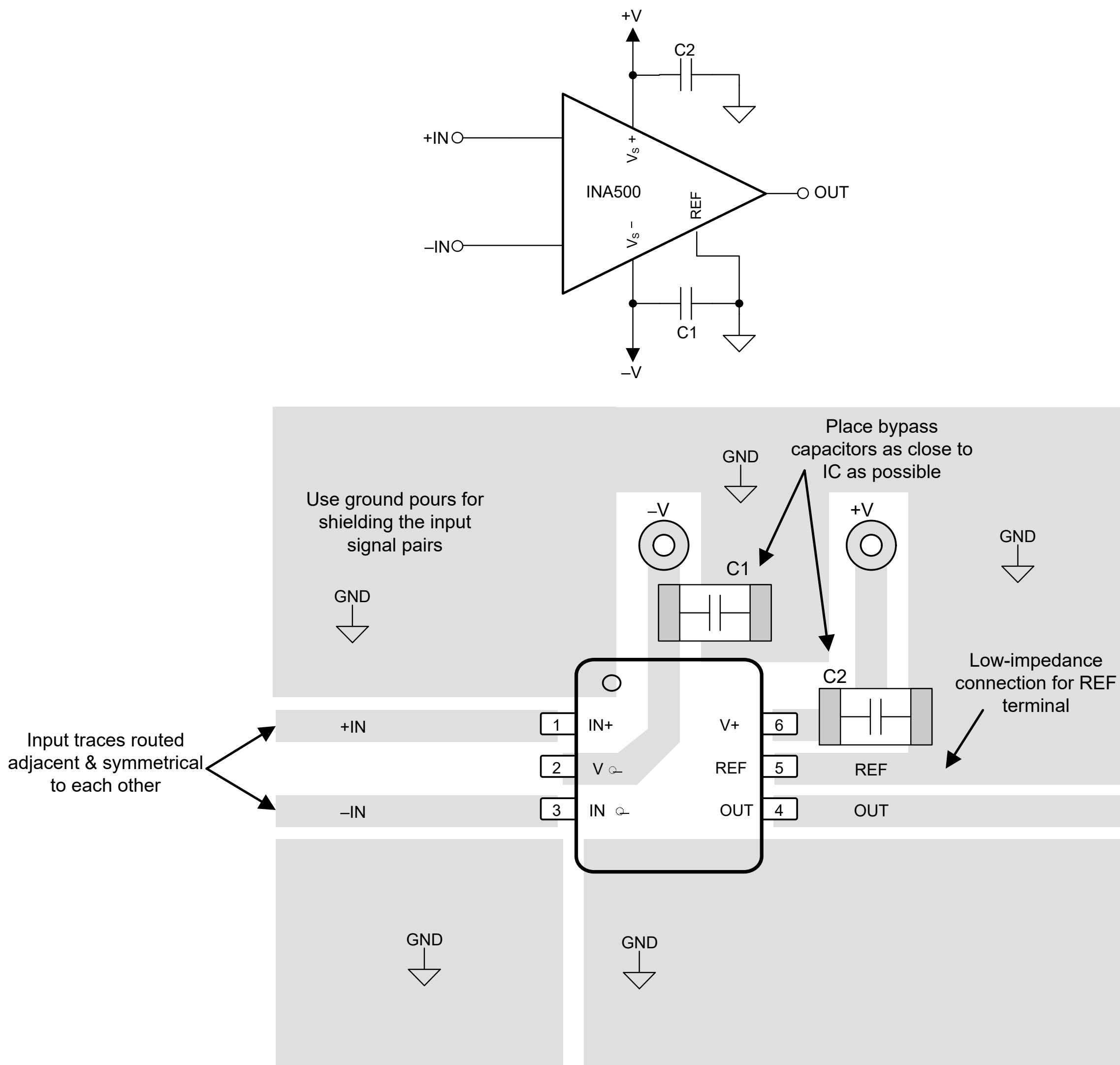


Figure 8-4. Example Schematic and Associated PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

- *SPICE-based analog simulation program — TINA-TI software folder*
- *Analog Engineers Calculator*

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2024) to Revision B (March 2024) — **Page**

- Changed the status of DBV, DCK packages of INA500B and INA500C from: *preview* to: *active* 2
- Added *Electrical Characteristics* table for gain options of 0.5 and 0.25.. 4

Changes from Revision * (December 2023) to Revision A (January 2024) **Page**

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA500AIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3B4H	Samples
INA500AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1RJ	Samples
INA500BIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3B6H	Samples
INA500BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1RK	Samples
INA500CIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3B5H	Samples
INA500CIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1RL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

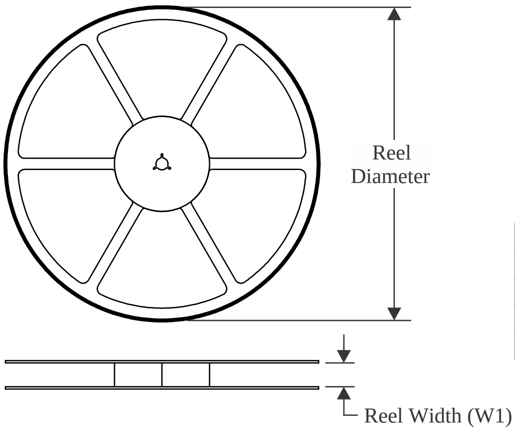
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

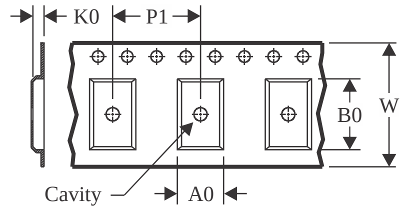
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

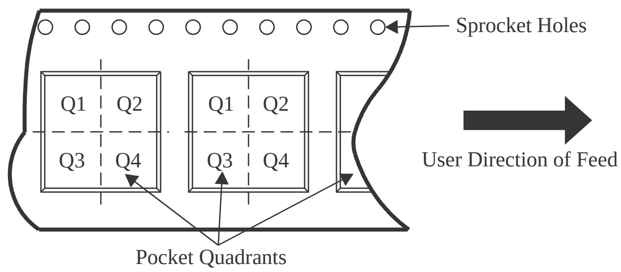


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

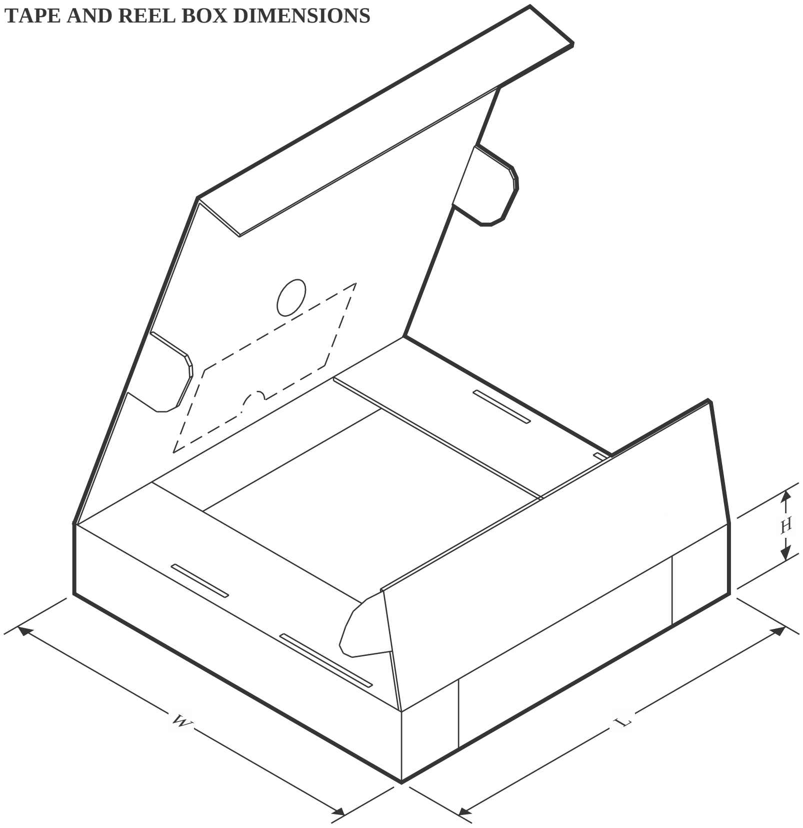
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

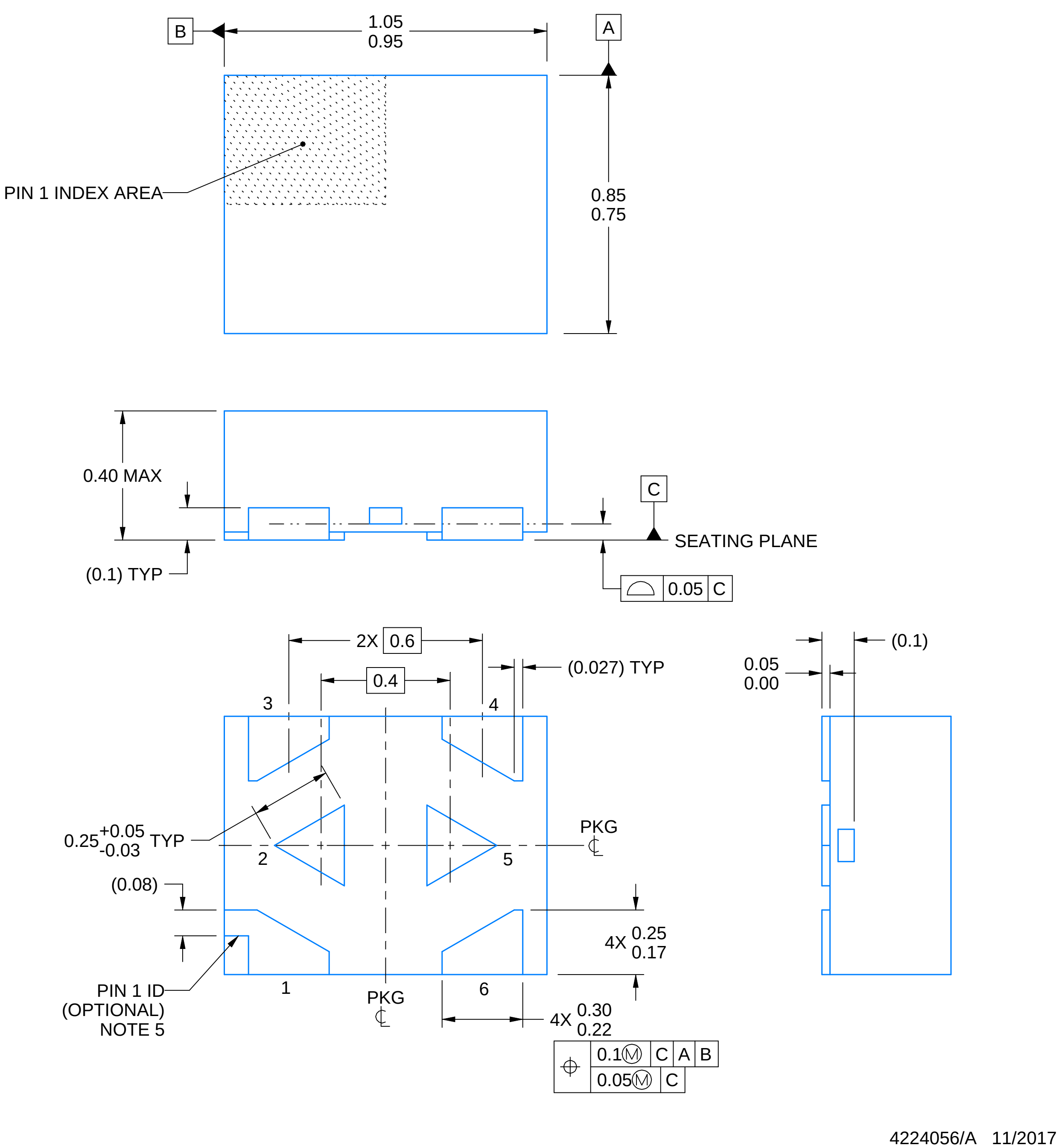
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA500AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA500AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA500BIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA500BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA500CIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA500CIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



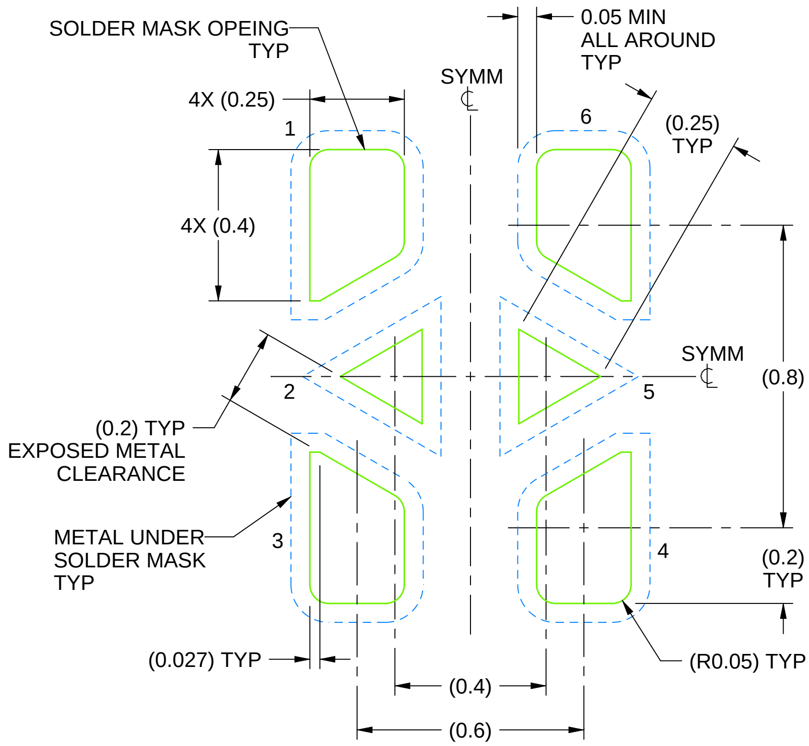
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA500AIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA500AIDCKR	SC70	DCK	6	3000	190.0	190.0	30.0
INA500BIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA500BIDCKR	SC70	DCK	6	3000	190.0	190.0	30.0
INA500CIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
INA500CIDCKR	SC70	DCK	6	3000	190.0	190.0	30.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

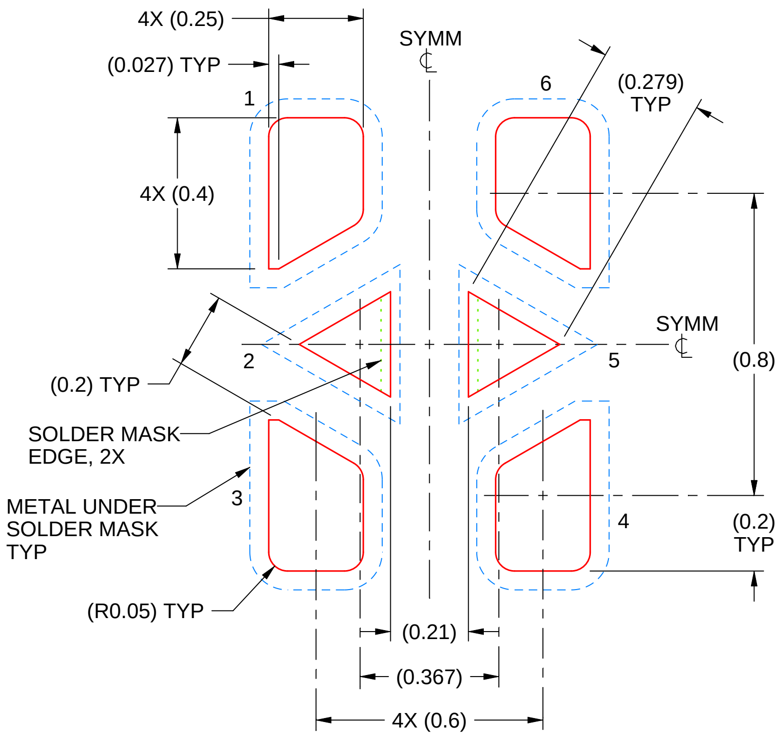


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4224056/A 11/2017

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4224056/A 11/2017

NOTES: (continued)

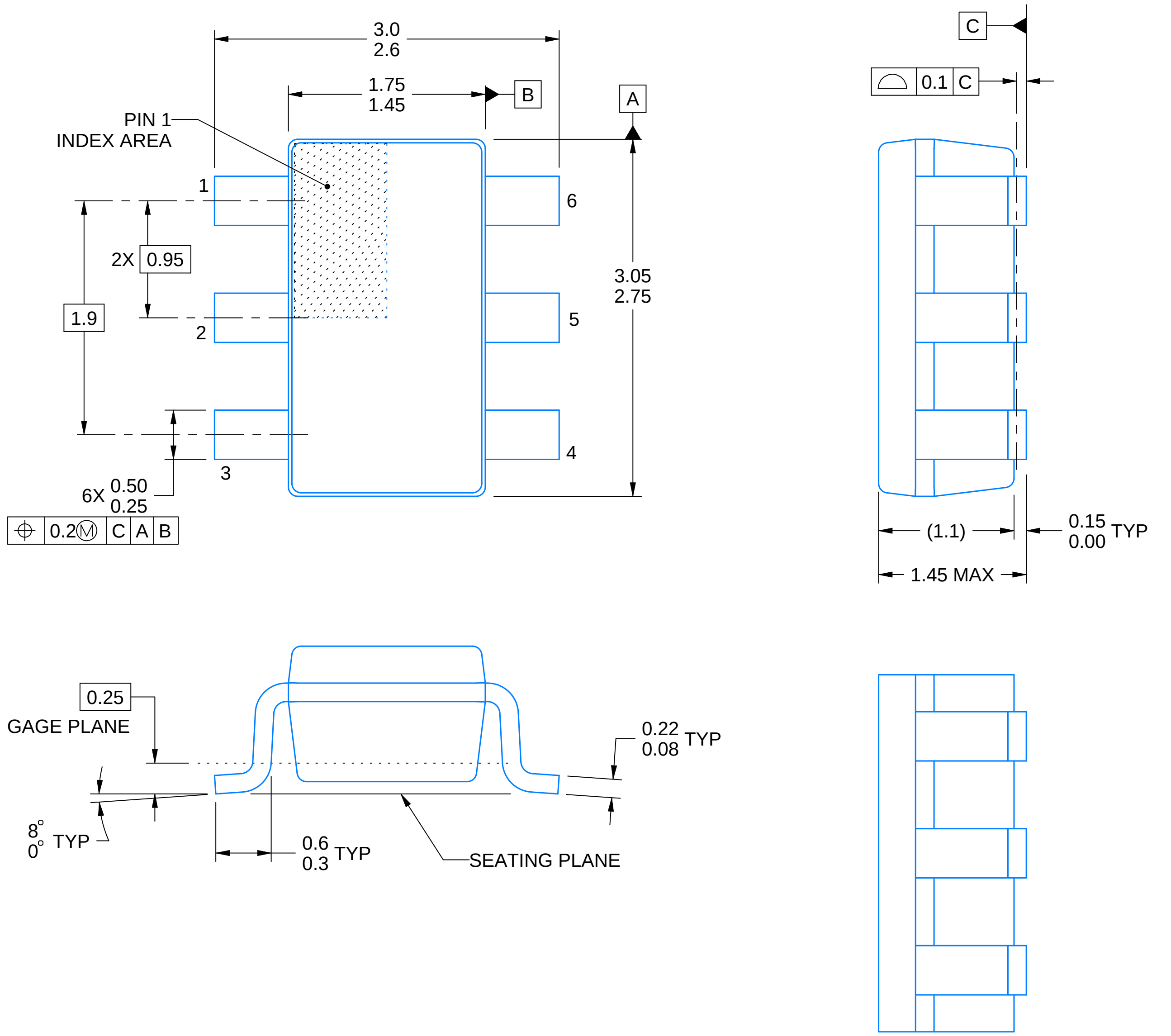
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

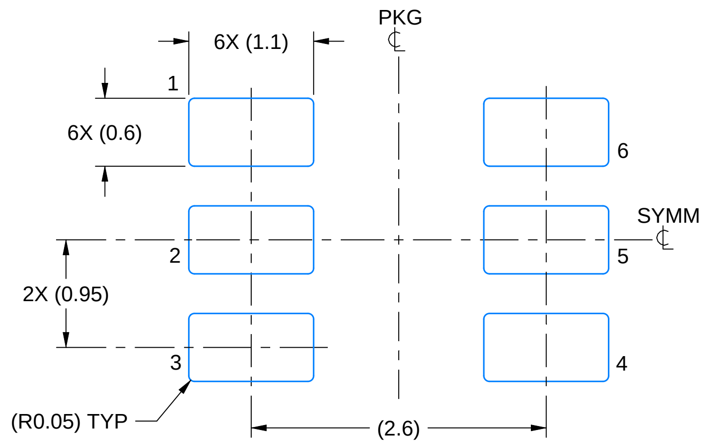


ALTERNATIVE PACKAGE SINGULATION VIEW

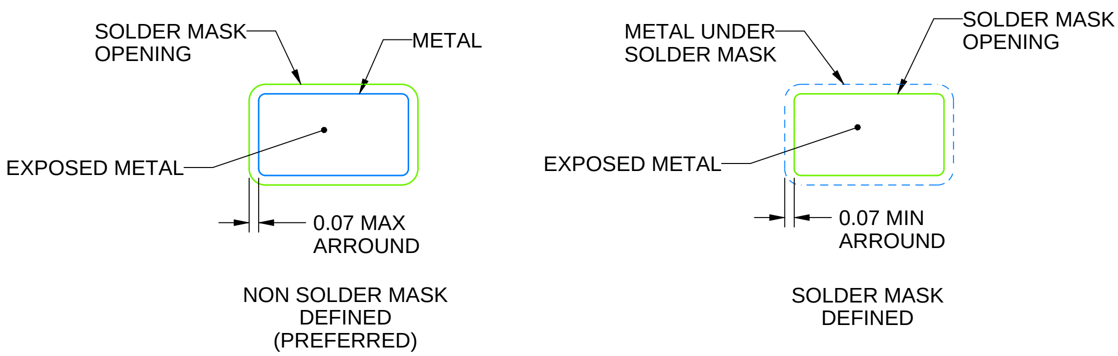
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

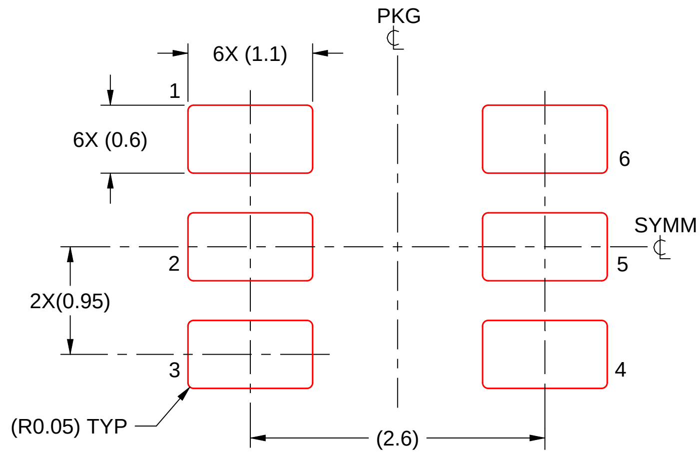


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



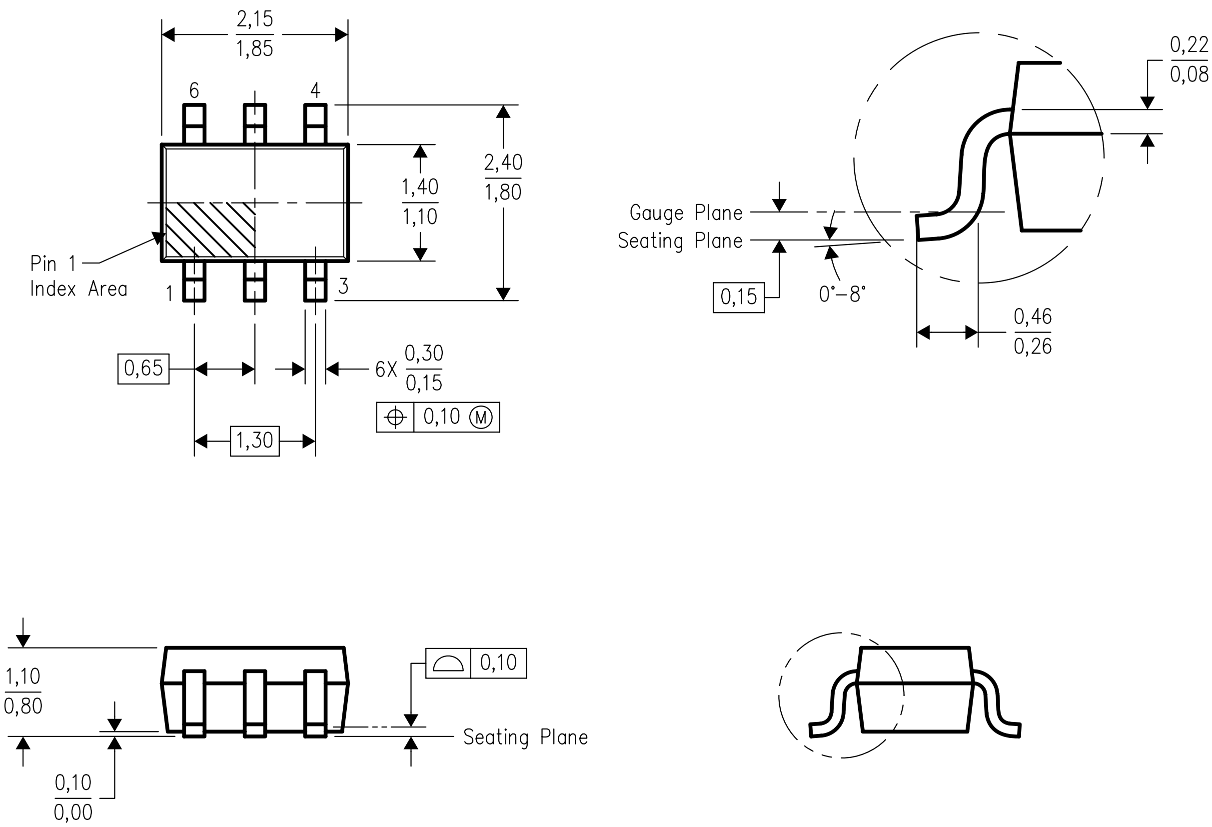
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

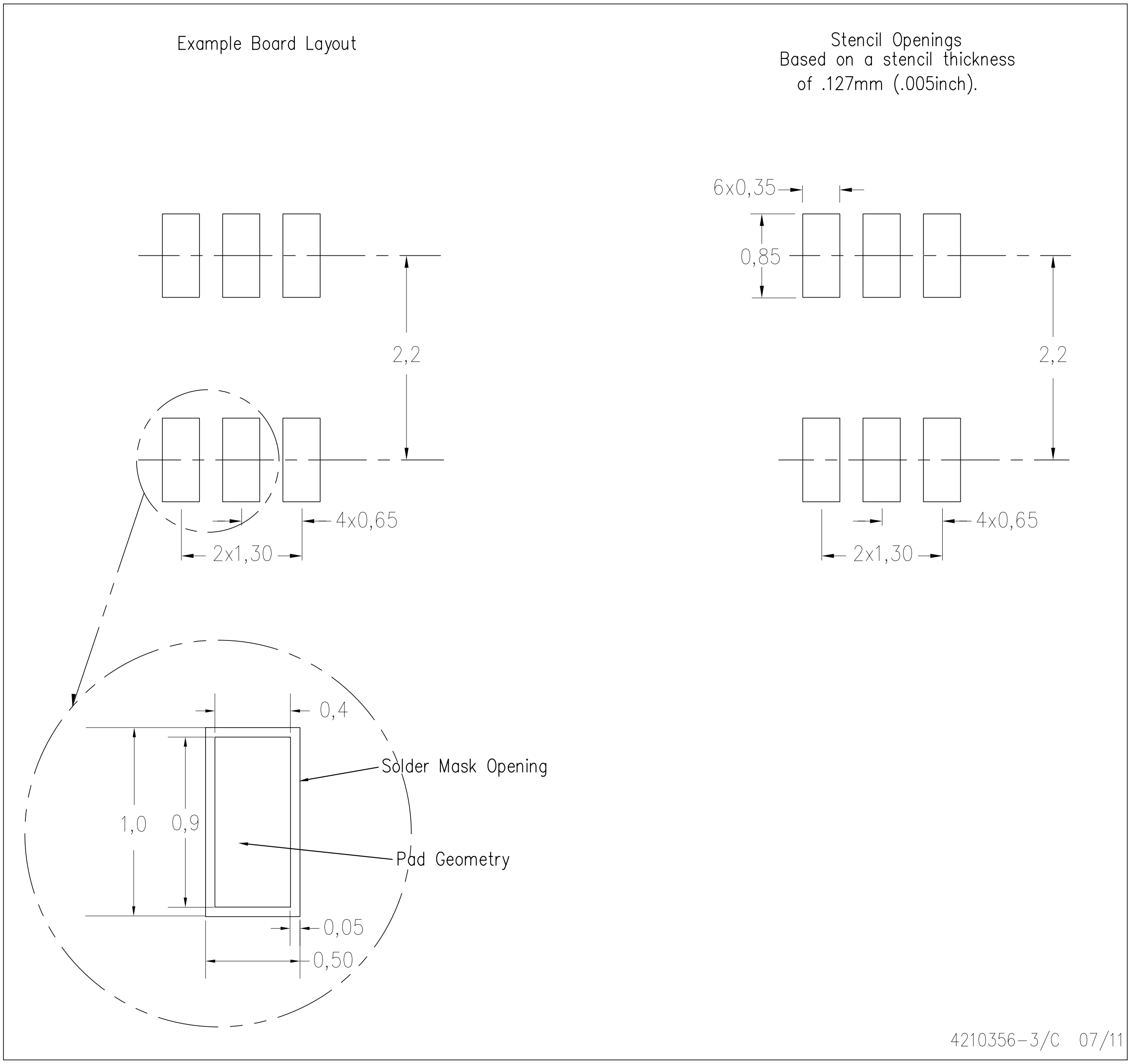
DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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