

## QUAD DIFFERENTIAL COMPARATOR

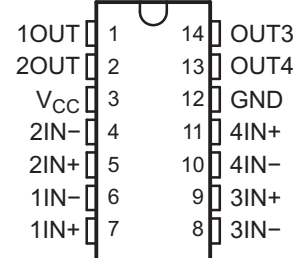
Check for Samples: [LM239A-EP](#)

### FEATURES

- **Wide Supply Ranges**
  - **Single Supply: 2 V to 36 V**  
(Tested to 30 V for Non-V Devices and 32 V for V-Suffix Devices)
  - **Dual Supplies:  $\pm 1$  V to  $\pm 18$  V**  
(Tested to  $\pm 15$  V for Non-V Devices and  $\pm 16$  V for V-Suffix Devices)
- **Low Supply-Current Drain Independent of Supply Voltage: 0.8 mA (Typ)**
- **Low Input Bias Current: 25 nA (Typ)**
- **Low Input Offset Current: 5 nA (Typ)**
- **Low Input Offset Voltage: 2 mV (Typ)**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage:  $\pm 36$  V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military ( $-55^{\circ}\text{C}/125^{\circ}\text{C}$ ) Temperature Range<sup>(1)</sup>**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D OR PW PACKAGE  
(TOP VIEW)


(1) Custom temperature ranges available

### DESCRIPTION/ORDERING INFORMATION

These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible, as long as the difference between the two supplies is 2 V to 36 V, and  $V_{CC}$  is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

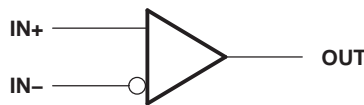
**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOP - D	Tape and reel	LM239AQDREP	LM239AEP
-55°C to 125°C	SOP - D	Tape and reel	LM239AMDREP	LM239AME
	TSSOP - PW	Tape and reel	LM239AMPWREP	LM239AE

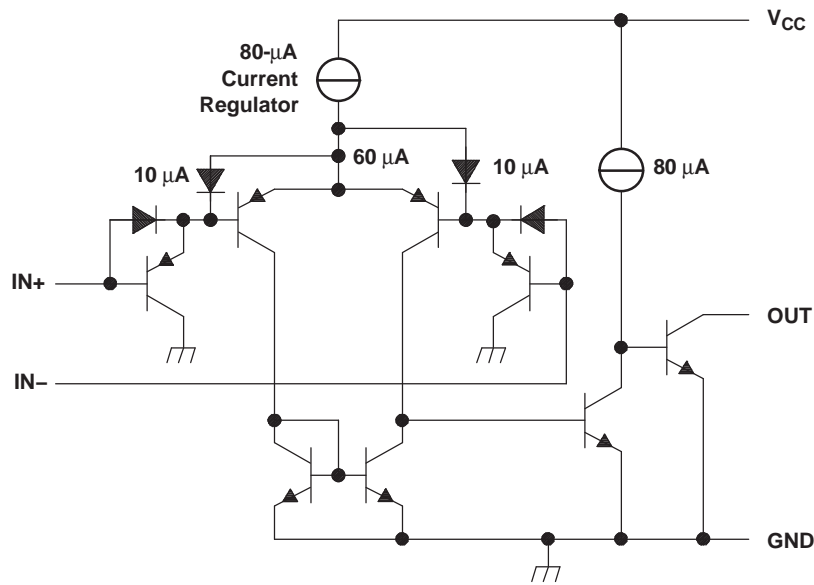
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**SYMBOL (EACH COMPARATOR)**



**SCHEMATIC (EACH COMPARATOR)**



All current values shown are nominal.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		36	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±36	V
V <sub>I</sub>	Input voltage range (either input)	-0.3	36	V
V <sub>O</sub>	Output voltage		36	V
I <sub>O</sub>	Output current		20	mA
	Duration of output short circuit to ground <sup>(4)</sup>		Unlimited	
θ <sub>JA</sub>	Package thermal impedance, junction to free air <sup>(5)</sup> (6)		86	°C/W
T <sub>J</sub>	Operating virtual-junction temperature		136	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C
T <sub>stg</sub>	Storage temperature range <sup>(7)</sup>	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V<sub>CC</sub> can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of T<sub>J</sub> (max), θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A) / \theta_{JA}$ . Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.
- (7) Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

## ELECTRICAL CHARACTERISTICS

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		$T_A$ <sup>(2)</sup>	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{CC} = 5\text{ V to } 30\text{ V}$ , $V_{IC} = V_{ICR\text{ min}}$ , $V_O = 1.4\text{ V}$		25°C		1	2.5	mV
				Full range			5.5	
$I_{IO}$	Input offset current	$V_O = 1.4\text{ V}$		25°C		5	50	nA
				Full range			150	
$I_{IB}$	Input bias current	$V_O = 1.4\text{ V}$		25°C		-25	-250	nA
				Full range			-400	
$V_{ICR}$	Common-mode input-voltage range <sup>(3)</sup>			25°C		0 to $V_{CC} - 1.5$		V
				Full range			0 to $V_{CC} - 2$	
$A_{VD}$	Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$ , $V_O = 1.4\text{ V to } 11.4\text{ V}$ , $R_L \geq 15\text{ k}\Omega$ to $V_{CC}$		25°C		50	200	V/mV
$I_{OH}$	High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C		0.1	50	nA
			$V_{OH} = 30\text{ V}$	Full range			1	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{ID} = -1\text{ V}$ , $I_{OL} = 4\text{ mA}$		25°C		150	400	mV
				Full range			700	
$I_{OL}$	Low-level output current	$V_{ID} = -1\text{ V}$ , $V_{OL} = 1.5\text{ V}$		25°C		6	16	mA
$I_{CC}$	Supply current (four comparators)	$V_O = 2.5\text{ V}$ , No load		25°C		0.8	2	mA

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.  
(2) Full range (MIN to MAX) for LM139 and LM139A is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . All characteristics are measured with zero common-mode input voltage, unless otherwise specified.  
(3) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $V_{CC+} - 1.5\text{ V}$ ; however, one input can exceed  $V_{CC}$ , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

## SWITCHING CHARACTERISTICS

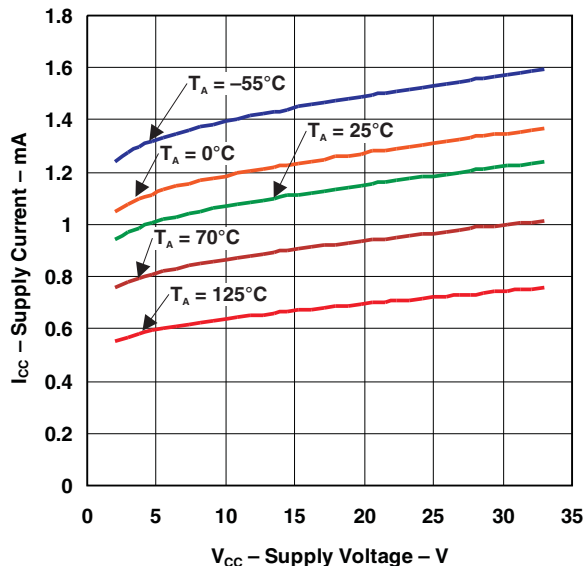
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	$R_L$ connected to 5 V through 5.1 k $\Omega$ , $C_L = 15\text{ pF}$ <sup>(1)</sup> <sup>(2)</sup>	100-mV input step with 5-mV overdrive	1.3	$\mu\text{s}$
		TTL-level input step	0.3	

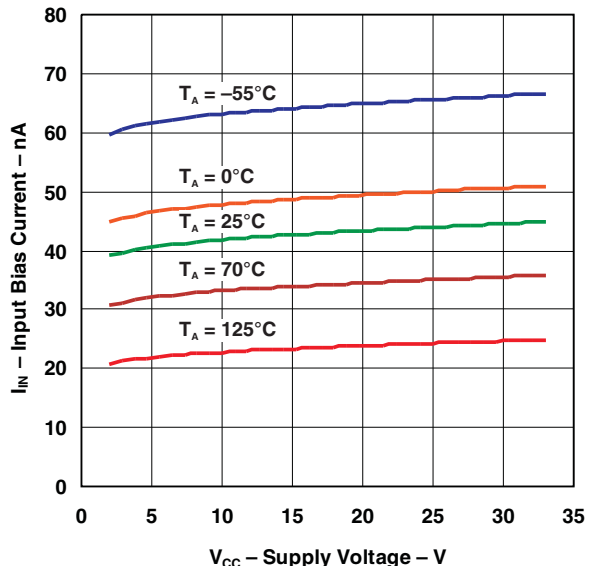
- (1)  $C_L$  includes probe and jig capacitance.  
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS

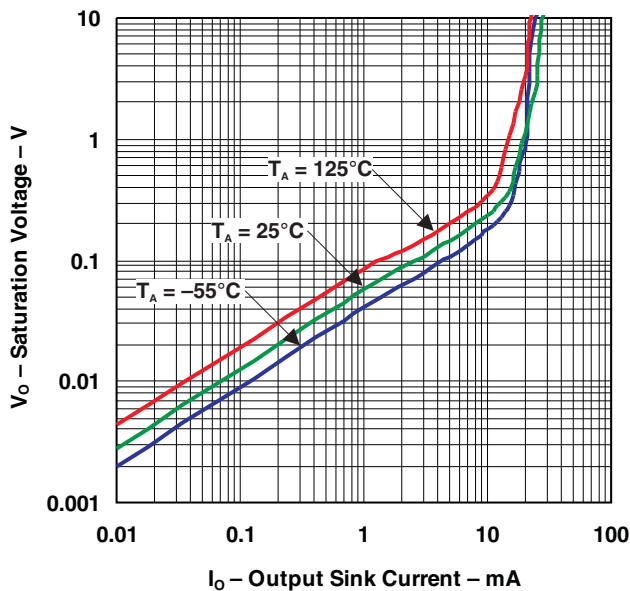
SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE



INPUT BIAS CURRENT  
vs  
SUPPLY VOLTAGE

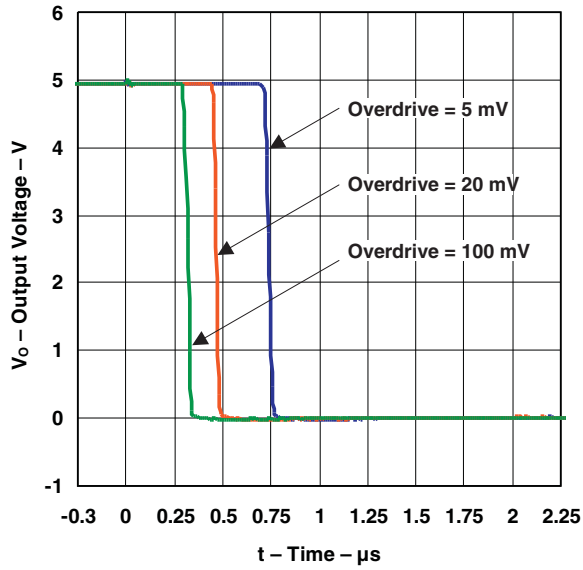


OUTPUT SATURATION VOLTAGE

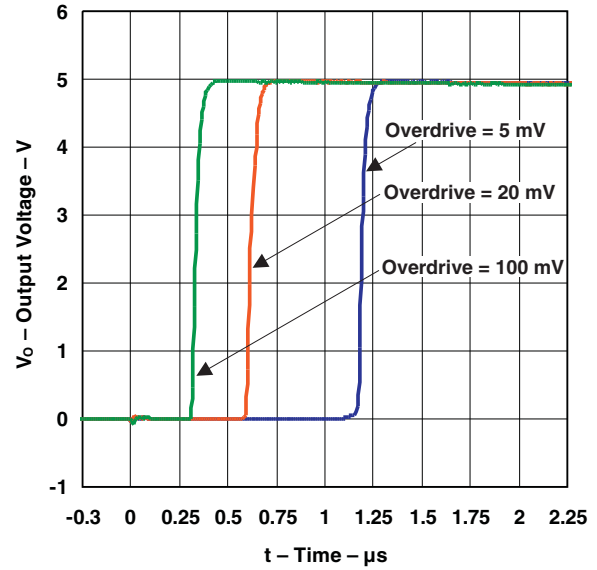


**TYPICAL CHARACTERISTICS (continued)**

**RESPONSE TIME FOR VARIOUS OVERDRIVES  
NEGATIVE TRANSITION**



**RESPONSE TIME FOR VARIOUS OVERDRIVES  
POSITIVE TRANSITION**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM239AMDREP	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM239AME	<a href="#">Samples</a>
LM239AMPWREP	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM239AE	<a href="#">Samples</a>
LM239AQDREP	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM239AEP	<a href="#">Samples</a>
V62/03672-01XE	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM239AEP	<a href="#">Samples</a>
V62/03672-02XE	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM239AME	<a href="#">Samples</a>
V62/03672-02YE	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM239AE	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LM239A-EP :**

- Catalog: [LM239A](#)
- Automotive: [LM239A-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM239AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239AMPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM239AQDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM239AMDREP	SOIC	D	14	2500	353.0	353.0	32.0
LM239AMPWREP	TSSOP	PW	14	2000	356.0	356.0	35.0
LM239AQDREP	SOIC	D	14	2500	340.5	336.1	32.0



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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