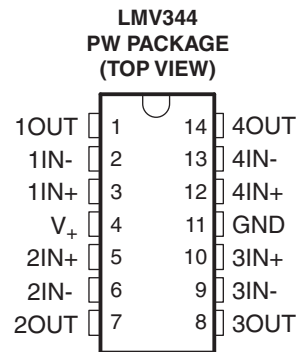
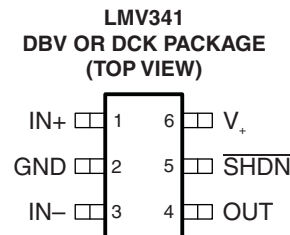


RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS

FEATURES

- Qualified for Automotive Applications
- 2.7-V and 5-V Performance
- Rail-to-Rail Output Swing
- Input Bias Current: 1 pA Typ
- Input Offset Voltage: 0.25 mV Typ
- Low Supply Current: 100 μ A Typ
- Gain Bandwidth: 1 MHz Typ
- Slew Rate: 1 V/ μ s Typ
- Turn-On Time From Shutdown: 5 μ s Typ
- Input Referred Voltage Noise (at 10 kHz): 20 nV/ $\sqrt{\text{Hz}}$



DESCRIPTION/ORDERING INFORMATION

The LMV341 and LMV344 devices are single and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typ) and an offset voltage of 0.25 mV (typ). The single supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from -0.2 V to 0.8 V from the positive supply rail. Additional features are a 20-nV/ $\sqrt{\text{Hz}}$ voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/ μ s slew rate, and 100- μ A current consumption per channel.

An extended industrial temperature range from -40°C to 125°C makes this device suitable for automotive applications.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 125°C	SC-70 – DCK	Reel of 3000	LMV341QDCKRQ1	RR_
	SOT-23 – DBV	Reel of 3000	LMV341QDBVRQ1	RCH_
	TSSOP – PW	Reel of 2000	LMV344IPWRQ1	LMV344Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

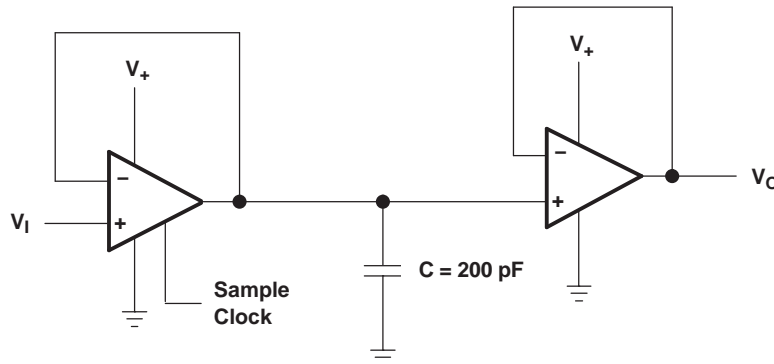
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

APPLICATION CIRCUIT: SAMPLE-AND-HOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V ₊	Supply voltage ⁽²⁾		5.5 V
V _{ID}	Differential input voltage ⁽³⁾		±5.5 V
V _I	Input voltage range (either input)		0 to 5.5 V
θ _{JA}	Package thermal impedance ⁽⁴⁾⁽⁵⁾	DBV package	165°C/W
		DCK package	259°C/W
		PW package	113°C/W
T _J	Operating virtual junction temperature		150°C
T _{stg}	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V₊ specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (5) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V ₊	Supply voltage (single-supply operation)	2.5	5.5	V
T _A	Operating free-air temperature	–40	125	°C

ESD PROTECTION

TEST CONDITIONS	TYP	UNIT
Human-Body Model (HBM)	2000	V
Machine Model (MM)	200	V

ELECTRICAL CHARACTERISTICS

 $V_+ = 2.7\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	LMV341			LMV344			UNIT	
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX		
V _{IO}	Input offset voltage	25°C	0.25		4	0.25		4	mV	
		Full range			4.5			4.5		
α_{VIO}	Average temperature coefficient of input offset voltage	Full range	1.7			1.7			$\mu\text{V}/^\circ\text{C}$	
I _{IB}	Input bias current	25°C	1		120	1		120	pA	
		–40°C to 85°C			250			250		
		–40°C to 125°C			3			3	nA	
I _{IO}	Input offset current	25°C	6.6			6.6			fA	
CMRR	Common-mode rejection ratio	$0 \leq V_{ICR} \leq 1.7\text{ V}$	40	80		56	80		dB	
		$0 \leq V_{ICR} \leq 1.6\text{ V}$	Full range			50				
k _{SVR}	Supply-voltage rejection ratio	$2.7\text{ V} \leq V_+ \leq 5\text{ V}$	45	82		65	82		dB	
		Full range			60					
V _{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB	25°C	0	–0.2 to 1.9	1.7	0	–0.2 to 1.9	1.7	V
A _V	Large-signal voltage gain ⁽²⁾	R _L = 10 kΩ to 1.35 V	25°C	73	113		78	113	dB	
			Full range	66			70			
		R _L = 2 kΩ to 1.35 V	25°C	70	103		72	103		
			Full range	63			64			
V _O	Output swing (delta from supply rails)	R _L = 2 kΩ to 1.35 V	Low level	25°C	24	60		24	60	mV
				Full range	95			95		
			High level	25°C	26	60		26	60	
				Full range	95			95		
		R _L = 10 kΩ to 1.35 V	Low level	25°C	5	30		5	30	
				Full range	40			40		
			High level	25°C	5.3	30		5.3	30	
				Full range	40			40		
I _{CC}	Supply current (per channel)	25°C	100	170		100	170	μA		
		Full range			230					
I _{OS}	Output short-circuit current	Sourcing	25°C	20	32		18	24	mA	
		Sinking	15			24				
SR	Slew rate	R _L = 10 kΩ ⁽³⁾	25°C	1			1			V/μs
GBM	Unity-gain bandwidth	R _L = 10 kΩ, C _L = 200 pF	25°C	1			1			MHz
Φ _m	Phase margin	R _L = 100 kΩ	25°C	72			72			deg
G _m	Gain margin	R _L = 100 kΩ	25°C	20			20			dB
V _n	Equivalent input noise voltage	f = 1 kHz	25°C	40			40			nV/√Hz
I _n	Equivalent input noise current	f = 1 kHz	25°C	0.001			0.001			pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A _V = 1, R _L = 600 Ω, V _I = 1 V _{PP}	25°C	0.017			0.017			%

(1) Typical values represent the most likely parametric norm.

(2) $\text{GND} + 0.2\text{ V} \leq V_O \leq V_+ - 0.2\text{ V}$

(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

SHUTDOWN CHARACTERISTICS

$V_+ = 2.7\text{ V}$, $GND = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$V_{SD} = 0\text{ V}$	25°C		0.045	1000	nA
			Full range			1.5	μA
$t_{(on)}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C	1.7 to 2.7	2.4 to 2.7		V
		Shutdown mode		0 to 1	0 to 0.8		

ELECTRICAL CHARACTERISTICS

 $V_+ = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A	LMV341			LMV344			UNIT		
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX			
V _{IO}	Input offset voltage	25°C	0.25		4	0.25		4	mV		
		Full range			4.5			4.5			
α_{VIO}	Average temperature coefficient of input offset voltage	Full range	1.9			1.9			$\mu\text{V}/^\circ\text{C}$		
I _{IB}	Input bias current	25°C	1		200	1		200	pA		
		–40°C to 85°C	375			375					
		–40°C to 125°C	5			5			nA		
I _{IO}	Input offset current	25°C	6.6			6.6			fA		
CMRR	Common-mode rejection ratio	$0 \leq V_{ICR} \leq 4\text{ V}$	46		86	56		86	dB		
		$0 \leq V_{ICR} \leq 3.9\text{ V}$	Full range			50					
k _{SVR}	Supply-voltage rejection ratio	25°C	45		82	65		82	dB		
		Full range	44			60					
V _{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB	25°C	0	–0.2 to 4.2	4	0	–0.2 to 4.2	4	V	
A _V	Large-signal voltage gain ⁽²⁾	R _L = 10 kΩ to 2.5 V	25°C	78		116	78		116	dB	
			Full range	70			70				
		R _L = 2 kΩ to 2.5 V	25°C	72		107	72		107		
			Full range	64			64				
V _O	Output swing (delta from supply rails)	R _L = 2 kΩ to 2.5 V	Low level	25°C	32		67	32		60	mV
				Full range	95			95			
			High level	25°C	34		60	34		60	
				Full range	95			95			
		R _L = 10 kΩ to 2.5 V	Low level	25°C	7		30	7		30	
				Full range	45			40			
			High level	25°C	7		30	7		30	
				Full range	40			40			
I _{CC}	Supply current (per channel)	25°C	107		200	107		200	μA		
		Full range	260			260					
I _{OS}	Output short-circuit current	Sourcing	25°C	85		113	70		90	mA	
		Sinking	50			75					
SR	Slew rate	R _L = 10 kΩ ⁽³⁾	25°C	1			1			V/μs	
GBM	Unity-gain bandwidth	R _L = 10 kΩ, C _L = 200 pF	25°C	1			1			MHz	
Φ _m	Phase margin	R _L = 100 kΩ	25°C	70			70			deg	
G _m	Gain margin	R _L = 100 kΩ	25°C	20			20			dB	
V _n	Equivalent input noise voltage	f = 1 kHz	25°C	39			39			nV/√Hz	
I _n	Equivalent input noise current	f = 1 kHz	25°C	0.001			0.001			pA/√Hz	
THD	Total harmonic distortion	f = 1 kHz, A _V = 1, R _L = 600 Ω, V _I = 1 V _{PP}	25°C	0.012			0.012			%	

(1) Typical values represent the most likely parametric norm.

(2) $\text{GND} + 0.2\text{ V} \leq V_O \leq V_+ - 0.2\text{ V}$

(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

SHUTDOWN CHARACTERISTICS

$V_+ = 5\text{ V}$, $\text{GND} = 0\text{ V}$, $V_{IC} = V_O = V_+/2$, $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(\text{SHDN})}$	Supply current in shutdown mode (per channel)	$V_{SD} = 0\text{ V}$	25°C		0.033	1	μA
			Full range			1.5	
$t_{(\text{on})}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		3.1 to 5	4.5 to 5	V
		Shutdown mode			0 to 1	0 to 0.8	

TYPICAL CHARACTERISTICS

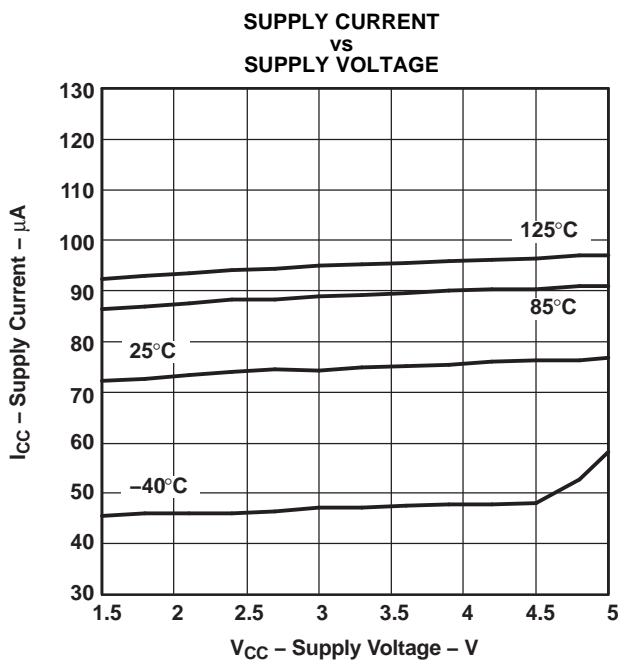


Figure 1.

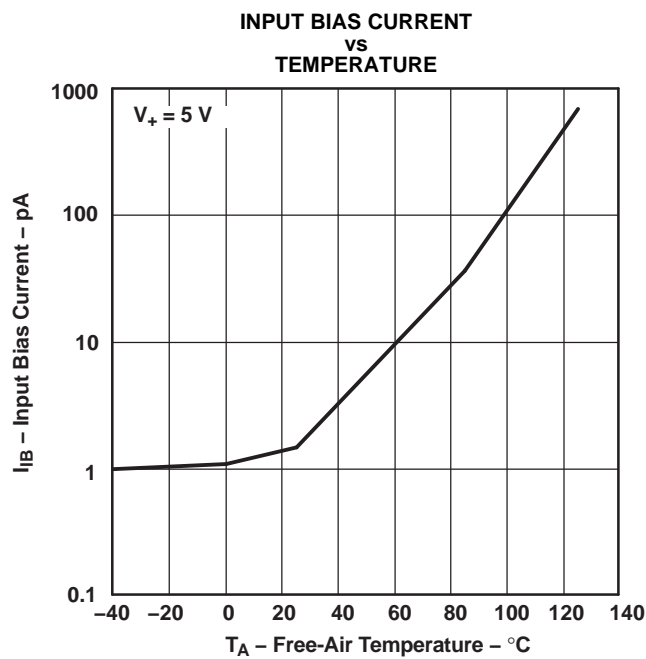


Figure 2.

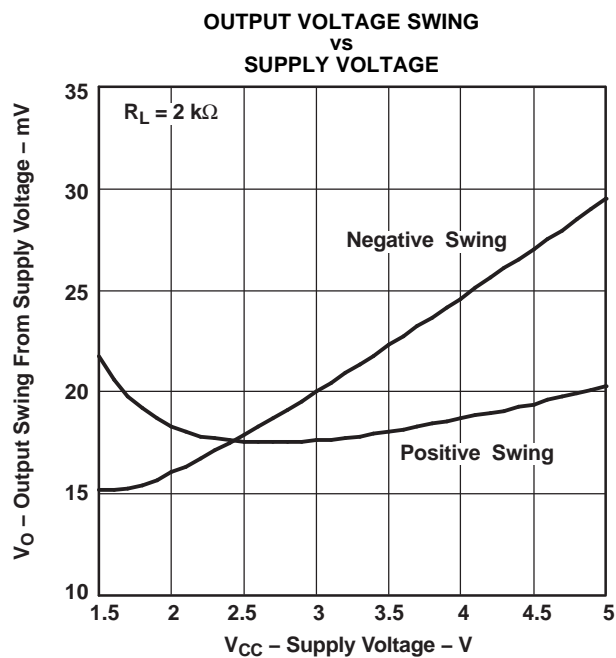


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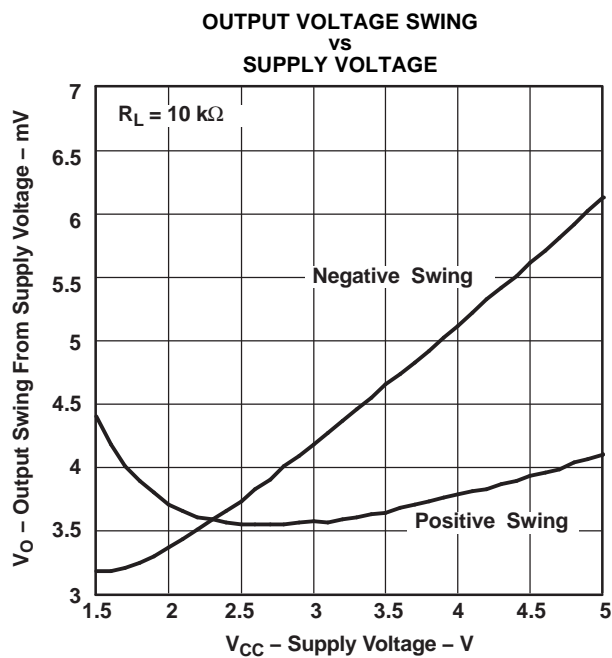
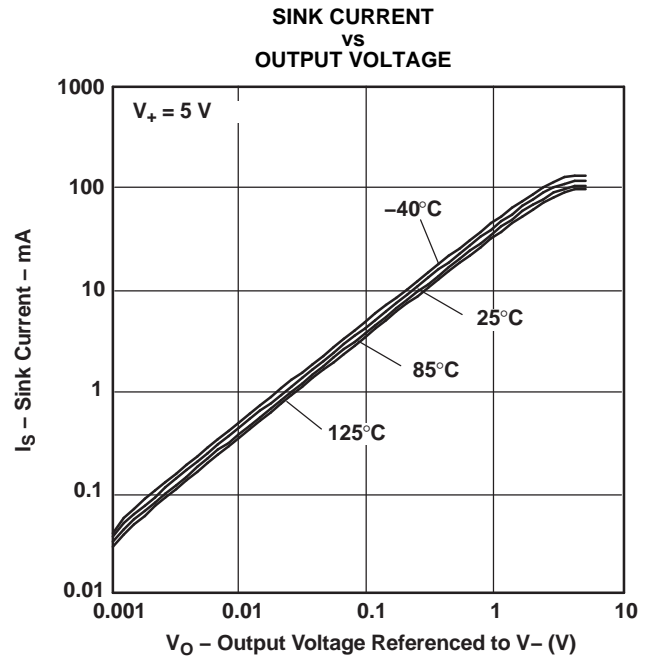
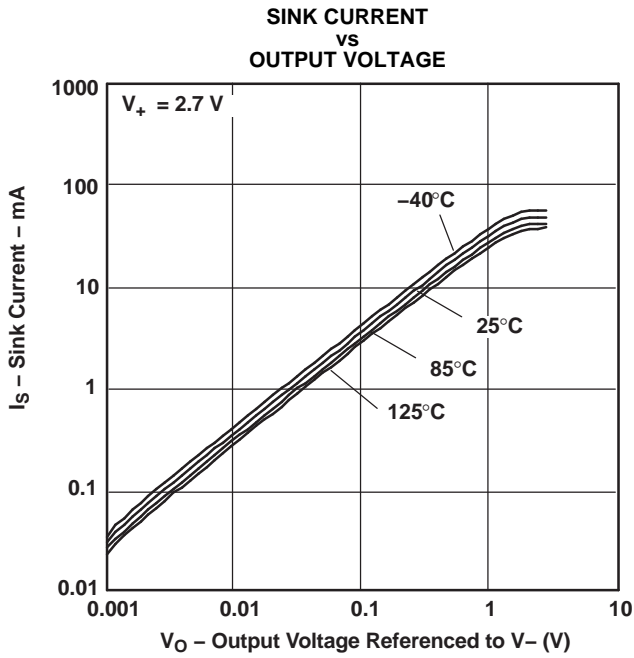
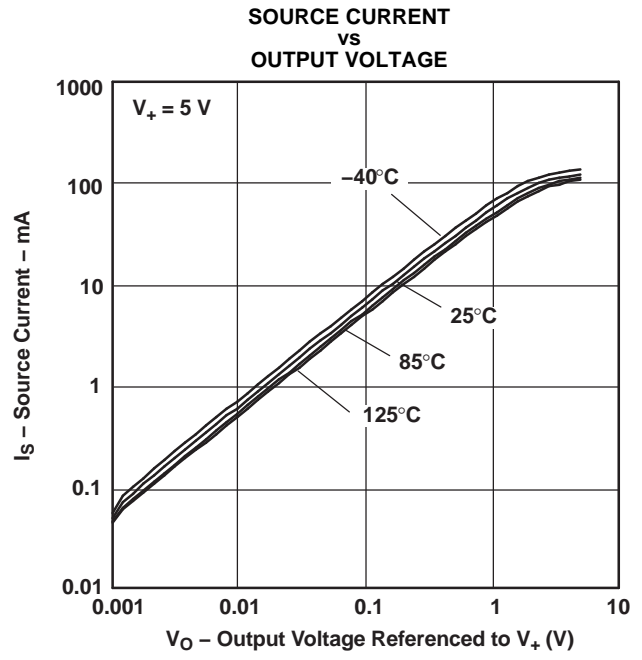
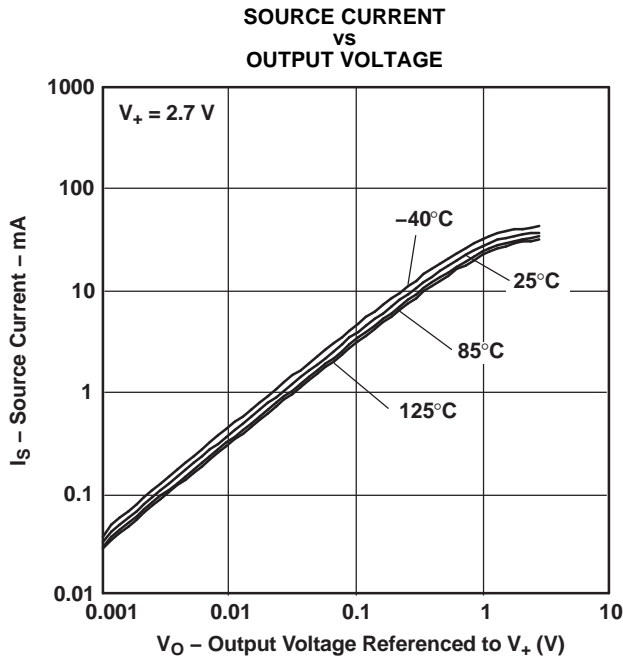


Figure 4.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

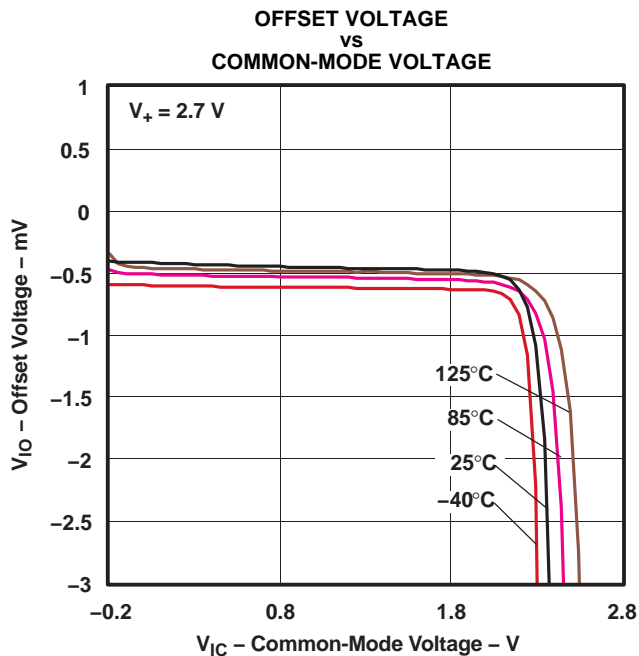


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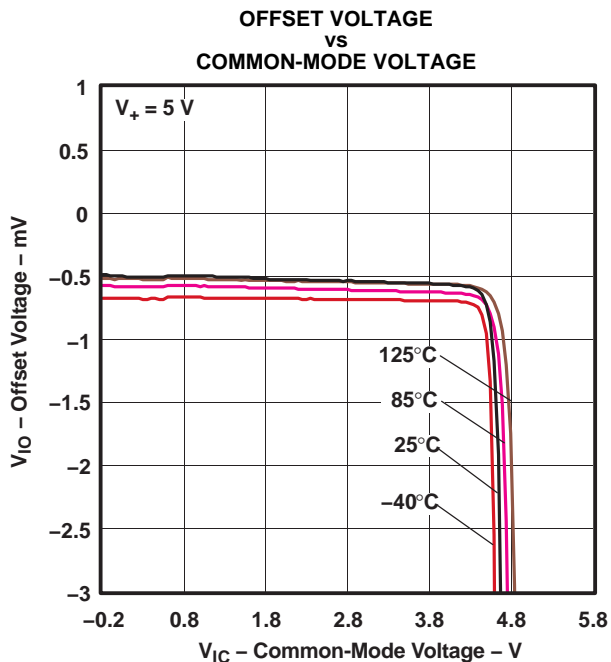


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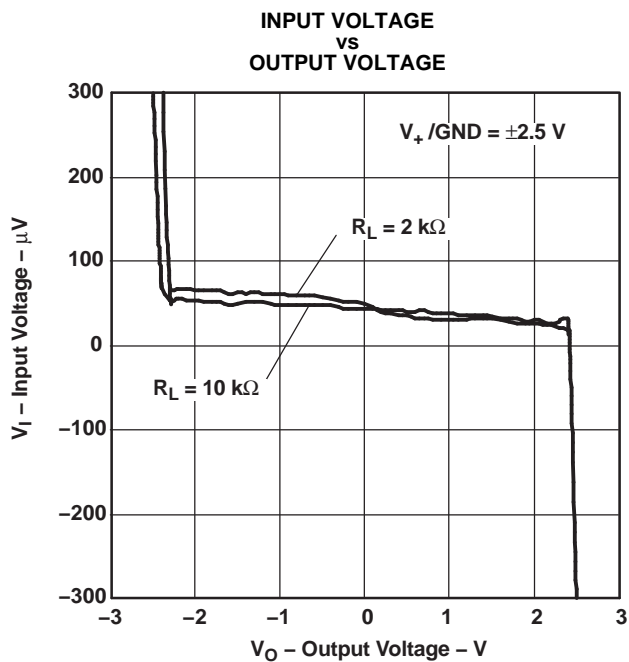


Figure 11.

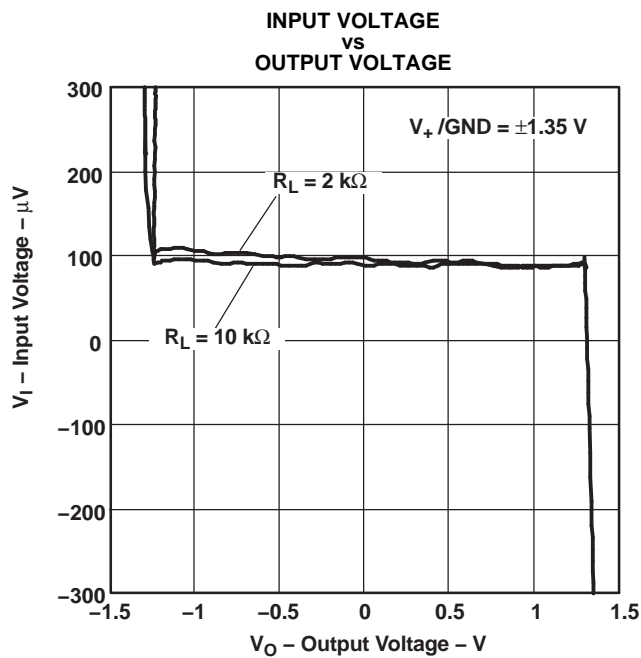


Figure 12.

TYPICAL CHARACTERISTICS (continued)

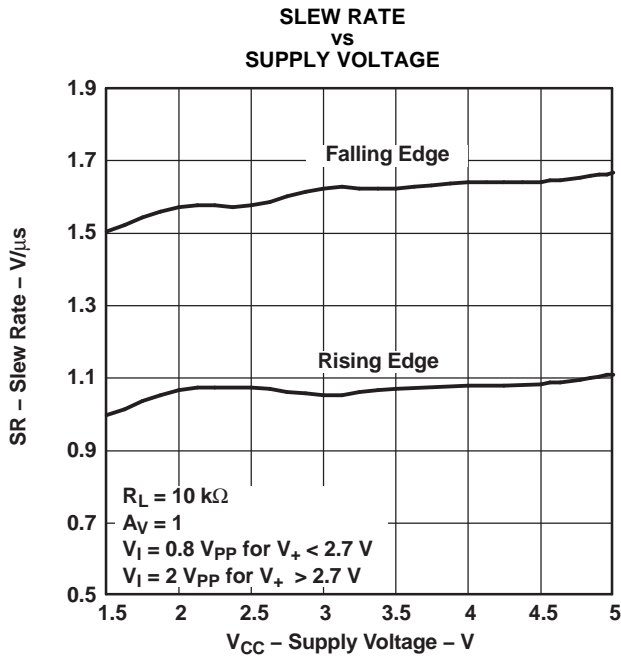


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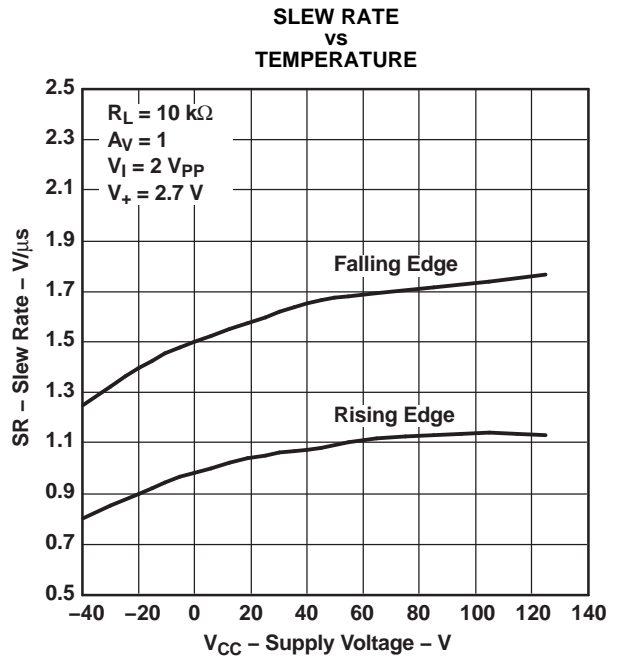


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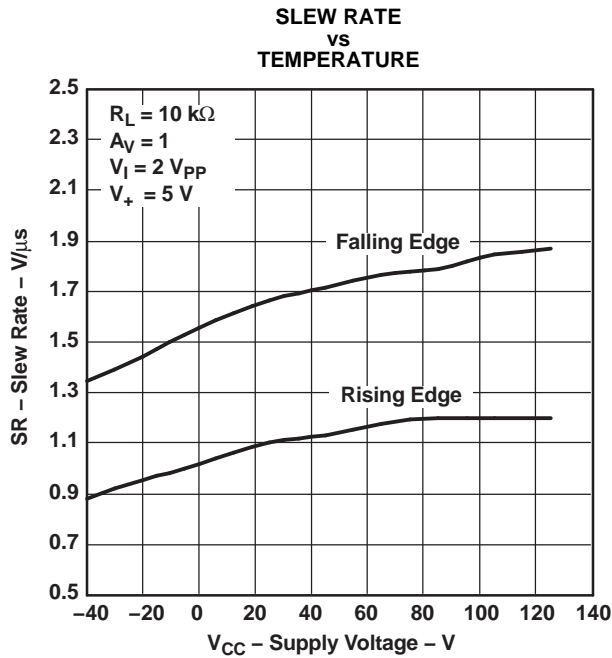


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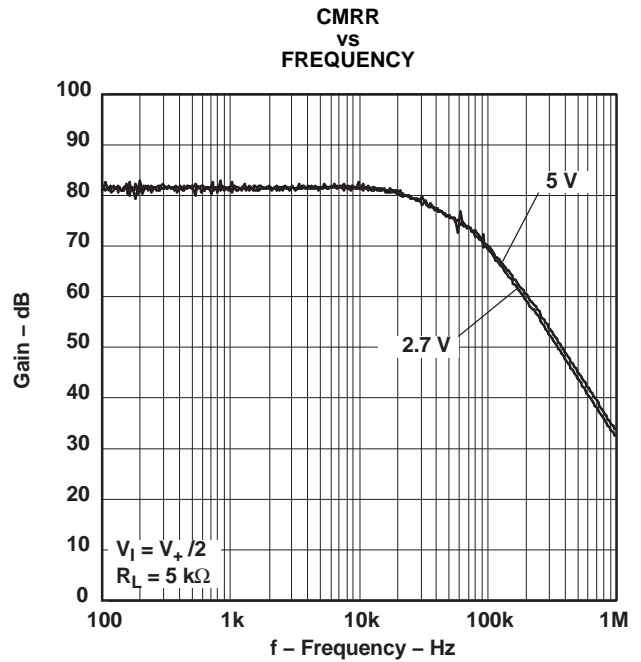


Figure 16.

TYPICAL CHARACTERISTICS (continued)

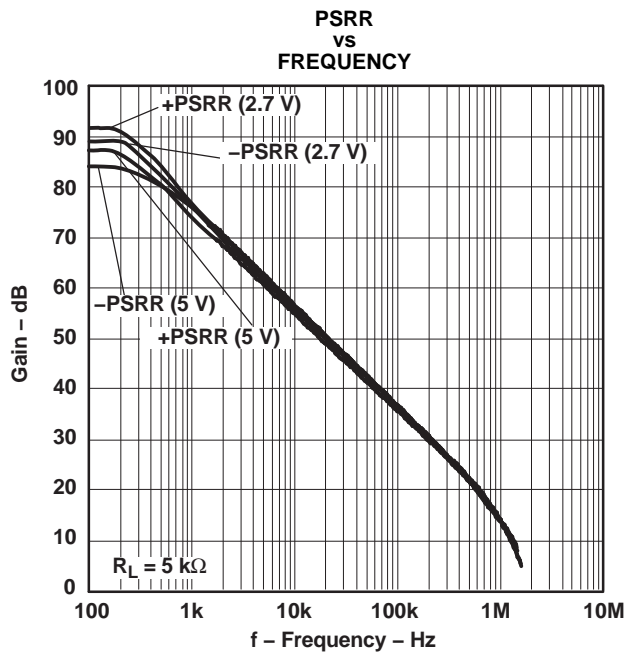


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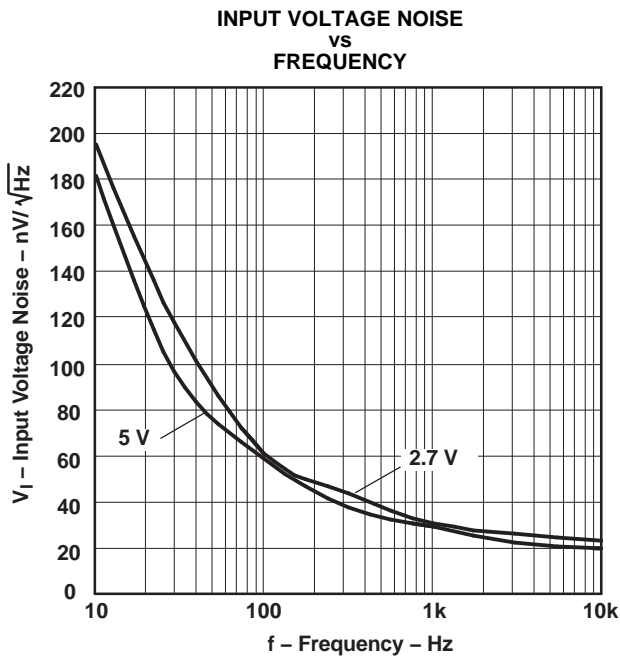


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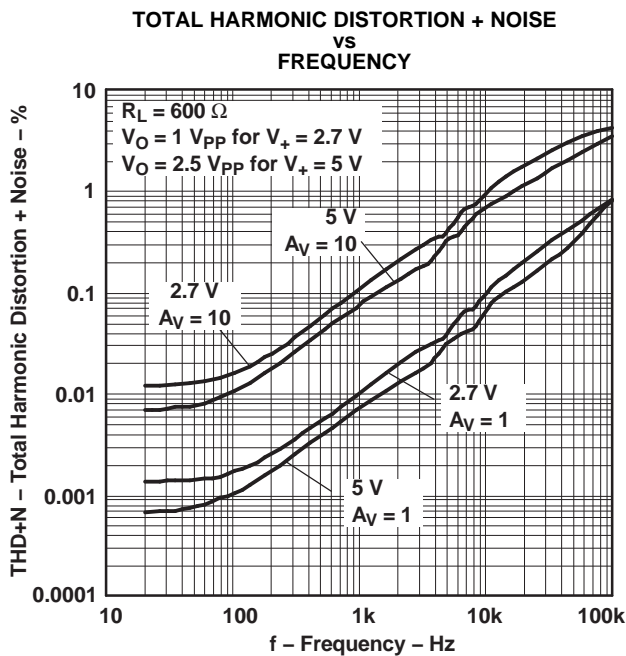


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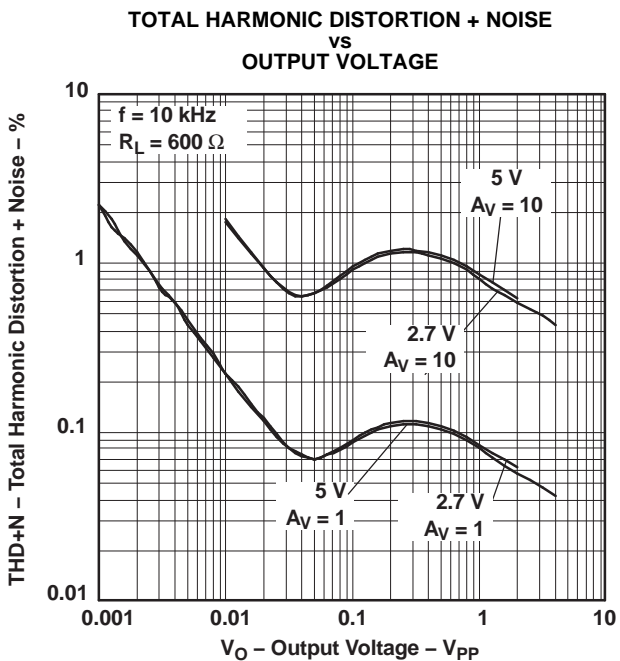


Figure 20.

TYPICAL CHARACTERISTICS (continued)

GAIN AND PHASE MARGIN
vs
FREQUENCY
($T_A = -40^\circ\text{C}, 25^\circ\text{C}, 125^\circ\text{C}$)

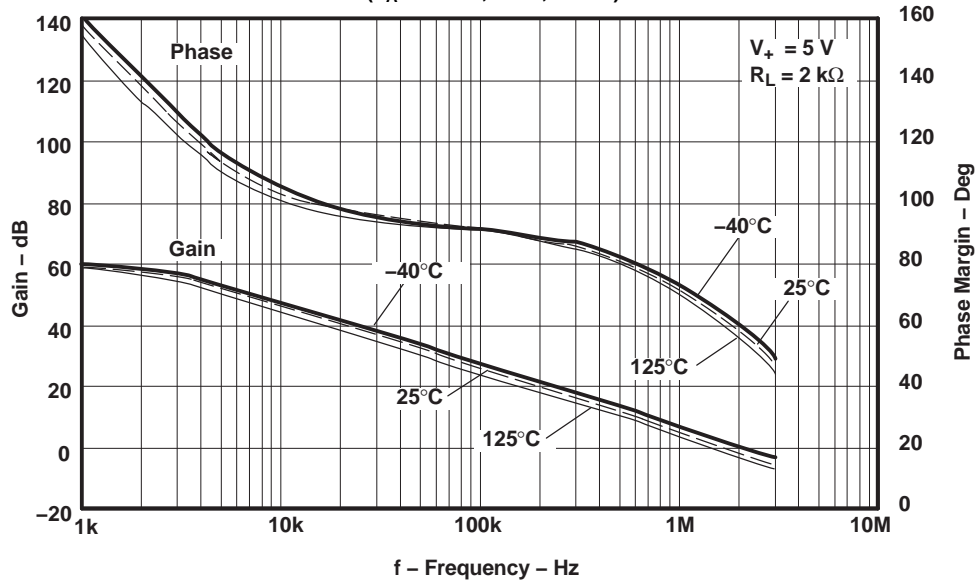


Figure 21.

GAIN AND PHASE MARGIN
vs
FREQUENCY
($R_L = 600\ \Omega, 2\text{ k}\Omega, 100\text{ k}\Omega$)

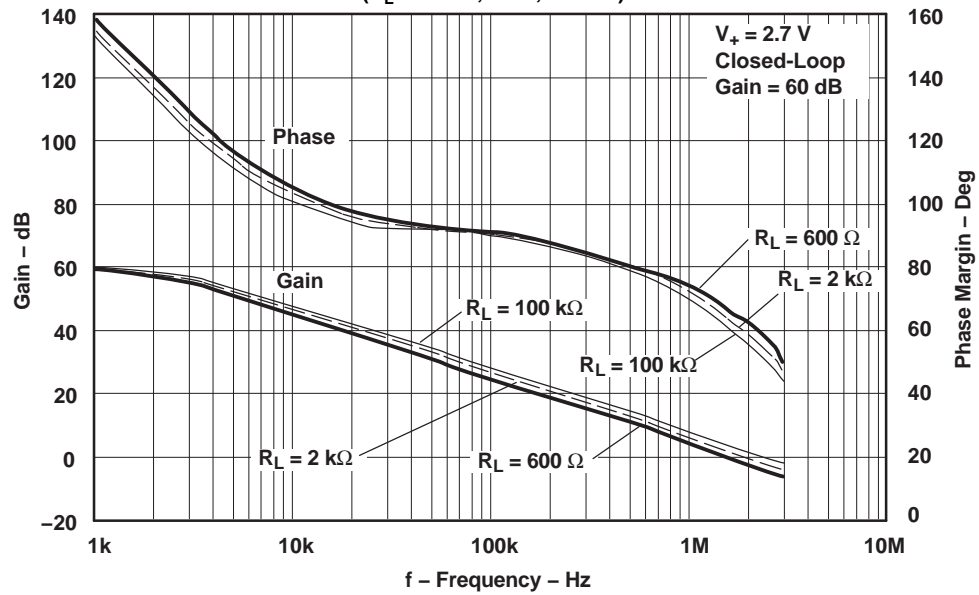


Figure 22.

TYPICAL CHARACTERISTICS (continued)

GAIN AND PHASE MARGIN
vs
FREQUENCY
($R_L = 600 \Omega, 2 \text{ k}\Omega, 100 \text{ k}\Omega$)

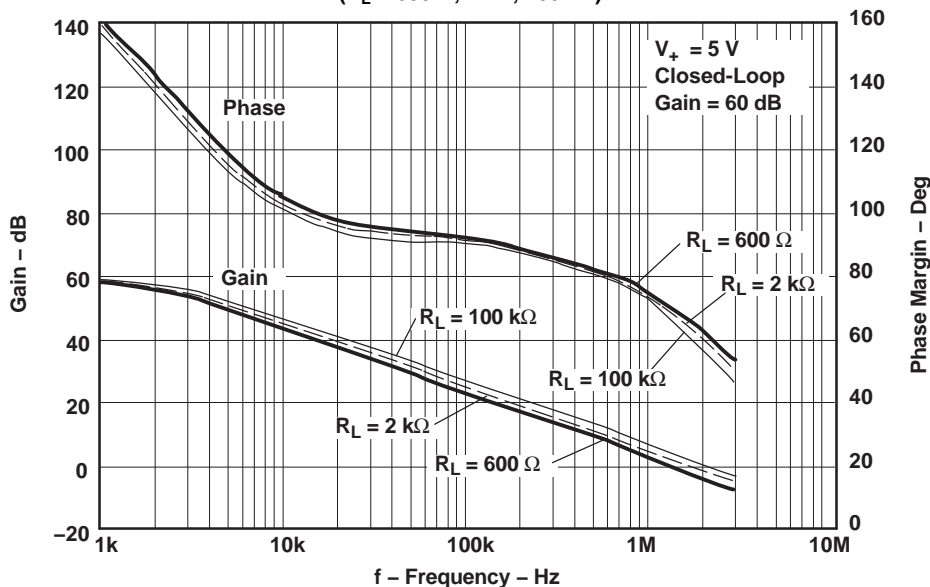


Figure 23.

GAIN AND PHASE MARGIN
vs
FREQUENCY
($C_L = 0 \text{ pF}, 100 \text{ pF}, 500 \text{ pF}, 1000 \text{ pF}$)

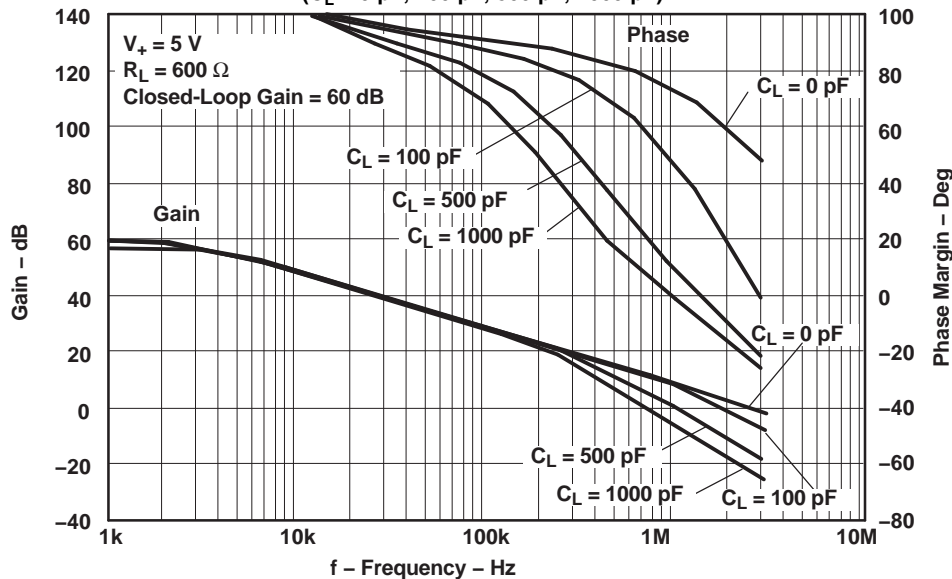


Figure 24.

TYPICAL CHARACTERISTICS (continued)

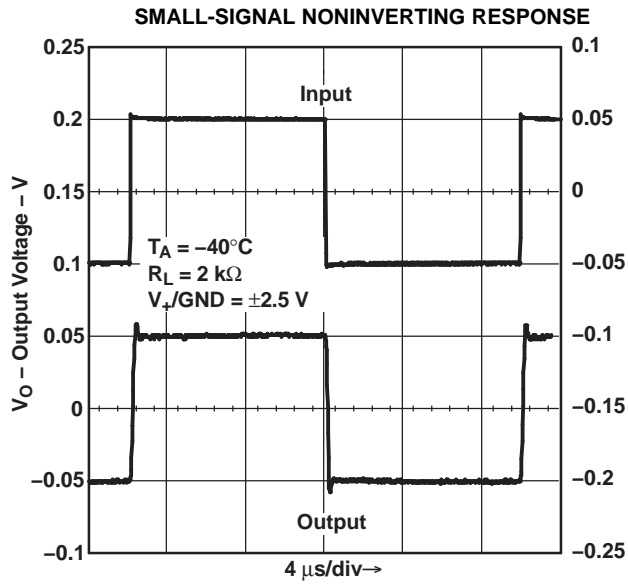


Figure 25.

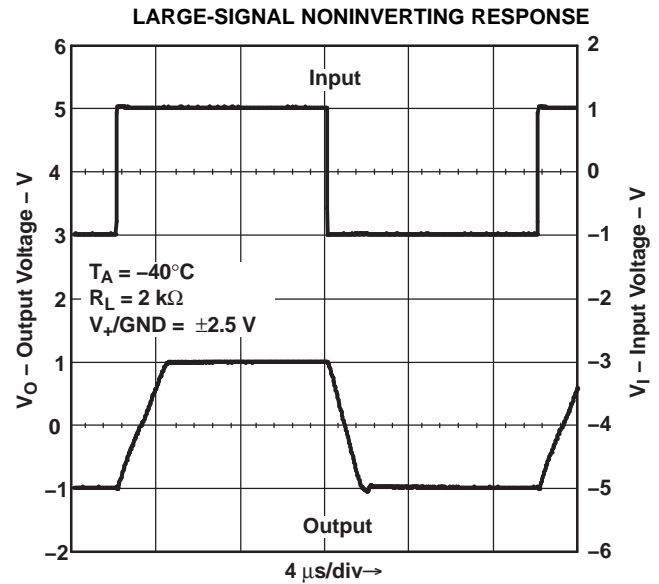


Figure 26.

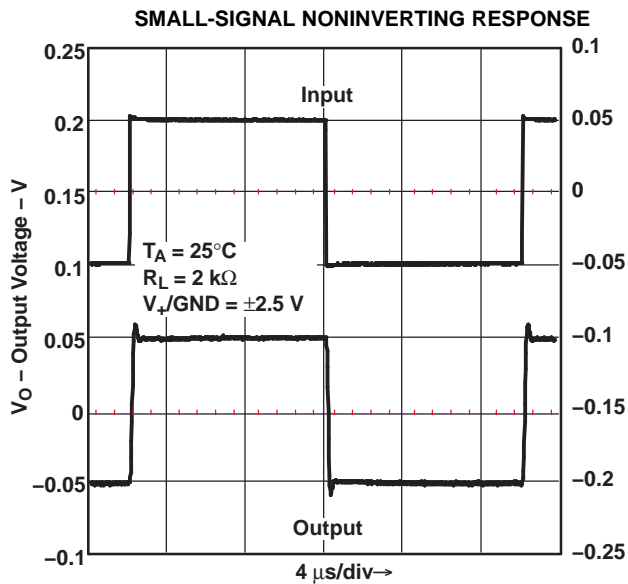


Figure 27.

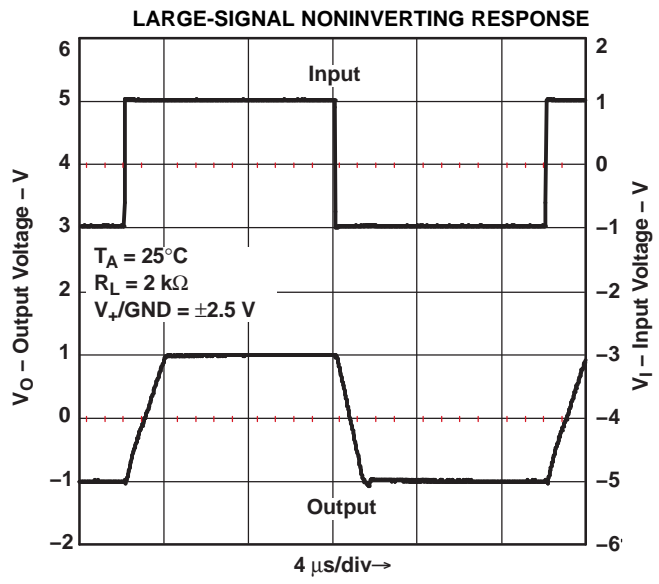


Figure 28.

TYPICAL CHARACTERISTICS (continued)

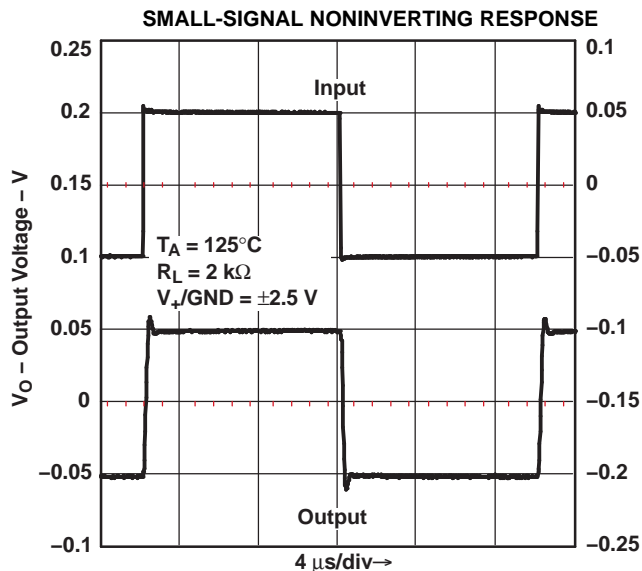


Figure 29.

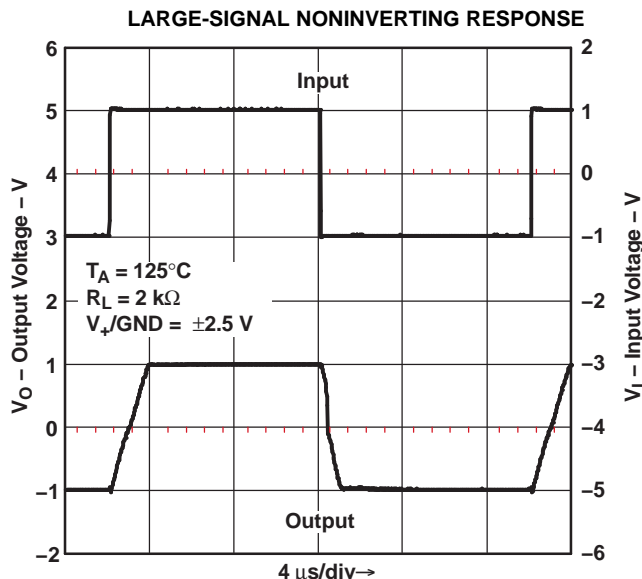


Figure 30.

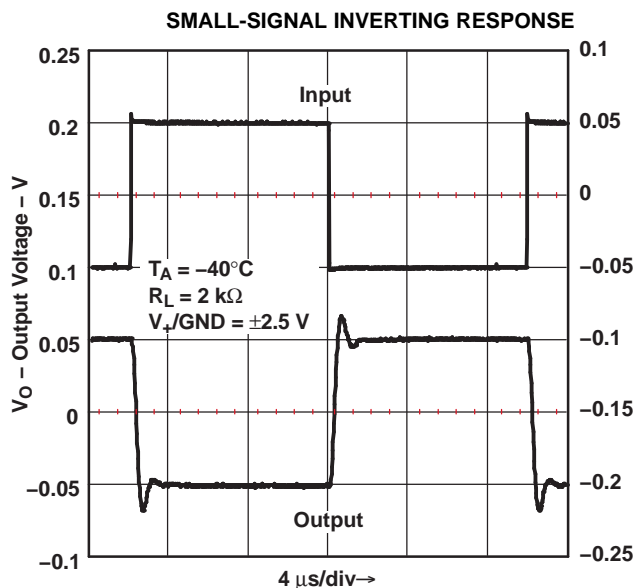


Figure 31.

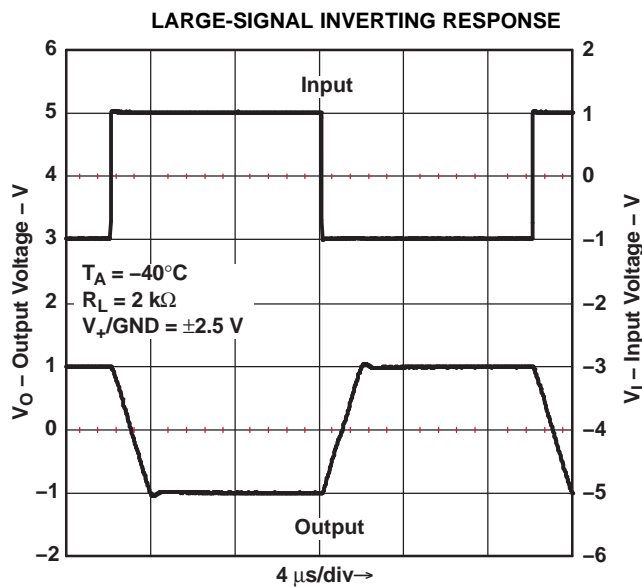


Figure 32.

TYPICAL CHARACTERISTICS (continued)

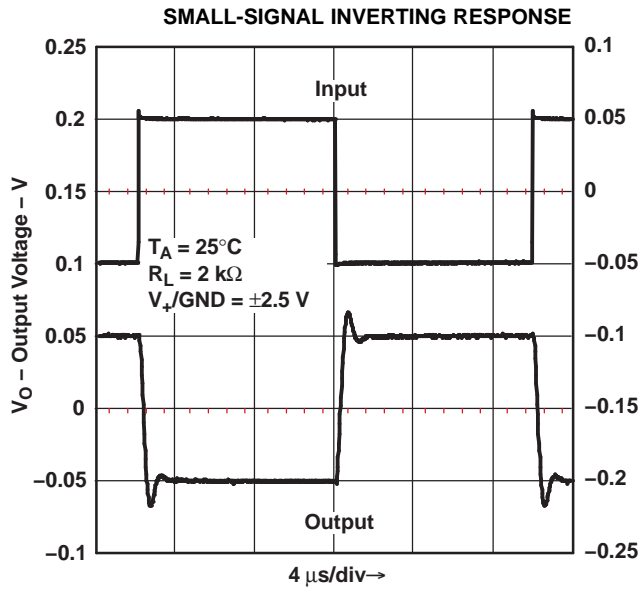


Figure 33.

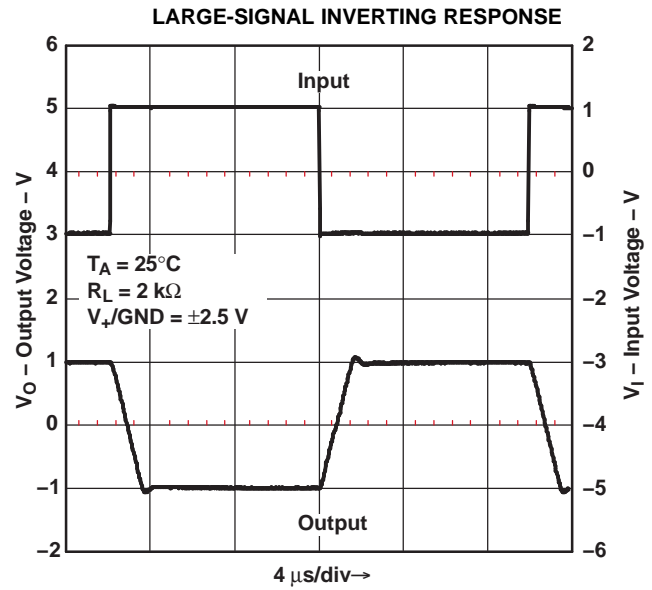


Figure 34.

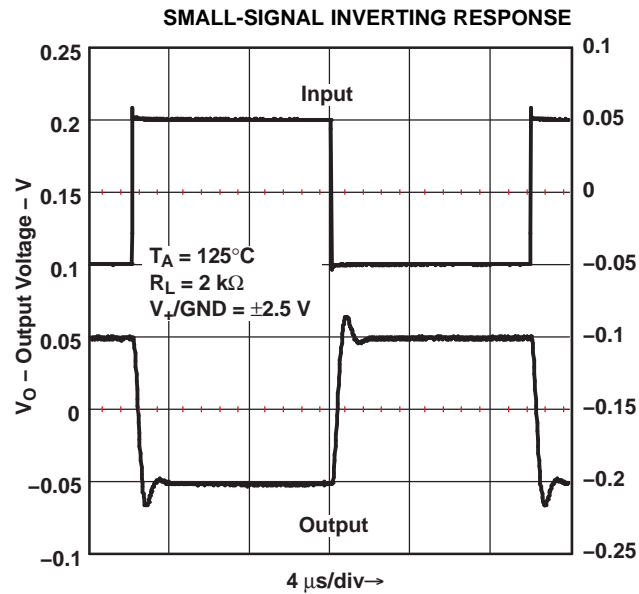


Figure 35.

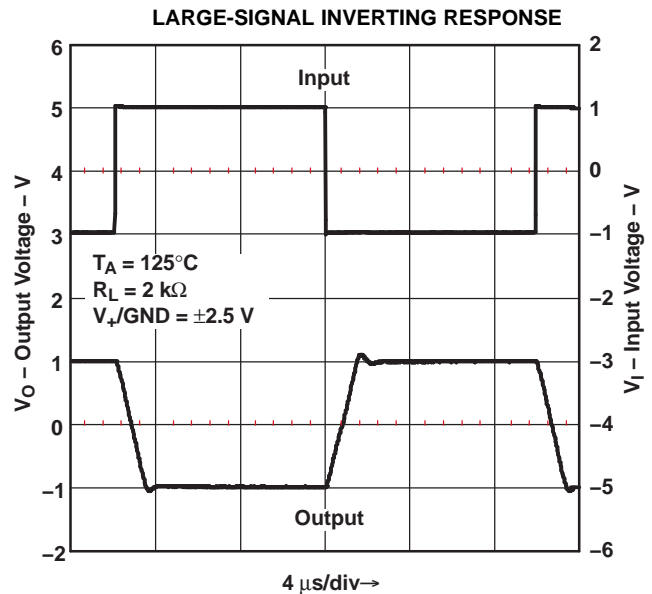


Figure 36.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV341QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RCHE	Samples
LMV341QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RRE	Samples
LMV344IPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMV341-Q1, LMV344-Q1 :

- Catalog: [LMV341](#), [LMV344](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV341QDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
LMV344IPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
LMV341QDCKRQ1	SC70	DCK	6	3000	200.0	183.0	25.0
LMV344IPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

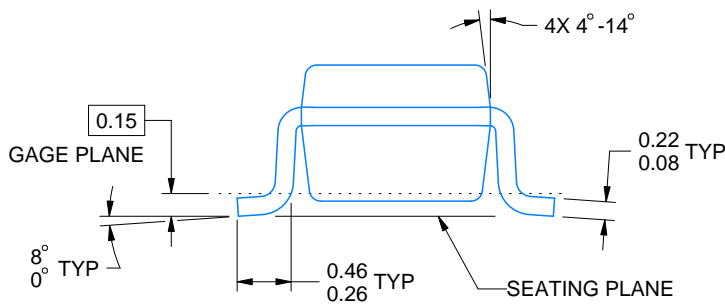
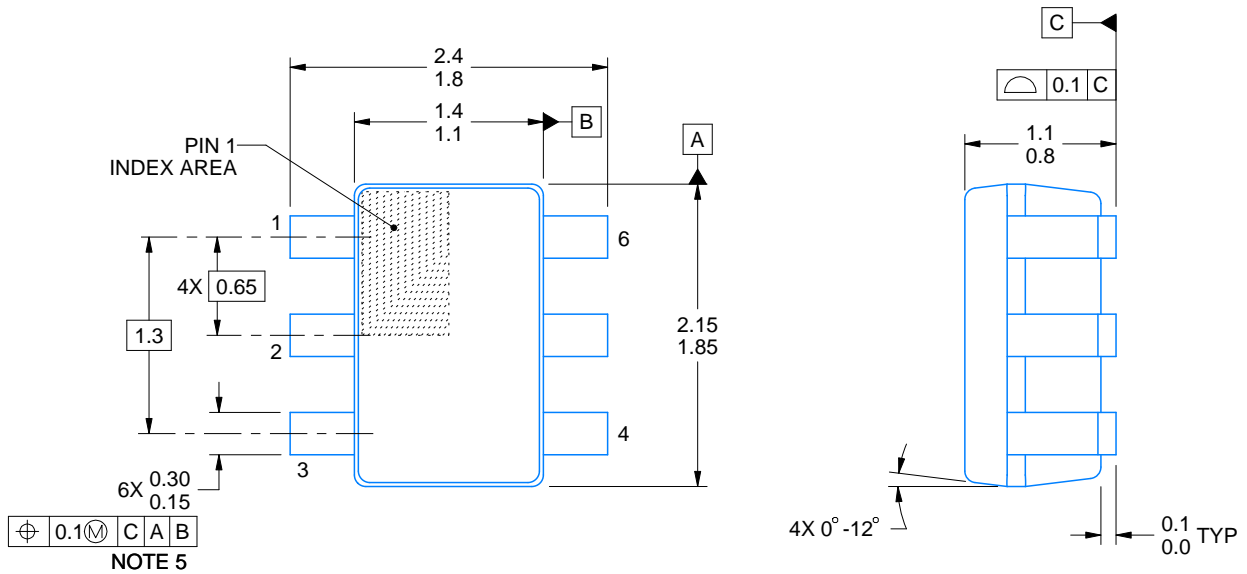
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

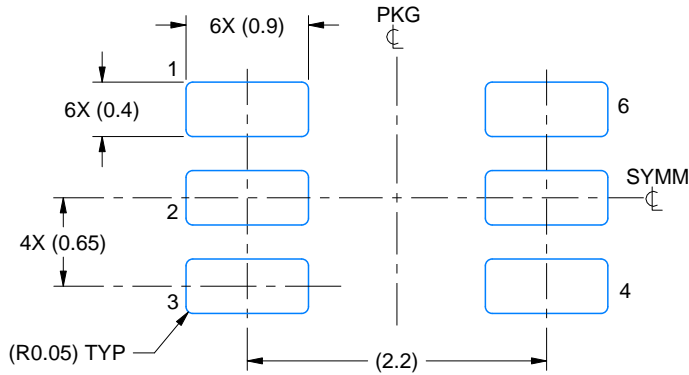
SMALL OUTLINE TRANSISTOR



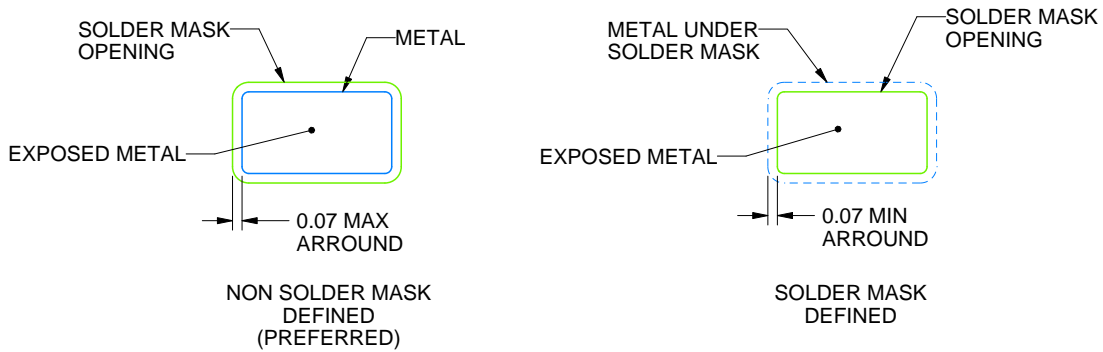
4214835/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

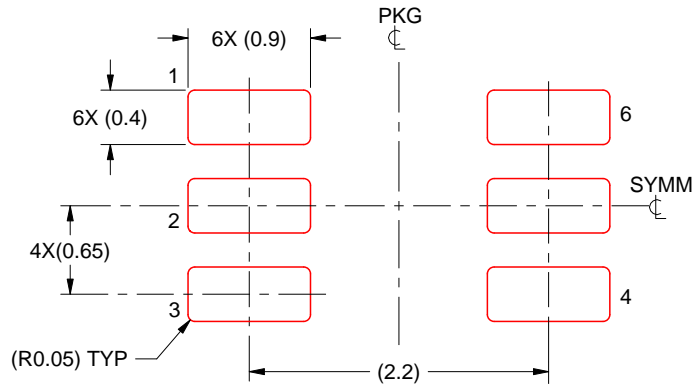


SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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