

## LP3999 Low Noise 150mA Voltage Regulator for RF/Analog Applications

Check for Samples: [LP3999](#)

### FEATURES

- 5 pin DSBGA Package
- Stable with Ceramic Capacitor
- Logic Controlled Enable
- Fast Turn-on
- Thermal-overload and short-circuit protection
- $-40$  to  $+125^{\circ}\text{C}$  junction temperature range for operation

### KEY SPECIFICATIONS

- 2.5V to 6.0V Input Range
- Accurate Output Voltage;  $\pm 75\text{mV} / 2\%$
- 60 mV Typical Dropout with 150 mA Load.  $V_{\text{out}} > 2.5\text{V}$
- Virtually Zero Quiescent Current when Disabled
- 10  $\mu\text{Vrms}$  Output Noise Over 10Hz to 100kHz
- Stable with a 1  $\mu\text{F}$  Output Capacitor
- Ensured 150 mA Output Current
- Fast Turn-on Time; 140  $\mu\text{s}$  (Typ.)

### APPLICATIONS

- GSM Portable Phones
- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- Bluetooth Devices
- Portable Information Appliances
- Handheld MP3 Devices

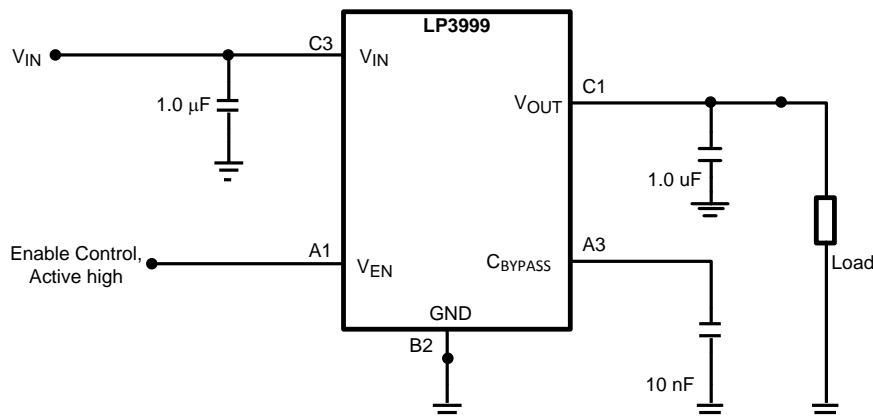
### DESCRIPTION

The LP3999 regulator is designed to meet the requirements of portable wireless battery-powered applications and will provide an accurate output voltage with low noise and low quiescent current. Ideally suited for powering RF/Analog devices this device will also be used to meet more general circuit requirements.

For battery powered applications the low dropout and low ground current provided by the device allows the lifetime of the battery to be maximized. The inclusion of an Enable(disable) control can be used by the system to further extend the battery lifetime by reducing the power consumption to virtually zero. Should the application require a device with an active disable function please refer to device LP3995.

The LP3999 also features internal protection against short-circuit currents and over-temperature conditions.

### Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

### DESCRIPTION (CONTINUED)

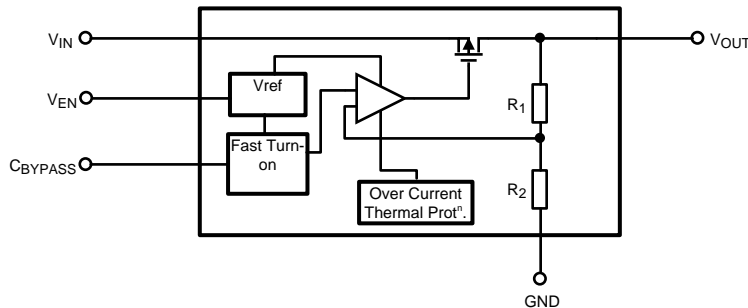
The LP3999 is designed to be stable with small 1.0  $\mu\text{F}$  ceramic capacitors. The small outline of the LP3999 DSBGA package with the required ceramic capacitors can realize a system application within minimal board area.

Performance is specified for a  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.

The device is available in DSBGA package. For other package options contact your local TI sales office.

The device is available in fixed output voltages in the ranges of 1.5V to 3.3V. For availability, please contact your local TI sales office.

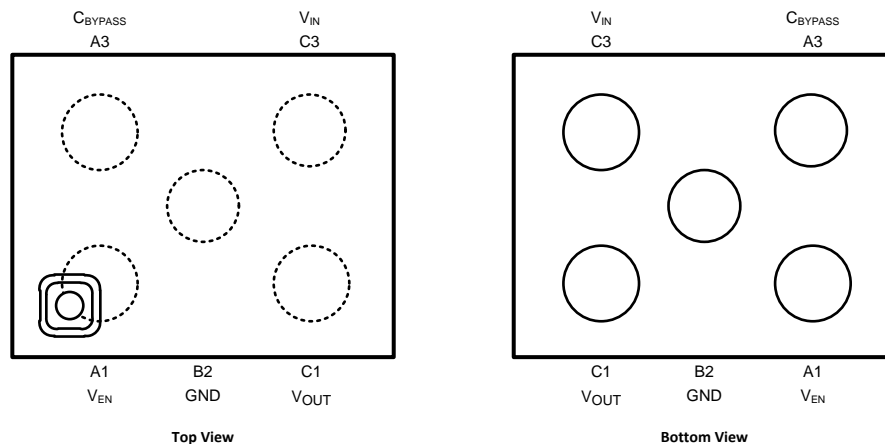
### Block Diagram



### PIN DESCRIPTIONS

Pin No.	Symbol	Name and Function
A1	$V_{EN}$	Enable Input; Disables the Regulator when $\leq 0.4\text{V}$ . Enables the regulator when $\geq 0.9\text{V}$
B2	GND	Common Ground
C1	$V_{OUT}$	Voltage output. Connect this output to the load circuit.
C3	$V_{IN}$	Voltage Supply Input
A3	$C_{BYPASS}$	Bypass Capacitor connection. Connect a 0.01 $\mu\text{F}$ capacitor for noise reduction.

### Connection Diagram



**5 Bump DSBGA Package**  
**See Package Number YZR0005**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)(2)</sup>

Orderable Device	Output Voltage (V)
LP399ITL-1.5/NOPB	1.5
LP399ITLX-1.5/NOPB	
LP399ITL-1.8/NOPB	1.8
LP399ITLX-1.8/NOPB	
LP399ITL-1.875/NOPB	1.875
LP399ITLX-1.875/NOPB	
LP399ITL-2.4/NOPB	2.4
LP399ITLX-2.4/NOPB	
LP399ITL-2.5/NOPB	2.5
LP399ITLX-2.5/NOPB	
LP399ITL-2.8/NOPB	2.8
LP399ITLX-2.8/NOPB	
LP399ITL-3.3/NOPB	3.3
LP399ITLX-3.3/NOPB	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
 (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

Input Voltage ( $V_{IN}$ )	-0.3 to 6.5V
Output Voltage	-0.3 to ( $V_{IN} + 0.3V$ ) to 6.5V (max)
Enable Input Voltage	-0.3 to 6.5V
Junction Temperature	150°C
Lead/Pad Temperature <sup>(4)</sup>	
DSBGA	260°C
Storage Temperature	-65 to +150°C
Continuous Power Dissipation <sup>(5)</sup>	Internally limited
ESD <sup>(6)</sup>	
Human Body Model	2 kV
Machine Model	200V

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.  
 (2) All voltages are with respect to the potential at the GND pin.  
 (3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**  
 (4) For further information on these packages please refer to application notes AN-1112 Micro SMD Package Wafer Level Chip Scale Package [SNVA009](#).  
 (5) Internal Thermal shutdown circuitry protects the device from permanent damage.  
 (6) The human body is 100 pF discharge through 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

## Operating Ratings <sup>(1)</sup>

Input Voltage (V <sub>IN</sub> )	2.5 to 6.0V
Enable Input Voltage	0 to 6.0V
Junction Temperature	-40 to +125°C
Ambient Temperature Range <sup>(2)</sup>	-40 to 85°C

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A(max)</sub>) is dependant on the maximum operating junction temperature (T<sub>J(max-op)</sub>), the maximum power dissipation (P<sub>D(max)</sub>), and the junction to ambient thermal resistance in the application (θ<sub>JA</sub>). This relationship is given by:
- $$T_{A(max)} = T_{J(max-op)} - (P_{D(max)} \times \theta_{JA}).$$

## Thermal Properties<sup>(1)</sup>

Junction to Ambient Thermal Resistance	
θ <sub>JA</sub> (DSBGA pkg.)	255°C/W

- (1) Junction to ambient thermal resistance is highly dependant on the application and board layout. In applications where high thermal dissipation is possible, special care must be paid to thermal issues in the board design.

## Electrical Characteristics

Unless otherwise noted, V<sub>EN</sub> = 1.5, V<sub>IN</sub> = V<sub>OUT(NOM)</sub> + 1.0V, C<sub>IN</sub> = 1 μF, I<sub>OUT</sub> = 1 mA, C<sub>OUT</sub> = 1 μF, C<sub>BP</sub> = 0.01 μF. Typical values and limits appearing in normal type apply for T<sub>J</sub> = 25°C. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to +125°C. <sup>(1)</sup> <sup>(2)</sup>

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V <sub>IN</sub>	Input Voltage			2.5	6.0	V
<b>DEVICE OUTPUT: 1.5 ≤ V<sub>OUT</sub> &lt; 1.8V</b>						
ΔV <sub>OUT</sub>	Output Voltage Tolerance	I <sub>OUT</sub> = 1 mA		-50	50	mV
				<b>-75</b>	<b>75</b>	
	Line Regulation Error	V <sub>IN</sub> = (V <sub>OUT(NOM)</sub> +1.0V) to 6.0V, I <sub>OUT</sub> = 1 mA		<b>-3.5</b>	<b>3.5</b>	mV/V
	Load Regulation Error	I <sub>OUT</sub> = 1 mA to 150 mA	10		<b>75</b>	μV/mA
PSRR	Power Supply Rejection Ratio <sup>(3)</sup>	f = 1 kHz, I <sub>OUT</sub> = 1 mA	58			dB
		f = 10 kHz, I <sub>OUT</sub> = 1 mA	58			
<b>DEVICE OUTPUT: 1.8 ≤ V<sub>OUT</sub> &lt; 2.5V</b>						
ΔV <sub>OUT</sub>	Output Voltage Tolerance	I <sub>OUT</sub> = 1 mA		-50	50	mV
				<b>-75</b>	<b>75</b>	
	Line Regulation Error	V <sub>IN</sub> = (V <sub>OUT(NOM)</sub> +1.0V) to 6.0V, I <sub>OUT</sub> = 1 mA		<b>-2.5</b>	<b>2.5</b>	mV/V
	Load Regulation Error	I <sub>OUT</sub> = 1 mA to 150 mA	10		<b>75</b>	μV/mA
PSRR	Power Supply Rejection Ratio <sup>(3)</sup>	f = 1 kHz, I <sub>OUT</sub> = 1 mA	60			dB
		f = 10 kHz, I <sub>OUT</sub> = 1 mA	60			
<b>DEVICE OUTPUT: 2.5 ≤ V<sub>OUT</sub> ≤ 3.3V</b>						
ΔV <sub>OUT</sub>	Output Voltage Tolerance	I <sub>OUT</sub> = 1 mA		-2	2	% of V <sub>OUT(NOM)</sub>
				<b>-3</b>	<b>3</b>	
	Line Regulation Error	V <sub>IN</sub> = (V <sub>OUT(NOM)</sub> +1.0V) to 6.0V, I <sub>OUT</sub> = 1 mA		<b>-0.1</b>	<b>0.1</b>	%/V
	Load Regulation Error	I <sub>OUT</sub> = 1 mA to 150 mA	0.0004		<b>0.002</b>	%/mA

- (1) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production at T<sub>J</sub> = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (2) V<sub>OUT(NOM)</sub> is the stated output voltage option for the device.
- (3) This electrical specification is ensured by design.

## Electrical Characteristics (continued)

Unless otherwise noted,  $V_{EN} = 1.5$ ,  $V_{IN} = V_{OUT(NOM)} + 1.0V$ ,  $C_{IN} = 1 \mu F$ ,  $I_{OUT} = 1$  mA,  $C_{OUT} = 1 \mu F$ ,  $C_{BP} = 0.01 \mu F$ . Typical values and limits appearing in normal type apply for  $T_J = 25^\circ C$ . Limits appearing in **boldface** type apply over the full temperature range for operation,  $-40$  to  $+125^\circ C$ . <sup>(1)</sup> <sup>(2)</sup>

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
V <sub>DO</sub>	Dropout Voltage	I <sub>OUT</sub> = 1 mA	0.4		<b>2</b>	mV
		I <sub>OUT</sub> = 150 mA	60		<b>100</b>	
PSRR	Power Supply Rejection Ratio <sup>(3)</sup>	f = 1 kHz, I <sub>OUT</sub> = 1 mA	60			dB
		f = 10 kHz, I <sub>OUT</sub> = 1 mA	50			
<b>FULL V<sub>OUT</sub> RANGE</b>						
I <sub>LOAD</sub>	Load Current	See <sup>(4)</sup> and <sup>(3)</sup>		0		μA
I <sub>Q</sub>	Quiescent Current	V <sub>EN</sub> = 1.5V, I <sub>OUT</sub> = 0 mA	85		<b>150</b>	μA
		V <sub>EN</sub> = 1.5V, I <sub>OUT</sub> = 150 mA	140		<b>200</b>	
		V <sub>EN</sub> = 0.4V	0.003		<b>1.5</b>	
I <sub>SC</sub>	Short Circuit Current Limit		450			mA
E <sub>N</sub>	Output Noise Voltage <sup>(3)</sup>	BW = 10 Hz to 100 kHz, V <sub>IN</sub> = 4.2V, No Load	10			μVrms
		BW = 10 Hz to 100 kHz, V <sub>IN</sub> = 4.2V, 1mA Load	30			
T <sub>SHUTDOWN</sub>	Thermal Shutdown	Temperature	160			°C
		Hysteresis	20			
<b>ENABLE CONTROL CHARACTERISTICS</b>						
I <sub>EN</sub>	Maximum Input Current at V <sub>EN</sub> Input	V <sub>EN</sub> = 0.0V and V <sub>IN</sub> = 6.0V	0.001			μA
V <sub>IL</sub>	Low Input Threshold				<b>0.4</b>	V
V <sub>IH</sub>	High Input Threshold			<b>0.9</b>		V
<b>TIMING CHARACTERISTICS</b>						
T <sub>ON</sub>	Turn On Time <sup>(5)</sup>	To 95% Level <sup>(6)</sup>	140			μs

(4) The device maintains the regulated output voltage without load.

(5) This electrical specification is ensured by design.

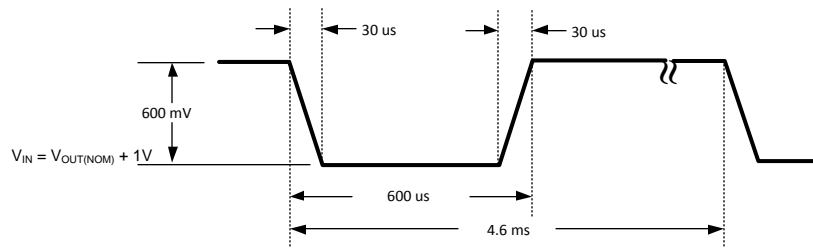
(6) Time from V<sub>EN</sub> = 0.9V to V<sub>OUT</sub> = 95% (V<sub>OUT(NOM)</sub>)

## Recommended Output Capacitor

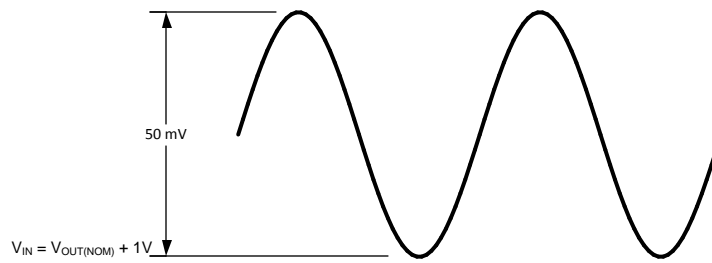
Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
C <sub>OUT</sub>	Output Capacitor	Capacitance <sup>(1)</sup>	1.0	0.70		μF
		ESR		5	500	mΩ

(1) The capacitor tolerance should be 30% or better over temperature. Recommended capacitor type is X7R however dependant on application X5R, Y5V and Z5U can also be used.

**INPUT TEST SIGNALS**



**Figure 1. Line Transient Response Input Test Signal**



**Figure 2. PSRR Input Test Signal**

### TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified,  $C_{IN} = C_{OUT} = 1.0 \mu\text{F}$  Ceramic,  $V_{IN} = V_{OUT} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ .

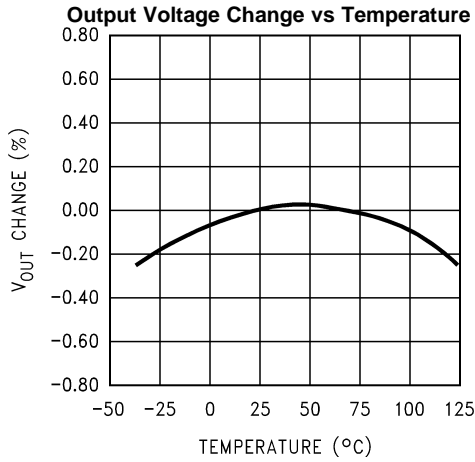


Figure 3.

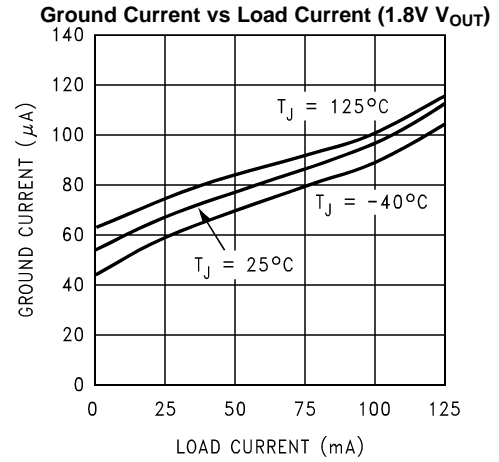


Figure 4.

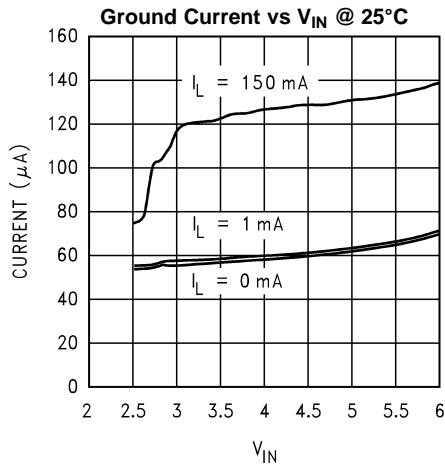


Figure 5.

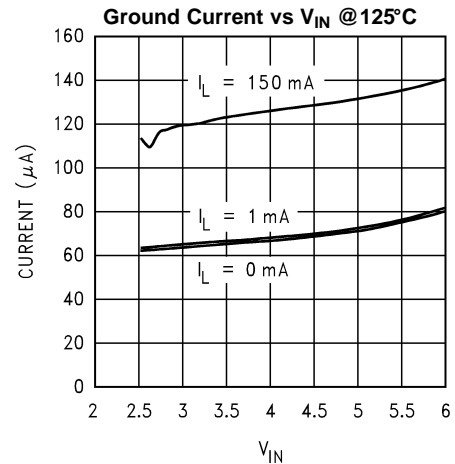


Figure 6.

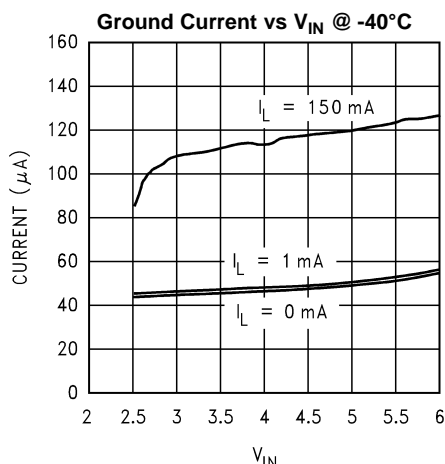


Figure 7.

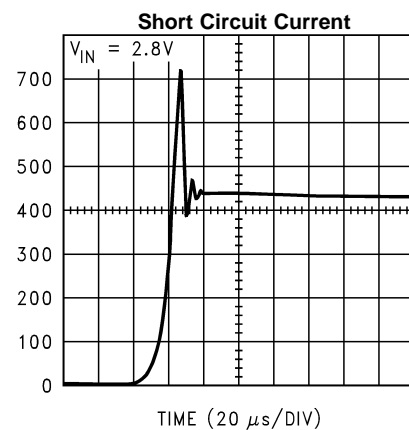


Figure 8.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $C_{IN} = C_{OUT} = 1.0 \mu\text{F}$  Ceramic,  $V_{IN} = V_{OUT} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ .

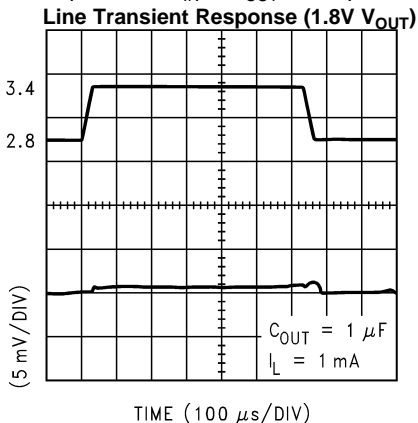


Figure 9.

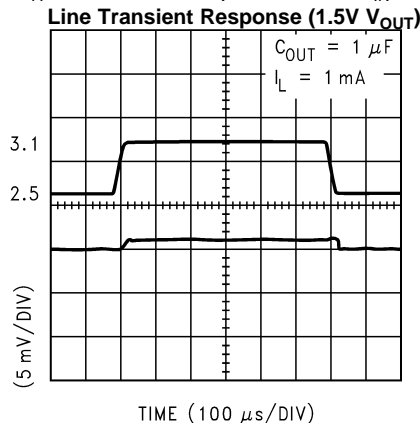


Figure 10.

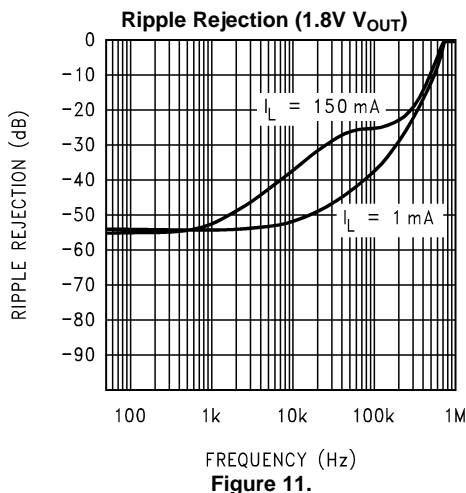


Figure 11.

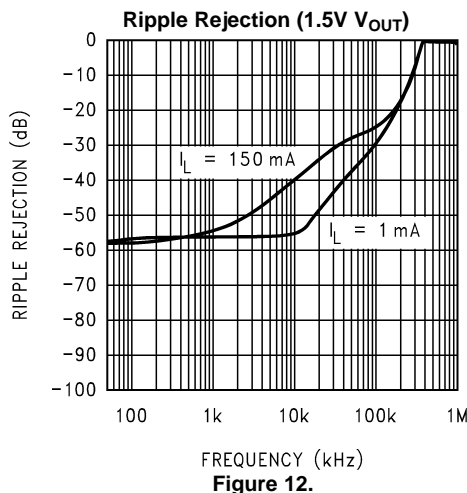


Figure 12.

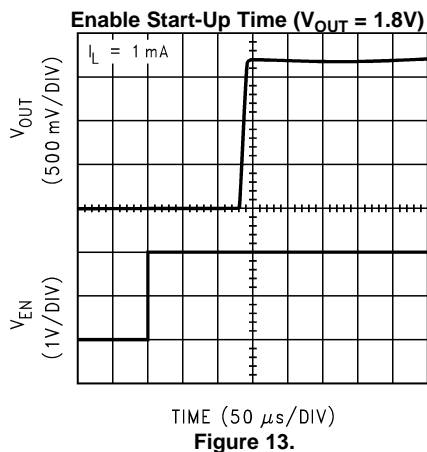


Figure 13.

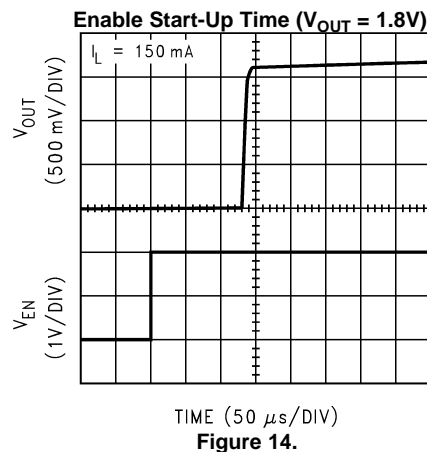


Figure 14.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Unless otherwise specified,  $C_{IN} = C_{OUT} = 1.0 \mu\text{F}$  Ceramic,  $V_{IN} = V_{OUT} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ , Enable pin is tied to  $V_{IN}$ .

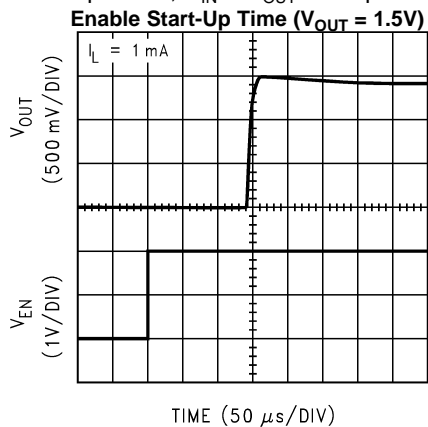


Figure 15.

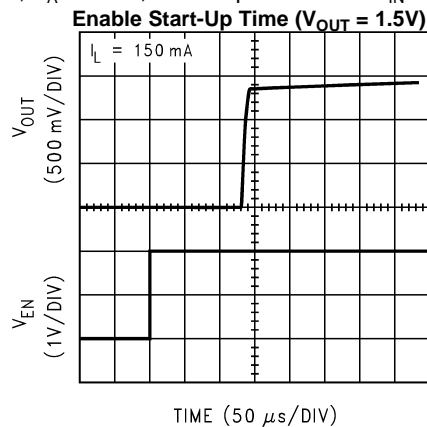


Figure 16.

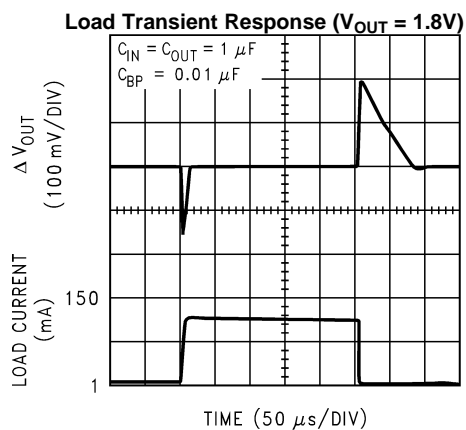


Figure 17.

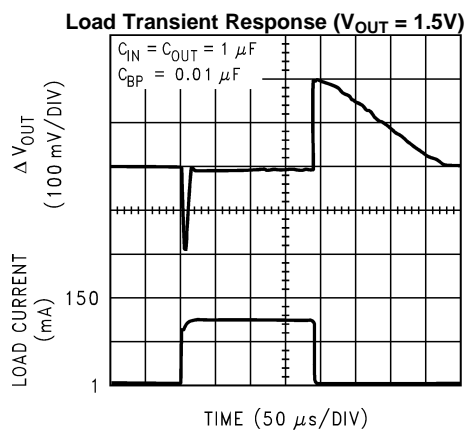


Figure 18.

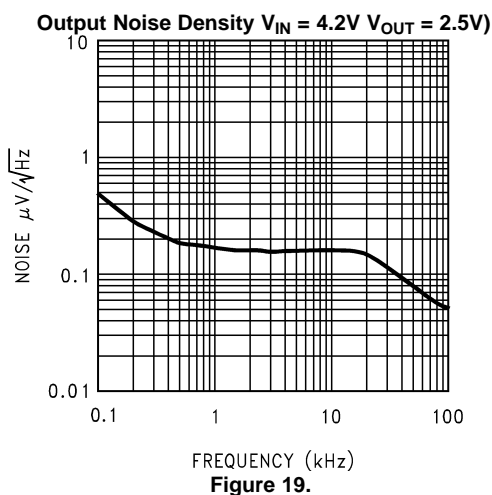


Figure 19.

## APPLICATION HINTS

### POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

Re-stating the equation given in <sup>(1)</sup> in the electrical specification section, the allowable power dissipation for the device in a given package can be calculated:

$$P_D = \frac{(T_{J(\text{MAX})} - T_A)}{\theta_{JA}} \quad (1)$$

With a  $\theta_{JA} = 255^\circ\text{C/W}$ , the device in the DSBGA package returns a value of 392 mW with a maximum junction temperature of  $125^\circ\text{C}$ .

The actual power dissipation across the device can be represented by the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

### EXTERNAL CAPACITORS

In common with most regulators, the LP3999 requires external capacitors to ensure stable operation. The LP3999 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

### INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0  $\mu\text{F}$  capacitor be connected between the LP3999 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the **ESR** (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain  $\approx 1.0 \mu\text{F}$  over the entire operating temperature range.

### OUTPUT CAPACITOR

The LP3999 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in the 1.0 [to 10  $\mu\text{F}$ ] range, and with ESR between 5 m $\Omega$  to 500 m $\Omega$ , is suitable in the LP3999 application circuit.

For this device the output capacitor should be connected between the  $V_{OUT}$  pin and ground.

It may also be possible to use tantalum or film capacitors at the device output,  $V_{OUT}$ , but these are not as attractive for reasons of size and cost (see the section [CAPACITOR CHARACTERISTICS](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 m $\Omega$  to 500 m $\Omega$  for stability.

(1) In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A(\text{max})}$ ) is dependant on the maximum operating junction temperature ( $T_{J(\text{max-op})}$ ), the maximum power dissipation ( $P_{D(\text{max})}$ ), and the junction to ambient thermal resistance in the application ( $\theta_{JA}$ ). This relationship is given by:

$$T_{A(\text{max})} = T_{J(\text{max-op})} - (P_{D(\text{max})} \times \theta_{JA})$$

## NO-LOAD STABILITY

The LP3999 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

## CAPACITOR CHARACTERISTICS

The LP3999 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1  $\mu\text{F}$  to 4.7  $\mu\text{F}$ , ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1  $\mu\text{F}$  ceramic capacitor is in the range of 20 m $\Omega$  to 40 m $\Omega$ , which easily meets the ESR requirement for stability for the LP3999.

The temperature performance of ceramic capacitors varies by type. Most large value ceramic capacitors ( $\geq 2.2$   $\mu\text{F}$ ) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within  $\pm 15\%$  over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1  $\mu\text{F}$  to 4.7  $\mu\text{F}$  range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

## NOISE BYPASS CAPACITOR

A bypass capacitor should be connected between the  $C_{\text{BYPASS}}$  pin and ground to significantly reduce the noise at the regulator output. This device pin connects directly to a high impedance node within the bandgap reference circuitry. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The use of a 0.01  $\mu\text{F}$  bypass capacitor is strongly recommended to prevent overshoot on the output during start-up.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High quality ceramic capacitors with NPO or COG dielectric typically have very low leakage. Polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDO's, the addition of a noise reduction capacitor does not effect the transient response of the device.

## ENABLE OPERATION

The LP3999 may be switched ON or OFF by a logic input at the ENABLE pin,  $V_{\text{EN}}$ . A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3 nA. If the application does not require the shutdown feature, the  $V_{\text{EN}}$  pin should be tied to  $V_{\text{IN}}$  to keep the regulator output permanently on. To ensure proper operation, the signal source used to drive the  $V_{\text{EN}}$  input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under  $V_{\text{IL}}$  and  $V_{\text{IH}}$ .

## FAST TURN ON

Fast turn-on is ensured by control circuitry within the reference block allowing a very fast ramp of the output voltage to reach the target voltage. There is no active turn-off on this device. Refer to LP3995 for a similar device with active turn-off.

## DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI's AN-1112 Application Report ([SNVA009](#)).

Referring to the section *Surface Mount Assembly Considerations*, it should be noted that the pad style which must be used with the 5 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

### **DSBGA LIGHT SENSITIVITY**

Exposing the DSBGA device to direct sunlight will cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

Light with wavelengths in the red and infra-red part of the spectrum have the most detrimental effect thus the fluorescent lighting used inside most buildings has very little effect on performance. Tests carried out on a DSBGA test board showed a negligible effect on the regulated output voltage when brought within 1 cm of a fluorescent lamp. A deviation of less than 0.1% from nominal output voltage was observed.

---

## REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
<ul style="list-style-type: none"><li>Changed layout of National Data Sheet to TI format .....</li></ul>	<a href="#">12</a>

---

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3999ITL-1.8/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITL-2.4/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITL-2.5/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITL-3.3/NOPB	ACTIVE	DSBGA	YZR	5	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITLX-1.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITLX-2.5/NOPB	ACTIVE	DSBGA	YZR	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITLX-2.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>
LP3999ITLX-3.3/NOPB	ACTIVE	DSBGA	YZR	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3999ITL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITL-2.4/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITL-3.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITLX-2.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITLX-2.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3999ITLX-3.3/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

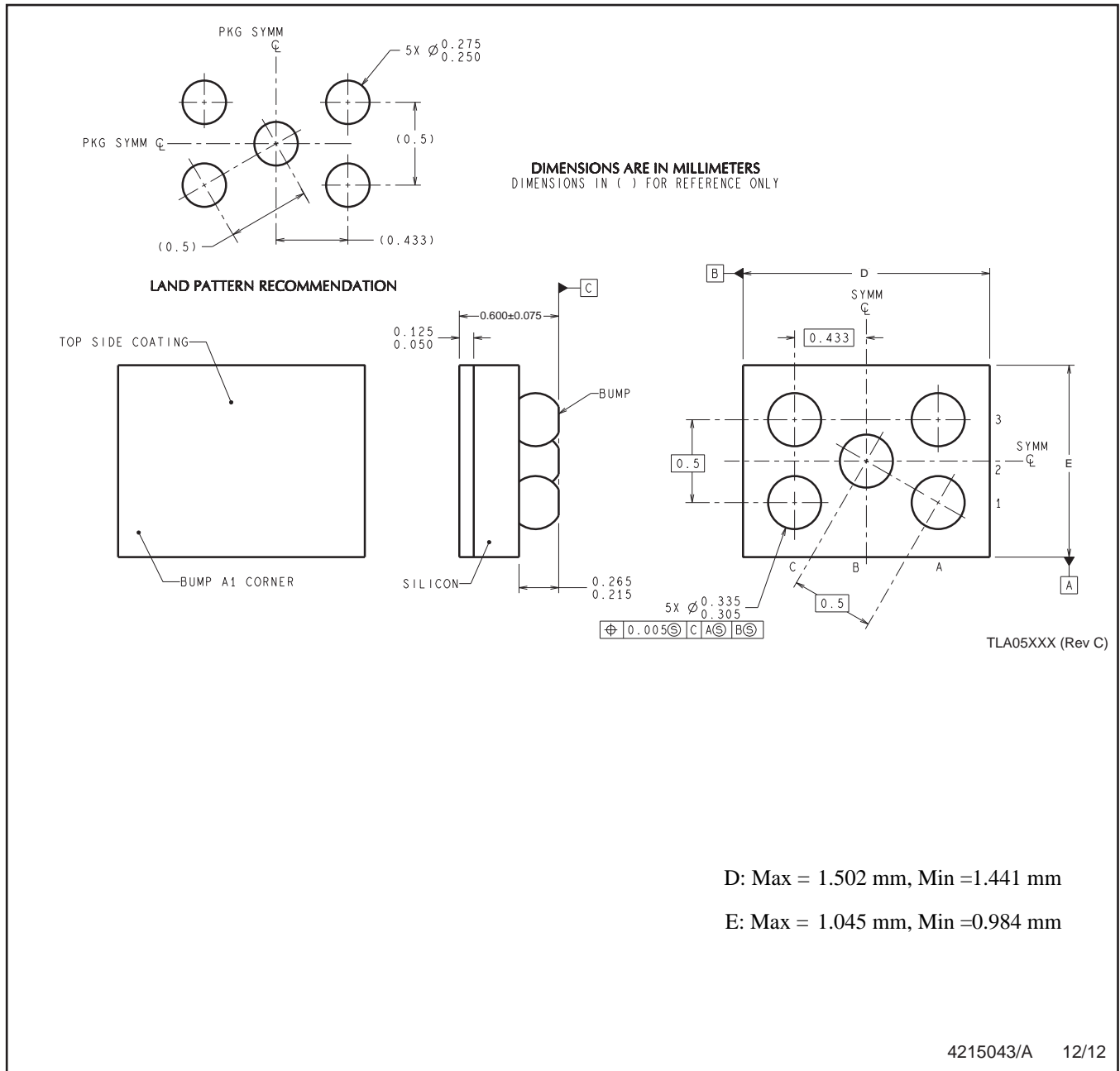


**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3999ITL-1.8/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3999ITL-2.4/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3999ITL-2.5/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3999ITL-3.3/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3999ITLX-1.8/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3999ITLX-2.5/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3999ITLX-2.8/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3999ITLX-3.3/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0

YZR0005



D: Max = 1.502 mm, Min = 1.441 mm

E: Max = 1.045 mm, Min = 0.984 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated