24-BIT, 96-kHz STEREO A/D CONVERTER WITH 6 × 2-CHANNEL MUX AND PGAE

FEATURES

- **Multiplexer and Programmable-Gain Amplifier (PGA)**
  - **6×2-Channel Single-Ended Inputs**
  - **Multiplexed Output**
  - **Maximum Input Level: 2.4 V rms**
  - **Input Resistance: 50 kΩ, Minimum**
  - **PGA Gain: 11-dB to –11-dB Range, 0.5 dB/Step**
- **24-Bit Delta-Sigma Stereo A/D Converter**
- **Antialiasing Filter Included**
- **Oversampling Decimation Filter**
  - **Oversampling Frequency: ×64**
  - **Pass-Band Ripple: ±0.05 dB**
  - **Stop-Band Attenuation: –65 dB**
  - **On-Chip High-Pass Filter: 0.91 Hz (48 kHz)**
- **High Performance**
  - **THD+N: 0.0023% (Typically)**
  - **SNR: 101 dB (Typically)**
  - **Dynamic Range: 102 dB (Typically)**
- **PCM Audio Interface**
  - **Master/Slave Mode Selectable**
  - **Data Formats: 24-Bit Left-Justified, 24-Bit I^2S, 16-, 24-Bit Right-Justified**
- **Mode Control by Serial Interface:**
  - **With SPI Control (PCM1850A)**
  - **With I^2C Control (PCM1851A)**
- **Sampling Rate: 16–96 kHz**
- **System Clock: 256 f_s, 384 f_s, 512 f_s, 768 f_s**
- **Dual Power Supplies: 5 V for Analog, 3.3 V for Digital**
- **Package: 32-Pin TQFP**

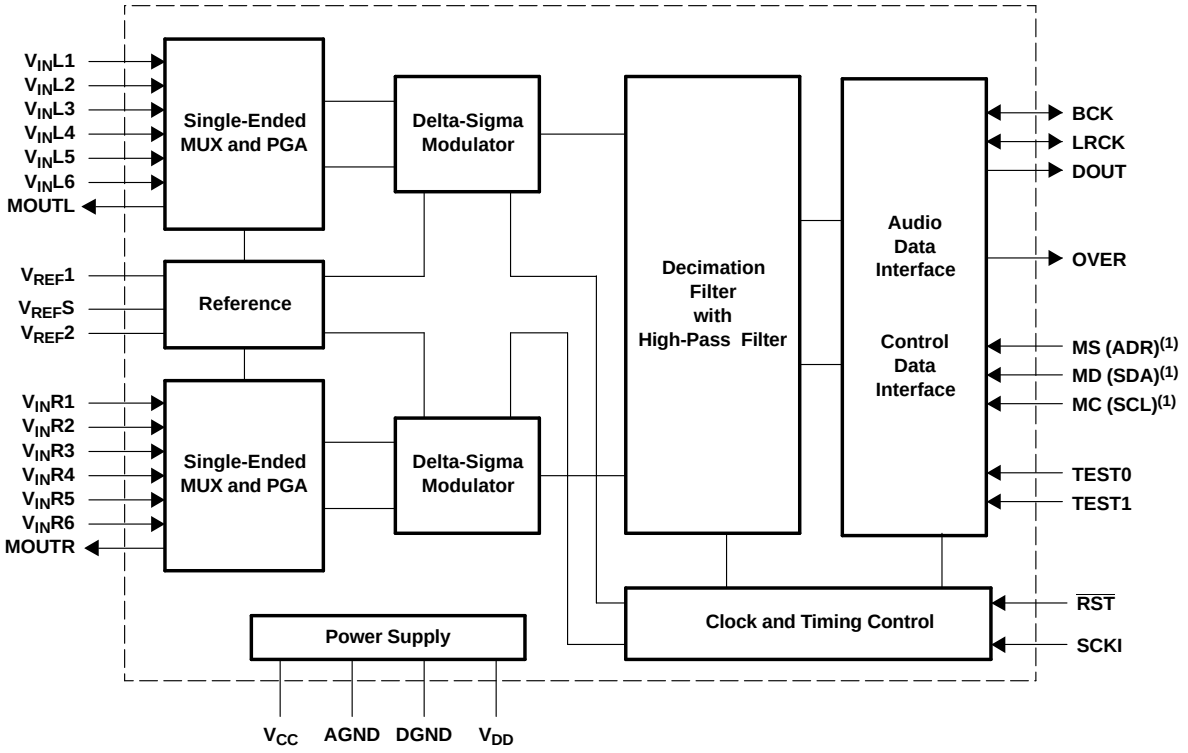
APPLICATIONS

- **DVD/HDD/DVD+HDD Recorder**
- **AV Amplifier Receiver**
- **CD Recorder**
- **MD Recorder**
- **Multitrack Recorder**
- **Electric Musical Instrument**

DESCRIPTION

The PCM1850A/1851A is a high-performance, low-cost, single-chip stereo analog-to-digital converter with a single-ended analog front end that consists of a 6-stereo-input multiplexer and wide-range PGA. The PCM1850A/1851A includes a delta-sigma modulator with 64-times oversampling, a digital decimation filter and a low-cut filter that removes the dc component of the input signal. For various applications, the PCM1850A/1851A supports two modes (master and slave) and four data formats through a serial control interface, SPI for the PCM1850A and I^2C for the PCM1851A. The PCM1850A/1851A is suitable for a wide variety of cost-sensitive DVD/CD/MD recorder and receiver applications where good performance and operation from a 5-V analog supply and 3.3-V digital supply is required. The PCM1850A/1851A is fabricated using a highly advanced CMOS process and is available in a small 32-pin TQFP package.

BLOCK DIAGRAM



(1) PCM1850A (PCM1851A)

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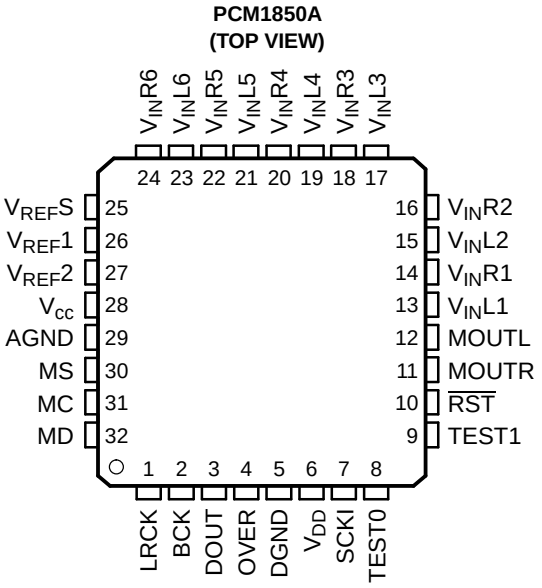
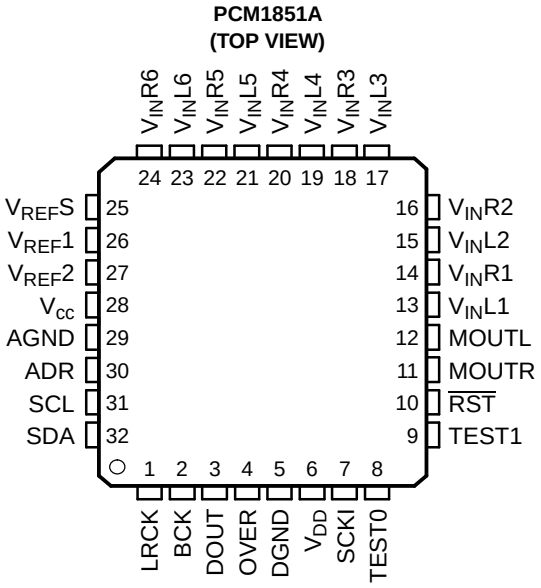
PIN ASSIGNMENTS





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TERMINAL FUNCTIONS

PCM1850A

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	29	—	Analog GND
BCK	2	I/O	Bit clock input/output(1)
DGND	5	—	Digital GND
DOUT	3	O	Audio data output
LRCK	1	I/O	Sampling clock input/output(1)
MC	31	I	Mode-control clock input(2)
MD	32	I	Mode-control data input(2)
MOUTL	12	O	Multiplexer output, L-channel
MOUTR	11	O	Multiplexer output, R-channel
MS	30	I	Mode-control select input(3)
OVER	4	O	Overflow flag
$\overline{RST}$	10	I	Reset, active-LOW(3)
SCKI	7	I	System clock input; 256 f_S, 384 f_S, 512 f_S, or 768 f_S(2)
TEST0	8	I	Test 0, must be connected to GND(3)
TEST1	9	I	Test 1, must be connected to GND(3)
V_{CC}	28	—	Analog power supply, 5-V
V_{DD}	6	—	Digital power supply, 3.3-V
$V_{IN}L1$	13	I	Analog input 1, L-channel
$V_{IN}L2$	15	I	Analog input 2, L-channel
$V_{IN}L3$	17	I	Analog input 3, L-channel
$V_{IN}L4$	19	I	Analog input 4, L-channel
$V_{IN}L5$	21	I	Analog input 5, L-channel
$V_{IN}L6$	23	I	Analog input 6, L-channel
$V_{IN}R1$	14	I	Analog input 1, R-channel
$V_{IN}R2$	16	I	Analog input 2, R-channel
$V_{IN}R3$	18	I	Analog input 3, R-channel
$V_{IN}R4$	20	I	Analog input 4, R-channel
$V_{IN}R5$	22	I	Analog input 5, R-channel
$V_{IN}R6$	24	I	Analog input 6, R-channel
$V_{REF}S$	25	—	Reference S decoupling capacitor (= 0.5 V_{CC})
$V_{REF}1$	26	—	Reference 1 decoupling capacitor (= 0.5 V_{CC})
$V_{REF}2$	27	—	Reference 2 decoupling capacitor (= V_{CC})

(1) Schmitt-trigger input with internal pulldown resistor (50 kΩ, typically)
(2) Schmitt-trigger input, 5-V tolerant
(3) Schmitt-trigger input with internal pulldown resistor (50 kΩ, typically), 5-V tolerant

PCM1851A

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADR	30	I	Mode control address select input(1)
AGND	29	—	Analog GND
BCK	2	I/O	Bit clock input/output(2)
DGND	5	—	Digital GND
DOUT	3	O	Audio data output
LRCK	1	I/O	Sampling clock input/output(2)
MOUTL	12	O	Multiplexer output, L-channel
MOUTR	11	O	Multiplexer output, R-channel
OVER	4	O	Overflow flag
$\overline{RST}$	10	I	Reset, active-LOW(1)
SCKI	7	I	System clock input; 256 f_S, 384 f_S, 512 f_S, or 768 f_S(3)
SCL	31	I	Mode-control clock input(3)
SDA	32	I/O	Mode-control data input/output(4)
TEST0	8	I	Test 0, must be connected to GND(1)
TEST1	9	I	Test 1, must be connected to GND(1)
V_{CC}	28	—	Analog power supply, 5-V
V_{DD}	6	—	Digital power supply, 3.3-V
$V_{IN}L1$	13	I	Analog input 1, L-channel
$V_{IN}L2$	15	I	Analog input 2, L-channel
$V_{IN}L3$	17	I	Analog input 3, L-channel
$V_{IN}L4$	19	I	Analog input 4, L-channel
$V_{IN}L5$	21	I	Analog input 5, L-channel
$V_{IN}L6$	23	I	Analog input 6, L-channel
$V_{IN}R1$	14	I	Analog input 1, R-channel
$V_{IN}R2$	16	I	Analog input 2, R-channel
$V_{IN}R3$	18	I	Analog input 3, R-channel
$V_{IN}R4$	20	I	Analog input 4, R-channel
$V_{IN}R5$	22	I	Analog input 5, R-channel
$V_{IN}R6$	24	I	Analog input 6, R-channel
$V_{REF}S$	25	—	Reference S decoupling capacitor (= 0.5 V_{CC})
$V_{REF}1$	26	—	Reference 1 decoupling capacitor (= 0.5 V_{CC})
$V_{REF}2$	27	—	Reference 2 decoupling capacitor (= V_{CC})

(1) Schmitt-trigger input with internal pulldown resistor (50 kΩ, typically), 5-V tolerant
(2) Schmitt-trigger input with internal pulldown resistor (50 kΩ, typically)
(3) Schmitt-trigger input, 5-V tolerant
(4) Schmitt-trigger input/open-drain LOW output, 5-V tolerant

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage	–0.3 to 6.5	V
V_{DD}		–0.3 to 4	V
	Ground voltage differences: AGND, DGND	±0.1	V
	Digital input voltage: LRCK, BCK, DOUT, OVER	–0.3 to (V_{DD} + 0.3) < 4	V
	Digital input voltage: $\overline{RST}$, SCKI, MS (ADR)(2), MC (SCL)(2), MD (SDA)(2), TEST0, TEST1	–0.3 to 6.5	V
	Analog input voltage: V_{IN}L1–6, V_{IN}R1–6	–3 to (V_{CC} + 3) < 9	V
	Analog input voltage: MOUTL, MOUTR, V_{REF}1, V_{REF}2, V_{REF}S	–0.3 to (V_{CC} + 0.3) < 6.5	V
	Input current (any pins except supplies)	±10	mA
	Ambient temperature under bias	–40 to 125	°C
	Storage temperature	–55 to 150	°C
	Junction temperature	150	°C
	Lead temperature (soldering)	260°C, 5 s	
	Package temperature (IR reflow, peak)	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) PCM1850A (PCM1851A)

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		4.5	5	5.5	V
V_{DD}	Digital supply voltage		2.7	3.3	3.6	V
	Analog input voltage, full scale (0 dB)	V_{CC} = 5 V, PGA gain = 5.5 dB		2		Vrms
	Digital input logic family			TTL		
	Digital input clock frequency	System clock	4.096		49.152	MHz
		Sampling clock	16		96	kHz
	Digital output load capacitance				20	pF
T_A	Operating free-air temperature		40		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1850APJT, PCM1851APJT			UNIT
			MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT — DATA FORMAT						
	Audio data interface format		Left-justified, I²S, right-justified			
	Audio data bit length			16, 24		bits
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency		16	48	96	kHz
	System clock frequency	256 f_S	4.096	12.288	24.576	MHz
		384 f_S	6.144	18.432	36.864	
		512 f_S	8.192	24.576	49.152	
		768 f_S	12.288	36.864	–	

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1850APJT, PCM1851APJT			UNIT
			MIN	TYP	MAX	
INPUT LOGIC						
V_{IH} (1)	Input logic level		2		V_{DD}	VDC
V_{IL} (1)			0		0.8	
V_{IH} (2)(3)			2		5.5	
V_{IL} (2)(3)			0		0.8	
I_{IH} (2)	Input logic current	$V_{IN} = V_{DD}$			±10	µA
I_{IL} (2)		V_{IN} = 0			±10	
I_{IH} (1)(3)		$V_{IN} = V_{DD}$		65	100	
I_{IL} (1)(3)		V_{IN} = 0			±10	
OUTPUT LOGIC						
V_{OH} (4)	Output logic level	I_{OUT} = –4 mA	2.8			VDC
V_{OL} (4)(5)		I_{OUT} = 4 mA			0.5	
AFE MULTPLEXER						
	Input channels			6		
	Input level for full scale			2	2.4	Vrms
	Center voltage (V_{REF}1)	Selected channel		0.5 V_{CC}		V
	Center voltage (V_{REF}S)	Unselected channel		0.5 V_{CC}		V
	Input impedance	Selected channel	50	169		kΩ
		Unselected channel	50	57		
AFE PGA						
	Gain range		–11	0	11	dB
	Gain step			0.5		dB
	Monotonicity			Specified		
	Antialiasing filter frequency response	–3 dB, PGA gain = –5.5 dB		300		kHz
MONITOR OUTPUT						
	Output level for full scale	AC-coupled, >10 kΩ		0.6 V_{CC}		Vp-p
	Output load	AC-coupled	10			kΩ
	THD+N (6)(7)	AC-coupled, 10 kΩ, 3 Vp-p output		0.0016%		
S/N	Signal-to-noise ratio (6)(7)	AC-coupled, 10 kΩ		104		dB
	Gain error (6)(7)	AC-coupled, 10 kΩ		–3		% of FSR
	Center voltage			0.5 V_{CC}		V
ADC						
	Resolution			24		bits
	Full-scale input voltage			0.6 V_{CC}		Vp-p

(1) Pins 1, 2: LRCK, BCK (In slave mode, Schmitt-trigger input, with 50-kΩ typical pulldown resistor)
(2) Pins 7, 31, 32: SCKI, MC/SCL (PCM1850A/1851A), MD/SDA (PCM1850A/1851A) (Schmitt-trigger input, 5-V tolerant)
(3) Pins 8–10, 30: TEST0, TEST1, RST, MS/ADR (PCM1850A/1851A) (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)
(4) Pins 1–4: LRCK, BCK (in master mode), DOUT, OVER
(5) Pin 32: SDA (PCM1851A) (open-drain LOW output)
(6) Analog performance specifications are tested with the System Two™ audio measurement system by Audio Precision™, using a 400-Hz HPF and 20-kHz LPF in the RMS mode at f_{IN} = 1 kHz.
(7) Reference level (0 dB) is specified as 2-V rms input on V_{IN}L[1:6] and V_{IN}R[1:6] pins with PGA gain of –5.5 dB.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1850APJT, PCM1851APJT			UNIT
			MIN	TYP	MAX	
ACCURACY						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±2	±5	% of FSR
	Bipolar zero error	High-pass filter bypass		±2		% of FSR
DYANAMIC PERFORMANCE (1) (2)						
THD+N	Total harmonic distortion + noise (3)	f_S = 48 kHz, V_{IN} = –0.5 dB (1.89 Vrms)		0.0023%	0.004%	
		f_S = 96 kHz (4), V_{IN} = –0.5 dB (1.89 Vrms)		0.0027%		
		f_S = 48 kHz, V_{IN} = –60 dB (2 mVrms)		1%		
		f_S = 96 kHz (4), V_{IN} = –60 dB (2 mVrms)		1%		
	Dynamic range (3)	f_S = 48 kHz, A-weighted	96	102		dB
		f_S = 96 kHz (4), A-weighted		102		
S/N	Signal-to-noise ratio (3)	f_S = 48 kHz, A-weighted	96	101		dB
		f_S = 96 kHz (4), A-weighted		102		
	Channel separation (between L-ch and R-ch) (3)	f_S = 48 kHz	92	98		dB
		f_S = 96 kHz (4)		100		
	Channel separation (among channels) (5)	f_S = 48 kHz	90	96		dB
		f_S = 96 kHz (4)		96		
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
	Delay time			17.4/f_S		s
	HPF frequency response	–3 dB		0.019 f_S		mHz

(1) Analog performance specifications are tested with the System Two™ audio measurement system by Audio Precision™, using a 400-Hz HPF and 20-kHz LPF in the RMS mode at f_{IN} = 1 kHz.
(2) Reference level (0 dB) is specified as 2-V rms input on V_{IN}L[1:6] and V_{IN}R[1:6] pins with PGA gain of –5.5 dB.
(3) Unselected channel inputs are terminated to AGND with 0.33 µF.
(4) f_S = 96 kHz, system clock = 256 f_S.
(5) 2-V rms input is applied to all unselected channels, and input of selected channel is terminated to AGND with 0.33 µF.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1850APJT, PCM1851APJT			UNIT
			MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	VDC
V_{DD}			2.7	3.3	3.6	
I_{CC}	Supply current (1)	Operational		28	35	mA
		Powered down (2)		190		µA
I_{DD}		f_S = 48 kHz		6	10	mA
		f_S = 96 kHz (3)		12		
		Powered down (2), PCM1850A		80		µA
		Powered down (2), PCM1851A		280		
	Power dissipation	Operating, f_S = 48 kHz		160	208	mW
		Operating, f_S = 96 kHz (3)		180		
		Powered down (2), PCM1850A		1.2		
		Powered down (2), PCM1851A		1.9		
TEMPERATURE RANGE						
	Operation temperature		–40		85	°C
	Thermal resistance (θ_{JA})			80		°C/W

(1) Minimum load on DOUT (pin 3), BCK (pin 2), LRCK (pin 1)
(2) Halt SCKI, BCK, LRCK.
(3) f_S = 96 kHz, system clock = 256 f_S.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted).

DIGITAL FILTER

Decimation Filter Frequency Response

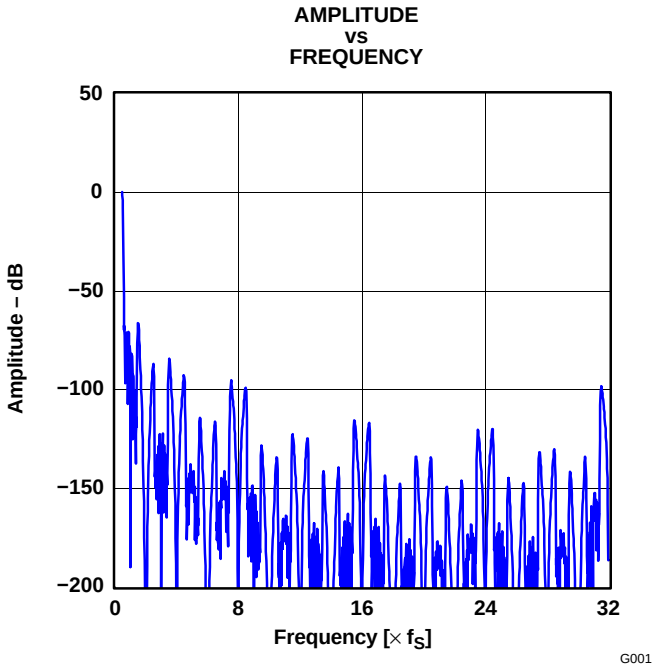


Figure 1. Overall Characteristics

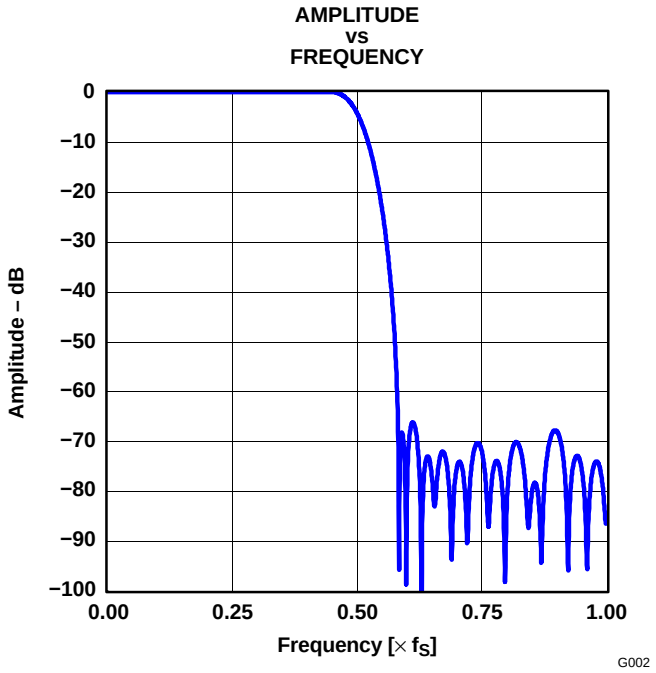


Figure 2. Stop-Band Attenuation Characteristics

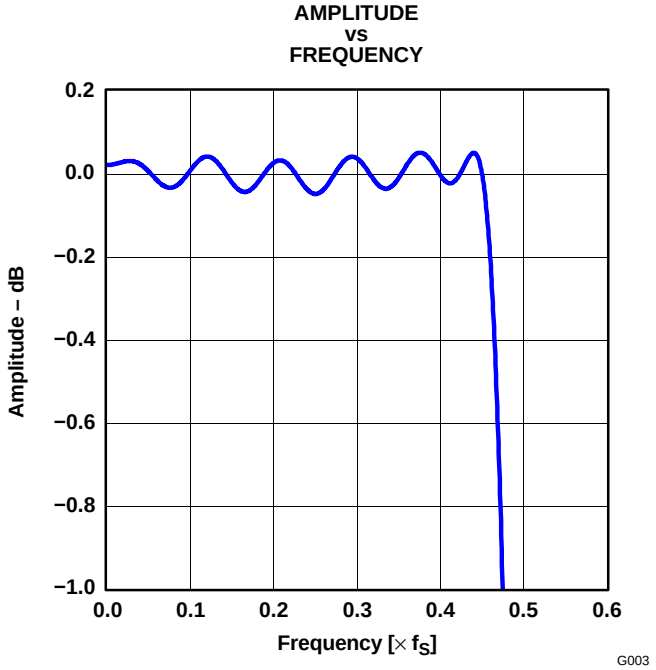


Figure 3. Pass-Band Ripple Characteristics

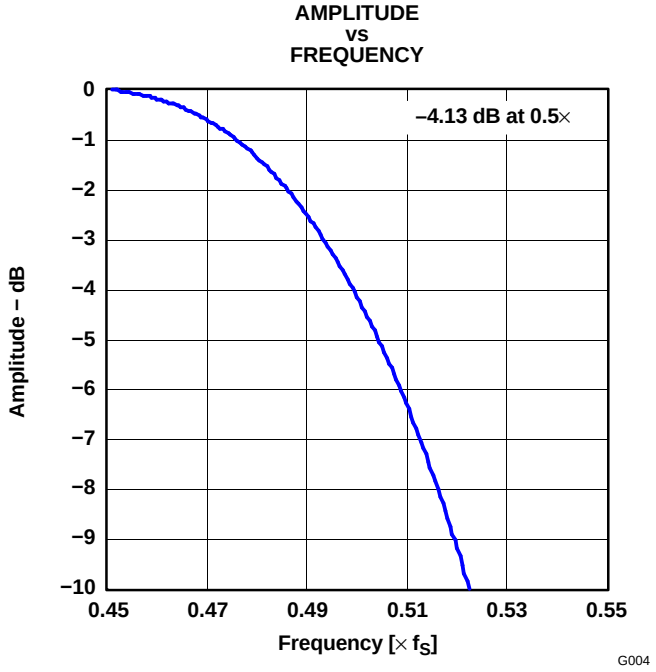


Figure 4. Transition-Band Characteristics

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTER (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted).

High-Pass Filter Frequency Response

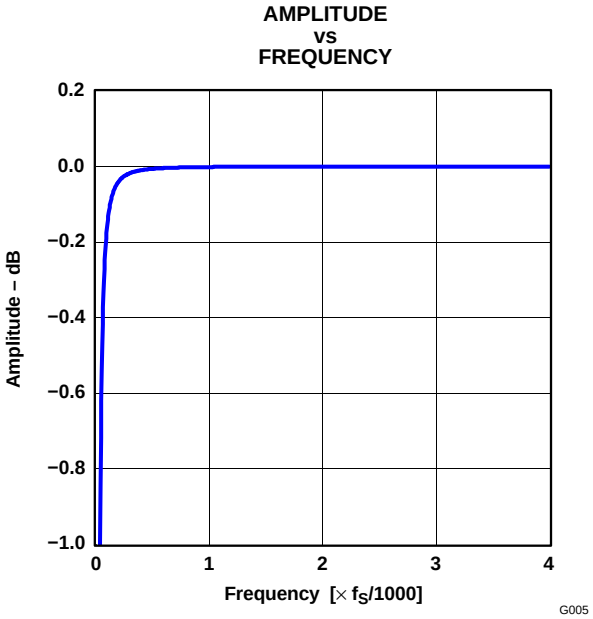


Figure 5. HPF Pass-Band Characteristics

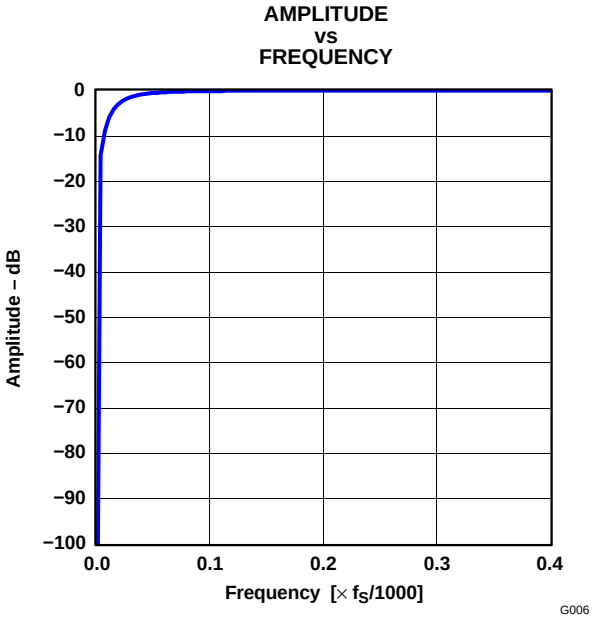


Figure 6. HPF Stop-Band Characteristics

ANALOG FILTER

Antialiasing Filter Frequency Response (at PGA Gain = –5.5 dB)

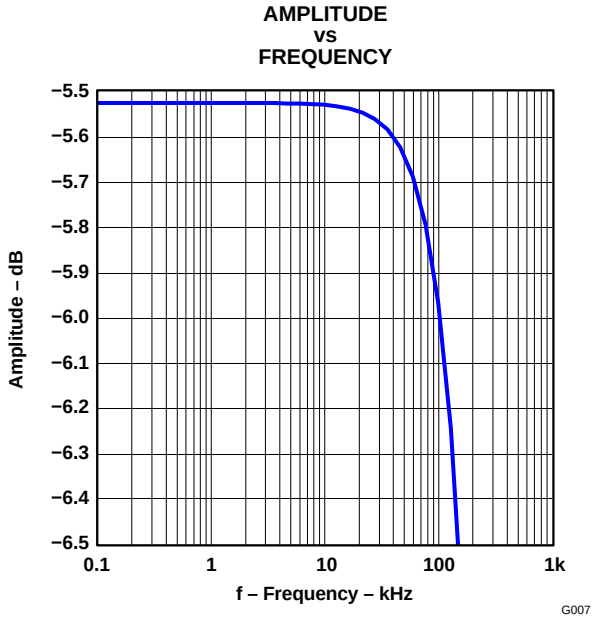


Figure 7. Antialiasing Filter Pass-Band Characteritics

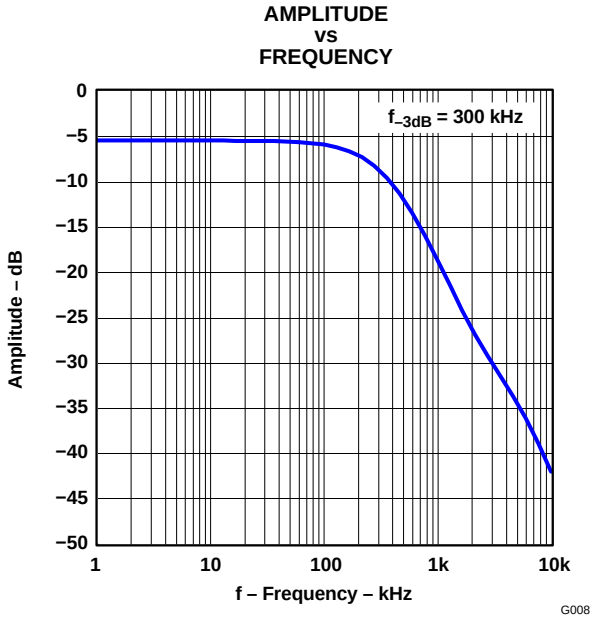


Figure 8. Antialiasing Filter Stop-Band Characteritics

TYPICAL PERFORMANCE CURVES AT PGA GAIN = –5.5 dB

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted).

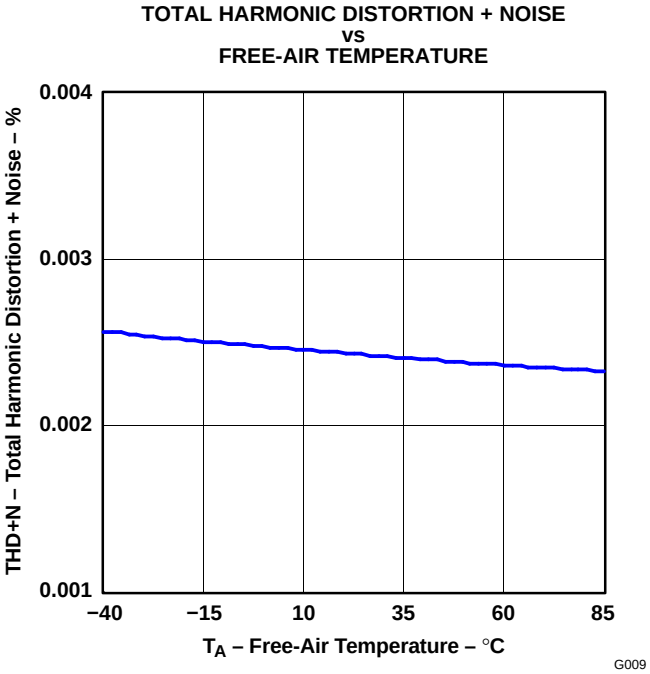


Figure 9.

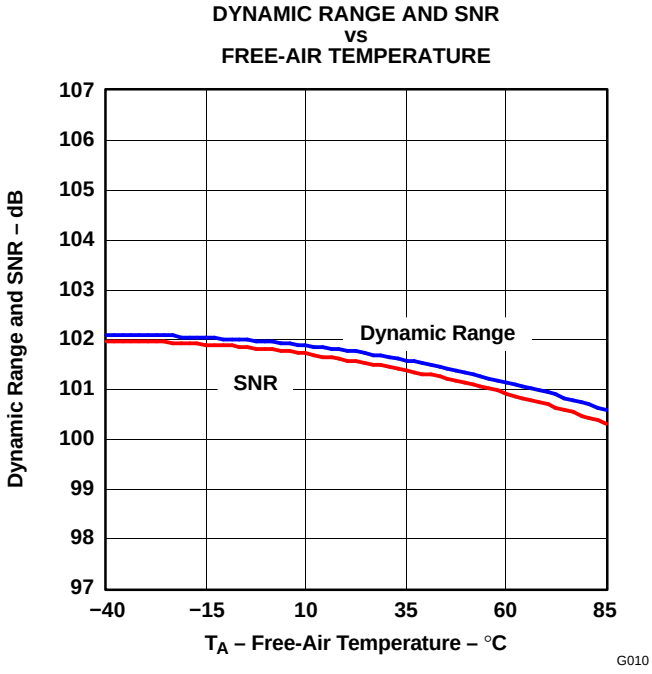


Figure 10.

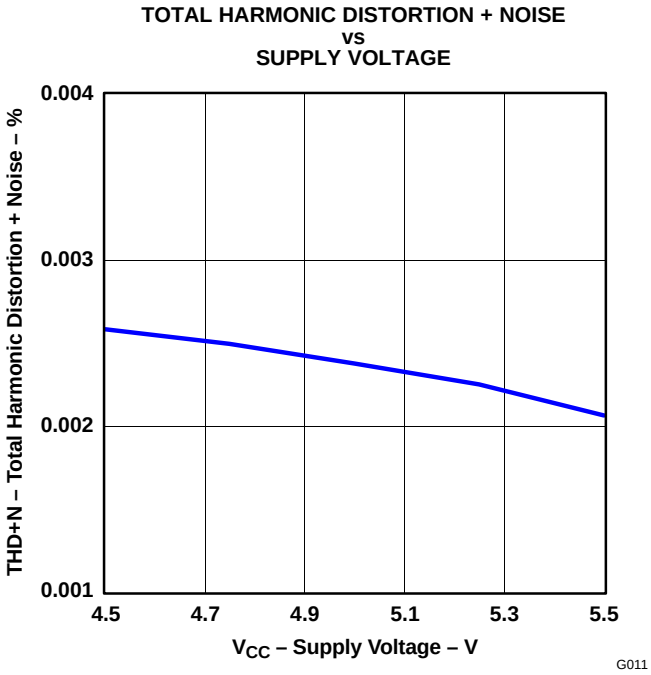


Figure 11.

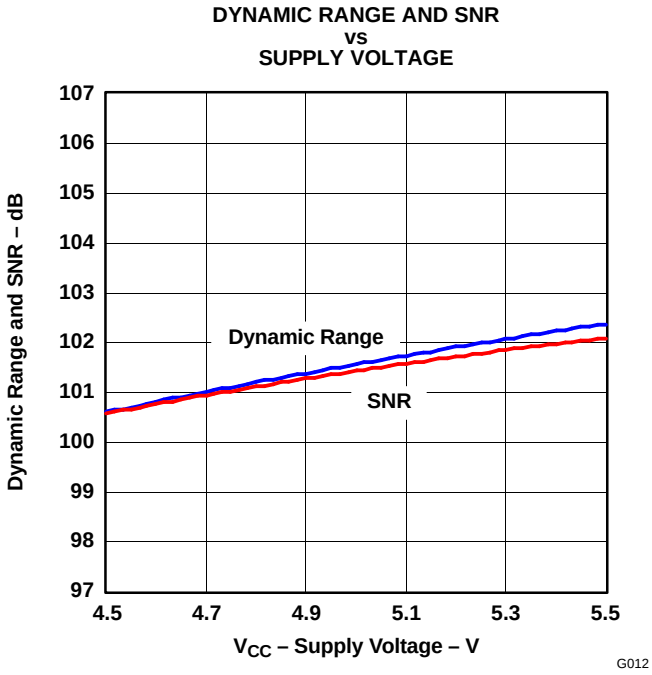


Figure 12.

TYPICAL PERFORMANCE CURVES AT PGA GAIN = –5.5 dB (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted).

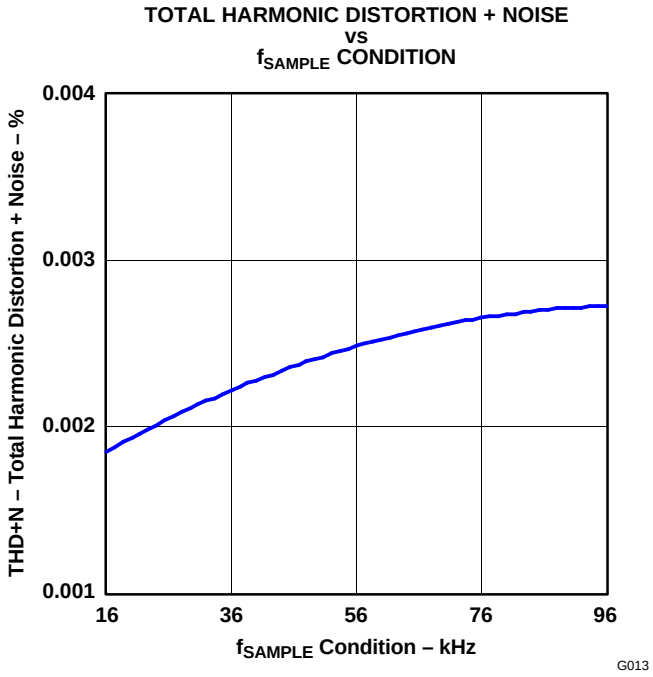


Figure 13.

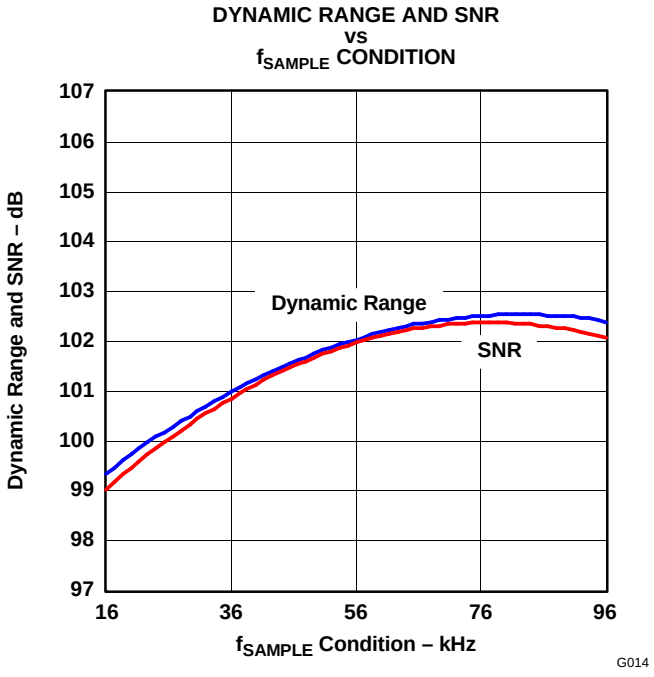


Figure 14.

OUTPUT SPECTRUM

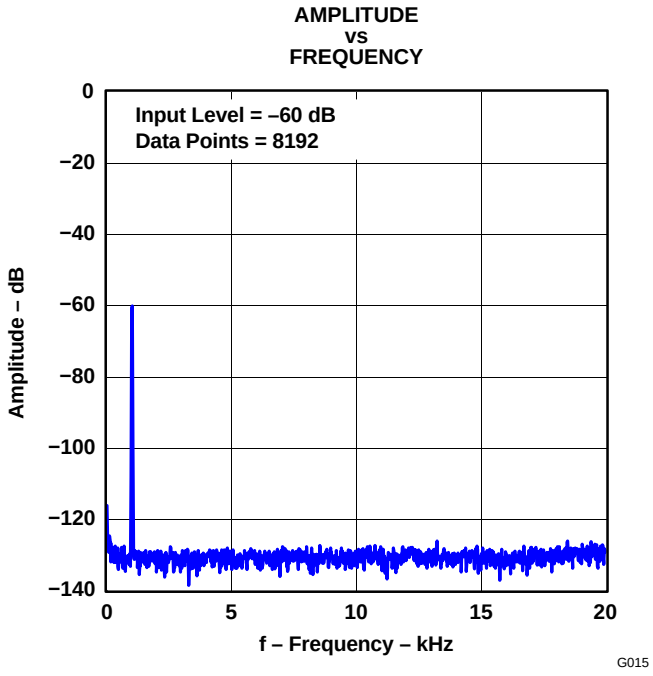


Figure 15.

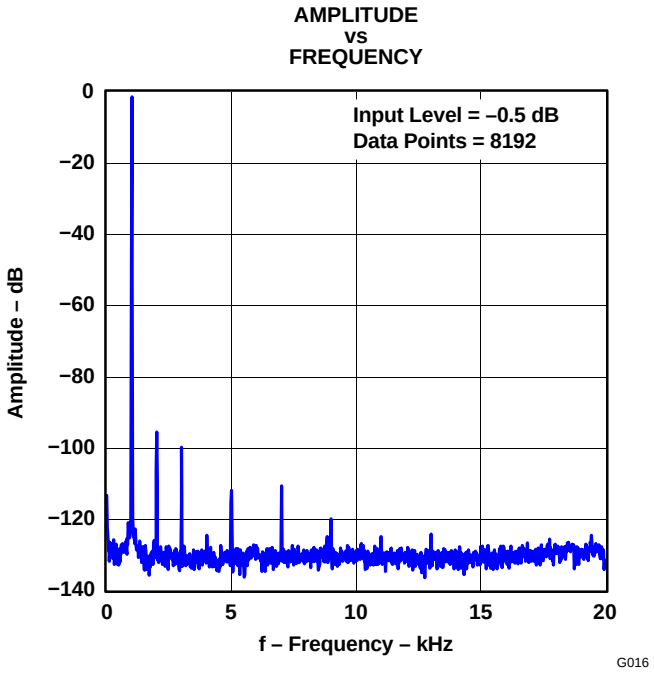


Figure 16.

TYPICAL PERFORMANCE CURVES AT PGA GAIN = –5.5 dB (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 48 kHz, system clock = 256 f_S, 24-bit data (unless otherwise noted).

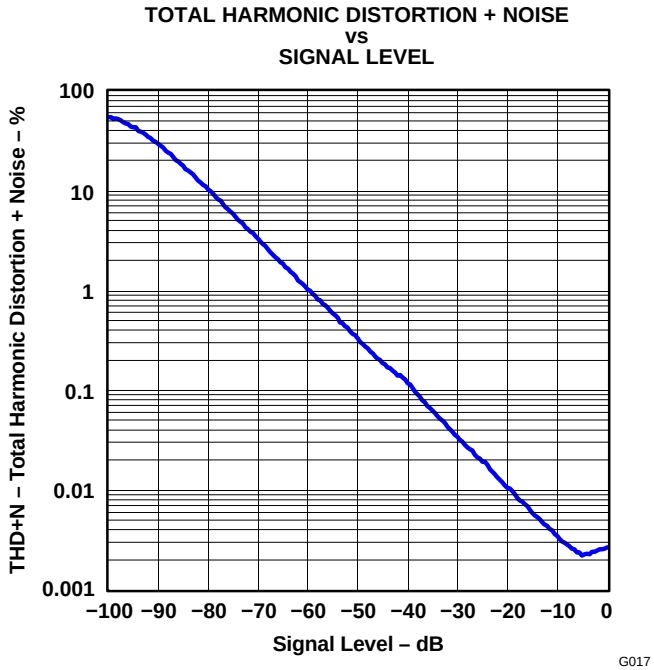


Figure 17.

SUPPLY CURRENT

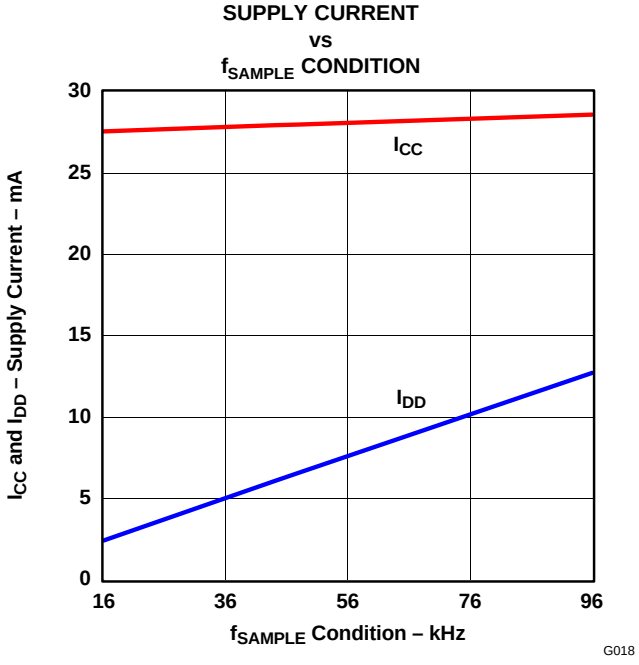


Figure 18.

PGA GAIN LINEARITY

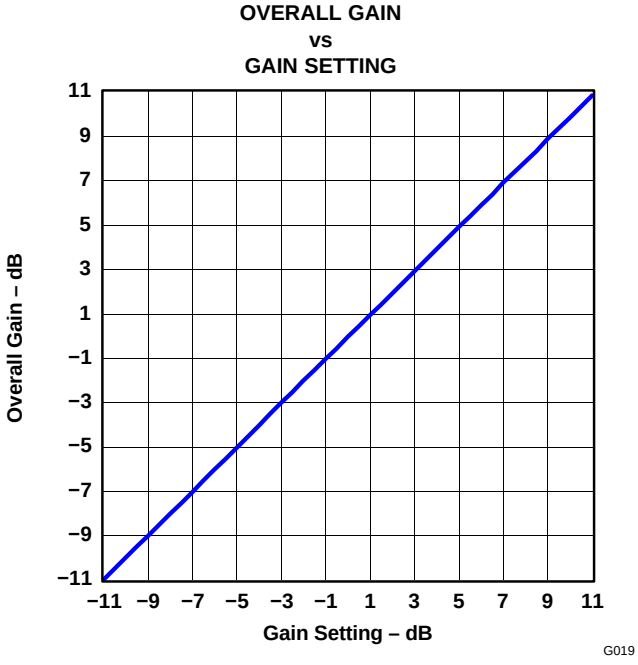


Figure 19.

DETAILED DESCRIPTION

SYSTEM CLOCK

The PCM1850A/1851A supports 256 f_S, 384 f_S, 512 f_S, and 768 f_S as the system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 7).

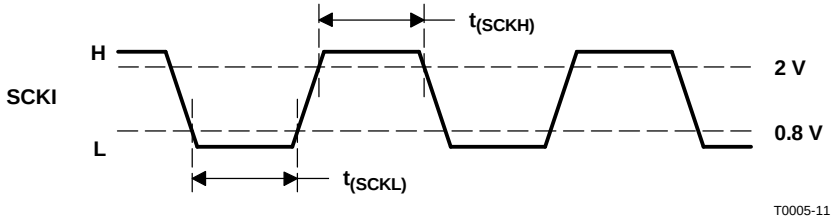
The PCM1850A/1851A has a system clock detection circuit which automatically senses if the system clock is operating at 256 f_S, 384 f_S, 512 f_S, or 768 f_S in slave mode. In master mode, the system clock frequency must be selected by mode control via the serial port. The 768-f_S system clock is not available in master mode or for f_S = 88.2 kHz and 96 kHz in the slave mode. The system clock is divided into 128 f_S and 64 f_S automatically, and these frequencies are used to operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows the relationship of typical sampling frequency to system clock frequency, and Figure 20 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)			
	256 f_S	384 f_S	512 f_S	768 f_S(1)
32	8.192	12.288	16.384	24.576
44.1	11.2896	16.9344	22.5792	33.8688
48	12.288	18.432	24.576	36.864
64	16.384	24.576	32.768	49.152
88.2	22.5792	33.8688	45.1584	—
96	24.576	36.864	49.152	—

(1) Slave mode only



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(SCKH)}$	System clock pulse duration, HIGH	8		ns
$t_{(SCKL)}$	System clock pulse duration, LOW	8		ns

Figure 20. System Clock Timing

POWER-ON-RESET SEQUENCE

The PCM1850A/1851A has an internal power-on-reset circuit, and initialization (reset) is performed automatically at the time that the power supply (V_{DD}) exceeds 2.2 V (typical). While V_{DD} < 2.2 V (typical) and for 1024 system clocks after V_{DD} > 2.2 V (typical), the PCM1850A/1851A stays in the reset state and the digital output is forced to zero. The digital output is valid after the reset state is released and the time of 4500/f_S has passed. At the moment of the power-on-reset release, the PCM1850A/1851A does not need a system clock. Figure 21 illustrates the internal power-on-reset timing and the digital output for power-on reset.

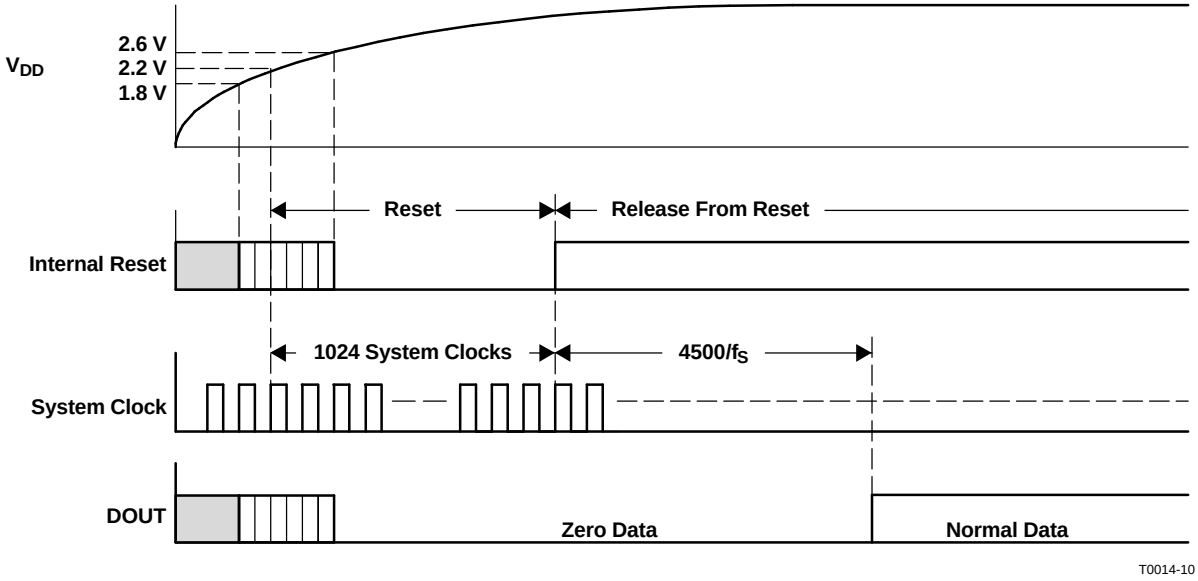


Figure 21. Internal Power-On-Reset Timing

ANALOG FRONT END

The PCM1850A/1851A has a built-in analog front-end circuit, which is shown in the block diagram of Figure 22. Selection of the multiplexer input and PGA gain is controlled by mode control via the serial port as shown in Table 2 and Table 3. The change of the input selection and the gain selection is performed immediately after the serial control packet for the change is sent. A popping noise or other unexpected transient response could be generated in the audio signal during channel and gain change. Because the PCM1850A/1851A has no zero-cross detection and no other buffering capability for channel and gain change, appropriate data handling in the digital domain is recommended to control transients.

The PCM1850A/1851A analog front end permits only ac input via an input capacitor; dc input is prohibited. A signal source resistance of less than 1 kΩ is recommended for the V_{IN}xx pins.

All unselected channel inputs are terminated V_{REF}S (= 0.5 V_{CC}) using a resistor, typically 57 kΩ.

The PCM1850A/1851A employs MOUTL/R pins (pins 12 and 11) to monitor the multiplexer output. The load on these pins must be ac-coupled and not less than 10 kΩ. The full-scale output level is typically 0.6 V_{CC}.

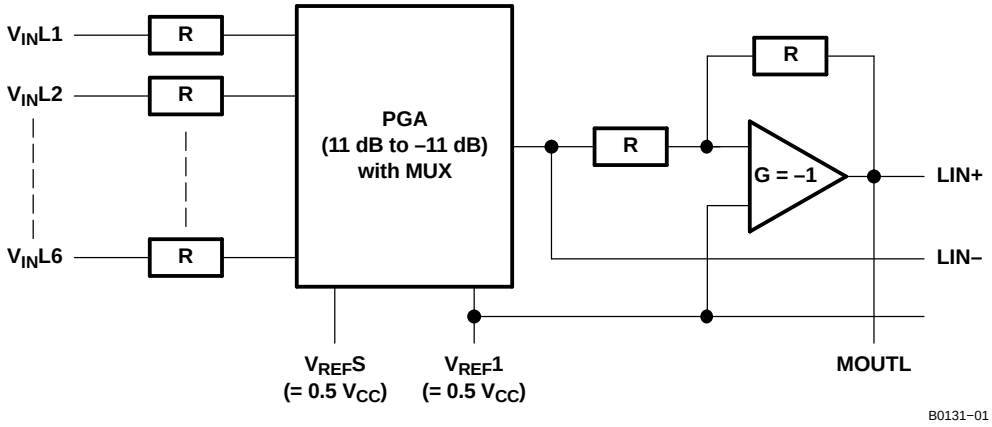


Figure 22. Analog Front-End Block Diagram (L-Channel)

Table 2. Multiplexer Input Selection

CH2	CH1	CH0	CHANNEL
0	0	0	Mute
0	0	1	Channel 1 (default)
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Mute

Table 3. PGA Gain Selection

PG5	PG4	PG3	PG2	PG1	PG0	PGA GAIN [dB]	R_{IN} [kΩ, Typical](1)
0	0	1	0	1	0	–11 (default)	201
0	0	1	0	1	1	–10.5	199
0	0	1	1	0	0	–10	196
0	0	1	1	0	1	–9.5	193
0	0	1	1	1	0	–9	190
0	0	1	1	1	1	–8.5	188
0	1	0	0	0	0	–8	185
0	1	0	0	0	1	–7.5	181
0	1	0	0	1	0	–7	178
0	1	0	0	1	1	–6.5	175
0	1	0	1	0	0	–6	172
0	1	0	1	0	1	–5.5	169
0	1	0	1	1	0	–5	165
0	1	0	1	1	1	–4.5	162
0	1	1	0	0	0	–4	158
0	1	1	0	0	1	–3.5	155
0	1	1	0	1	0	–3	151
0	1	1	0	1	1	–2.5	147
0	1	1	1	0	0	–2	144
0	1	1	1	0	1	–1.5	140
0	1	1	1	1	0	–1	136
0	1	1	1	1	1	–0.5	133
1	0	0	0	0	0	0	129
1	0	0	0	0	1	0.5	125
1	0	0	0	1	0	1	122
1	0	0	0	1	1	1.5	118
1	0	0	1	0	0	2	114
1	0	0	1	0	1	2.5	111
1	0	0	1	1	0	3	107
1	0	0	1	1	1	3.5	103
1	0	1	0	0	0	4	100
1	0	1	0	0	1	4.5	96
1	0	1	0	1	0	5	93
1	0	1	0	1	1	5.5	89
1	0	1	1	0	0	6	86
1	0	1	1	0	1	6.5	83
1	0	1	1	1	0	7	80
1	0	1	1	1	1	7.5	77
1	1	0	0	0	0	8	73
1	1	0	0	0	1	8.5	70
1	1	0	0	1	0	9	68
1	1	0	0	1	1	9.5	65
1	1	0	1	0	0	10	62
1	1	0	1	0	1	10.5	59
1	1	0	1	1	0	11	57

(1) $R_{IN}(k\Omega, \text{typical}) = 258/(1 + 10^{GAIN/20})$
The PCM1850A/1851A becomes mute for PG[5:0] values other than those listed.

SERIAL AUDIO DATA INTERFACE

The PCM1850A/1851A interfaces with the audio system through BCK (pin 2), LRCK (pin 1), and DOUT (pin 3).

Interface Mode

The PCM1850A/1851A supports both master and slave modes as interface modes, and they are selected by mode control via the serial port as shown in Table 4.

In master mode, the PCM1850A/1851A provides the timing for serial audio data communications between the PCM1850A/1851A and the digital audio processor or external circuit. While in slave mode, the PCM1850A/1851A receives the timing for data transfer from an external controller.

Table 4. Interface Mode

MD1	MD0	INTERFACE MODE
0	0	Slave mode (256 f_S, 384 f_S, 512 f_S, 768 f_S) (default)
0	1	Master mode (256 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (512 f_S)

Master Mode

In master mode, BCK and LRCK work as output pins, and these pins are controlled by timing which is generated in the clock and timing control circuit of the PCM1850A/1851A. The frequency of BCK is fixed at 64 $\times$ LRCK. A 768-f_S system clock is not available in master mode.

Slave Mode

In slave mode, BCK and LRCK work as input pins. The PCM1850A/1851A accepts the 64 BCK/LRCK or 48 BCK/LRCK (only for 384 f_S SCKI) format. A 768-f_S system clock is not available for f_S = 88.2 kHz and 96 kHz in slave mode.

Data Format

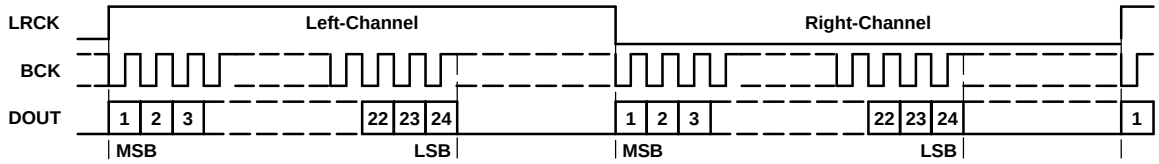
The PCM1850A/1851A supports four audio data formats in both master and slave modes, and they are selected by mode control via the serial port as shown in Table 5. Figure 23 illustrates the data formats in both slave and master modes.

Table 5. Data Format

FORMAT NO.	FMT2	FMT1	FMT0	FORMAT
0	1	0	1	Left-justified, 24-bit
1	1	0	0	I^2S, 24-bit, (default)
2	0	0	0	Right-justified, 24-bit
3	0	1	1	Right-justified, 16-bit

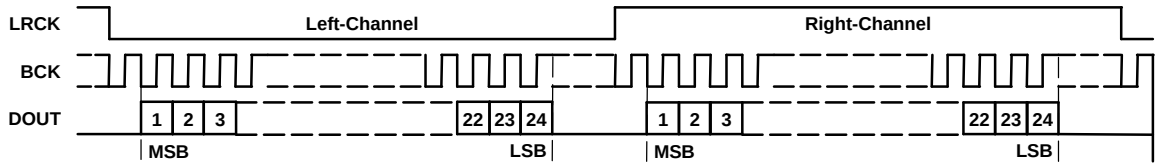
FORMAT 0: FMT[2:0] = 101b

24-Bit, MSB-First, Left-Justified



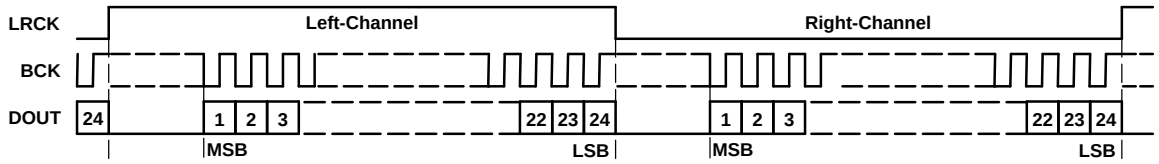
FORMAT 1: FMT[2:0] = 100b

24-Bit, MSB-First, I²S



FORMAT 2: FMT[2:0] = 000b

24-Bit, MSB-First, Right-Justified



FORMAT 3: FMT[2:0] = 011b

16-Bit, MSB-First, Right-Justified

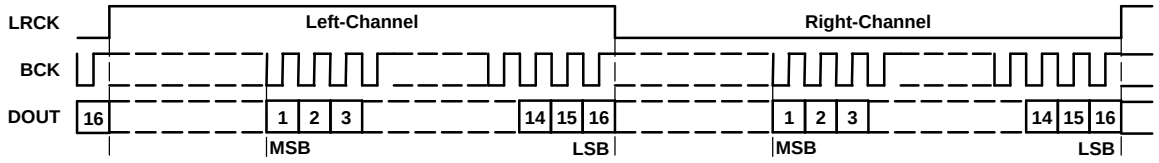


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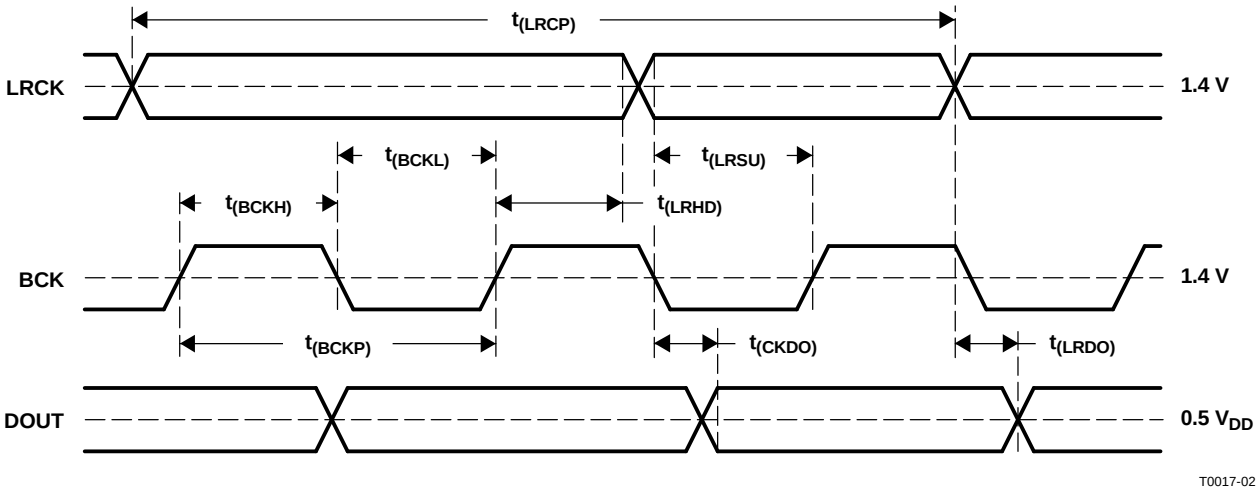
Figure 23. Audio Data Format
(LRCK, BCK Work as Inputs in Slave Mode and Outputs in Master Mode)

Interface Timing

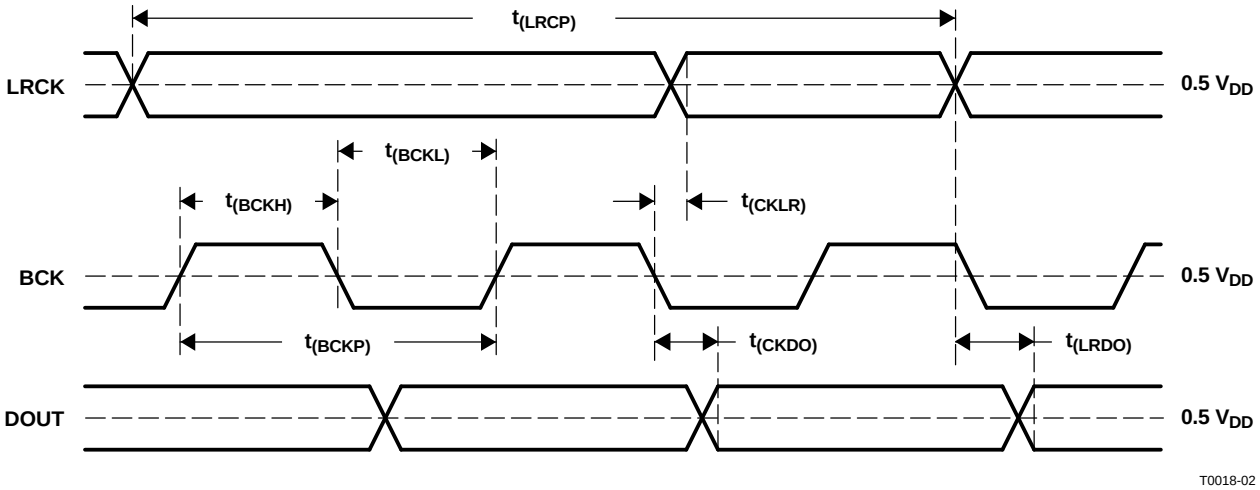
Figure 24 and Figure 25 illustrate the interface timing in slave and master modes, respectively.



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150			ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	60			ns
$t_{(BCKL)}$	BCK pulse duration, LOW	60			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	20			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	20			ns
$t_{(LRCP)}$	LRCK period	10			µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rise time of all signals			10	ns
t_f	Fall time of all signals			10	ns

NOTE: Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rise and fall times are measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT is 20 pF.

Figure 24. Audio Data Interface Timing (Slave Mode: LRCK, BCK Work as Inputs)



SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	1/(64 f_S)	1000	ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	60	0.5 $t_{(BCKP)}$	400	ns
$t_{(BCKL)}$	BCK pulse duration, LOW	60	0.5 $t_{(BCKP)}$	400	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	$1/f_S$	60	µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rise time of all signals			10	ns
t_f	Fall time of all signals			10	ns

NOTE: Timing measurement reference level is 0.5 V_{DD}. Rise and fall times are measured from 10% to 90% of IN/OUT signal swing. Load capacitance of all signals is 20 pF.

Figure 25. Audio Data Interface Timing (Master Mode: LRCK, BCK Work as Outputs)

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1850A/1851A operates under LRCK, synchronized with system clock SCKI. The PCM1850A/1851A does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCKs/frame (±5 BCKs for 48 BCKs/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within $1/f_S$ and digital output is forced into the BPZ code until resynchronization between LRCK and SCKI is completed.

In the case of changes less than ±5 BCKs for 64 BCKs/frame (±4 BCKs for 48 BCKs/frame), resynchronization with simultaneous discontinuity in the digital output does not occur.

Figure 26 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1850A/1851A might generate some noise in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal creates a discontinuity of data in the digital output, which could generate some noise in the audio signal.

It is recommended to set $\overline{\text{RST}}$ (pin 10) to LOW to get stable analog performance when the sampling rate, interface mode, or data format is changed.

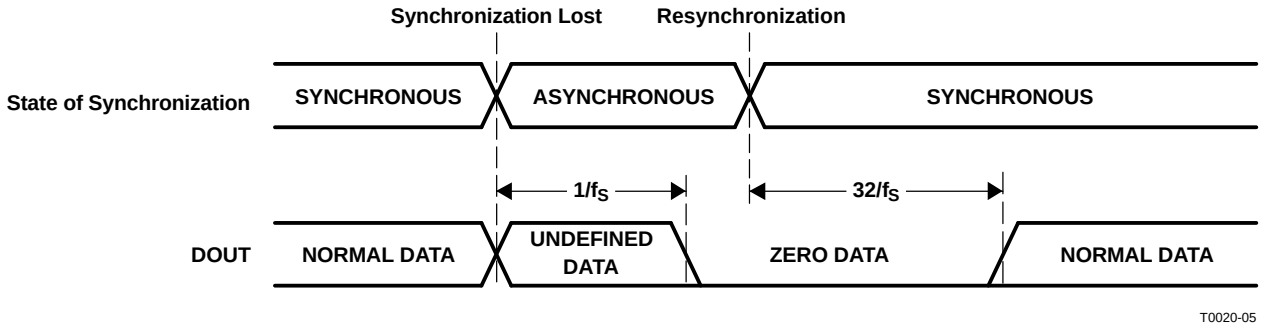


Figure 26. ADC Digital Output for Loss of Synchronization and Resynchronization

Power-Down Control

$\overline{\text{RST}}$ (pin 10) controls the entire ADC operation. During reset mode, the supply current of the analog section is shut off and the digital section is initialized. DOUT (pin 3) is also disabled. Halting SCKI, BCK, and LRCK is recommended to minimize power dissipation.

$\overline{\text{RST}}$	POWER-DOWN MODE
LOW	Reset and power-down modes
HIGH	Normal operation mode

Overflow Flag Output

The PCM1850A/1851A has an output flag (pin 4) that indicates when overflow occurs in the L-channel or R-channel, and this flag remains HIGH at least during the $8192/f_S$ time for a momentary overflow occurrence.

HPF Bypass Control

The built-in HPF function for dc component rejection can be bypassed via the serial port. In bypass mode, the dc component of the analog input signal, the internal dc offset, etc., are converted and included in the digital output data.

BYP	HPF (HIGH-PASS FILTER) MODE
0	Normal (no dc component on DOUT) mode (default)
1	Bypass (dc component on DOUT) mode

System Reset Control

The system reset control is used to resynchronize the system via the serial port when the system clock frequency, interface mode, and data format are changed. Change them while SRST = LOW. If they are changed during normal operation, analog performance can be degraded.

SRST	SYSTEM RESET
0	Resynchronization
1	Normal operation (default)

Mode Register Reset Control

The MRST bit is used to reset the mode control register to its default settings via the serial port.

MRST	MODE REGISTER RESET
0	Set default value
1	Normal operation (default)

SPI SERIAL CONTROL PORT FOR MODE CONTROL (PCM1850A)

The user-programmable built-in functions of the PCM1850A can be controlled through a serial control port with the SPI format. All operations for the serial control port use 16-bit data words. Figure 27 shows the control data word format. The most-significant bit must be set to 0. Seven bits, labeled IDX[6:0], set the register index (or address) for write operations. The least-significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 28 shows the functional timing diagram for writing to the serial control port. MS (pin 30) is held at a logic-1 state until a register needs to be written. To start the register write cycle, MS is set to logic-0. Sixteen clocks are then provided on MC (pin 31), corresponding to the 16 bits of the control data word on MD (pin 32). After the sixteenth clock cycle has completed, the data is latched into the indexed mode control register in the write operation. To write the next data word, MS must be set to 1 once.

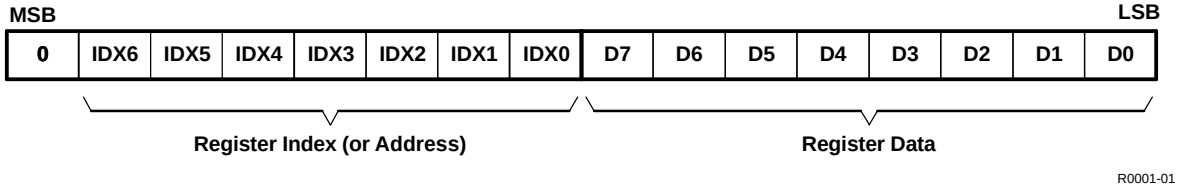


Figure 27. Control Data Word Format for MD

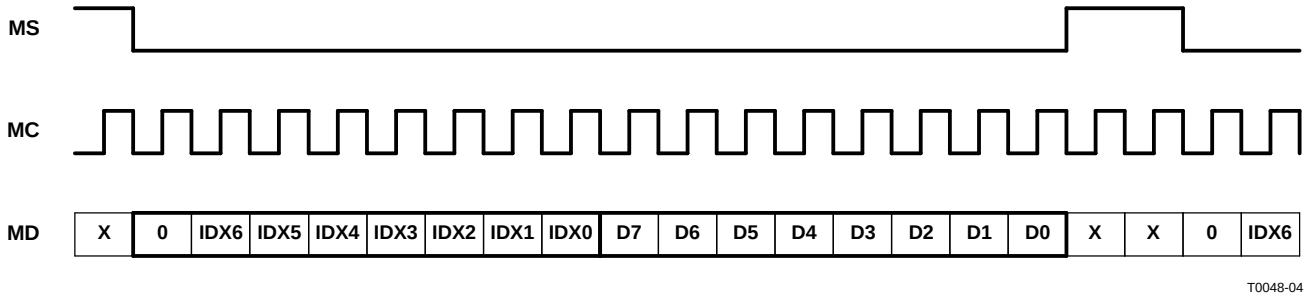
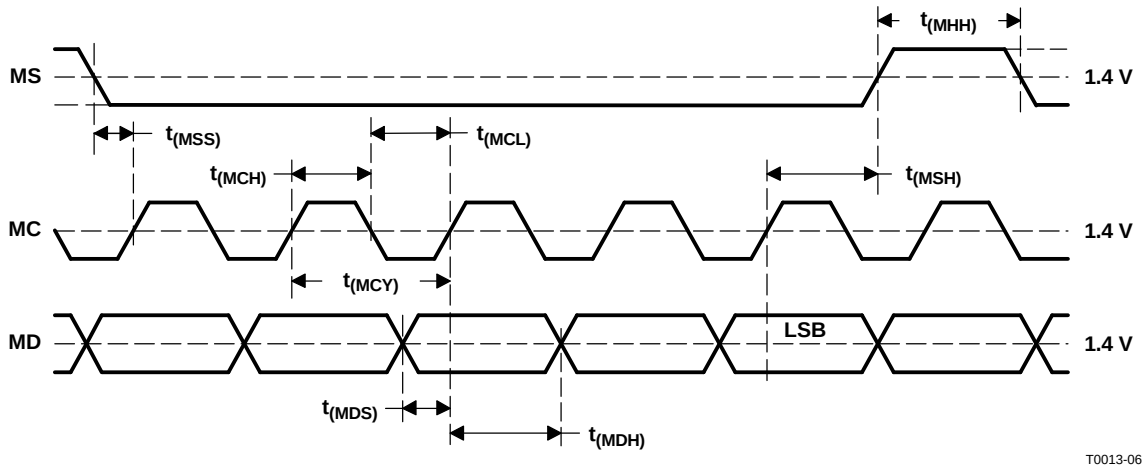


Figure 28. Serial Control Format

CONTROL INTERFACE TIMING REQUIREMENTS (PCM1850A)

Figure 29 shows a detailed timing diagram for the serial control interface of the PCM1850A. These timing parameters are critical for proper control port operation.



SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	100		ns
$t_{(MCL)}$	MC LOW-level time	40		ns
$t_{(MCH)}$	MC HIGH-level time	40		ns
$t_{(MHH)}$	MS HIGH-level time	80		ns
$t_{(MSS)}$	MS falling edge to MC rising edge	15		ns
$t_{(MSH)}$	MS hold time(1)	15		ns
$t_{(MDH)}$	MD hold time	15		ns
$t_{(MDS)}$	MD setup time	15		ns

(1) MC rising edge for LSB to MS rising edge

Figure 29. PCM1850A Control Interface Timing

I²C SERIAL CONTROL PORT FOR MODE CONTROL (PCM1851A)

The user-programmable built-in function of the PCM1851A can be controlled through the I²C-format serial control port, SDA (pin 32) and SCL (pin 31). The PCM1851A supports the I²C serial bus and the data transmission protocol for standard mode as a slave device. This protocol is explained in I²C specification 2.0.

Slave Address

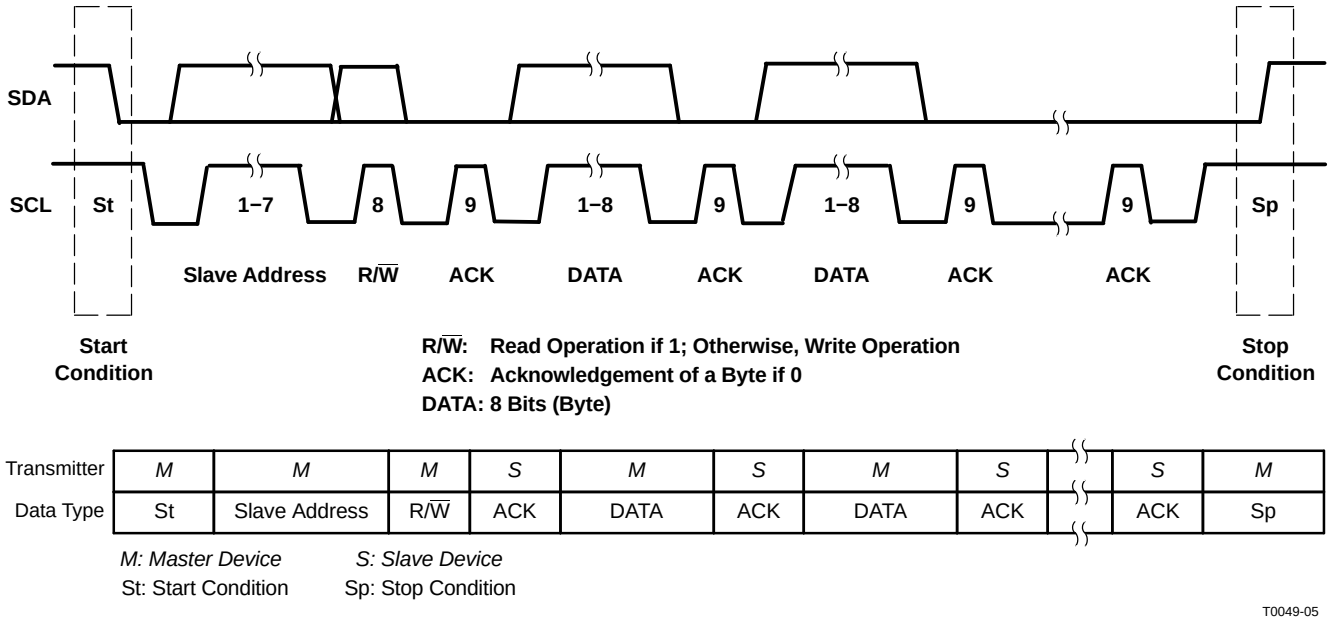
MSB LSB

1	0	0	1	0	1	ADR	R/nW

The PCM1851A has 7 bits for its own slave address. The first six bits (MSBs) of the slave address are factory preset to 100101. The last bit of the address byte is the device select bit, which can be user-defined by the ADR pin (pin 30). A maximum of two PCM1851As can be connected on the same bus at one time. Each PCM1851A responds when it receives its own slave address.

Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address with read/write bit, data if write or acknowledgement if read, and stop condition. The PCM1851A supports only slave receivers, so the R/$\overline{W}$ bit must be set to 0.



Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	Slave Address	R/W	ACK	DATA	ACK	DATA	ACK		ACK	Sp

M: Master Device *S: Slave Device*
St: Start Condition Sp: Stop Condition

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Figure 30. Basic I²C Framework

Write Operation

The PCM1851A has only the write mode. A master can write to any PCM1851A registers using single or multiple accesses. The master sends a PCM1851A slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by 1 automatically. When the index register reaches 33h, the next value is 31h. When undefined registers are accessed, the PCM1851A does not send an acknowledgement. Figure 31 is a diagram of the write operation. The register address and the write data are 8 bits and MSB-first format.

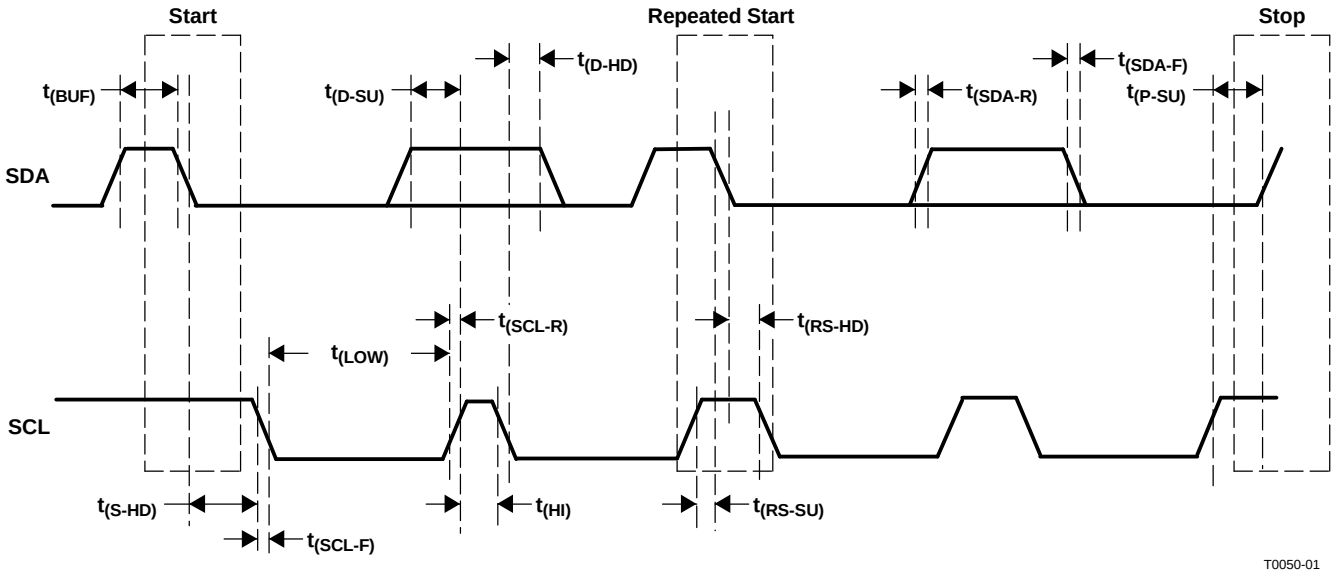
Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	Slave Address	W	ACK	Reg Address	ACK	Write Data 1	ACK	Write Data 2	ACK		ACK	Sp

M: Master Device *S: Slave Device*
St: Start Condition ACK: Acknowledge W: Write Sp: Stop Condition

R0002-03

Figure 31. Framework for Write Operation

TIMING DIAGRAM



SYMBOL	PARAMETER	MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency		100	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	4.7		µs
$t_{(LOW)}$	Low period of the SCL clock	4.7		µs
$t_{(HI)}$	High period of the SCL clock	4		µs
$t_{(RS-SU)}$	Setup time for START/repeated START condition	4.7		µs
$t_{(S-HD)}$, $t_{(RS-HD)}$	Hold time for START/repeated START condition	4		µs
$t_{(D-SU)}$	Data setup time	250		ns
$t_{(D-HD)}$	Data hold time	0	900	ns
$t_{(SCL-R)}$	Rise time of SCL signal	20 + 0.1 C_B	1000	ns
$t_{(SCL-F)}$	Fall time of SCL signal	20 + 0.1 C_B	1000	ns
$t_{(SDA-R)}$	Rise time of SDA signal	20 + 0.1 C_B	1000	ns
$t_{(SDA-F)}$	Fall time of SDA signal	20 + 0.1 C_B	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	4		µs
C_B	Capacitive load for SDA and SCL lines		400	pF
V_{NH}	Noise margin at HIGH level for each connected device (including hysteresis)	0.2 V_{DD}		V

Figure 32. PCM1851A Control Interface Timing Requirements

MODE CONTROL REGISTERS

User-Programmable Mode Control Functions

The PCM1850A/1851A has several user-programmable functions which are accessed via control registers. The registers are programmed using the serial control port which is discussed in the *SPI Serial Control Port for Mode Control (PCM1850A)* and *I^2C Serial Control Port for Mode Control (PCM1851A)* sections of this data sheet. Table 6 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table 7. Each register includes an index (or address) indicated by the IDX[6:0] bits B[14:8].

Table 6. User-Programmable Mode Control Functions

FUNCTION	RESET DEFAULT	REGISTER	BIT(S)
Mode register reset	Normal operation	31	MRST
PGA gain control	–11 dB	31	PG[5:0]
Multiplexer input channel control	Channel 1	32	CH[2:0]
HPF bypass control	HPF enable	33	BYP
System reset	Normal operation	33	SRST
Audio interface mode control	Slave	33	MD[1:0]
Audio interface format control	I^2S	33	FMT[2:0]

Table 7. Mode Control Register Map

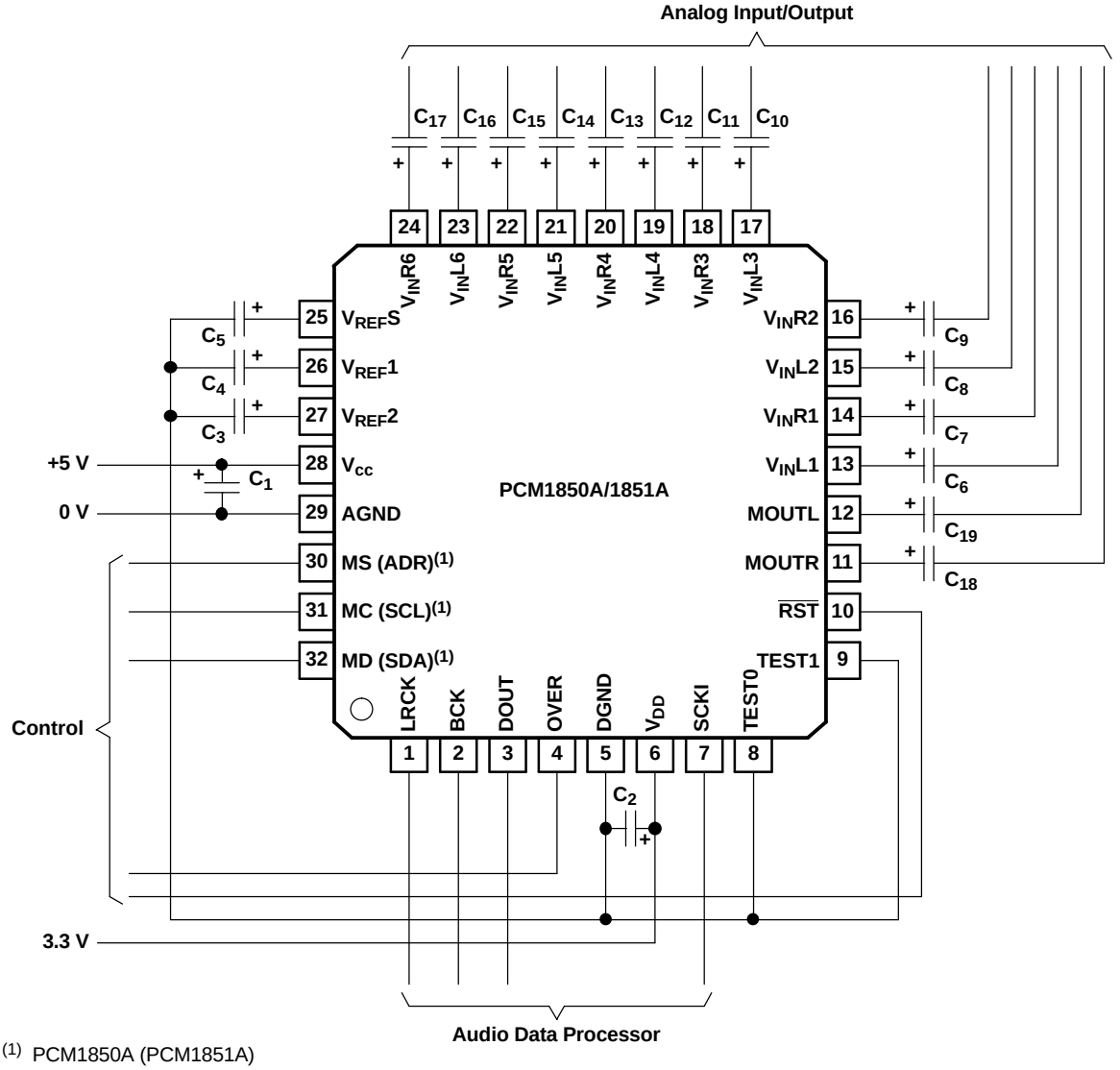
HEX	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 31	0	0	1	1	0	0	0	1	RSV(1)	MRST	PG5	PG4	PG3	PG2	PG1	PG0
Register 32	0	0	1	1	0	0	1	0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	CH2	CH1	CH0
Register 33	0	0	1	1	0	0	1	1	BYP	SRST	RSV(1)	MD1	MD0	FMT2	FMT1	FMT0

(1) RSV bits must be always written as 0. No values can be written in address 30h.

APPLICATION INFORMATION

TYPICAL CIRCUIT CONNECTION DIAGRAM

The following figure illustrates a typical circuit connection diagram for six stereo inputs and an analog monitor.



(1) PCM1850A (PCM1851A)

S0181-01

NOTE: C_1, C_2: 0.1-µF ceramic and 10-µF electrolytic capacitors are recommended, depending on layout and power supply.
C_3, C_4, C_5: 0.1-µF ceramic and 10-µF electrolytic capacitors are recommended.
C_6–C_{17}: A 0.33-µF capacitor gives a 2.9-Hz (τ = 0.33 µF × 169 kΩ) typical cutoff frequency at the HPF input in normal operation, and it requires power-on settling time with a 56-ms time constant in the power-on initialization period. Cutoff frequency and time constant depend on PGA gain. Cutoff frequency varies from 2.4 Hz to 8.5 Hz for 0.33 µF. DC-coupled input is inhibited for the analog input, V_{IN}L[1:6] and V_{IN}R[1:6].
C_{18}–C_{19}: A 2.2-µF capacitor with a 10-kΩ load gives a 7.2-Hz cutoff frequency.

APPLICATION INFORMATION (continued)

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} Pins

The digital and analog power supply lines to the PCM1850A/1851A must be bypassed to the corresponding ground pins with 0.1-μF ceramic and 10-μF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

AGND, DGND Pins

To maximize the dynamic performance of the PCM1850A/1851A, the analog and digital grounds are not connected internally. These grounds must have low impedance to avoid digital noise feeding back into the analog ground. Therefore, they should be connected directly to each other under the parts to reduce the potential of a noise problem.

V_{IN}L[1:6], V_{IN}R[1:6] Pins

A 0.33-μF capacitor is recommended as the ac-coupling capacitor, which gives a 2.4- to 8.5-Hz cutoff frequency. If higher full-scale input voltage is required, it can be adjusted by adding only one series resistor to each V_{IN}xx pin, but a signal source resistance less than 1 kΩ is recommended for these pins in order to keep accuracy of the gain control command and to maintain crosstalk performance.

MOUTL, MOUTR Pins

An ac-coupled light load is recommended; a 2.2-μF capacitor with a 10-kΩ load gives a 7.2-Hz cutoff frequency.

V_{REF}1, V_{REF}2, V_{REF}S Pins

Between V_{REF}1 and AGND, V_{REF}2 and AGND, and V_{REF}S and AGND, 0.1-μF ceramic and 10-μF electrolytic capacitors are recommended to ensure low source impedance of the ADC references. These capacitors should be located as close as possible to the V_{REF}1, V_{REF}2, and V_{REF}S pins to reduce dynamic errors on the ADC references. The differential voltage between V_{REF}2 and AGND sets the analog input full-scale range.

BCK and LRCK Pins (in Master Mode), DOUT Pin

These pins have enough load-driving capability. However, if the output line is long, locating a buffer near the PCM1850A/1851A and minimizing load capacitance is recommended in order to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

System Clock

Because the PCM1850A/1851A operates based on a system clock, the quality of the system clock can influence dynamic performance. Therefore, it is recommended to consider the system clock duty, jitter, and the time difference between the system clock transition and the BCK or LRCK transition in slave mode.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1851APJTR	OBSOLETE	TQFP	PJT	32		TBD	Call TI	Call TI	-40 to 85	PCM1851A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

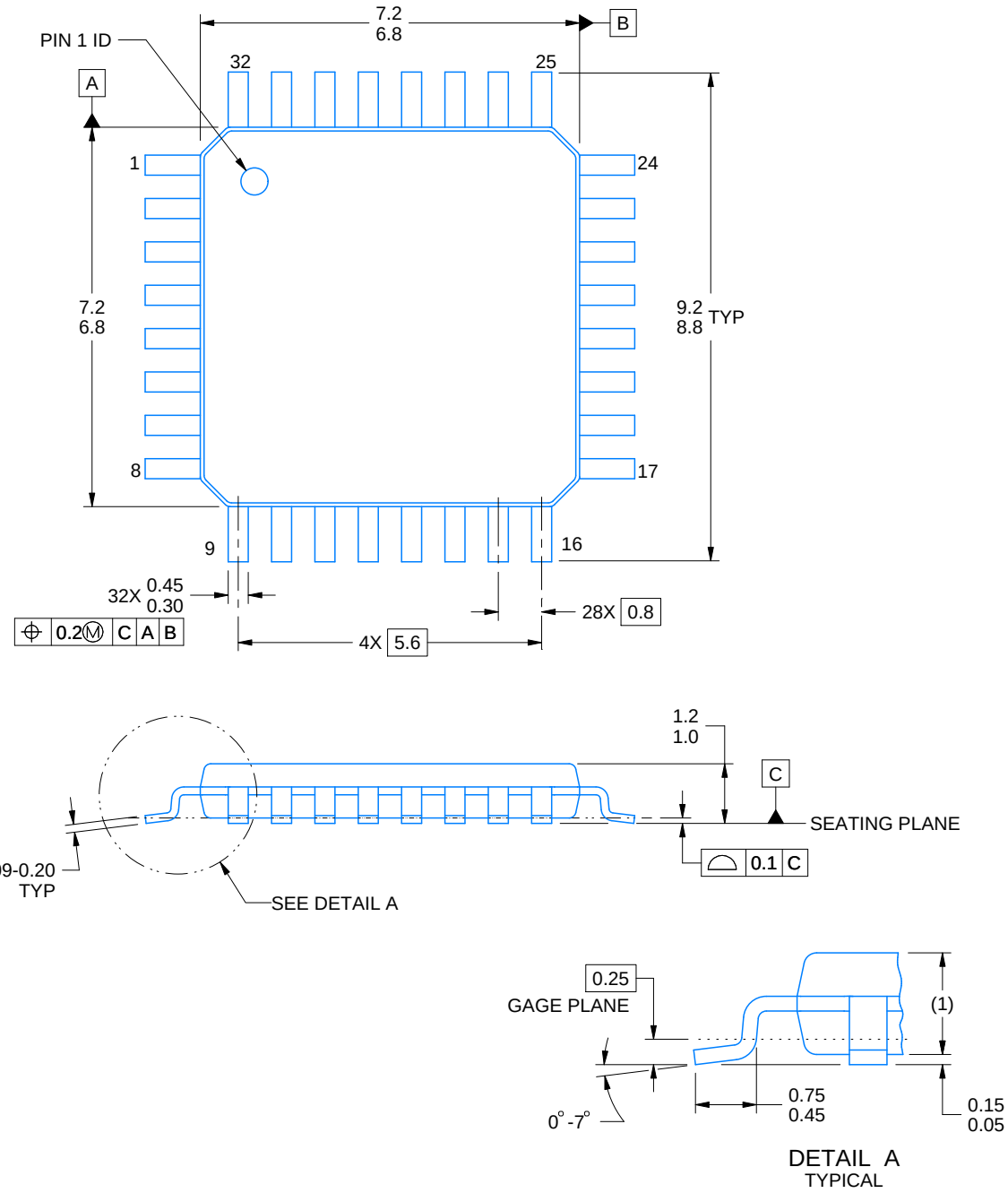
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PJT0032A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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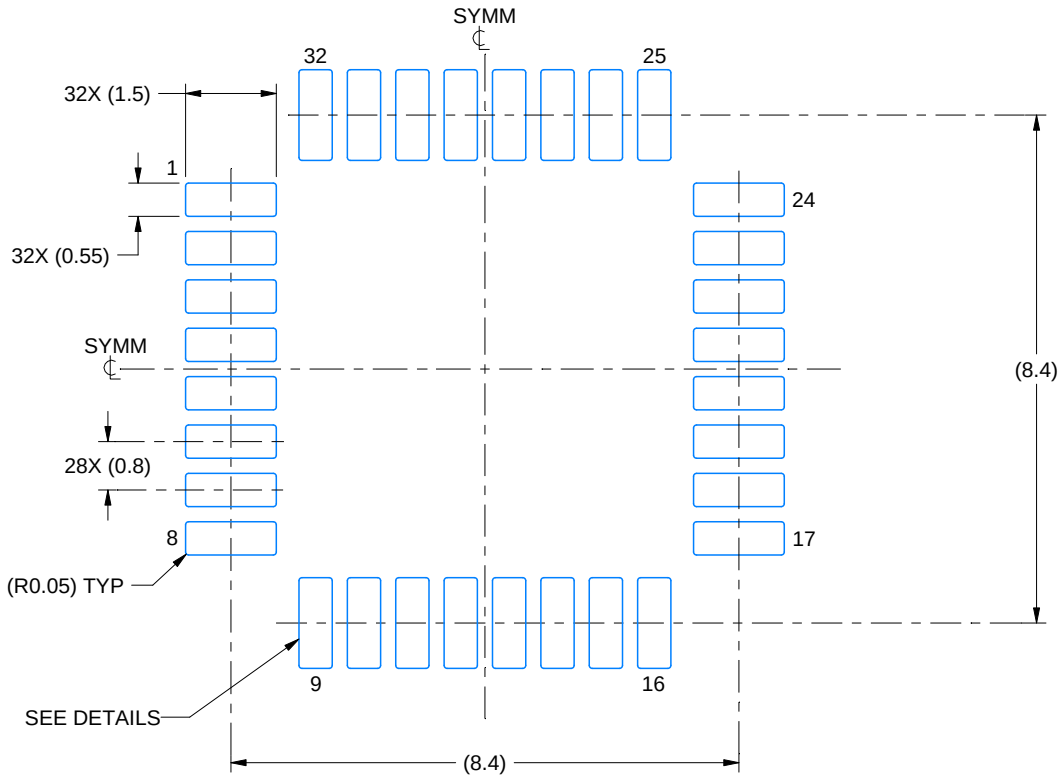
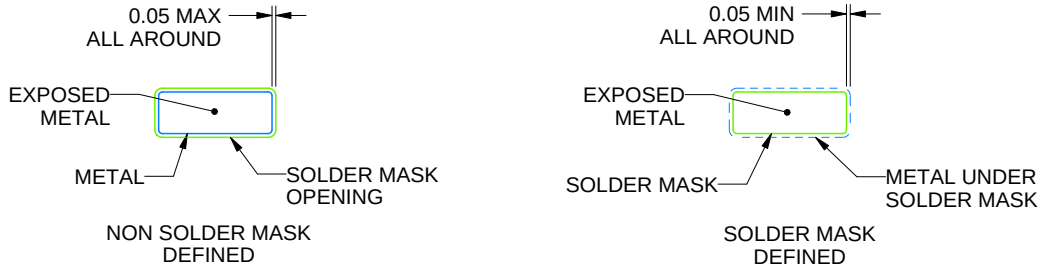
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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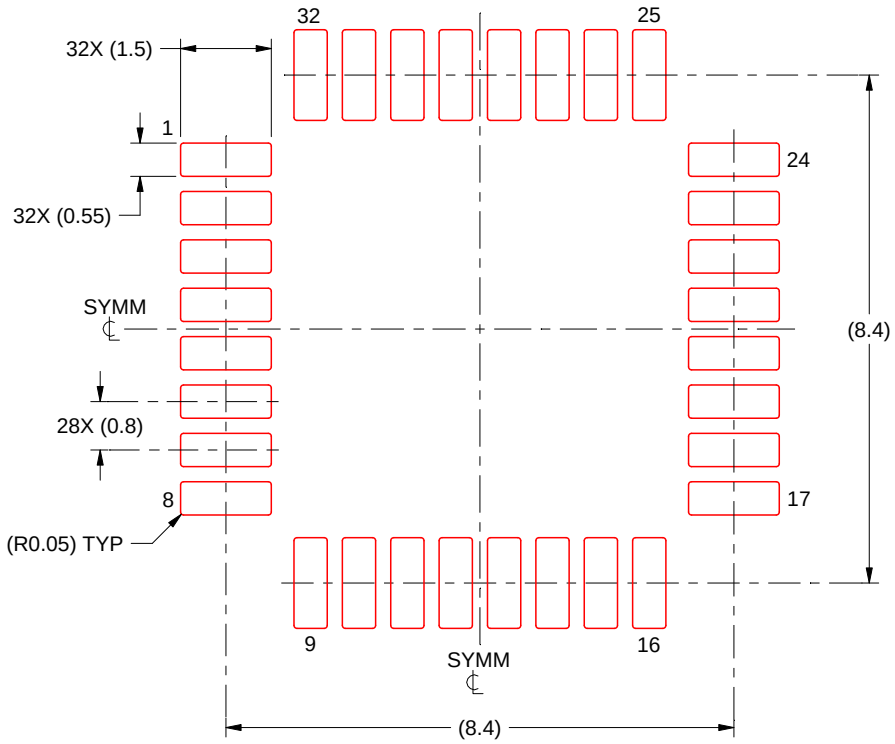
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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