SN65LVCP114 14.2-Gbps Quad 1:2-2:1 Mux, Linear-Redriver With Signal Conditioning

1 Features

- Quad 2:1 Mux and 1:2 Demux
- Multi-Rate Operation up to 14.2 Gbps Serial Data Rate
- Linear Receiver Equalization Which Increases Margin at System Level of Decision Feedback Equalizer
- Bandwidth: 18 GHz, Typical
- Per-Lane P/N Pair Inversion
- Port or Single Lane Switching
- Low Power: 150 mW/Channel, Typical
- Loopback Mode on All Three Ports
- I^2C Control in Addition to GPIO
- DIAG Mode That Outputs Data of Line Side Port to Both Fabric Side Ports
- 2.5-V or 3.3-V Single Power Supply
- PBGA Package 12-mm × 12-mm × 1-mm, 0.8-mm Terminal Pitch
- Excellent Impedance Matching to 100-Ω PCB Transmission Lines
- Small Package Size Provides Board Real Estate Saving
- Adjustable Output Swing Provides Flexible EMI and Crosstalk Control
- Low Power
- Supports 10GBASE-KR Applications With Ability to Transparency for Link Training

2 Applications

- High-Speed Redundancy Switch in Telecom and Data Communication
- Backplane Interconnect for 10G-KR, 16GFC

3 Description

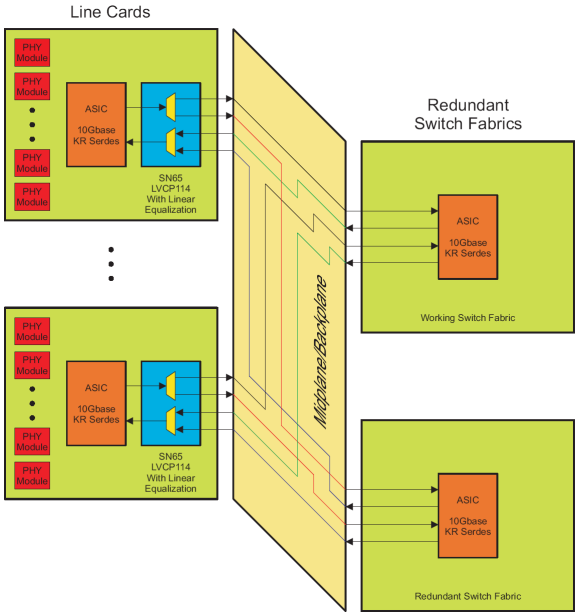
The SN65LVCP114 device is an asynchronous, protocol-agnostic, low-latency QUAD mux, linear-redriver optimized for use in systems operating at up to 14.2 Gbps. The device linearly compensates for channel loss in backplane and active-cable applications. The architecture of SN65LVCP114 linear-redriver is designed to work effectively with ASIC or FPGA products implementing digital equalization using decision feedback equalizer (DFE) technology. The SN65LVCP114 mux, linear-redriver preserves the integrity (composition) of the received signal, ensuring optimum DFE and system performance. The SN65LVCP114 provides a low-power mux-demux, linear-redriver solution while at the same time extending the effectiveness of DFE.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVCP114	NFBGA (167)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN65LVCP114 Typical Implementation



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2012) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Removed Typical Eq Gain Profile Curve graph in *Typical Characteristics*	11

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5 Description (continued)

SN65LVCP114 is configurable through GPIO or an I^2C interface.

A single 2.5-V or 3.3-V power supply supports the operation of the SN65LVCP114.

The SN65LVCP114 is packaged in a 12-mm × 12-mm × 1-mm PBGA package with 0.8-mm pitch.

The SN65LVCP114 has three ports; each port is a quad lane. The switch logic of SN65LVCP114 can be implemented to support a 2:1 MUX per lane, 1:2 DEMUX per lane, and independent lane switching. The receive equalization can be independently programmed for each of the ports. The SN65LVCP114 supports loopback on all three ports.

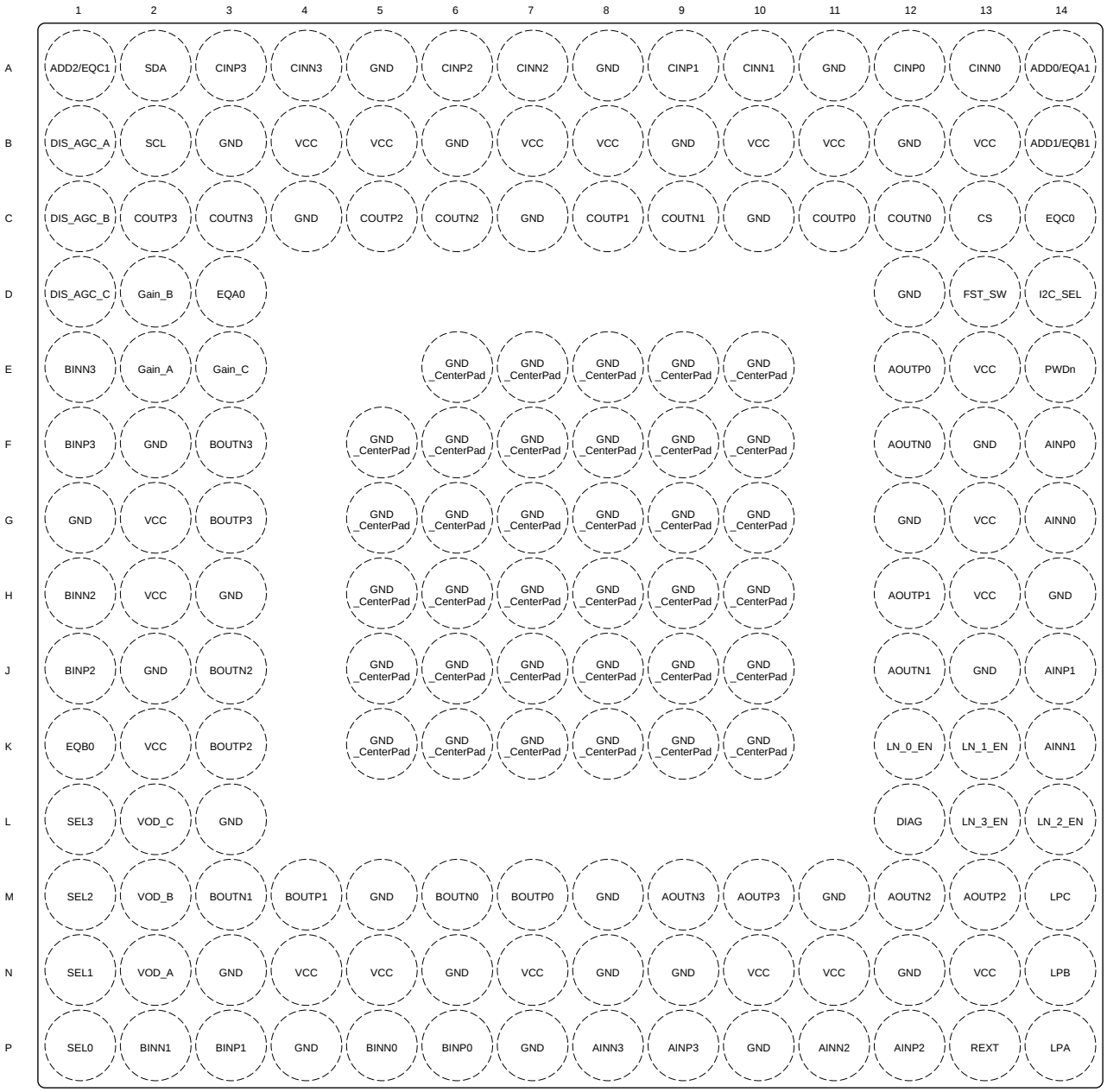
Table 1. Recommended Maximum Board Temperature

LOOP_A	LOOP_B	LOOP_C	DIAG	MAXIMUM BOARD TEMPERATURE (1)			
				V_{CC} = 2.5 V		V_{CC} = 3.3 V	
				V_{OD} = LOW	V_{OD} = HIGH	V_{OD} = LOW	V_{OD} = HIGH
LOW	LOW	LOW	LOW	85°C	85°C	85°C	75°C
LOW	LOW	LOW	HIGH	85°C	85°C	75°C	System Specific (2)
LOW	LOW	HIGH	LOW	85°C	85°C	85°C	75°C
LOW	LOW	HIGH	HIGH	85°C	85°C	85°C	75°C
LOW	HIGH	LOW	LOW	85°C	85°C	75°C	System Specific (2)
LOW	HIGH	LOW	HIGH	85°C	85°C	75°C	System Specific (2)
LOW	HIGH	HIGH	LOW	85°C	85°C	75°C	System Specific (2)
LOW	HIGH	HIGH	HIGH	85°C	85°C	75°C	System Specific (2)
HIGH	LOW	LOW	LOW	85°C	85°C	85°C	75°C
HIGH	LOW	LOW	HIGH	85°C	85°C	75°C	System Specific (2)
HIGH	LOW	HIGH	LOW	85°C	85°C	85°C	75°C
HIGH	LOW	HIGH	HIGH	85°C	85°C	75°C	System Specific (2)
HIGH	HIGH	LOW	LOW	85°C	85°C	75°C	System Specific (2)
HIGH	HIGH	LOW	HIGH	85°C	85°C	75°C	System Specific (2)
HIGH	HIGH	HIGH	LOW	85°C	85°C	75°C	System Specific (2)
HIGH	HIGH	HIGH	HIGH	85°C	85°C	75°C	System Specific (2)

(1) Maximum board temperature is allowed as long as the device maximum junction temperature is not exceeded.
(2) Texas Instruments recommends a system thermal and device use case power analysis to decide possible use of a heat sink.

6 Pin Configuration and Functions

ZJA Package
167-Pin NFBGA
Top View



Pin Functions

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
NAME	BALLS		
LINE-SIDE HIGH-SPEED I/O			
CINP0 CINN0	A12 A13	Input (with 50-Ω termination to input common mode)	Differential input, lane 0 line side.
CINP1 CINN1	A9 A10	Input (with 50-Ω termination to input common mode)	Differential input, lane 1 line side

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Pin Functions (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION	
NAME	BALLS			
CINP2 CINN2	A6 A7	Input (with 50-Ω termination to input common mode)	Differential input, lane 2 line side	
CINP3 CINN3	A3 A4	Input (with 50-Ω termination to input common mode)	Differential input, lane 3 line side	
COUTP0 COUTN0	C11 C12	Output	Differential output, lane 0 line side	
COUTP1 COUTN1	C8 C9	Output	Differential output, lane 1 line side	
COUTP2 COUTN2	C5 C6	Output	Differential output, lane 2 line side	
COUTP3 COUTN3	C2 C3	Output	Differential output, lane 3 line side	
SWITCH-SIDE HIGH-SPEED I/O				
AINP0 AINN0	F14G14	Input (with 50-Ω termination to input common mode)	Differential input, lane 0, fabric switch_A_side	
AINP1 AINN1	J14 K14	Input (with 50-Ω termination to input common mode)	Differential input, lane 1, fabric switch_A_side	
AINP2 AINN2	P12 P11	Input (with 50-Ω termination to input common mode)	Differential input, lane 2, fabric switch_A_side	
AINP3 AINN3	P9 P8	Input (with 50-Ω termination to input common mode)	Differential input, lane 3, fabric switch_A_side	
BINP0 BINN0	P6 P5	Input (with 50-Ω termination to input common mode)	Differential input, lane 0, fabric switch_B_side	
BINP1 BINN1	P3 P2	Input (with 50-Ω termination to input common mode)	Differential input, lane 1, fabric switch_B_side	
BINP2 BINN2	J1 H1	Input (with 50-Ω termination to input common mode)	Differential input, lane 2, fabric switch_B_side	
BINP3 BINN3	F1 E1	Input (with 50-Ω termination to input common mode)	Differential input, lane 3, fabric switch_B_side	
AOUTP0 AOUTN0	E12 F12	Output	Differential output, lane 0, fabric switch_A_side	
AOUTP1 AOUTN1	H12 J12	Output	Differential output, lane 1, fabric switch_A_side	
AOUTP2 AOUTN2	M13 M12	Output	Differential output, lane 2, fabric switch_A_side	
AOUTP3 AOUTN3	M10 M9	Output	Differential output, lane 3, fabric switch_A_side	
BOUTP0 BOUTN0	M7 M6	Output	Differential output, lane 0, fabric switch_B_side	
BOUTP1 BOUTN1	M4 M3	Output	Differential output, lane 1, fabric switch_B_side	
BOUTP2 BOUTN2	K3 J3	Output	Differential output, lane 2, fabric switch_B_side	
BOUTP3 BOUTN3	G3 F3	Output	Differential output, lane 3, fabric switch_B_side	
CONTROL SIGNALS				
ADD0/EQA1 ADD1/EQB1 ADD2/EQC1	A14 B14 A1	Input, 2.5-V or 3.3-V CMOS - 3-state	**GPIO mode** EQ control pins. EQA1 and EQA0 pins are 3-state and control the EQ gain of port A. EQ control pins. EQB1 and EQB0 pins are 3-state and control the EQ gain of port B. EQ control pins. EQC1 and EQC0 pins are 3-state and control the EQ gain of port C. Refer to Table 5 for detailed information about equalization.	**I^2C mode** ADD0 along with pins ADD1 and ADD2 comprise the three bits of the I^2C slave address.
EQA0 EQB0 EQC0	D3 K1 C14	Input, 2.5-V or 3.3-V CMOS - 3-state	**GPIO mode** EQ control pins. EQA1 and EQA0 pins are 3-state and control theEQ gain of port A. EQ control pins. EQB1 and EQB0 pins are 3-state and control theEQ gain of port B. EQ control pins. EQC1 and EQC0 pins are 3-state and control theEQ gain of port C. Refer to Table 5 for detailed information about equalization.	**I^2C mode** No action needed
LPA LPB LPC	P14 N14 M14	Input (with 48-kΩ pulldown) 2.5-V or 3.3-V CMOS	**GPIO mode** LPx enables loopback for port x HIGH: Loopback enabled LOW: Loopback disabled See Table 2 and Figure 14	**I^2C mode** No action needed

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Pin Functions (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION	
NAME	BALLS			
SEL0 SEL1 SEL2 SEL3	P1 N1 M1 L1	Input (with 48-kΩ pulldown) 2.5-V or 3.3-V CMOS	**GPIO mode** SELx, A or B switch control for lane x HIGH: port B is selected LOW: port A is selected See Table 2	**I²C mode** No action needed
REXT	P13	Input, analog	External bias resistor, 1,200 Ω to ground	
CS	C13	Input (with 48-kΩ pulldown) 2.5-V or 3.3-V CMOS	**GPIO mode** No action needed	**I²C mode** HIGH: acts as chip select LOW: disables I²C interface
PWDn	E14	Input (with 48-kΩ pullup) 2.5-V or 3.3-V CMOS	LOW: Powers down the device, inputs off and outputs disabled, resets I²C HIGH: Normal operation	
DIAG	L12	Input (with 48-kΩ pulldown) 2.5-V or 3.3-V CMOS	**GPIO mode** HIGH: Enables the same data on the line side (Port C) to be output on both fabric side ports (Port A and Port B). LOW: Normal operation See Table 2 and Figure 15	**I²C mode** No action needed
LN_0_EN LN_1_EN LN_2_EN LN_3_EN	K12 K13 L14 L13	Input (with 48-kΩ pullup) 2.5-V or 3.3-V CMOS	**GPIO mode** LN_x_EN = High, enables lane x of ports A, B, and C LN_x_EN = Low, disables lane x of ports A, B, and C	**I²C mode** No action needed
DIS_AGC_A DIS_AGC_B DIS_AGC_C	B1 C1 D1	Input (with 48-kΩ pulldown) 2.5-V or 3.3-V CMOS	**GPIO mode** Disables the AGC loop internal to the SN65LVCP114 DIS_AGC = High, disables the AGC loop DIS_AGC = Low, enables the AGC loop	**I²C mode** No action needed
VOD_A VOD_B VOD_C	N2 M2 L2	Input, 2.5-V or 3.3-V CMOS - 3-state	**GPIO mode** HIGH: selects VOD output range: 1.2 V maximum and a gain of 2.2 LOW: selects VOD output range: 600 mV maximum and a gain of 1.1 If the VOD_x signal is left floating, the signal defaults to 1.2 V maximum and a gain of 2.2	**I²C mode** No action needed
Gain_A Gain_B Gain_C	E2 D2 E3	Input, 2.5-V or 3.3-V CMOS - 3-state	**GPIO mode** HIGH: Receiver gain = 1 LOW: Receiver gain = 0.5 If the Gain_x signal is left floating, the signal defaults to 0.5	**I²C mode** No action needed
SDA	A2	Input / output, open-drain output	**GPIO mode** No action needed	**I²C mode** I²C data. Connect a 10-kΩ pullup resistor externally
SCL	B2	Input, open-drain input	**GPIO mode** No action needed	**I²C mode** I²C clock. Connect a 10-kΩ pullup resistor externally
FST_SW	D13	Input (with 48-kΩ pullup) 2.5-V or 3.3-V CMOS input	**GPIO mode** HIGH: Fast switching; the idle outputs are squelched (see tSM specification). LOW: Slow switching; the idle outputs are powered off (see tSM1 specification).	**I²C mode** No action needed
I2C_SEL	D14	Input (with 48-kΩ pulldown) 2.5-V or 3.3-V CMOS input	Configures the device in I²C or GPIO mode of operation HIGH: Enables I²C mode LOW: Enables GPIO mode	
POWER SUPPLY				
VCC	B4, B5, B7, B8, B10, B11, B13, E13, G2, G13, H2, H13, K2,N4, N5, N7, N10, N11, N13	Power, 2.5 V ±5% or 3.3 V ±5%	Power supply pins	
GROUND				
GND	A5, A8, A11, B3, B6, B9, B12, C4, C7, C10,D12, F2, F13,G1, G12, G1, G12, H3, H14,J2, J13, L3, M5,M8, M11, N3, N6, N8, N9, N12, P4, P7, P10	Ground	Ground pins	

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Pin Functions (continued)

PIN		DIRECTION TYPE SUPPLY	DESCRIPTION
NAME	BALLS		
GND_CenterPad	E6, E7 , E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7,G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7,K8, K9, K10	Ground	These pins must be connected to the GND plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]	–0.3	4	V
$V_{IN,DIFF}$	Differential voltage between xINx_P and xINx_N		±2.5	V
V_{IN+}, V_{IN-}	Voltage at xINx_P and xINx_N	–0.5	VCC + 0.5	V
V_{IO}	Voltage on control I/O pins	–0.3	VCC + 0.5	V
I_{IN+} I_{IN-}	Continuous current at high-speed differential data inputs (differential)	–25	25	mA
I_{OUT+} I_{OUT-}	Continuous current at high-speed differential data outputs	–25	25	mA
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1][2]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[3][4]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
	Operating data rate, dR			14.2	Gbps
	Supply voltage, V_{CC}, 2.5-V nominal supply	2.375	2.5	2.625	V
	Supply voltage, V_{CC}, 3.3-V nominal supply	3.135	3.3	3.465	V
	PSNR BG, bandgap circuitry PSNR, 10 Hz–10 GHz	20			dB
CONTROL INPUTS					
V_{IH}	High-level input voltage	0.8 × V_{CC}			
V_{IM}	Mid-level input voltage	V_{CC}/2 – 0.3		V_{CC}/2 + 0.3	V
V_{IL}	Low- level input voltage			0.2 × V_{CC}	V
T_C	Junction temperature[1]	–10		125	°C

(1) Use of θJB and φJB are recommended for thermal calculations. For more information about traditional and new thermal metrics, see IC Package Thermal Metrics application report, SPRA953.

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Recommended Operating Conditions (continued)

	MIN	NOM	MAX	UNIT
Maximum board temperature (1)			See Table 1	°C

7.4 Thermal Information

THERMAL METRIC (1)		SN65LVCC114 ZJA (NFBGA) 167 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics (V_{CC} 2.5 V ±5%)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation, loopback mode	Ports A, B, and C in loopback mode with all 12 channels active. VOD = LOW		1800	2300	mW
PD_N	Device power dissipation, normal mode	Device configured in mux-demux mode with 8 channels active. VOD = LOW		1400	1800	mW
PD_{OFF}	Device power dissipation, lanes disabled	All 4 lanes disabled. See the I^2C section for device configuration.		50		mW
PD_{STB}	Device power dissipation, standby	All 12 channels active, VOD = LOW, FAST_SW = HIGH. See the I^2C section for device configuration.		1800	2300	mW

7.6 Electrical Characteristics (V_{CC} 3.3 V ±5%)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation, loopback mode	Ports A, B, and C in loopback mode with all 12 channels active. VOD = LOW		2500	3150	mW
PD_N	Device power dissipation, normal mode	Device configured in mux-demux mode with 8 channels active. VOD = LOW		1800	2500	mW
PD_{OFF}	Device power dissipation, lanes disabled	All 4 lanes disabled. See the I^2C section for device configuration.		50		mW
PD_{STB}	Device power dissipation, standby	All 12 channels active, VOD = LOW, FAST_SW = HIGH. See I^2C section for device configuration.		2500	3150	mW

7.7 Electrical Characteristics (V_{CC} 3.3 V ±5%, 2.5 V ±5%)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
CMOS DC SPECIFICATIONS						
I_{IH}	High-level input current	$V_{IN} = 0.9 \times V_{CC}$			80	µA
I_{IL}	Low-level input current	$V_{IN} = 0.1 \times V_{CC}$	-80			µA
CML INPUTS (AINP[3:0], AINN[3:0], BINP[3:0], BINN[3:0], CINP[3:0], CINN[3:0])						
r_{IN}	Differential input resistance	INx_P to INx_N		100		Ω
V_{INPP}	Input linear dynamic range	Gain = 0.5		1200		mVpp

(1) All typical values are at 25°C and with 2.5-V and 3.3-V supply, unless otherwise noted.

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Electrical Characteristics (V_{CC} 3.3 V ±5%, 2.5 V ±5%) (continued)

over operating conditions range. All parameters are referenced to package pins (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ICM}	Common-mode input voltage	Internally biased		V_{CC} – 0.3		V
SCD11	Input differential to common-mode conversion	100 MHz to 7.1GHz		–25		dB
SDD11	Differential input return loss	100 MHz to 7.1GHz		–10		dB
CML OUTPUTS (AOUTP[3:0], AOUTN[3:0], BOUTP[3:0], BOUTN[3:0], COUTP[3:0], COUTN[3:0])						
V_{OD}	Output linear dynamic range	R_L = 100 Ω, V_{OD} = High		1200		mV_{PP}
		R_L = 100 Ω, V_{OD} = Low		600		
V_{OS}	Output offset voltage	R_L = 100 Ω, 0 V applied at inputs			20	mV_{PP}
$V_{CM,RIP}$	Common-mode output ripple	K28.5 pattern at 14.2 Gbps, no interconnect loss, V_{OD} = HIGH		10	20	mV_{RMS}
$V_{OD,RIP}$	Differential path output ripple	K28.5 pattern at 14.2Gbps, no interconnect loss, V_{IN} = 1200 mVpp. Outputs squelched.			20	mV_{PP}
V_{OCM}	Output common mode voltage	See Figure 9		V_{CC} – 0.35		V
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			±10		mV
t_{PLH}	Low-to-high propagation delay	See Figure 1		200		ps
t_{PHL}	High-to-low propagation delay			200		ps
$t_{SK(O)}$	Inter-pair output skew (2)	All outputs terminated with 100 Ω. See Figure 3		50		ps
$t_{SK(PP)}$	Part-to-part skew(3)				100	ps
t_R	Rise time	Input signal with 30-ps rise time, 20% to 80%. See Figure 2		31		ps
t_F	Fall time	Input signal with 30-ps fall time, 20% to 80%. See Figure 2		31		ps
SDD22	Differential output return loss	100 MHz to 7.1 GHz		–10		dB
SCC22	Common-mode output return loss	100 MHz to 7.1 GHz		–5		dB
t_{SM}	Multiplexer switch time	Mux to valid output (idle outputs are squelched)		100		ns
t_{SM1}		Mux to valid output (idle outputs are turned off)		10		µs
Ch_{iso}	Channel-to-channel isolation(4)	Frequency at 5.1625 GHz		52.2		dB
		Frequency at 7.1 GHz		43.5		
OUT_{NOISE}	Output referred noise	10 MHz to 7.1 GHz. No other noise source present. V_{OD} = LOW			1500	$µV_{RMS}$
		10 MHz to 7.1 GHz. No other noise source present. V_{OD} = HIGH			3000	
Vpre	Output pre-cursor pre-emphasis	Input signal with 3.75-dB pre-cursor and measured on the output signal. See Figure 4. Vpre = 20 log(V3/V2)		5		dB
Vpst	Output post-cursor pre-emphasis	Input signal with 12-dB post-cursor and measure on the output signal. See Figure 4. Vpst = 20 log(V1/V2)		14		dB
r_{OT}	Single-ended output resistance	Single-ended on-chip terminations to VCC, outputs are AC-coupled		50		Ω
r_{OM}	Output termination mismatch at 1 MHz	$\Delta rom = 2 \times \frac{rp - rn}{rp + rn} \times 100$			5%	
EQUALIZATION						
EQ_{Gain}	At 7.1 GHz input signal	Equalization gain, EQ = MAX	10	15		dB
DJ1	TX residual deterministic jitter at 10.3125 Gbps	Tx launch amplitude = 0.6 Vpp, EQ = 1.3 dB, VOD and GAIN are high. Test channel = 0". See Figure 11.		0.08		UIp-p
DJ2	TX residual deterministic jitter at 14.2 Gbps	Tx launch amplitude = 0.6 Vpp, EQ = 1.3 dB, VOD and GAIN are high. Test channel = 0". See Figure 11.		0.06		UIp-p
DJ3	RX residual deterministic jitter at 10.3125 Gbps	Tx launch amplitude = 0.6 Vpp, test channel = 12" (9-dB loss at 5 GHz), EQ = 13.9 dB, VOD and GAIN are high. See Figure 10.		0.04		UIp-p
DJ4	RX residual deterministic Jitter at 14.2 Gbps	Tx launch amplitude = 0.6 Vpp, test channel = 8" (9-dB loss at 7 GHz), EQ = 13.9 dB, VOD = LOW and GAIN = HIGH. See Figure 10.		0.08		UIp-p

(2) $t_{SK(O)}$ is the magnitude of the time difference between the channels within a Port. For more information, see *SN65LVCP114 Guidelines for Skew Compensation*, SLLA323.
(3) $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) All noise sources added.

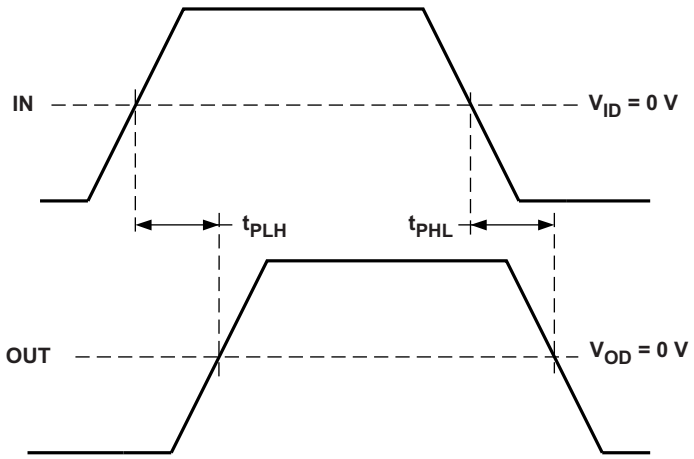

Figure 1. Propagation Delay, Input to Output

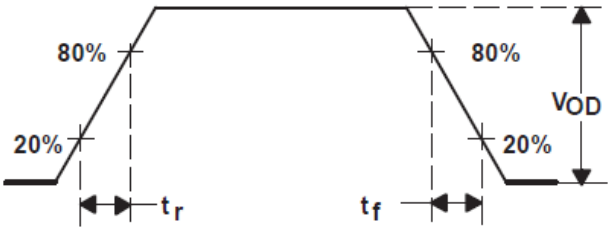

Figure 2. Output Rise and Fall Times

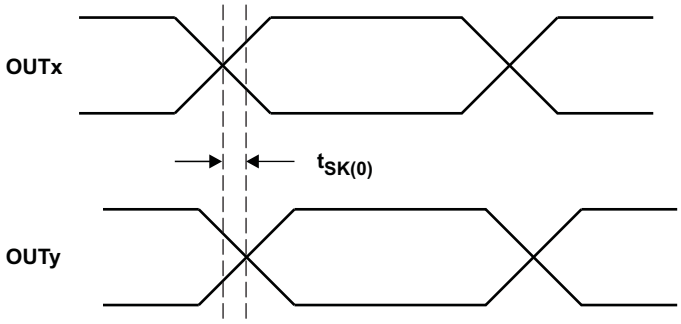

Figure 3. Output Inter-Pair Skew

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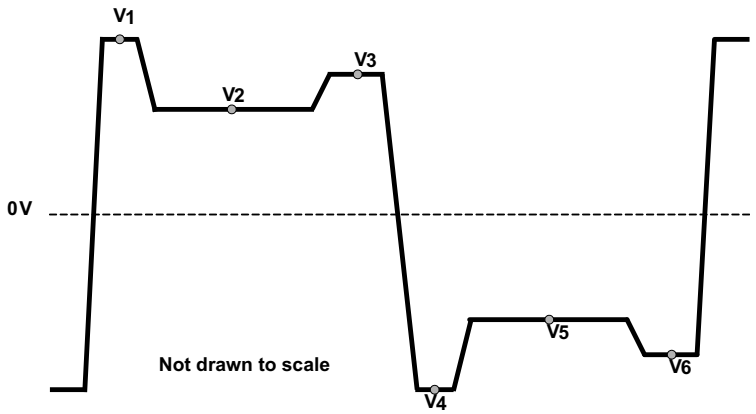

Figure 4. VPRE and VPOST [The Test Pattern is 1111111100000000 (Eight 1s, Eight 0s)]

7.8 Typical Characteristics

Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

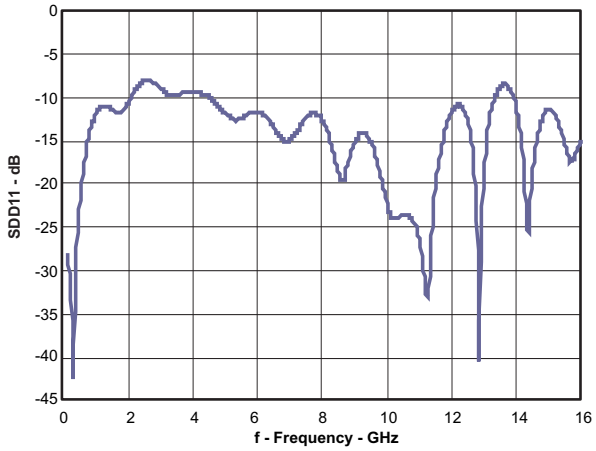

Figure 5. Differential Input Return Loss

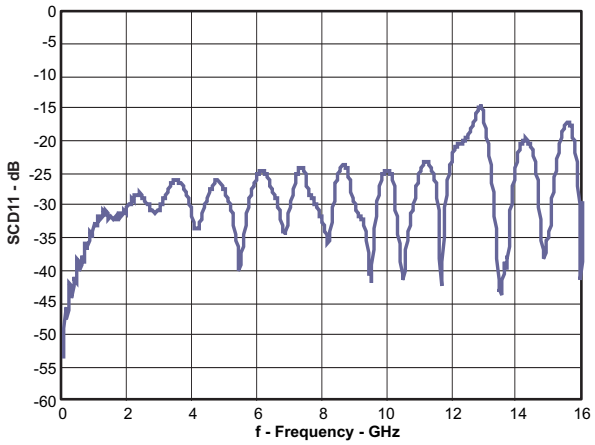

Figure 6. Differential to Common-Mode Conversion

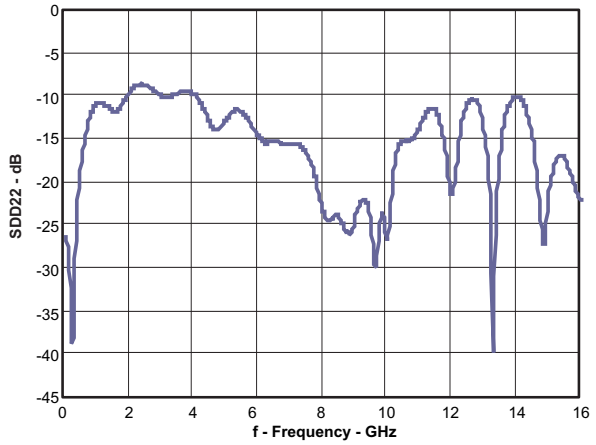

Figure 7. Differential Output Return Loss

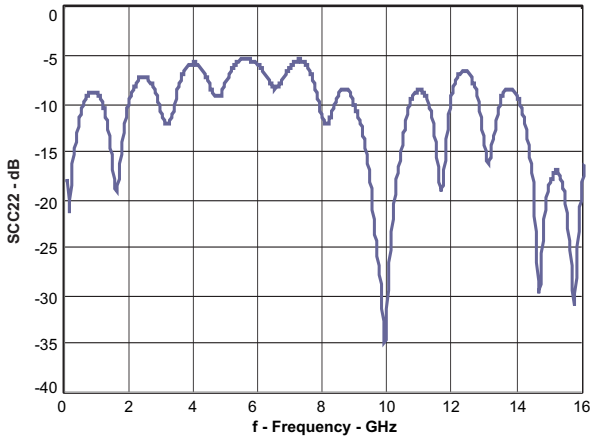

Figure 8. Common-Mode Output Return Loss

8 Parameter Measurement Information

8.1 Test Circuits

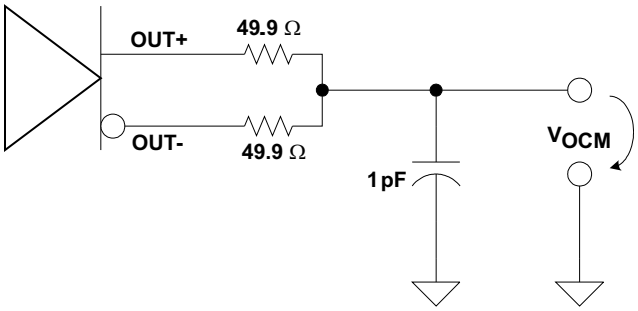

Figure 9. Common-Mode Output-Voltage Test Circuit

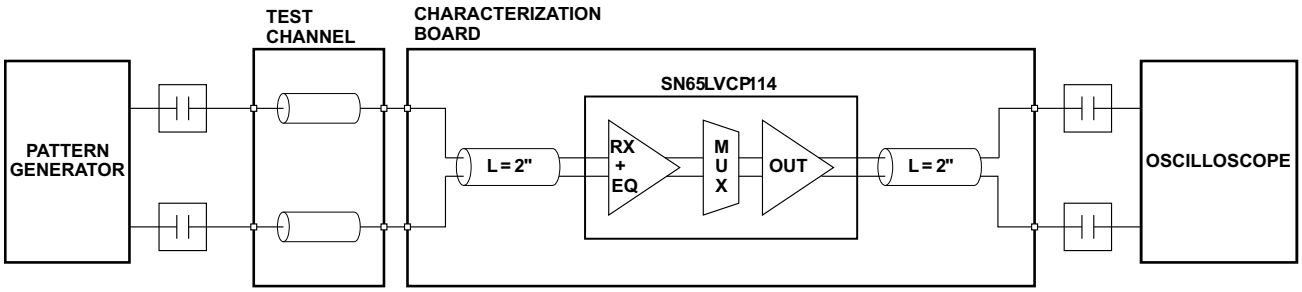

Figure 10. Receive-Side Performance Test Circuit

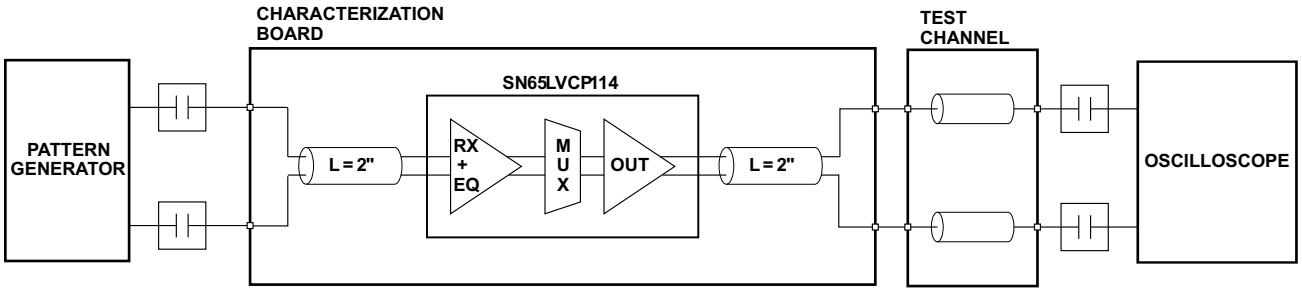

Figure 11. Transmit-Side Performance Test Circuit

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8.2 Equivalent Input and Output Schematic Diagrams

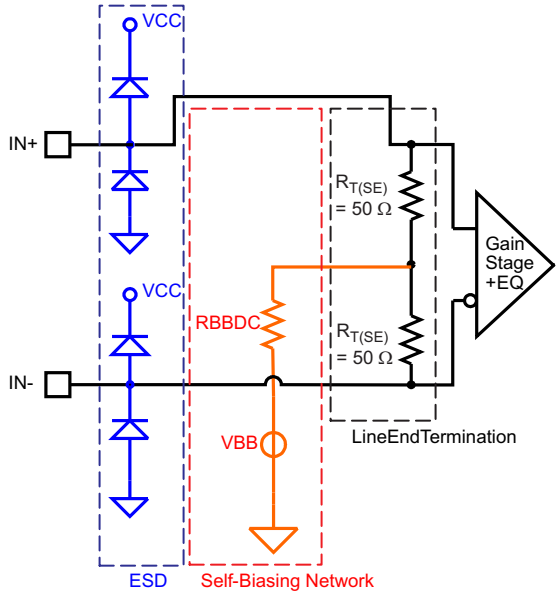

Figure 12. Equivalent Input Circuit Design

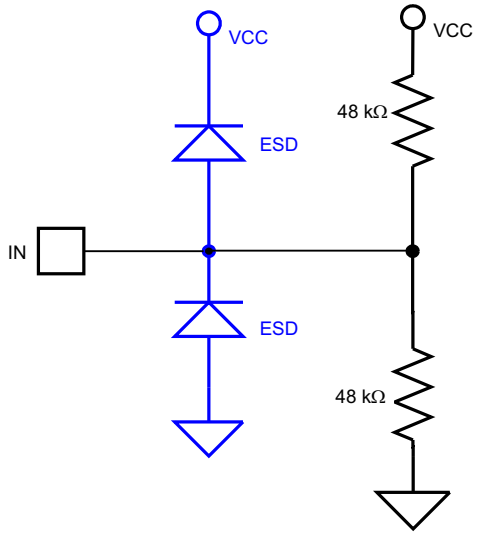

Figure 13. 3-Level Input Biasing Network

8.3 Functional Definitions

Table 2. Loopback, Diag, and Sel Controls

LOOP_A	LOOP_B	LOOP_C	DIAG	SEL[3:0]	OUTPUT PORT A	OUTPUT PORT B	OUTPUT PORT C
0	0	0	0	0	In_Port_C[3:0]	idle	In_Port_A[3:0]
0	0	0	0	1	idle	In_Port_C[3:0]	In_Port_B[3:0]
0	0	0	1	0	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_A[3:0]
0	0	0	1	1	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_B[3:0]
0	0	1	0	0	In_Port_C[3:0]	Idle	In_Port_C[3:0]
0	0	1	0	1	Idle	In_Port_C[3:0]	In_Port_C[3:0]
0	0	1	1	0	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
0	0	1	1	1	In_Port_C[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
0	1	0	0	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
0	1	0	0	1	Idle	In_Port_B[3:0]	In_Port_B[3:0]
0	1	0	1	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
0	1	0	1	1	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_B[3:0]
0	1	1	0	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_C[3:0]
0	1	1	0	1	Idle	In_Port_B[3:0]	In_Port_C[3:0]
0	1	1	1	0	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_C[3:0]
0	1	1	1	1	In_Port_C[3:0]	In_Port_B[3:0]	In_Port_C[3:0]
1	0	0	0	0	In_Port_A[3:0]	Idle	In_Port_A[3:0]
1	0	0	0	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_B[3:0]
1	0	0	1	0	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_A[3:0]
1	0	0	1	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_B[3:0]
1	0	1	0	0	In_Port_A[3:0]	Idle	In_Port_C[3:0]
1	0	1	0	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
1	0	1	1	0	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
1	0	1	1	1	In_Port_A[3:0]	In_Port_C[3:0]	In_Port_C[3:0]
1	1	0	0	0	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_A[3:0]

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Functional Definitions (continued)

Table 2. Loopback, Diag, and Sel Controls (continued)

LOOP_A	LOOP_B	LOOP_C	DIAG	SEL[3:0]	OUTPUT PORT A	OUTPUT PORT B	OUTPUT PORT C
1	1	0	0	1	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_B[3:0]
1	1	0	1	0	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_A[3:0]
1	1	0	1	1	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_B[3:0]
1	1	1	0	0	In_Port_A[3:0]	In_Port_B[3:0]	In_Port_C[3:0]

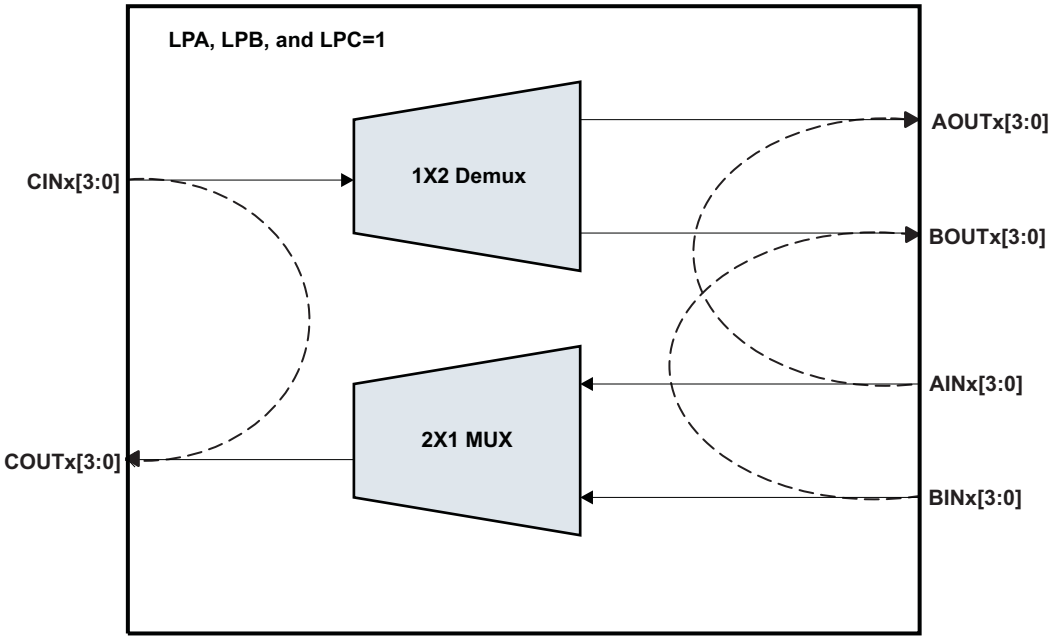

Figure 14. Loopback Mode

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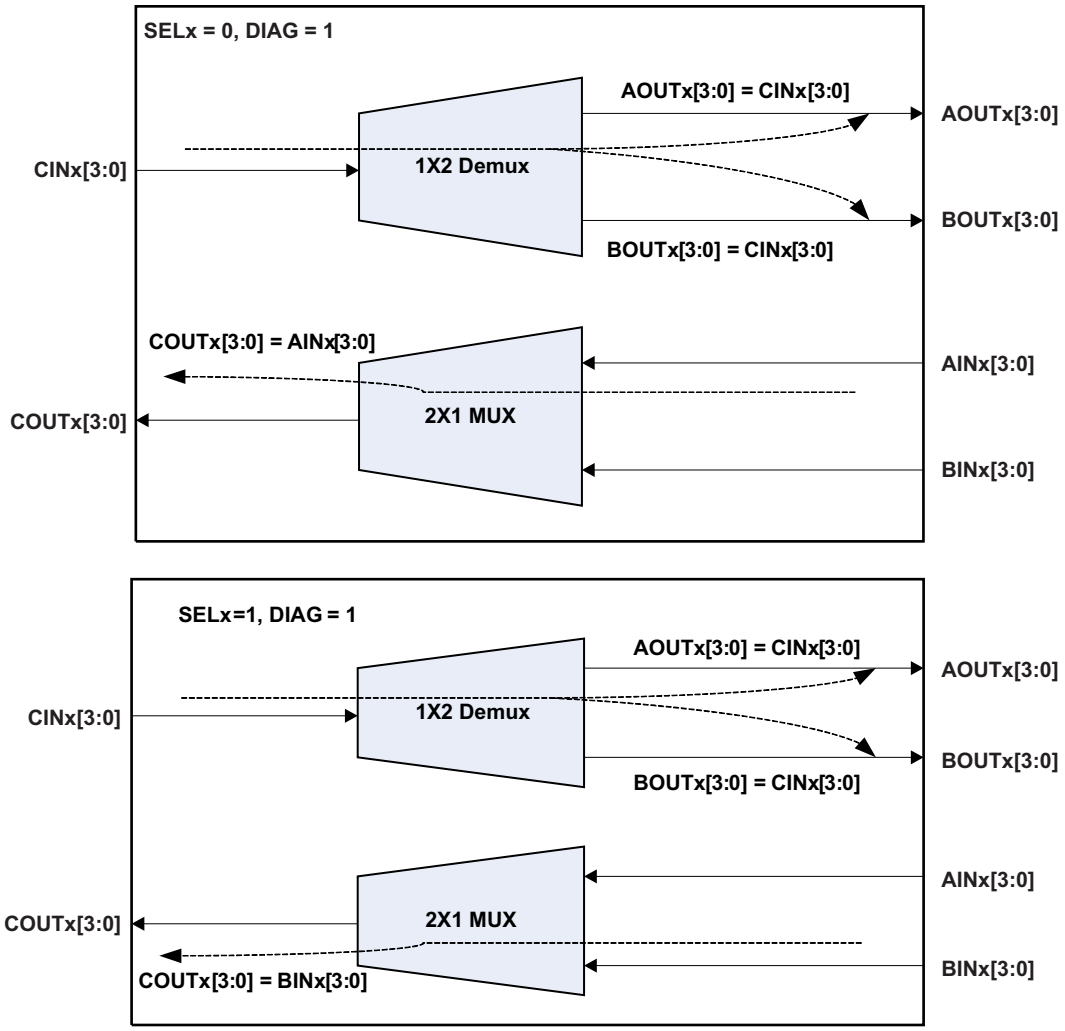

Figure 15. Diagnostic Mode

Table 3. Overall Gain Settings

GAIN_x	INPUT GAIN [dB]	VOD_x	VOD GAIN [dB]	EQ[x]0	EQ[x]1	TOTAL DC GAIN [dB]	TOTAL EQ GAIN (7 GHz) [dB]
LOW	–6	LOW	1	LOW	LOW	–5	1.3
LOW	–6	LOW	1	LOW	HiZ	–5	2
LOW	–6	LOW	1	LOW	HIGH	–5	3.6
LOW	–6	LOW	1	HiZ	LOW	–8	5
LOW	–6	LOW	1	HiZ	HiZ	–8	6.5
LOW	–6	LOW	1	HiZ	HIGH	–8	8.3
LOW	–6	LOW	1	HIGH	LOW	–11	10
LOW	–6	LOW	1	HIGH	HiZ	–11	11.9
LOW	–6	LOW	1	HIGH	HIGH	–11	13.9
LOW	–6	HIGH	6.8	LOW	LOW	0.8	1.3
LOW	–6	HIGH	6.8	LOW	HiZ	0.8	2
LOW	–6	HIGH	6.8	LOW	HIGH	0.8	3.6
LOW	–6	HIGH	6.8	HiZ	LOW	–2.2	5
LOW	–6	HIGH	6.8	HiZ	HiZ	–2.2	6.5
LOW	–6	HIGH	6.8	HiZ	HIGH	–2.2	8.3
LOW	–6	HIGH	6.8	HIGH	LOW	–5.2	10
LOW	–6	HIGH	6.8	HIGH	HiZ	–5.2	11.9
LOW	–6	HIGH	6.8	HIGH	HIGH	–5.2	13.9
HIGH	0	LOW	1	LOW	LOW	1	1.3
HIGH	0	LOW	1	LOW	HiZ	1	2
HIGH	0	LOW	1	LOW	HIGH	1	3.6
HIGH	0	LOW	1	HiZ	LOW	–2	5
HIGH	0	LOW	1	HiZ	HiZ	–2	6.5
HIGH	0	LOW	1	HiZ	HIGH	–2	8.3
HIGH	0	LOW	1	HIGH	LOW	–5	10
HIGH	0	LOW	1	HIGH	HiZ	–5	11.9
HIGH	0	LOW	1	HIGH	HIGH	–5	13.9
HIGH	0	HIGH	6.8	LOW	LOW	6.8	1.3
HIGH	0	HIGH	6.8	LOW	HiZ	6.8	2
HIGH	0	HIGH	6.8	LOW	HIGH	6.8	3.6
HIGH	0	HIGH	6.8	HiZ	LOW	3.8	5
HIGH	0	HIGH	6.8	HiZ	HiZ	3.8	6.5
HIGH	0	HIGH	6.8	HiZ	HIGH	3.8	8.3
HIGH	0	HIGH	6.8	HIGH	LOW	0.8	10
HIGH	0	HIGH	6.8	HIGH	HiZ	0.8	11.9
HIGH	0	HIGH	6.8	HIGH	HIGH	0.8	13.9

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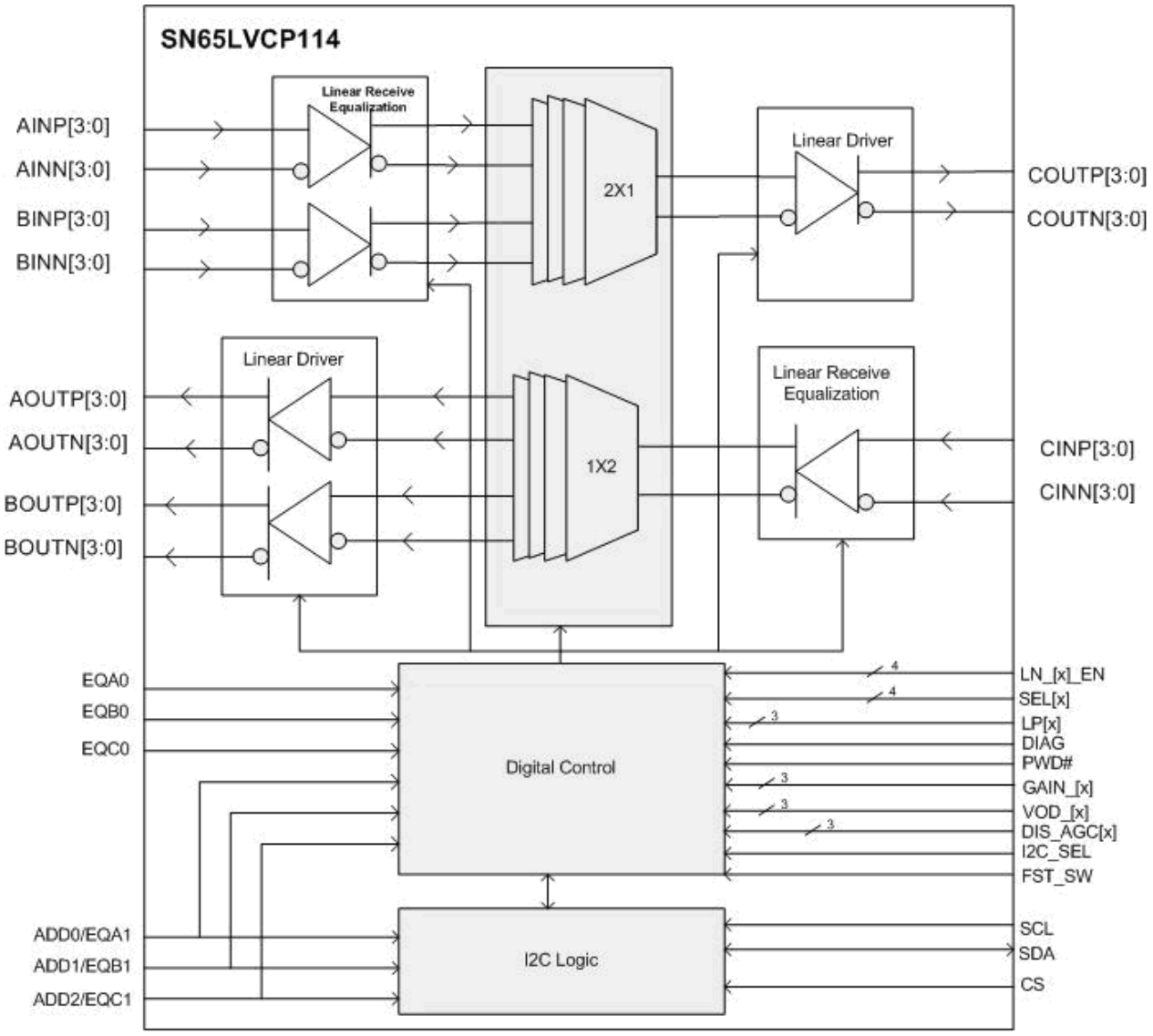
9 Detailed Description

9.1 Overview

The SN65LVCP114 device is an asynchronous, protocol-agnostic, low-latency QUAD mux, linear-redriver optimized for use in systems operating at up to 14.2 Gbps. The device linearly compensates for channel loss in backplane and active-cable applications. The architecture of SN65LVCP114 linear-redriver is designed to work effectively with ASIC or FPGA products implementing digital equalization using decision feedback equalizer (DFE) technology. The SN65LVCP114 mux, linear-redriver preserves the integrity of the received signal, ensuring optimum DFE and system performance. The SN65LVCP114 device provides a low-power mux-demux, linear-redriver solution while at the same time extending the effectiveness of DFE. The SN65LVCP114 device supports 2:1 MUX and 1:2 DEMUX with independent lane switching. For each receiver port, equalization can be independent. All ports support loop-back configuration. Configuration can be done through GPIO or an I^2C interface.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power Down

Use a 5-kΩ pullup for normal operation. To power down the SN65LVCP114, tie this pin to GND. In power-down mode, Inputs are off, outputs are disabled, and I^2C is reset. Power-down mode can be set, writing a 1 to register 0x00 bit 6.

9.3.2 Lane Enable

Each lane can be enabled individually using pin LN_x_EN or register 0x12[3:0]. This enables lane x for all ports.

Table 4. Lane Enable

LN_x_EN/REGISTER 0x12[3:0]	FUNCTION
0	Lane disabled
1	Lane enabled

9.3.3 Gain and Equalization

Equalization can be configured using EQx[1:0] pins or registers 0x03[3:0], 0x07[3:0], and 0x0B[3:0]. The SN65LVCP114 device includes several possible equalizations to select the optimum value. Also, the GAINx pin or registers 0x04[1:0], 0x08[1:0], and 0x0C[1:0] can be used to attenuate the input signal.

If input swing is larger than 600 mVpp, set gain to 0.5. Otherwise, set gain to 1.

Table 5. EQ Settings

EQx[1:0]	REGISTER 0x03[3:0], 0x07[3:0], 0x0B[3:0]	PEAKING (dB)
0b00	0b0XXX	1.3
0b0Z	0b1000	2
0b01	0b1001	3.6
0bZ0	0b1010	5
0bZZ	0b1011	6.5
0bZ1	0b1100	8.3
0b10	0b1101	10
0b1Z	0b1110	11.9
0b11	0b111	13.9

Table 6. RX DC Gain

GAINx	REGISTERS 0x04[1:0], 0x08[1:0], 0x0C[1:0]	GAIN
0	0bX0	0.5 (–6 dB)
1	0bX1	1 (0 dB)

9.3.4 VOD

Output swing can be selected between two ranges with an associated gain. Notice the range sets a maximum value not a constant value.

Table 7. Output Swing

VOD_x	REGISTERS 0x04[5:4], 0x08[5:4], 0x0C[5:4]	MAXIMUM VALUE	GAIN
0	0b01	0.6 V	1.1 (1 dB)
1	0b00, 0b10, 0b11	1.2 V	2.2 (6.8 dB)

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9.3.5 AGC

When AGC is enabled, the part-to-part gain variation can be reduced. AGC can be disabled for each port through DIS_AGCx or registers 0x02[0], 0x06[0], and 0x0A[0].

Table 8. AGC Enable

DIS_AGCx/REGISTERS 0x02[0], 0x06[0], 0x0A[0]	FUNCTION
0	AGC loop enabled
1	AGC loop disabled

9.3.6 GPIO or I^{2}C Configuration

To configure this device using GPIO, set I2C_SEL = LOW. Using GIO, you have access to the most of the configuration, to power down the device, control equalization, select port, select VOD range, set loop-back mode, set diagnostic mode, enable lanes, enable AGC, select gain, and enable fast switching.

To configure this device using I^{2}C set I2C_SEL = HIGH. Besides the configuration you have with GPIO, using I^{2}C allows you to disable outputs, power-down inputs and switch polarity of outputs. In this mode, use pins ADDx to set I^{2}C address. See *Programming* for a detailed explanation.

9.3.7 Fast Switching

Idle outputs can be disabled or squelched. When outputs are squelched, switching is faster; when outputs are disabled, power is saved. This configuration is done with the FST_SW pin or registers 0x02[3], 0x06[3], and 0x0A[3].

Table 9. Fast Switching

FST_SW/REGISTER 0x02[3], 0x06[3], 0x0A[3]	FUNCTION
0	Disable idle outputs
1	Squelch idle outputs

9.3.8 Power-Down Input Stages

Each port can power down its input stages to save power when not used. Power down affects all the lanes of the port; to configure it, use registers 0x03[7], 0x07[7], and 0x08[7] for port A, B, and C respectively.

Table 10. Power Down

REGISTERS 0x03[7], 0x07[7], 0x08[7]	FUNCTION
0	Normal
1	Power down

9.3.9 Disable Output Lanes

The SN65LVCP114 device can disable every output lane independently. Use register 0x02[7:4] to disable output lanes of port A, register 0x06[7:4] to disable output lanes of port B, and register 0x0A[7:4] to disable output lanes of port C.

Table 11. Disable Output Lanes

REGISTERS 0x03[7], 0x07[7], 0x08[7]	FUNCTION
0	Enabled
1	Disabled

9.3.10 Polarity Switch

Every lane can switch its polarity independently. Port A is configured through register 0x10[3:0], port B is configured through register 0x10[7:4], and port C is configured through register 0x11[3:0]. See Table 16 for a detailed explanation.

9.4 Device Functional Modes

The SN65LVCP114 device has three modes of operation: Normal mode, loopback mode, and diagnostic mode. For all possible combinations of these modes, see Table 2.

9.4.1 Normal Mode

In this mode, the SN65LVCP114 functions like a switch. C port will connect to A or B port depending on values of SELx or register 0x01[3:0], each lane is configured independently.

Table 12. Port Select

SELx/REGISTER 0x01[3:0]	PORT CONNECTED TO C
0	A
1	B

9.4.2 Loopback

In loopback mode, the selected port transmits on its output what it is receiving on its input. Each port has independent loopback configuration. This configuration can be selected using the LPx pins or register 0x01[6:4]. See Figure 14 for a graphical representation.

Table 13. Loopback Mode

LPx/REGISTER 0x01[6:4]	FUNCTION
0	Loop disabled
1	Loop enabled

9.4.3 Diagnostic

When in diagnostic mode, data incoming on port C is reflected in both A and B ports. Data outgoing on port C depends on the value of SELx. This mode can be selected using DIAG pin or register 0x01[7]. See Figure 15 for a graphical representation.

Table 14. Diagnostic Mode

DIAG/REGISTER 0x01[7]	FUNCTION
0	Diagnostic disabled
1	Diagnostic enabled

9.5 Programming

9.5.1 Two-Wire Serial Interface and Control Logic

The SN65LVCP114 device uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCL pins require external 10-kΩ pullups to V_{CC}.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The SN65LVCP114 device is a slave device only, which means that it cannot initiate a transmission itself; it always relies on the availability of the SCL signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0000ADD[2:0]) followed by an 8th bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD[2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7-bit slave address is 0000000.
3. 8-bit register address
4. 8-bit register data word

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Programming (continued)

5. STOP command

Regarding timing, the SN65LVCP114 device is I^{2}C compatible. Figure 16 shows the typical timing, and Figure 17 shows the data transfer. Table 15 defines the parameters forFigure 16.

Bus Idle: Both SDA and SCL lines remain HIGH

Start data transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer:A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still must communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line, and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be considered. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

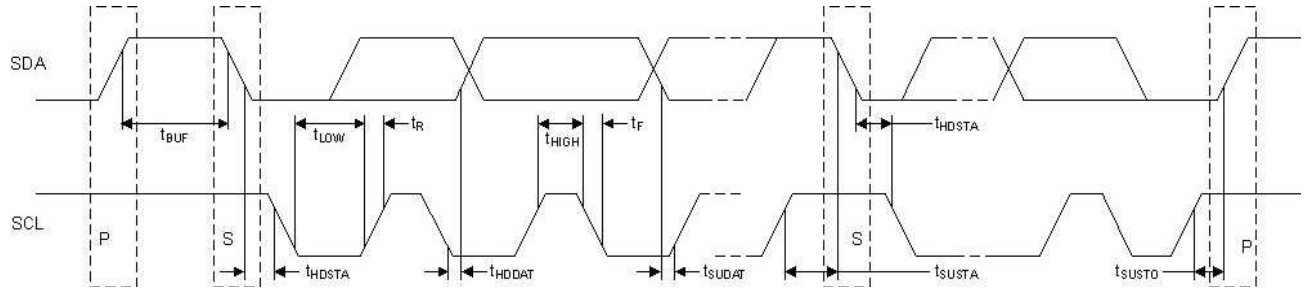

Figure 16. Two-Wire Serial Interface Timing Diagram

Table 15. Two-Wire Serial Interface Timing Diagram Definitions

PARAMETER		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated.	0.6		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HIGH}	High period of the SCL clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data hold time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

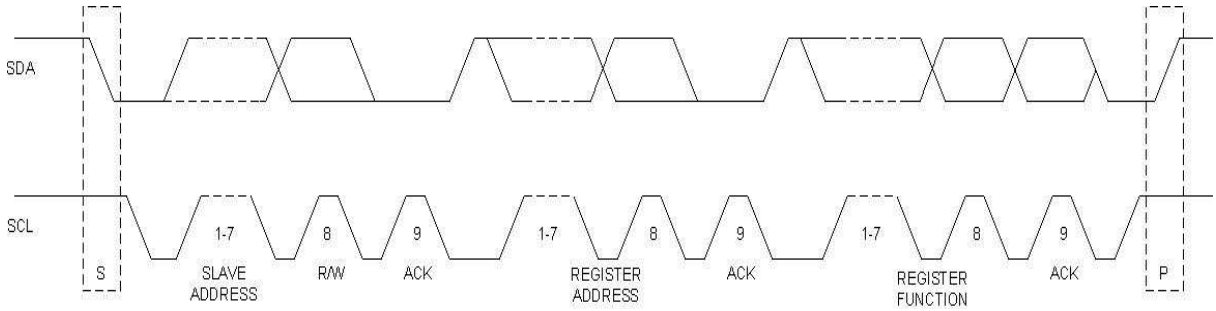

Figure 17. Two-Wire Serial Interface Data Transfer

9.6 Register Maps

9.6.1 SN65LVCP114 Register Mapping Information

9.6.1.1 Register 0x00

Figure 18. Register 0x00 (General Device Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SW_GPIO	PWRDOWN						RSVD

9.6.1.2 Register 0x01

Figure 19. Register 0x01 (Device Control Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIAG	LOOP[C]	LOOP[B]	LOOP[A]	SEL[3]	SEL[2]	SEL[1]	SEL[0]

9.6.1.3 Register 0x02

Figure 20. Register 0x02 (Port A Control Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT_DIS_0	OUT_DIS_1	OUT_DIS_2	OUT_DIS_3	FAST_SW	RSVD		DIS_AGC

9.6.1.4 Register 0x03

Figure 21. Register 0x03 (Port A Input Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INOFF	RSVD	RSVD	RSVD	EQ3	EQ2	EQ1	EQ0

9.6.1.5 Register 0x04

Figure 22. Register 0x04 (Port A Output Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		VOD1	VOD0			GAIN1	GAIN0

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9.6.1.6 Register 0x06

Figure 23. Register 0x06 (Port B Control Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT_DIS_0	OUT_DIS_1	OUT_DIS_2	OUT_DIS_3	FAST_SW	RSVD		DIS_AGC

9.6.1.7 Register 0x07

Figure 24. Register 0x07 (Port B Input Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INOFF	RSVD	RSVD	RSVD	EQ3	EQ2	EQ1	EQ0

9.6.1.8 Register 0x08

Figure 25. Register 0x08 (Port B Output Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		VOD1	VOD0			GAIN1	GAIN0

9.6.1.9 Register 0x0A

Figure 26. Register 0x0A (Port C Control Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT_DIS_0	OUT_DIS_1	OUT_DIS_2	OUT_DIS_3	FAST_SW	RSVD		DIS_AGC

9.6.1.10 Register 0x0B

Figure 27. Register 0x0B (Port C Input Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INOFF	RSVD	RSVD	RSVD	EQ3	EQ2	EQ1	EQ0

9.6.1.11 Register 0x0C

Figure 28. Register 0x0C (Port C Output Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		VOD1	VOD0			GAIN1	GAIN0

9.6.1.12 Register 0x0D

Figure 29. Register 0x0D (Reserved Settings) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

9.6.1.13 Register 0x0F

Figure 30. Register 0x0F (Reserved Settings) Read Only

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

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9.6.1.14 Register 0x10

Figure 31. Register 0x10 (Polarity Control Settings for Port A and B) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
POL_B[3]	POL_B[2]	POL_B[1]	POL_B[0]	POL_A[3]	POL_A[2]	POL_A[1]	POL_A[0]

9.6.1.15 Register 0x11

Figure 32. Register 0x11 (Polarity Control Settings for Port C) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				POL_C[3]	POL_C[2]	POL_C[1]	POL_C[0]

9.6.1.16 Register 0x12

Figure 33. Register 0x12 (Lane Enable) R/W

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				LN_EN[3]	LN_EN[2]	LN_EN[1]	LN_EN[0]

9.6.1.17 Register Descriptions

Table 16. SN65LVCP114 Register Descriptions

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x00	7	SW_GPIO	Switching logic is controlled by GPIO or I^2C: 1 = GPIO control 0 = I^2C control	00000000
	6	PWRDOWN	Power down the device: 0 = Normal operation 1 = Power down	
	5			
	4			
	3			
	2			
	1			
	0	RSVD	For TI use only	

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Table 16. SN65LVCP114 Register Descriptions (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x01	7	DIAG	Enables Diag Mode: 0 = Disable 1 = Enable	00000000
	6	LOOP[C]	Enables port C loopback: 0 = Disable 1 = Enable	
	5	LOOP[B]	Enables port B loopback: 0 = Disable 1 = Enable	
	4	LOOP[A]	Enables port A loopback: 0 = Disable 1 = Enable	
	3	SEL[3]	Lane 3, port A or port B switch control: 0 = Port A selected 1 = Port B selected	
	2	SEL[2]	Lane 2, port A or port B switch control: 0 = Port A selected 1 = Port B selected	
	1	SEL[1]	Lane 1, port A or port B switch control: 0 = Port A selected 1 = Port B selected	
	0	SEL[0]	Lane 0, port A or port B switch control: 0 = Port A selected 1 = Port B selected	
0x02 0x06 0x0A	7	OUT_DIS0	Disables output lane 0: 0 = Enable 1 = Disable	00001100
	6	OUT_DIS1	Disables output lane 1: 0 = Enable 1 = Disable	
	5	OUT_DIS2	Disables output lane 2: 0 = Enable 1 = Disable	
	4	OUT_DIS3	Disables output lane 3: 0 = Enable 1 = Disable	
	3	FAST_SW	Fast switch: 0 = Idle outputs are disabled (save power) 1 = Idle outputs are squelched (fast switch time)	
	2	RSVD	For TI use only	
	1			
	0	DIS_AGC	AGC loop: 0 = Enable 1 = Disable	
0x03 0x07 0x0B	7	IN_OFF	Power down input stages: 0 = Normal 1 = Power down	00000000
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	EQ3	Selects peaking equalization. Register 0x03 configures PortA, 0x07 configures port B and 0x0B configures port C. Refer to table x in feature description for detailed information.	

Table 16. SN65LVCP114 Register Descriptions (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x04 0x08 0x0C	7			00000000
	6			
	5	VOD1	VOD control [VOD1:VOD0]: 00 = 1200 mV maximum 01 = 600 mV maximum 10 = 1200 mV maximum 11 = 1200 mV maximum	
	4	VOD0		
	3			
	2			
	1	GAIN1	GAIN control [GAIN1:GAIN0]: 00 = 0.5 01 = 1 10 = 0.5 11 = 1	
	0	GAIN0		
0x05 0x09 0x0E	7			00000000
	6			
	5			
	4			
	3			
	2			
	1			
	0			
0x0D	7	RSVD	For TI use only	00000000
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	
0x0F	7	RSVD	For TI use only	00010001
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	

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Table 16. SN65LVCP114 Register Descriptions (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x10	7	POL_B[3]	Polarity switch of output lane 3 of port B: 0 = Normal 1 = Switched	00000000
	6	POL_B[2]	Polarity switch of output lane 2 of port B: 0 = Normal 1 = Switched	
	5	POL_B[1]	Polarity switch of output lane 1 of port B: 0 = Normal 1 = Switched	
	4	POL_B[0]	Polarity switch of output lane 0 of port B 0 = Normal 1 = Switched	
	3	POL_A[3]	Polarity switch of output lane 3 of port A: 0 = Normal 1 = Switched	
	2	POL_A[2]	Polarity switch of output lane 2 of port A: 0 = Normal 1 = Switched	
	1	POL_A[1]	Polarity switch of output lane 1 of port A: 0 = Normal 1 = Switched	
	0	POL_A[0]	Polarity switch of output lane 0 of port A: 0 = Normal 1 = Switched	
0x11	7			00000000
	6			
	5			
	4			
	3	POL_C[3]	Polarity switch of output lane 3 of port C: 0 = Normal 1 = Switched	
	2	POL_C[2]	Polarity switch of output lane 2 of port C: 0 = Normal 1 = Switched	
	1	POL_C[1]	Polarity switch of output lane 1 of port C: 0 = Normal 1 = Switched	
	0	POL_C[0]	Polarity switch of output lane 0 of port C: 0 = Normal 1 = Switched	

Table 16. SN65LVCP114 Register Descriptions (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x12	7			00001111
	6			
	5			
	4			
	3	LN_EN_3	Lane 3 of ports A, B, and C: 0 = Disable 1 = Enable	
	2	LN_EN_2	Lane 2 of ports A, B, and C: 0 = Disable 1 = Enable	
	1	LN_EN_1	Lane 1 of ports A, B, and C: 0 = Disable 1 = Enable	
	0	LN_EN_0	Lane 0 of ports A, B, and C: 0 = Disable 1 = Enable	

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65LVCP114 device has enough equalization to be placed on the receiver side and compensate traces up to 24 inches. The SN65LVCP114 device can be placed on transmitter side and still have an open eye after a trace of 24 inches.

10.2 Typical Applications

10.2.1 Transmit-Side Typical Application

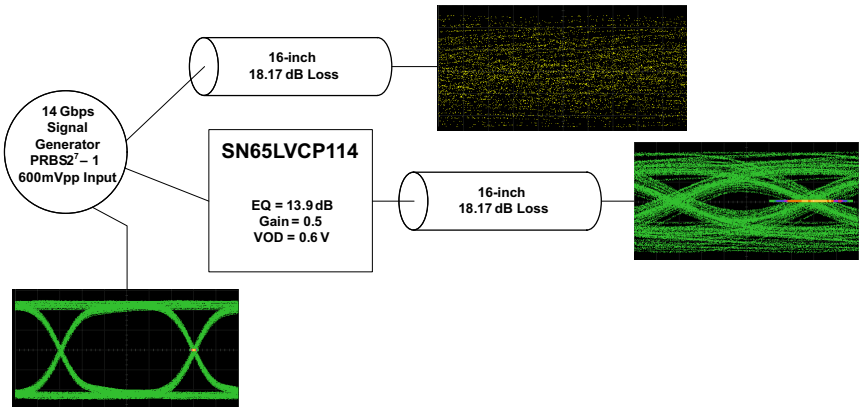

Figure 34. Transmit-Side Typical Application

10.2.1.1 Design Requirements

Table 17 lists the design parameters of the SN65LVCP114.

Table 17. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	3.3 V
VOD	600 mV
EQ	13.9 dB
GAIN	0.5 (–6 dB)
Trace length	16 inches

10.2.1.2 Detailed Design Procedure

- Determine the loss profile between transmitter and receiver.
- Based upon loss profile and signal swing, determine the optimal equalization settings.
- Select appropriate voltage output swing.
- If required select correct differential pair polarity.
- To set voltage logic levels on configuration pins, use a 5-kΩ pullup for high level, tie pin to GND for low level, and place a 5-kΩ pullup and 5-kΩ pulldown for HiZ.

10.2.1.3 Application Curves

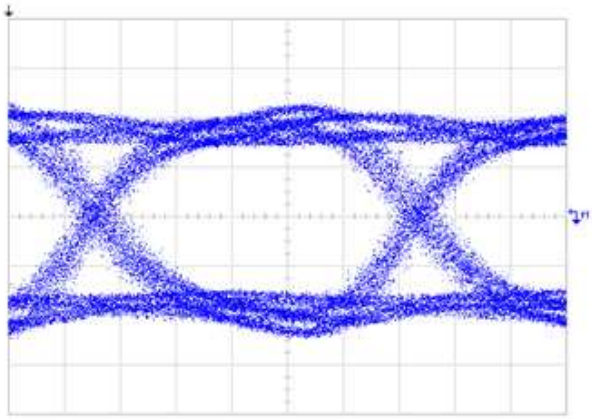

Figure 35. Input to SN65LVCP114

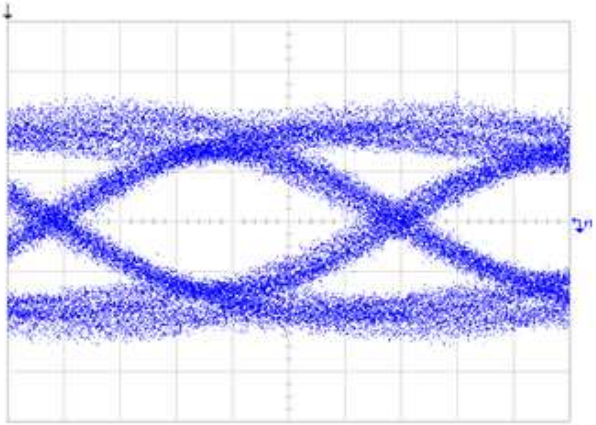

Figure 36. Output to SN65LVCP114 After Trace

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10.2.2 Receive-Side Typical Application

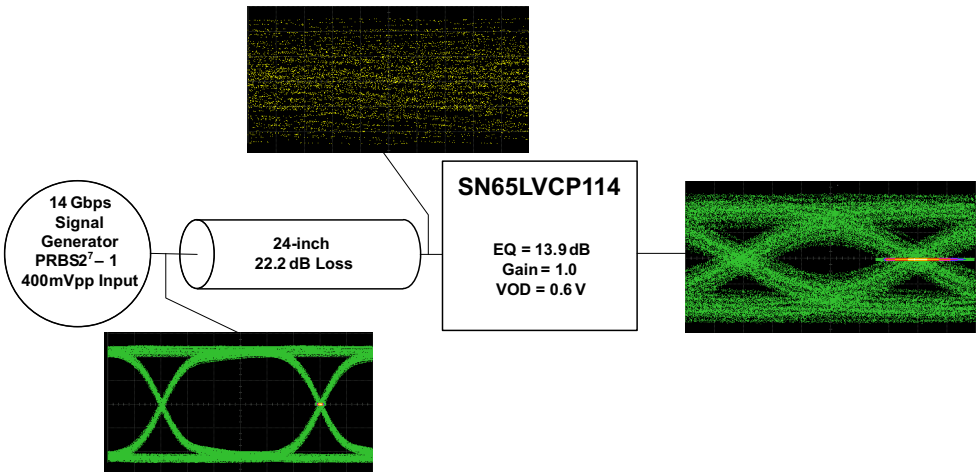

Figure 37. Receive-Side Typical Application

10.2.2.1 Design Requirements

Table 18 lists the design parameters of the SN65LVCP114.

Table 18. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	3.3 V
VOD	600 mV
EQ	13.9 dB
Gain	1 (0 dB)
Trace lenght	24 inches

10.2.2.2 Detailed Design Procedure

- Determine the loss profile between transmitter and receiver.
- Based upon the loss profile and signal swing, determine the optimal equalization settings.
- Select appropriate voltage output swing.
- If required, select the correct differential pair polarity.
- To set voltage logic levels on configuration pins, use a 5-kΩ pullup for high level, tie pin to GND for low level, and place a 5-kΩ pullup and 5-kΩ pulldown for HiZ.

10.2.2.3 Application Curves

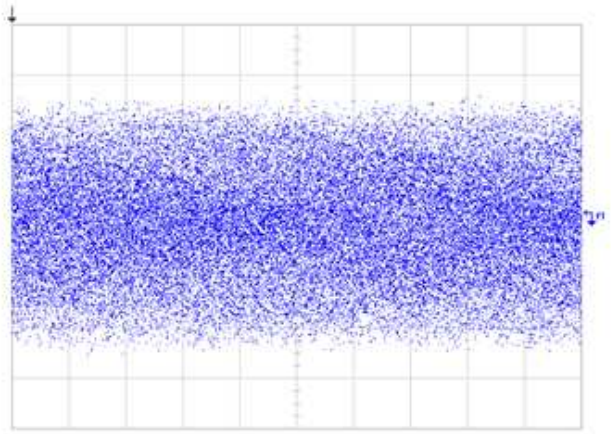

Figure 38. Input to SN65LVCP114

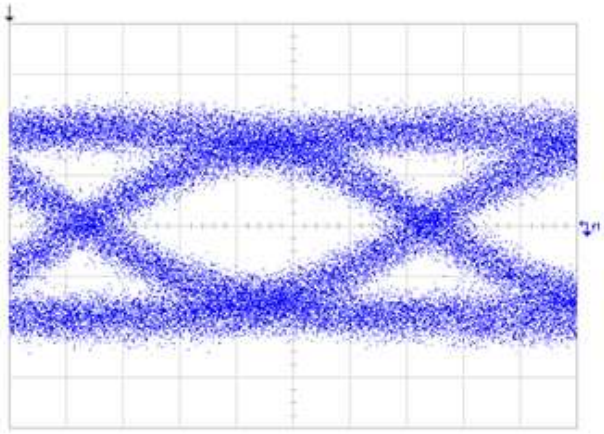

Figure 39. Output to SN65LVCP114 After Trace

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11 Power Supply Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65LVCP114 power pins. TI recommends placing one 0.01-µF and one 0.1-µF ceramic capacitors at each power pin. The distance between the SN65LVCP114 and capacitors must be minimized to reduce loop inductance and provide optimal noise filtering. A 100-pF ceramic capacitor can be placed at each power pin to optimize the EMI performance.

12 Layout

12.1 Layout Guidelines

TI recommends using at a minimum a four-layer stack-up to accomplish a low-EMI PCB design.

- It is important to match the electrical length of these high-speed traces to minimize both inter-pair and intrapair skew.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high frequency bypass capacitance significantly

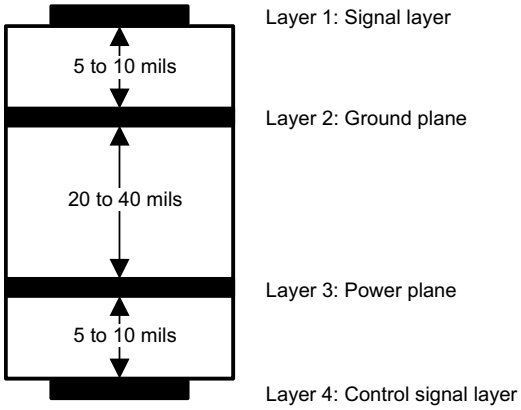

Figure 40. PCB Stack

12.2 Layout Example

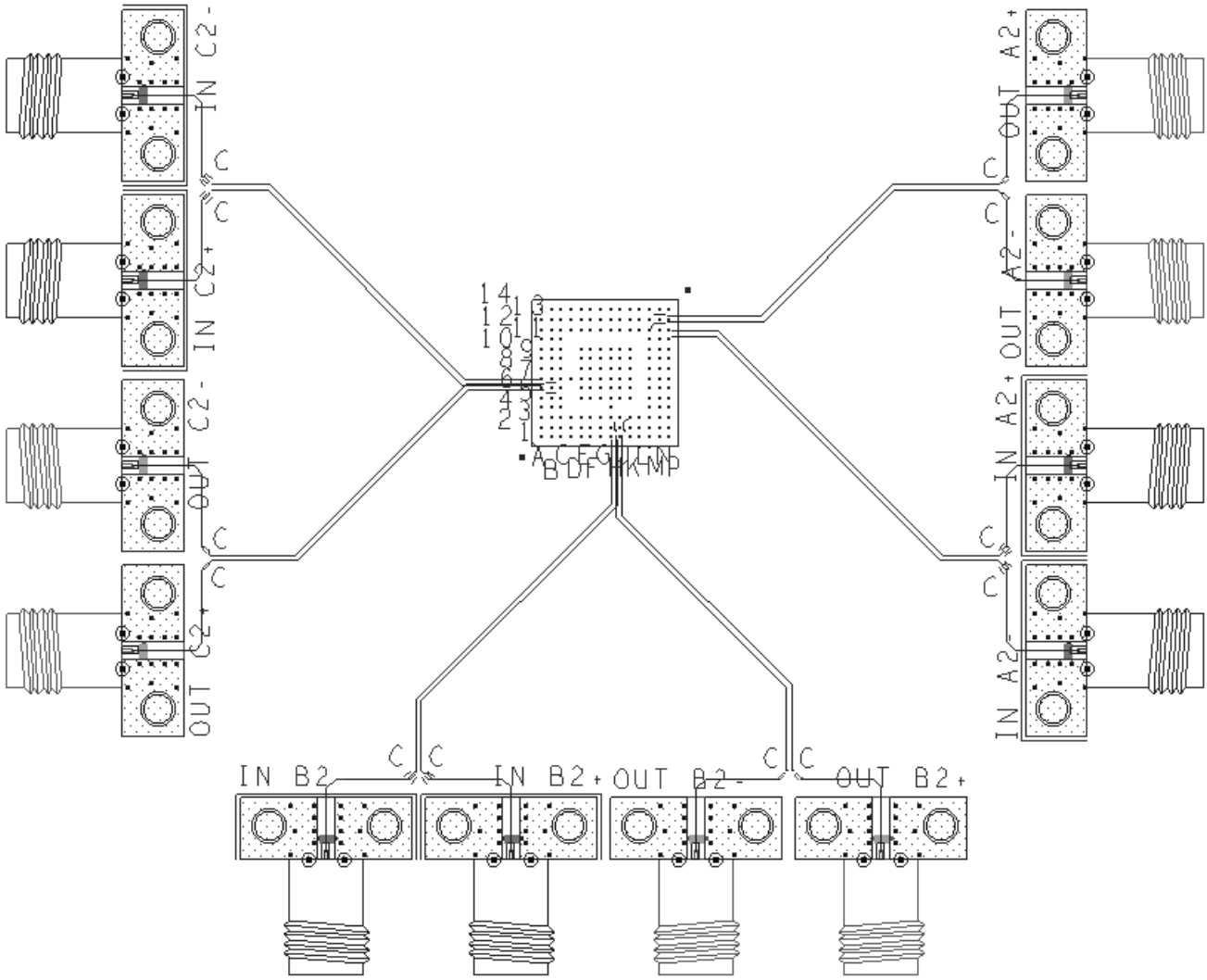

Figure 41. Layout Example

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documenation

For related documentation, see the following:

SN65LVCP114 Guidelines for Skew Compensation, SLLA323.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

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13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVCP114ZJA	Obsolete	Production	NFBGA (ZJA) | 167	-	-	Call TI	Call TI	-40 to 85	SN65LVCP114

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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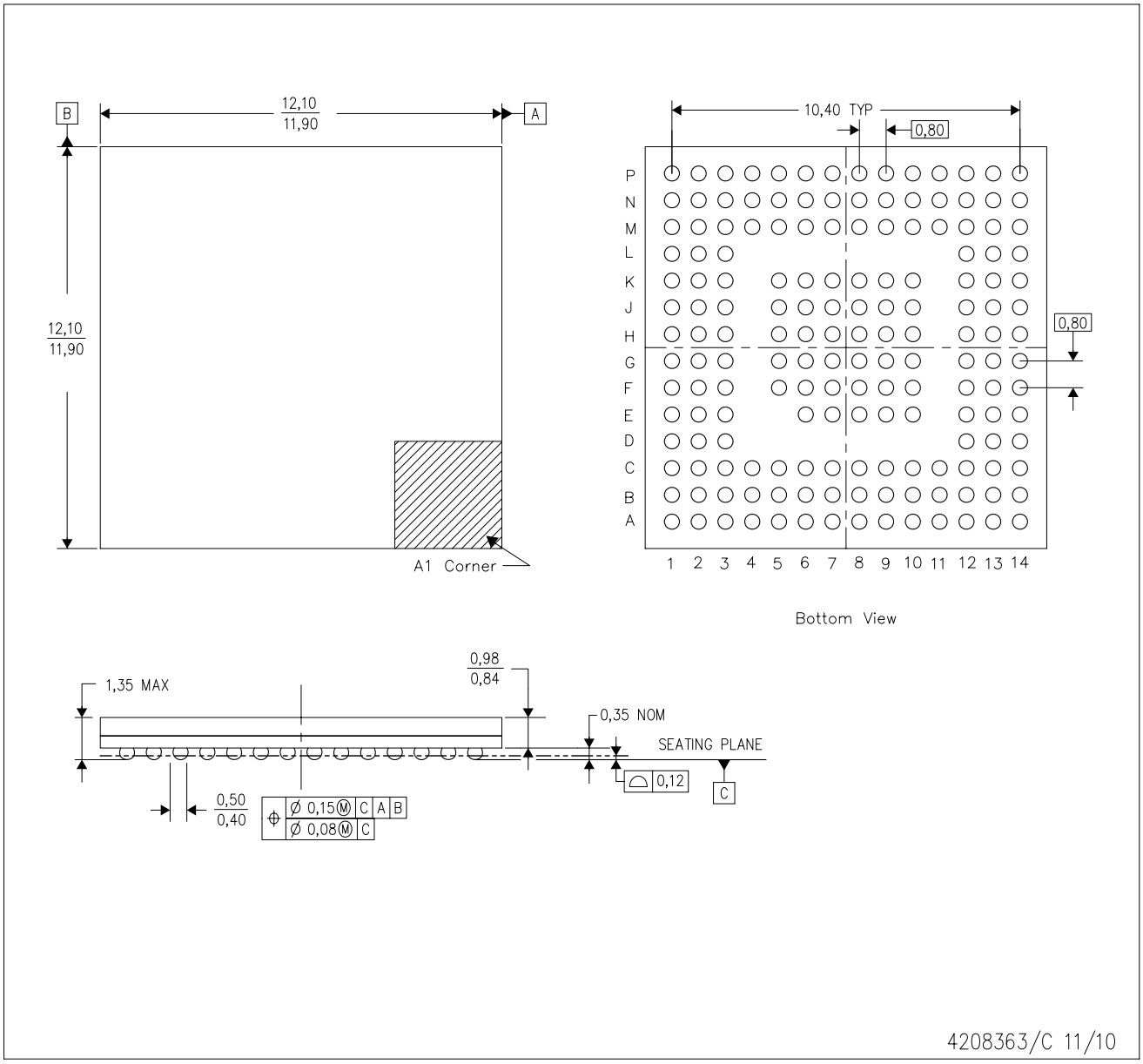
ZJA (S–PBGA–N167) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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