

SN74AC240-Q1 Automotive Octal Buffer/Driver with 3-State Outputs

1 Features

- Qualified for automotive applications
- Operation of 2V to 6V V_{CC}
- Inputs accept voltages to 6V
- Max t_{pd} of 6.5ns at 5V

2 Applications

- [Debounce a switch](#)
- [Redrive digital signals](#)
- [Drive transmission lines with logic](#)

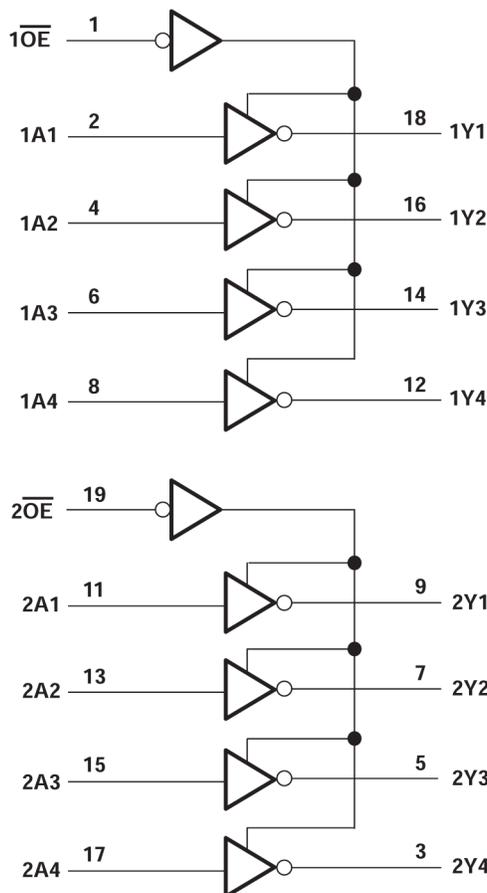
3 Description

This octal buffer and line driver is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE ⁽³⁾ |
|--------------|------------------------|-----------------------------|--------------------------|
| SN74AC240-Q1 | PW (TSSOP, 20) | 6.5mm × 6.4mm | 6.5mm × 4.4mm |

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

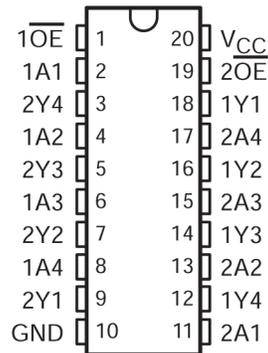


Figure 4-1. DW or PW Package (Top View)

Table 4-1. Pin Functions

| NAME ⁽¹⁾ | PIN | TYPE | DESCRIPTION |
|---------------------|-----|------|-----------------|
| 1OE | 1 | I | Output enable 1 |
| 1A1 | 2 | I | 1A1 input |
| 2Y4 | 3 | O | 2Y4 output |
| 1A2 | 4 | I | 1A2 input |
| 2Y3 | 5 | O | 2Y3 output |
| 1A3 | 6 | I | 1A3 input |
| 2Y2 | 7 | O | 2Y2 output |
| 1A4 | 8 | I | 1A4 input |
| 2Y1 | 9 | O | 2Y1 output |
| GND | 10 | — | Ground pin |
| 2A1 | 11 | I | 2A1 input |
| 1Y4 | 12 | O | 1Y4 output |
| 2A2 | 13 | I | 2A2 input |
| 1Y3 | 14 | O | 1Y3 output |
| 2A3 | 15 | I | 2A3 input |
| 1Y2 | 16 | O | 1Y2 output |
| 2A4 | 17 | I | 2A4 input |
| 1Y1 | 18 | O | 1Y1 output |
| 2OE | 19 | I | Output enable 2 |
| VCC | 20 | — | Power pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------------------------|---------------------------|---|-----------------------|--------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| V _I ⁽²⁾ | Input voltage range | -0.5 | V _{CC} + 0.5 | V |
| V _O ⁽²⁾ | Output voltage range | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | (V _I < 0 or V _I > V _{CC}) | | ±20 mA |
| I _{OK} | Output clamp current | (V _O < 0 or V _O > V _{CC}) | | ±20 mA |
| I _O | Continuous output current | (V _O = 0 to V _{CC}) | | ±50 mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-------------------------|-----------------|------|
| V _{CC} | Supply voltage | 2 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 3 V | 2.1 | V |
| | | V _{CC} = 4.5 V | 3.15 | |
| | | V _{CC} = 5.5 V | 3.85 | |
| V _{IL} | Low-level input voltage | V _{CC} = 3 V | 0.9 | V |
| | | V _{CC} = 4.5 V | 1.35 | |
| | | V _{CC} = 5.5 V | 1.65 | |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 3 V | -12 | mA |
| | | V _{CC} = 4.5 V | -24 | |
| | | V _{CC} = 5.5 V | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 3 V | 12 | mA |
| | | V _{CC} = 4.5 V | 24 | |
| | | V _{CC} = 5.5 V | 24 | |
| Δt/Δv | Input transition rise or fall rate | | 8 | ns/V |
| T _A | Operating free-air temperature | -40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | DW | PW | UNIT | |
|-------------------------------|---|---------|-------|------|
| | 20 PINS | 20 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽²⁾ | 58 | 126.2 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | T _A = -40°C TO 125°C | | T _A = -40°C TO 85°C | | UNIT |
|---|---|--|-----------------------|-----|------|---------------------------------|------|--------------------------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 3 V | 2.9 | | | 2.9 | | 2.9 | V | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{OH} = -12 mA | 3 V | 2.56 | | | 2.4 | | 2.46 | | |
| | | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | I _{OH} = -24 mA | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| | I _{OH} = -50 mA ⁽¹⁾ | 5.5 V | | | | 3.85 | | | | |
| I _{OH} = -75 mA ⁽¹⁾ | 5.5 V | | | | | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 3 V | | | 0.1 | | 0.1 | 0.1 | V | |
| | | 4.5 V | | | 0.1 | | 0.1 | 0.1 | | |
| | | 5.5 V | | | 0.1 | | 0.1 | 0.1 | | |
| | I _{OL} = 12 mA | 3 V | | | 0.36 | | 0.5 | 0.44 | | |
| | | 4.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | I _{OL} = 24 mA | 5.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | I _{OL} = 50 mA ⁽¹⁾ | 5.5 V | | | | | 1.65 | | | |
| I _{OL} = 75 mA ⁽¹⁾ | 5.5 V | | | | | | 1.65 | | | |
| I _I | Data inputs | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | μA | |
| | Control inputs | V _I = V _{CC} or GND | | | | ±0.1 | | ±1 | | |
| I _{OZ} ⁽²⁾ | | V = V _{CC} or GND, V(OE) = V _{IL} or V _{IH} | 5.5 V | | | ±0.25 | | ±5 | ±2.5 | μA |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 80 | 40 | μA |
| C _i | | V _I = V _{CC} or GND | 5 V | | | 2.5 | | | | pF |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

5.5 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | T _A = 25°C | | | T _A = -40°C TO 125°C | | T _A = -40°C TO 85°C | | UNIT |
|------------------|--------------|-------------|-----------------------|-----|------|---------------------------------|------|--------------------------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | 1.5 | 6 | 8 | 1 | 11 | 1 | 9 | ns |
| t _{PHL} | | | 1.5 | 5.5 | 8 | 1 | 10.5 | 1 | 8.5 | |
| t _{PZH} | OE | Y | 1.5 | 6 | 10.5 | 1 | 11.5 | 1 | 11 | ns |
| t _{PZL} | | | 1.5 | 7 | 10 | 1 | 13 | 1 | 11 | |
| t _{PHZ} | OE | Y | 1.5 | 7 | 10 | 1 | 12.5 | 1 | 10.5 | ns |
| t _{PLZ} | | | 1.5 | 7.5 | 10.5 | 1 | 13.5 | 1 | 11.5 | |

5.6 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

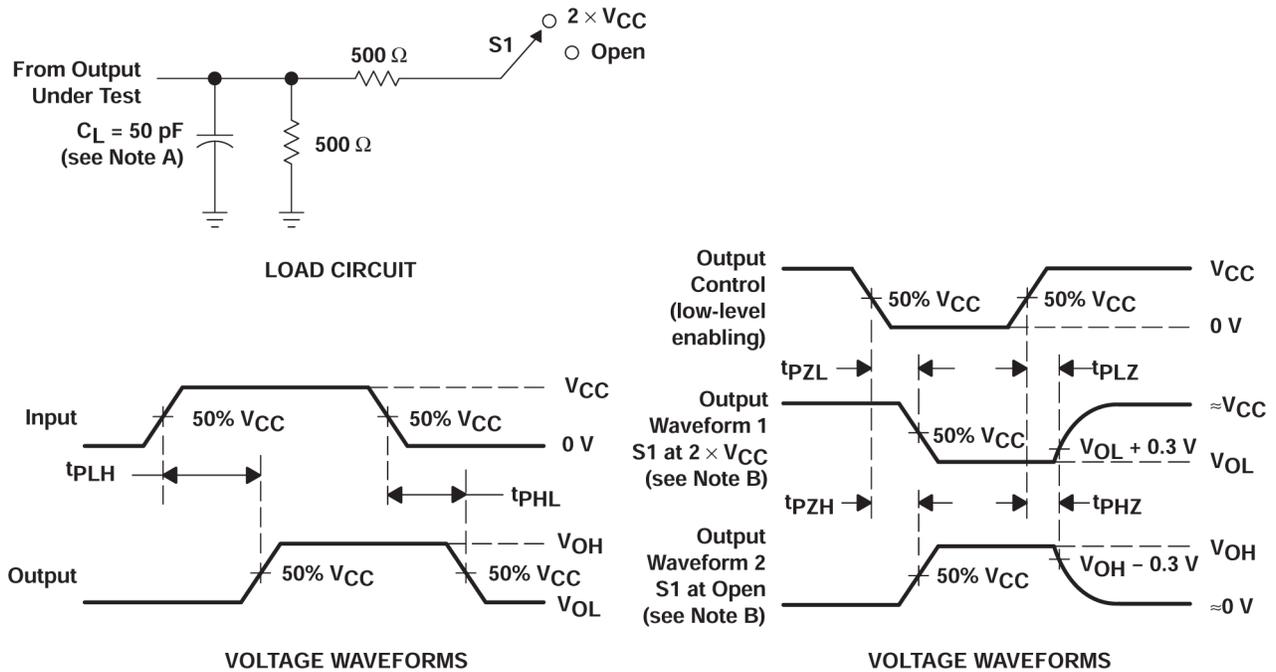
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C TO } 125^\circ\text{C}$ | | $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$ | | UNIT |
|-----------|------------------------|-------------|--------------------------|-----|-----|---|------|--|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1.5 | 4.5 | 6.5 | 1 | 8.5 | 1 | 7 | ns |
| t_{PHL} | | | 1.5 | 4.5 | 6 | 1 | 8 | 1 | 6.5 | |
| t_{PZH} | $\overline{\text{OE}}$ | Y | 1.5 | 5 | 7 | 1 | 9 | 1 | 8 | ns |
| t_{PZL} | | | 1.5 | 5.5 | 8 | 1 | 10.5 | 1 | 8.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Y | 2.5 | 6.5 | 9 | 1 | 10.5 | 1 | 9.5 | ns |
| t_{PLZ} | | | 2 | 6.5 | 9 | 1 | 11 | 1 | 9.5 | |

5.7 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|---|-----|------|
| C_{pd} Power dissipation capacitance per buffer/driver | $C_L = 50\text{ pF}$, $f = 1\text{ MHz}$ | 45 | pF |

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | Open |

7 Detailed Description

7.1 Overview

The SN74AC240 device is organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

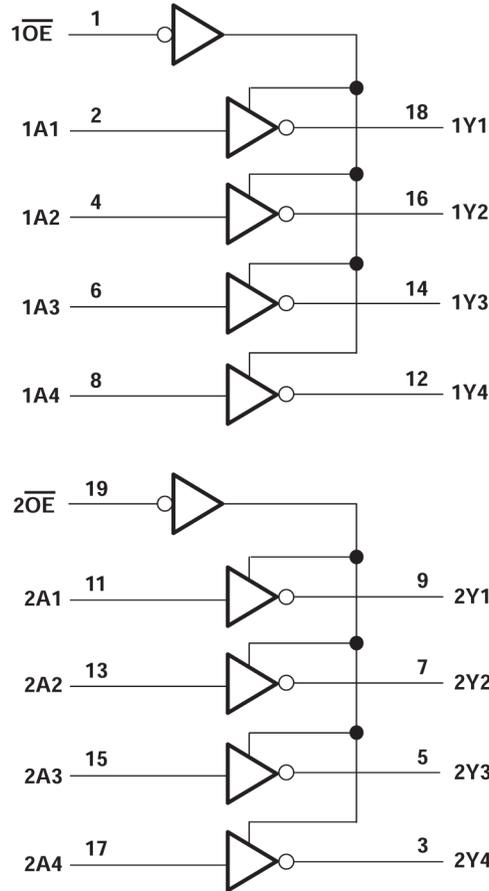


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

| INPUTS | | OUTPUT Y |
|-----------------|---|----------|
| \overline{OE} | A | |
| L | H | L |
| L | L | H |
| H | X | Z |

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.2.2 Layout Example

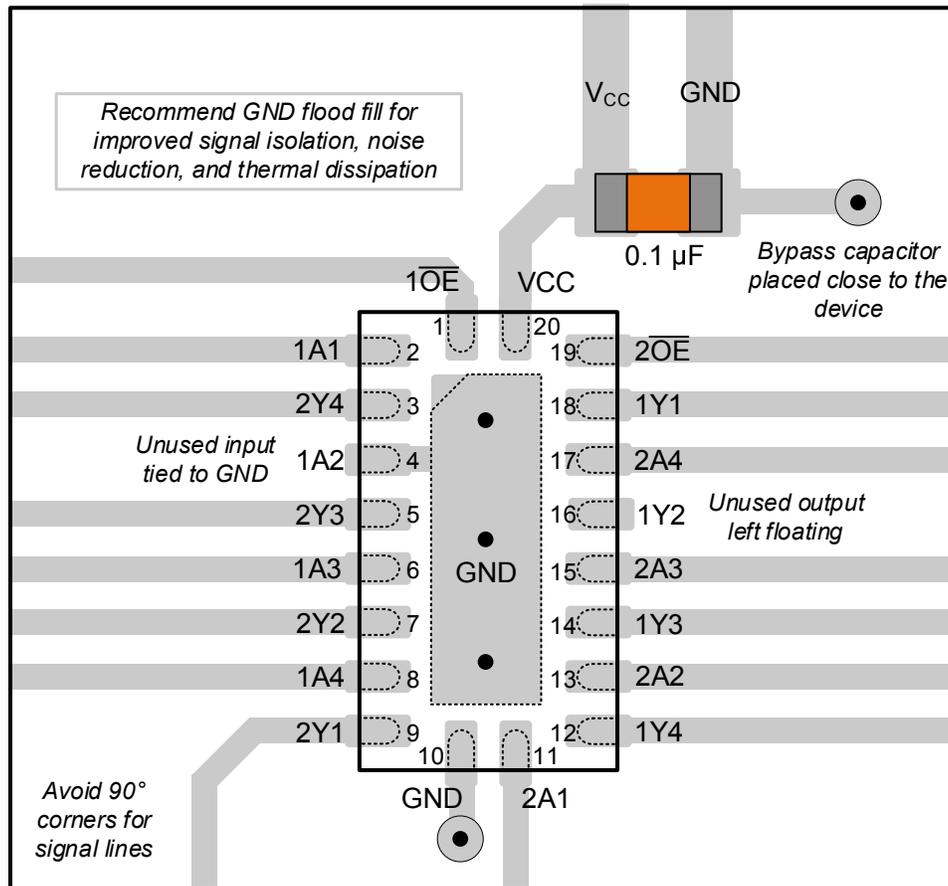


Figure 8-1. Example Layout for the SN74AC240-Q1

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74AC240-Q1 | Click here |

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (January 2008) to Revision B (March 2024) | Page |
|---|-------------|
| • Added <i>Applications</i> section, <i>Package Information</i> table, <i>Pin Functions</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Updated RθJA value: PW = 83 to 126.2, all values in °C/W | 4 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74AC240QPWRG4Q1 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC240Q | Samples |
| SN74AC240QPWRQ1 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC240Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

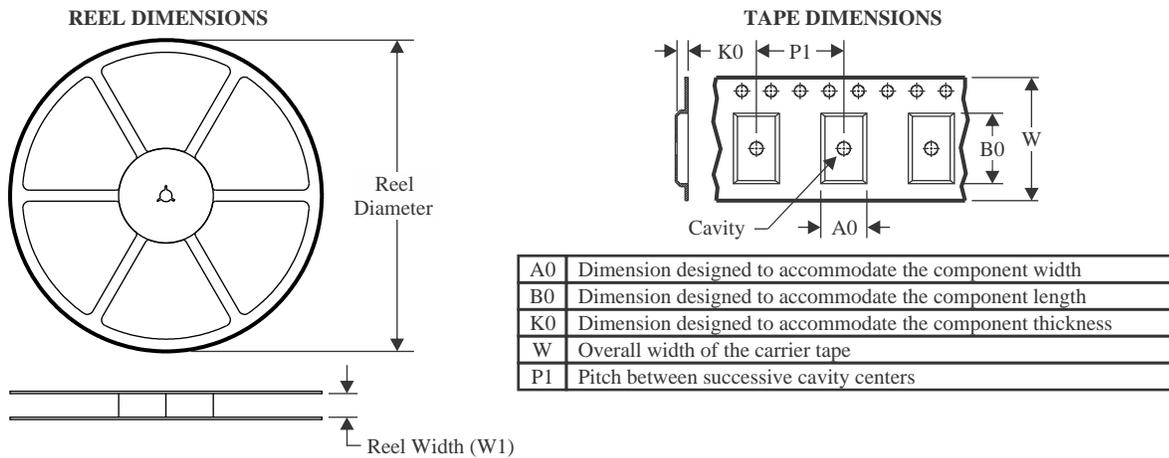
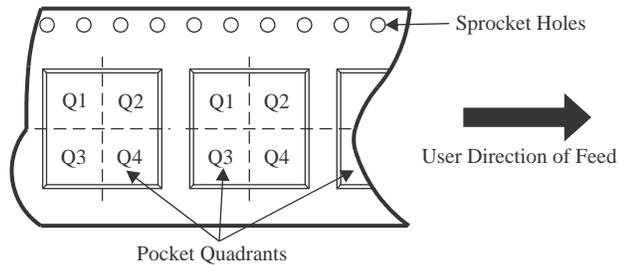
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AC240-Q1 :

- Catalog : [SN74AC240](#)
- Military : [SN54AC240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AC240QPWRG4Q1 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AC240QPWRQ1 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

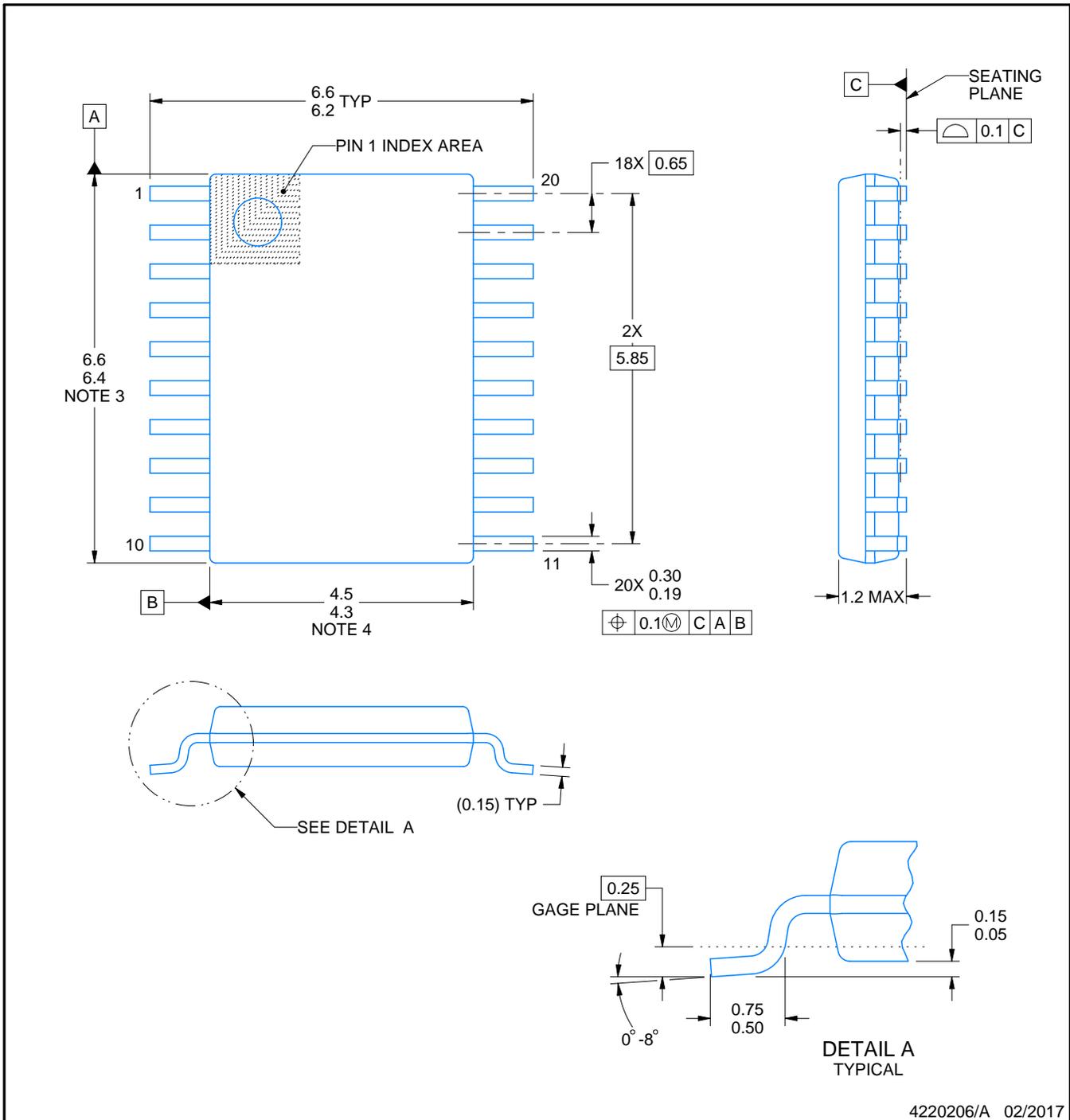
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AC240QPWRG4Q1 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AC240QPWRQ1 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

PW0020A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

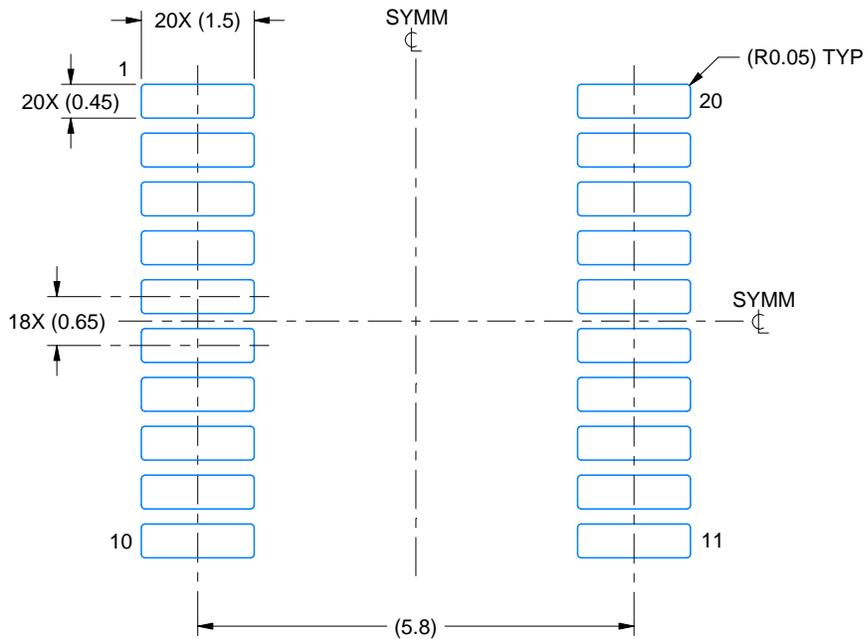
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

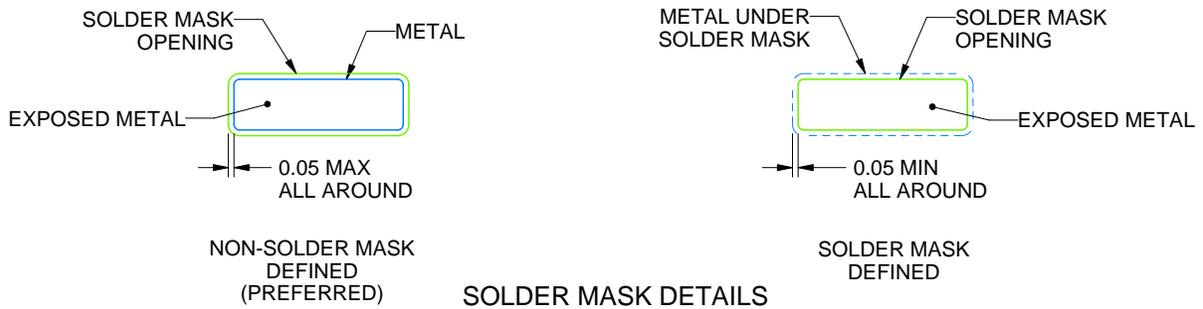
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

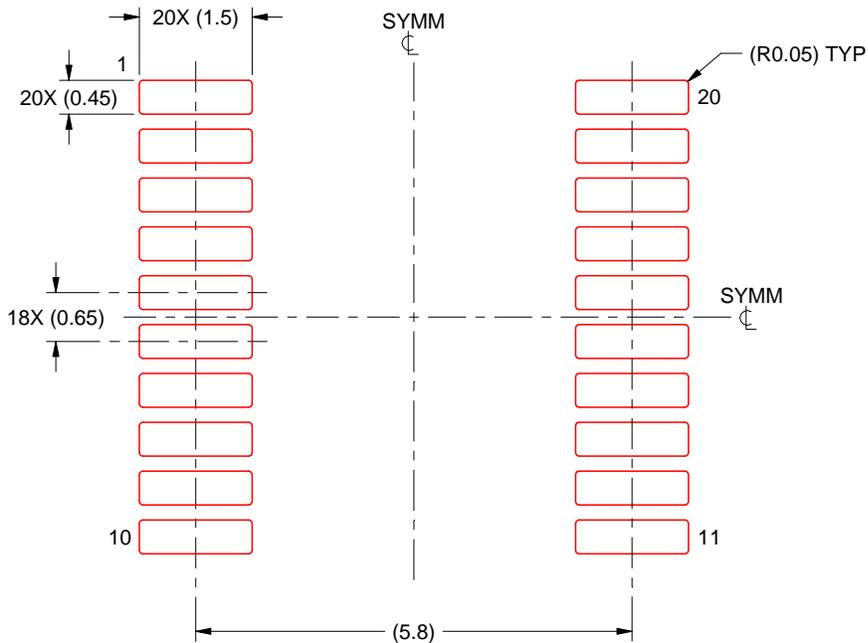
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

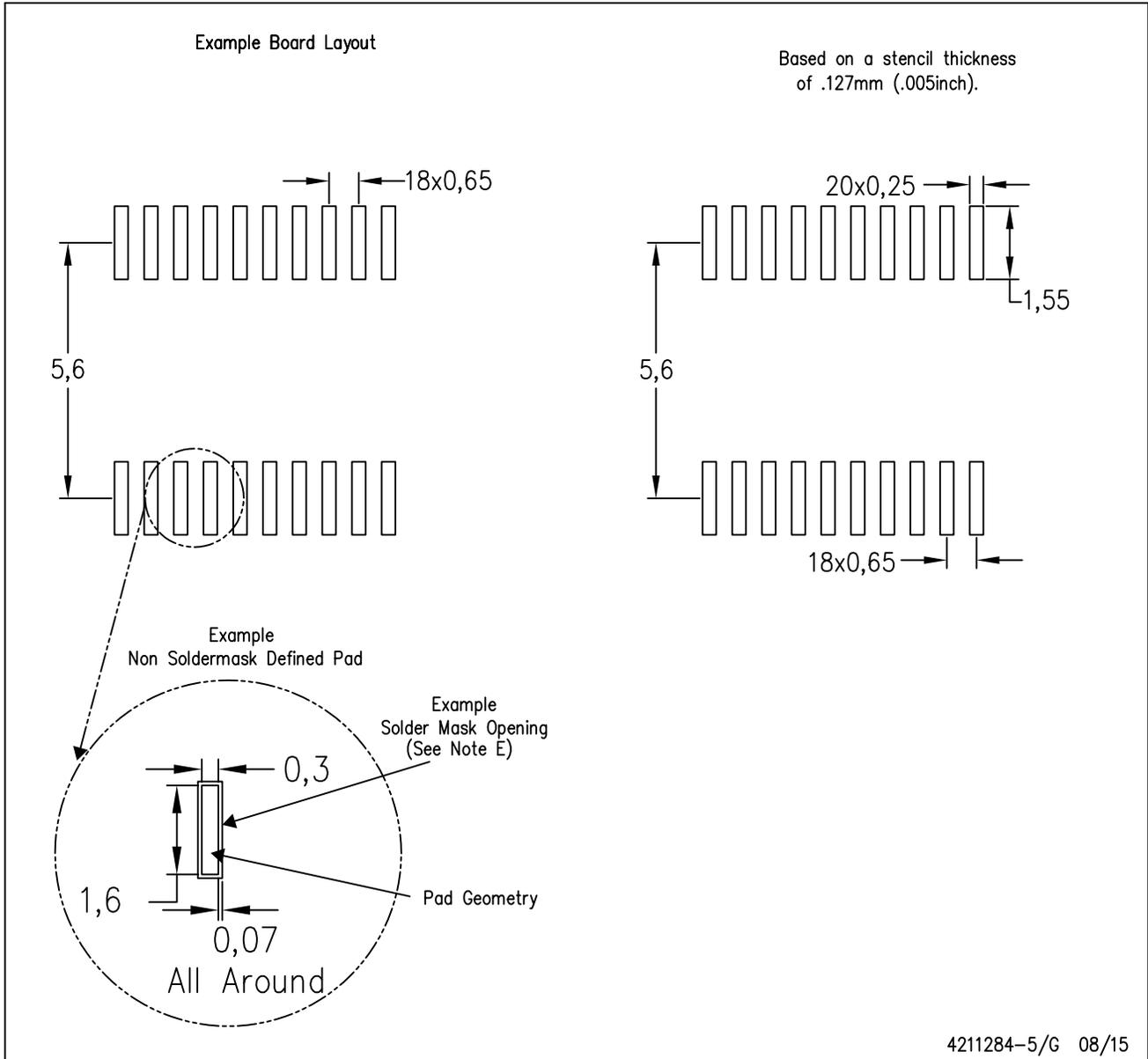
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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