

# SN74AS1008A QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER

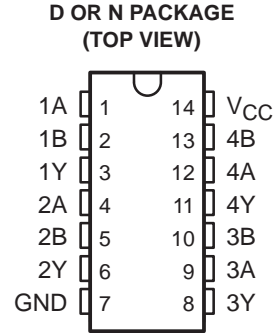
SDAS071B – DECEMBER 1982 – REVISED JANUARY 1995

- Driver Version of 'AS08
- Offers High Capacitive-Drive Capability
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs

## description

This device contains four independent 2-input positive-AND buffers/drivers. It performs the Boolean functions  $Y = A \bullet B$  or  $Y = \overline{A + B}$  in positive logic.

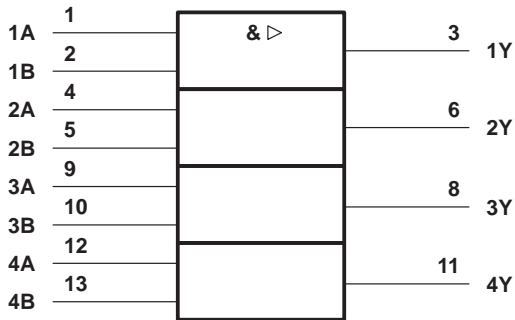
The SN74AS1008A is characterized for operation from 0°C to 70°C.



**FUNCTION TABLE  
(each gate)**

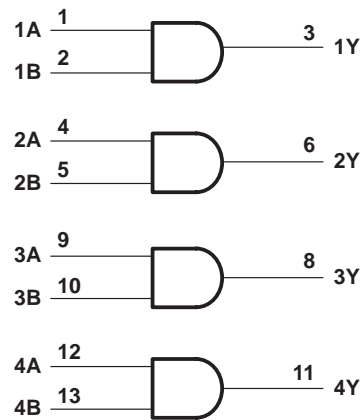
| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | H      |
| L      | X | L      |
| X      | L | L      |

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|  |                |
|--|----------------|
| Supply voltage, V <sub>CC</sub>                      | 7 V            |
| Input voltage, V <sub>I</sub>                        | 7 V            |
| Operating free-air temperature range, T <sub>A</sub> | 0°C to 70°C    |
| Storage temperature range                            | –65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN74AS1008A

## QUADRUPLE 2-INPUT POSITIVE-AND BUFFER/DRIVER

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### recommended operating conditions†

|          |                                | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| $V_{CC}$ | Supply voltage                 | 4.5 | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2   |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |     |     | 0.8 | V    |
| $I_{OH}$ | High-level output current      |     |     | -48 | mA   |
| $I_{OL}$ | Low-level output current       |     |     | 48  | mA   |
| $T_A$    | Operating free-air temperature | 0   |     | 70  | °C   |

† This high sink- or source-current device is not recommended for use above 40 MHz.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS  | MIN          | TYP‡ | MAX  | UNIT |
|-----------|--|--------------|------|------|------|
| $V_{IK}$  | $V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$                    |              |      | -1.2 | V    |
| $V_{OH}$  | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ |      |      | V    |
|           | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$                  | 2.4          | 3.2  |      |      |
|           | $V_{CC} = 4.5\text{ V}$ , $I_{OH} = -48\text{ mA}$                 | 2            |      |      |      |
| $V_{OL}$  | $V_{CC} = 4.5\text{ V}$ , $I_{OL} = 48\text{ mA}$                  |              | 0.35 | 0.5  | V    |
| $I_I$     | $V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$                       |              |      | 0.1  | mA   |
| $I_{IH}$  | $V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$                     |              |      | 20   | μA   |
| $I_{IL}$  | $V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$                     |              |      | -0.5 | mA   |
| $I_{OS}§$ | $V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$                    | -50          |      | -200 | mA   |
| $I_{CCH}$ | $V_{CC} = 5.5\text{ V}$ , $V_I = 4.5\text{ V}$                     |              | 5.6  | 9.5  | mA   |
| $I_{CCL}$ | $V_{CC} = 5.5\text{ V}$ , $V_I = 0$                                |              | 13.5 | 22   | mA   |

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

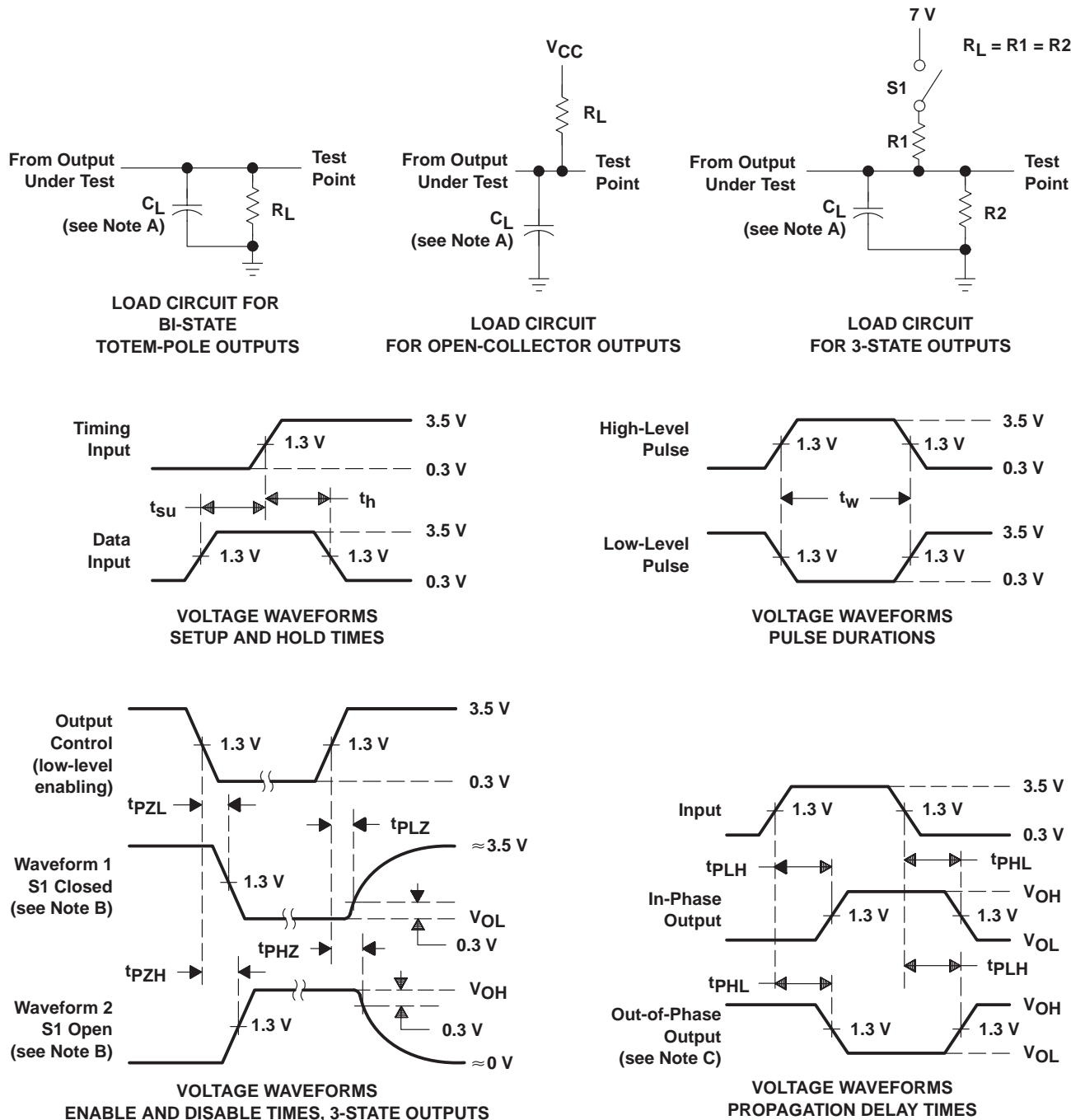
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

### switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ ,<br>$C_L = 50\text{ pF}$ ,<br>$R_L = 500\ \Omega$ ,<br>$T_A = \text{MIN to MAX}\parallel$ |     | UNIT |
|-----------|--------------|-------------|---|-----|------|
|           |              |             | MIN   | MAX |      |
| $t_{PLH}$ | A or B       | Y           | 1   | 6   | ns   |
| $t_{PHL}$ |              |             | 1   | 6   |      |

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AS1008AD     | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | AS1008A                 | <a href="#">Samples</a> |
| SN74AS1008ADE4   | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | AS1008A                 | <a href="#">Samples</a> |
| SN74AS1008AN     | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74AS1008AN            | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

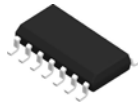
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**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74AS1008AD   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74AS1008ADE4 | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74AS1008AN   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74AS1008AN   | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.





# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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