

# SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

SDLS006

D2634, JANUARY 1981 (REVISED MARCH 1988)

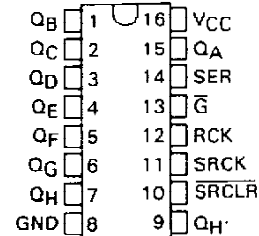
- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20 MHz

## description

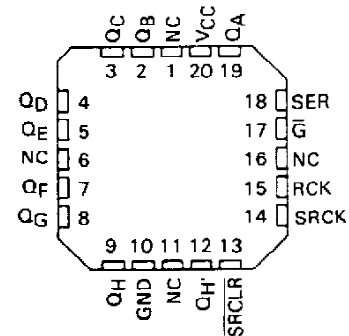
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

SN54LS595, SN54LS596 . . . J OR W PACKAGE  
SN74LS595, SN74LS596 . . . N PACKAGE  
(TOP VIEW)

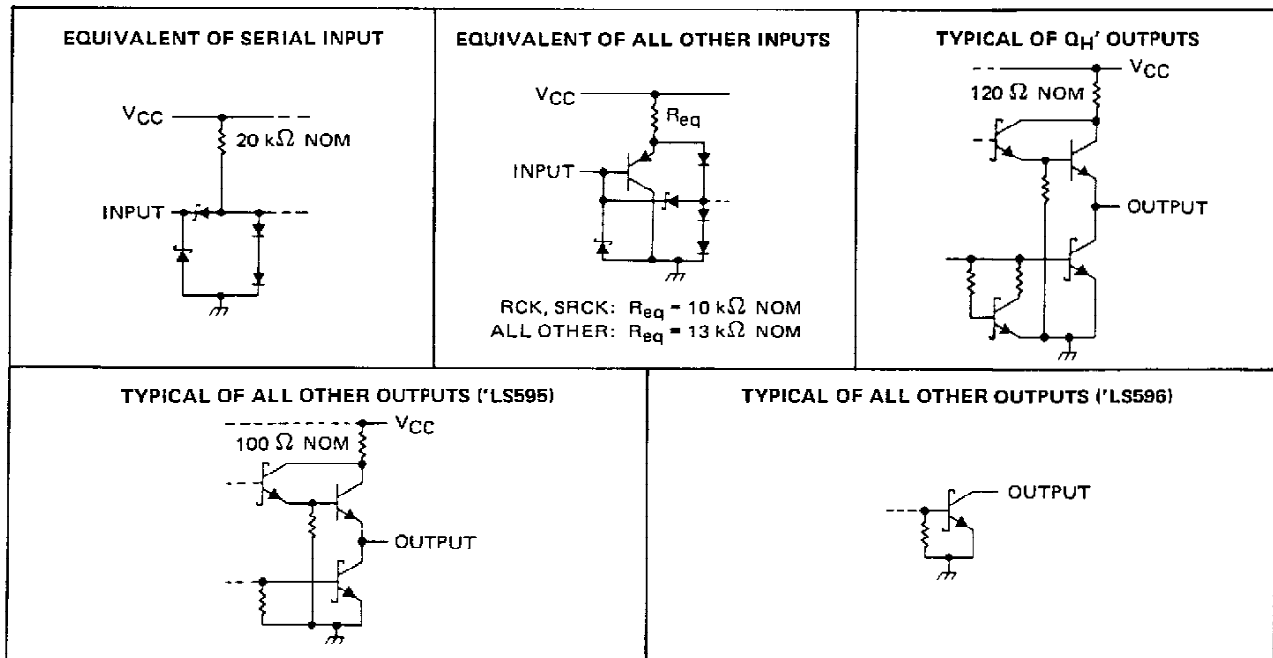


SN54LS595, SN54LS596 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## schematics of inputs and outputs



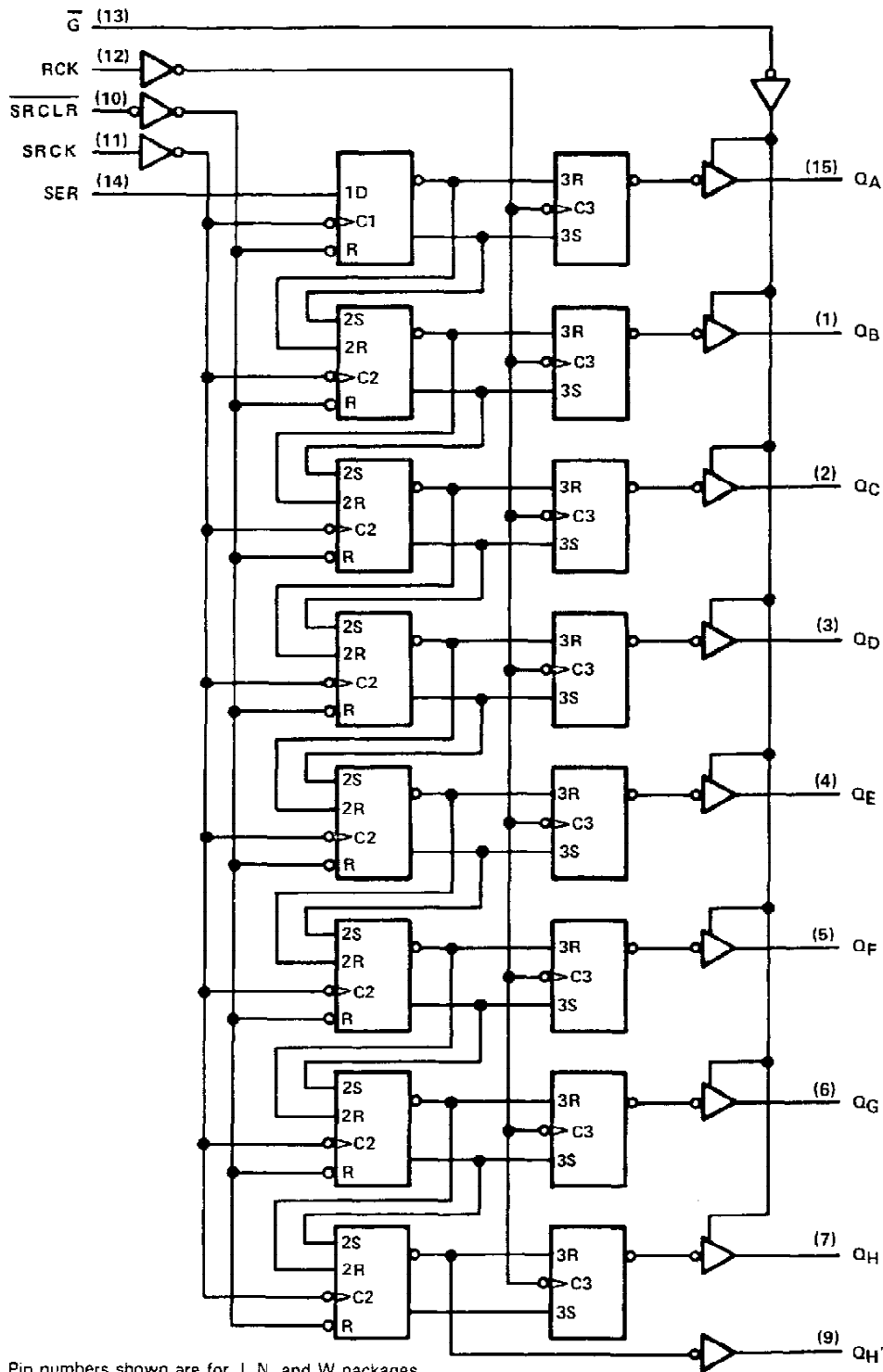
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# SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

logic diagram (positive logic)



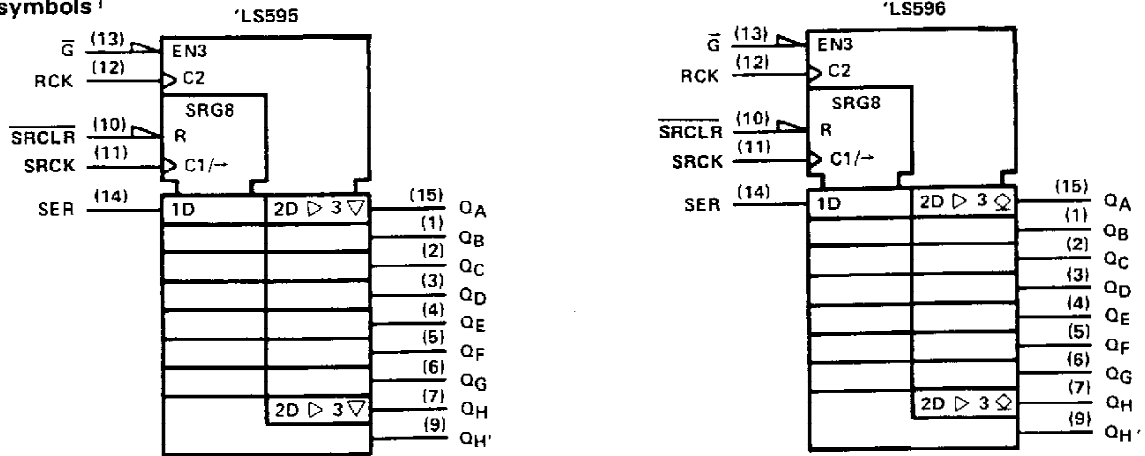
Pin numbers shown are for J, N, and W packages.

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# SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

logic symbols †



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596	-55°C to 125°C
SN74LS595, SN74LS596	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

## recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$V_{OH}$ High-level output voltage			5.5			5.5	V
$I_{OH}$ High-level output current	$Q_A$ thru $Q_H$ , 'LS596 only						mA
	$Q_H'$		-1			-1	
$I_{OL}$ Low-level output current	$Q_A$ thru $Q_H$ , 'LS595 only					-2.6	mA
	$Q_H'$		8			16	
	Q		12			24	
$f_{SRCK}$ Shift clock frequency	0		20	0		20	MHz
$t_w(SRCK)$ Duration of shift clock pulse	25			25			ns
$t_w(RCK)$ Duration of register clock pulse	20			20			ns
$t_w(SRCLR)$ Duration of shift clear pulse, low level	20			20			ns
$t_{su}$ Setup time	SRCLR inactive before SRCK †		20			20	ns
	SER before SRCK †		20			20	
	SRCK † before RCK † (see Note 2)		40			40	
	SRCLR low before RCK †		40			40	
$t_h$ Hold time	SER after SRCK †		0			0	ns
$T_A$ Operating free-air temperature	-55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.

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**SN54LS595, SN54LS596, SN74LS595, SN74LS596**  
**8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS <sup>5</sup>		SN74LS <sup>5</sup>		UNIT			
		MIN	TYP ‡	MAX	MIN		TYP ‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	V		
V <sub>OH</sub>	'LS595 Q Q <sub>H</sub> '	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OH</sub> = -1 mA	2.4	3.2				
			I <sub>OH</sub> = -2.6 mA			2.4	3.1		
			I <sub>OH</sub> = -1 mA	2.4	3.2	2.4	3.2		
I <sub>OH</sub>	'LS596 Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 5.5 V					0.1	0.1	mA
V <sub>OL</sub>	Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4		
			I <sub>OL</sub> = 24 mA			0.35	0.5		
			I <sub>OL</sub> = 8 mA	0.25	0.4	0.25	0.4		
			I <sub>OL</sub> = 16 mA			0.35	0.5		
I <sub>OZH</sub>	'LS595 Q	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 2.7 V			20		20	μA	
I <sub>OZL</sub>	'LS595 Q	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 0.4 V			-20		-20	μA	
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1		0.1	mA	
I <sub>IH</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20		20	μA	
I <sub>IL</sub>	SER	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4		-0.4		
	All others				-0.2		-0.2		
I <sub>OS</sub> §	'LS595 Q	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0 V			-30		-130		
	Q <sub>H</sub> '				-20		-100		
I <sub>CCH</sub>	'LS595	V <sub>CC</sub> = MAX, All possible inputs grounded, All outputs open			33		50		
	'LS596				30		45		
I <sub>CCL</sub>	'LS595	All possible inputs grounded, All outputs open			42		65		
	'LS596				36		55		
I <sub>CCZ</sub>	'LS595			44		65			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

**SN54LS595, SN54LS596, SN74LS595, SN74LS596**  
**8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS595			'LS596			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	SRCK ↑	$Q_H'$	$R_L = 1\text{ k}\Omega$ , $C_L = 30\text{ pF}$	12	18		14	21	ns	
$t_{PHL}$				17	25		20	30	ns	
$t_{PLH}$	RCK ↑	$Q_A$ thru $Q_H$	$R_L = 667\ \Omega$ , $C_L = 45\text{ pF}$	12	18		28	42	ns	
$t_{PHL}$				24	35		24	35	ns	
$t_{PZH}$	$\overline{G}$ ↓	$Q_A$ thru $Q_H$		20	30				ns	
$t_{PZL}$				25	38				ns	
$t_{PHZ}$	$\overline{G}$ ↑	$Q_A$ thru $Q_H$	$R_L = 667\ \Omega$ , $C_L = 5\text{ pF}$	20	30				ns	
$t_{PLZ}$				25	38				ns	
$t_{PLH}$	$\overline{G}$ ↑	$Q_A$ thru $Q_H$	$R_L = 667\ \Omega$ , $C_L = 45\text{ pF}$				40	60	ns	
$t_{PHL}$	$\overline{G}$ ↓	$Q_A$ thru $Q_H$					25	38	ns	
$t_{PHL}$	SRCLR ↓	$Q_H'$	$R_L = 1\text{ k}\Omega$ , $C_L = 30\text{ pF}$	24	35		24	35	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8671701EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J	<a href="#">Samples</a>
5962-8671701FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W	<a href="#">Samples</a>
5962-8671701FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W	<a href="#">Samples</a>
SN54LS595J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS595J	<a href="#">Samples</a>
SN54LS595J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS595J	<a href="#">Samples</a>
SN74LS595D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	LS595	
SN74LS595D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	LS595	
SN74LS595DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS595	<a href="#">Samples</a>
SN74LS595DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS595	<a href="#">Samples</a>
SN74LS595N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS595N	<a href="#">Samples</a>
SN74LS595N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS595N	<a href="#">Samples</a>
SNJ54LS595J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J	<a href="#">Samples</a>
SNJ54LS595J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J	<a href="#">Samples</a>
SNJ54LS595W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W	<a href="#">Samples</a>
SNJ54LS595W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS595, SN74LS595 :**

● Catalog : [SN74LS595](#)

● Military : [SN54LS595](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS595DR	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8671701FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS595N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS595W	W	CFP	16	25	506.98	26.16	6220	NA



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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