

# TPD1E10B09 Single-Channel ESD Protection Device in 0402 Package

## 1 Features

- Provides system-level ESD protection for I/O interfaces up to  $\pm 9$  V
- IEC 61000-4-2 level 4:
  - $\pm 20$  kV (air-gap discharge)
  - $\pm 20$  kV (contact discharge)
- IEC 61000-4-5 surge protection:
  - 4.5 a (8/20  $\mu$ s)
- I/O capacitance 10 pf (typical)
- $R_{DYN}$  0.5  $\omega$  (typical)
- DC breakdown voltage  $\pm 9.5$  V (minimum)
- Ultra low leakage current 100 nA (maximum)
- 13-V clamping voltage (maximum at  $I_{PP} = 1$  A)
- Industrial temperature range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Space-saving 0402 footprint (1 mm  $\times$  0.6 mm  $\times$  0.5 mm)

## 2 Applications

- End equipment:
  - [Tablets](#)
  - [Remote controllers](#)
  - [Wearables](#)
  - Set-top boxes
  - [Electronic point of sale \(EPOS\)](#)
  - eBooks
- Interfaces:
  - Audio lines
  - Push-buttons
  - General-purpose input and output (GPIO)

## 3 Description

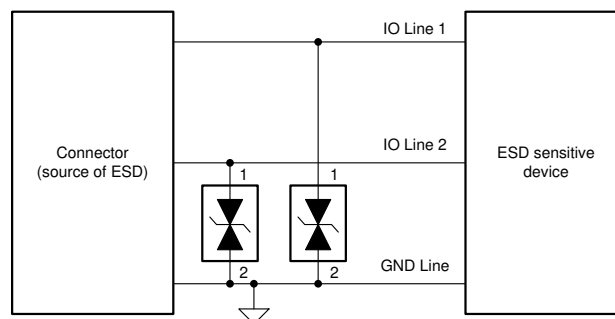
The TPD1E10B09 device is a single-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 package. This ESD protection diode offers  $\pm 20$  kV IEC 61000-4-2 (level 4) contact and air-gap ESD protection. The back-to-back TVS diode configuration allows for bipolar or bidirectional signal support. The 10-pF line capacitance is suitable for a wide range of applications supporting data rates up to 500 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-constrained applications.

Typical applications of this ESD protection TVS diode are circuit protection for audio lines (microphone, earphone, and speaker phone), SD interfacing, keypad or other buttons,  $V_{BUS}$  pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is good for the protection of end equipment like eBooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPD1E10B09	DPY (X1SON, 2)	1 mm $\times$ 0.6 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



**Application Schematic**



## Table of Contents

<b>1 Features</b> .....	1	7.3 Feature Description.....	8
<b>2 Applications</b> .....	1	7.4 Device Functional Modes.....	8
<b>3 Description</b> .....	1	<b>8 Application and Implementation</b> .....	9
<b>4 Revision History</b> .....	2	8.1 Application Information.....	9
<b>5 Pin Configuration and Functions</b> .....	3	8.2 Typical Application.....	9
<b>6 Specifications</b> .....	4	8.3 Power Supply Recommendations.....	10
6.1 Absolute Maximum Ratings.....	4	8.4 Layout.....	11
6.2 ESD Ratings.....	4	<b>9 Device and Documentation Support</b> .....	12
6.3 Recommended Operating Conditions.....	4	9.1 Receiving Notification of Documentation Updates....	12
6.4 Thermal Information.....	4	9.2 Support Resources.....	12
6.5 Electrical Characteristics.....	5	9.3 Trademarks.....	12
6.6 Typical Characteristics.....	6	9.4 Electrostatic Discharge Caution.....	12
<b>7 Detailed Description</b> .....	8	9.5 Glossary.....	12
7.1 Overview.....	8	<b>10 Mechanical, Packaging, and Orderable</b>	
7.2 Functional Block Diagram.....	8	<b>Information</b> .....	12

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (August 2015) to Revision E (September 2023)</b>	<b>Page</b>
• Changed the format of the <i>Package Information</i> table to include package lead size.....	1
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
<b>Changes from Revision C (June 2015) to Revision D (August 2015)</b>	<b>Page</b>
• Added capacitive measurement frequency.....	5
<b>Changes from Revision B (October 2012) to Revision C (June 2015)</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
<b>Changes from Revision A (March 2012) to Revision B (October 2012)</b>	<b>Page</b>
• Added <i>Thermal Information</i> table.....	4
<b>Changes from Revision * (February 2012) to Revision A (March 2012)</b>	<b>Page</b>
• Updated <i>Features</i> section.....	1
• Added graphs to <i>Typical Characteristics</i> section.....	6
• Added APPLICATION INFORMATION section.....	9

## 5 Pin Configuration and Functions

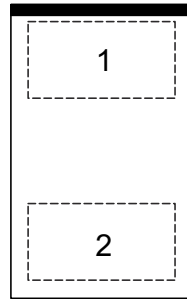


Figure 5-1. DPY Package, 2-Pin X1SON (Top View)

Table 5-1. Pin Functions

PIN	TYPE <sup>(1)</sup>	DESCRIPTION
1	I/O	ESD protected I/O
2		

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
	Operating temperature	-40	125	°C
$I_{PP}$	Peak pulse current (tp = 8/20 $\mu$ s)		4.5	A
$P_{PP}$	Peak pulse power (tp = 8/20 $\mu$ s)		90	W
$T_{stg}$	Storage temperature	-65	155	°C

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	
		IEC 61000-4-2 Contact Discharge	
		IEC 61000-4-2 Air-Gap Discharge	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Operating free-air temperature, $T_A$	-40		125	°C
	Operating voltage	Pin 1 to 2 or pin 2 to 1		9	V

### 6.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>	TPD1E10B09	UNIT
		DPY (X1SON)	
		2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	615.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	404.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	493.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	127.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	493.3	°C/W
P	Power Dissipation <sup>(2)</sup>	162	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Max junction temperature: 125°C; power dissipation calculated at 25°C ambient temperature using JEDEC High K board Standard. Not to be used for steady state power dissipation in the breakdown region.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage	Pin 1 to 2 or pin 2 to 1			9	V
$I_{LEAK}$	Leakage current	Pin 1 = 5 V, pin 2 = 0 V			100	nA
$V_{Clamp1,2}$	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	$I_{PP} = 1\text{ A}$ , $t_p = 8/20\ \mu\text{Sec}^{(2)}$			13	V
		$I_{PP} = 5\text{ A}$ , $t_p = 8/20\ \mu\text{Sec}^{(2)}$			17	
$V_{Clamp2,1}$	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	$I_{PP} = 1\text{ A}$ , $t_p = 8/20\ \mu\text{Sec}^{(2)}$			13	V
		$I_{PP} = 4.5\text{ A}$ , $t_p = 8/20\ \mu\text{Sec}^{(2)}$			20	
$R_{DYN}$	Dynamic resistance	Pin 1 to pin 2 <sup>(1)</sup>		0.5		$\Omega$
		Pin 2 to pin 1 <sup>(1)</sup>		0.5		
$C_{IO}$	I/O capacitance	$V_{IO} = 2.5\text{ V}$ ; $f = 1\text{ MHz}$		10		pF
$V_{BR1,2}$	Break-down voltage, pin 1 to pin 2	$I_{IO} = 1\text{ mA}$	9.5			V
$V_{BR2,1}$	Break-down voltage, pin 2 to pin 1	$I_{IO} = 1\text{ mA}$	9.5			V

(1) Extraction of  $R_{DYN}$  using least squares fit of TLP characteristics from  $I_{PP} = 10\text{ A}$  to  $I_{PP} = 20\text{ A}$ .

(2) Non-repetitive current pulse 8/20  $\mu\text{s}$  exponentially decaying waveform according to IEC 61000-4-5.

## 6.6 Typical Characteristics

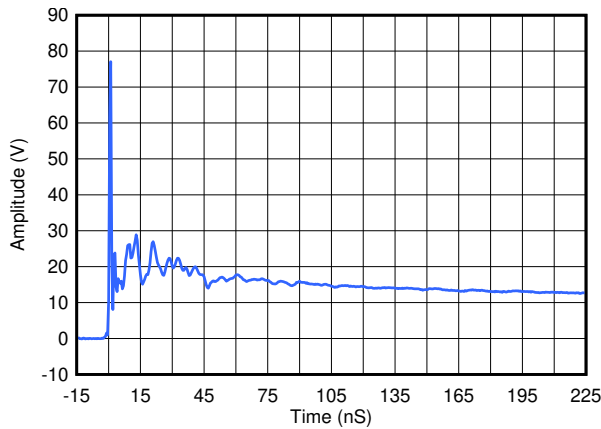


Figure 6-1. ESD Clamp Voltage +8 kV Contact ESD

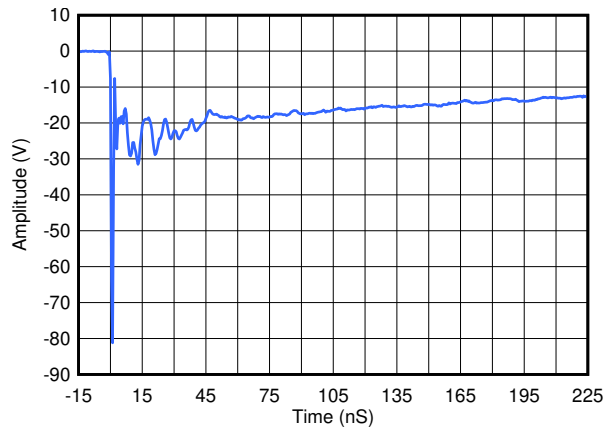


Figure 6-2. ESD Clamp Voltage -8 kV Contact ESD

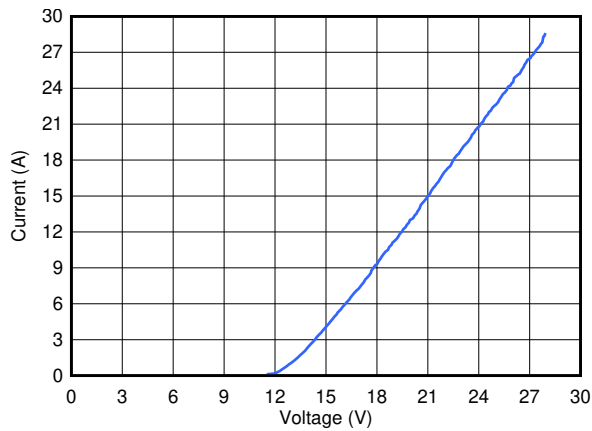


Figure 6-3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

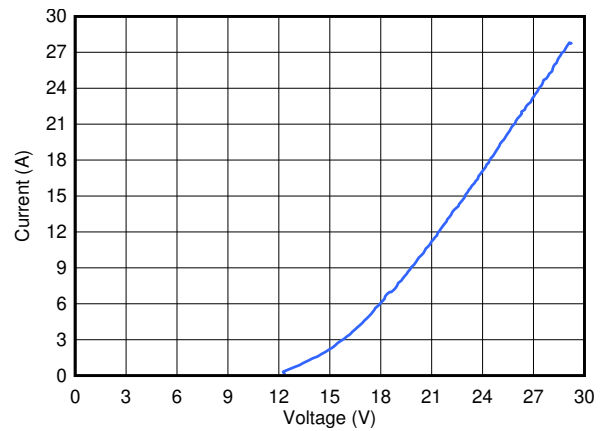


Figure 6-4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

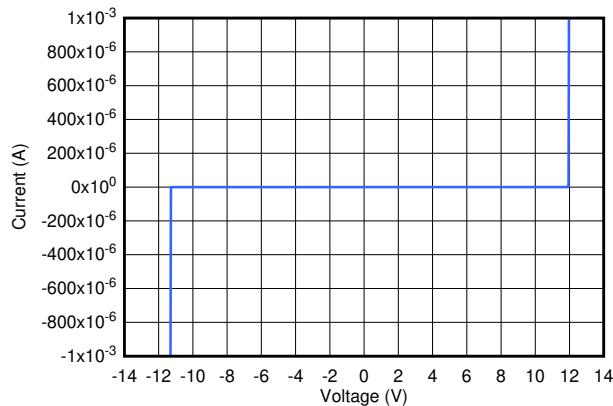


Figure 6-5. IV Curve

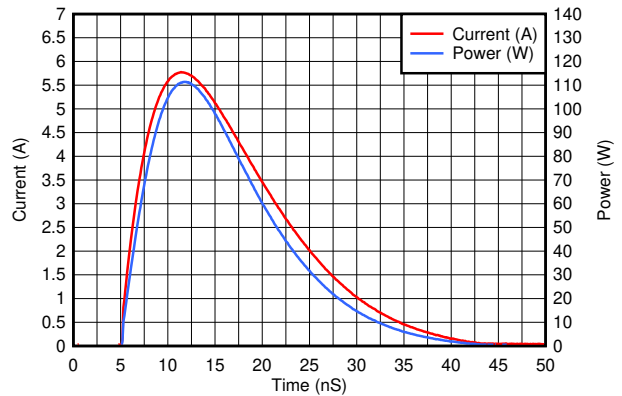
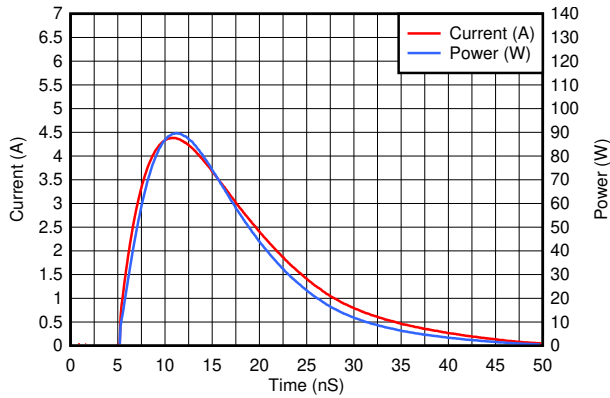
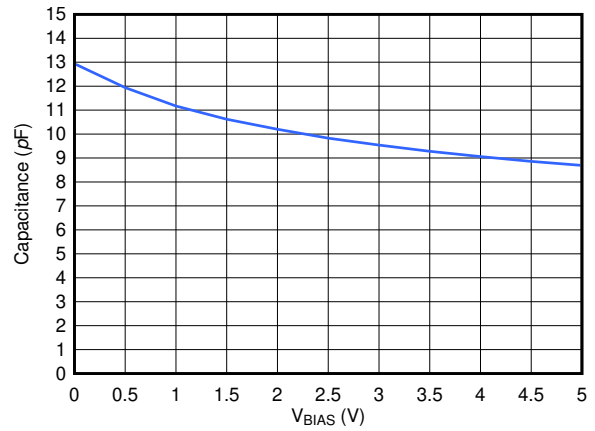


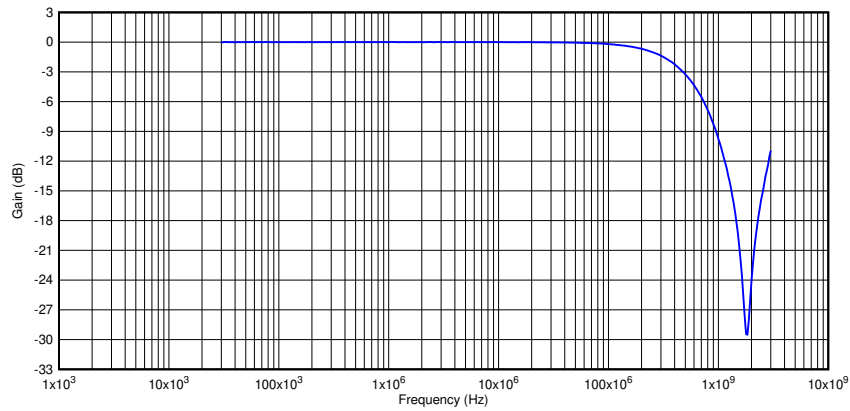
Figure 6-6. Positive Surge Waveform 8/20  $\mu$ s



**Figure 6-7. Negative Surge Waveform 8/20  $\mu$ s**



**Figure 6-8. Pin Capacitance Across  $V_{BIAS}$**



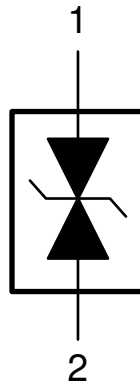
**Figure 6-9. Insertion Loss**

## 7 Detailed Description

### 7.1 Overview

TPD1E10B09 is a single-channel ESD TVS that provides  $\pm 20$ -kV IEC 61000-4-2 (Level 4) contact and air-gap ESD protection. The 10-pF back-to-back diode architecture is suitable for signals that range from  $-9$  V to 9 V and supports data rates up to 500 Mbps. The industry-standard 0402 package is convenient for placement in applications with limited space.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

TPD1E10B09 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to  $\pm 20$ -kV contact and  $\pm 20$ -kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 4.5-A surge current (IEC 61000-4-5 8/20  $\mu$ s). The I/O capacitance of 10 pF supports a data rate up to 500 Mbps. This clamping device has a small dynamic resistance of 0.5  $\Omega$  typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 13 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO, especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the  $V_{RWM}$ . The industrial temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

### 7.4 Device Functional Modes

TPD1E10B09 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below  $V_{RWM}$  and activates when the voltage between pin 1 and pin 2 goes above  $V_{BR}$ . During IEC ESD events, transient voltages as high as  $\pm 20$  kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.



## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The TPD1E10B09 is a single-channel back-to-back diode that protects one bidirectional signal line from electrostatic discharge and surge pulses. Because the diode is bidirectional, TPD1E10B09 protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10-pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode should be placed very close to the external connector for optimal performance. It is best to place the diode on the line that it is protecting.

Layout: Pin 1 of the diode should be right over the protected signal line. There should a thick and short trace from pin 2 to ground. For an example, see the [Layout](#) section.

### 8.2 Typical Application

A system with a human interface is vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E10B09 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a tolerable level to the protected IC.

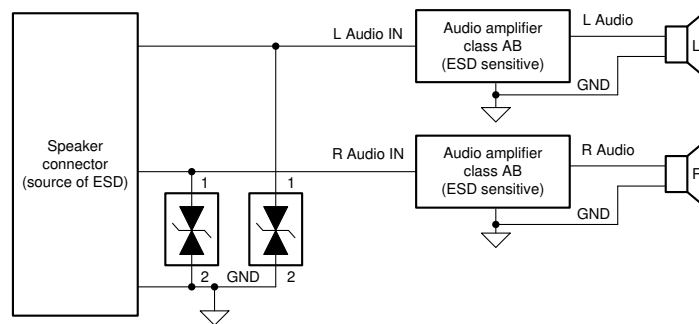


Figure 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

For this design example, two TPD1E10B09s will be used to protect left and right audio channels. [Table 8-1](#) lists the known system parameters for this audio application.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	-8 V to 8 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±15-kV Contact/ ±15-kV Air-Gap

## 8.2.2 Detailed Design Procedure

To begin the design process, consider the following parameters:

- Ensure the voltage range on the protected line does not exceed the reverse standoff voltage of the TVS diodes ( $V_{RWM}$ ).
- Ensure the operating frequency is supported by the I/O capacitance ( $C_{IO}$ ) of the TVS diode.
- Ensure the IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is  $-8\text{ V}$  to  $8\text{ V}$ . The  $V_{RWM}$  for the TVS is  $-9.5\text{ V}$  to  $9.5\text{ V}$ ; therefore, the bidirectional TVS will not break down during normal operation, and normal operation of the audio signal will not be affected due to the signal voltage range. In this application, a bidirectional TVS like TPD1E10B09 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from  $20\text{ Hz}$  to  $20\text{ kHz}$ ; filter the TVS I/O capacitance so that it does not distort this signal. With TPD1E10B09 typical capacitance of  $10\text{ pF}$ , which leads to a typical cutoff frequency of just under  $500\text{ MHz}$ , this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires protection for  $\pm 15\text{-kV}$  Contact and  $\pm 15\text{-kV}$  Air-Gap ESD, which is above the standard Level 4 IEC 61000-4-2 system-level ESD protection. A standard TVS cannot survive this level of IEC ESD stress. However, TPD1E10B09 can survive at least  $\pm 20\text{-kV}$  Contact and  $\pm 20\text{-kV}$  Air-Gap ESD. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. For instructions on properly laying out TPD1E10B09, see [Layout](#).

## 8.2.3 Application Curves

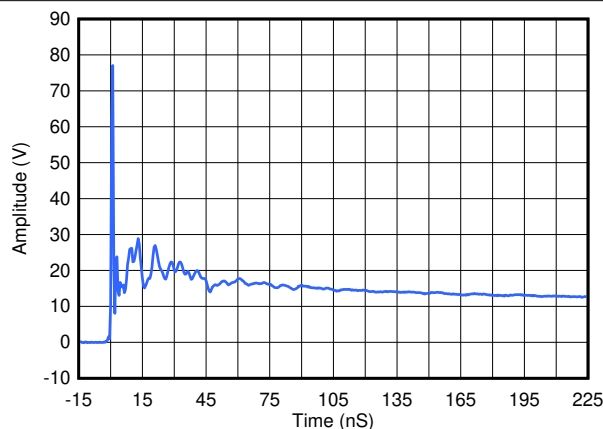


Figure 8-2. ESD Clamp Voltage +8-kV Contact ESD

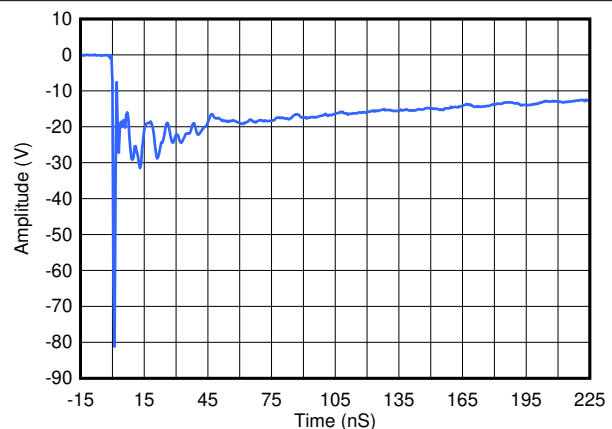


Figure 8-3. ESD Clamp Voltage -8-kV Contact ESD

## 8.3 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Do not violate the maximum specifications for each pin.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Use rounded corners with the largest radii possible on the protected traces between the TVS and the connector, thus eliminating any sharp corners.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path.

### 8.4.2 Layout Example

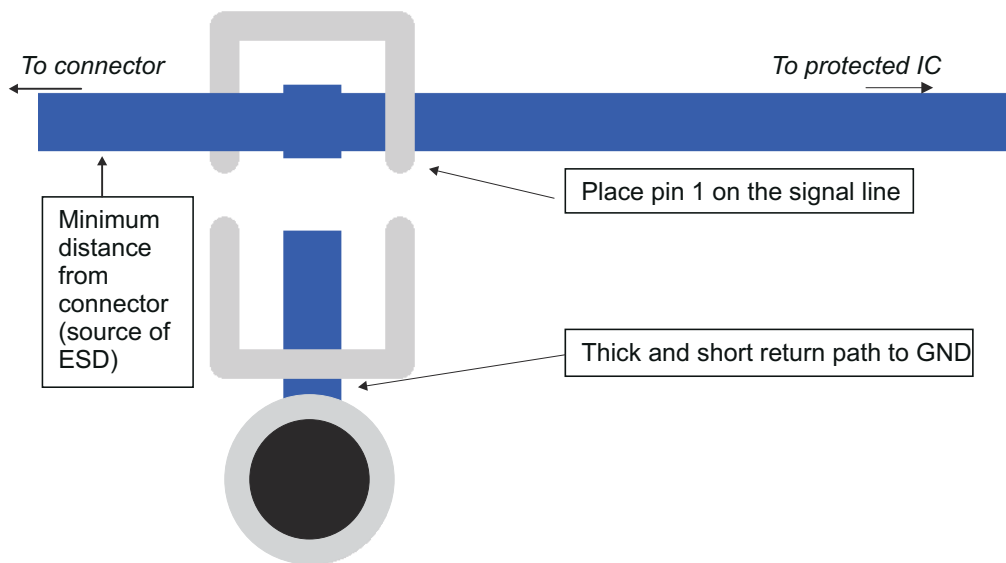


Figure 8-4. Layout Example

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E10B09DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A1, A2, A5, A6, B J)	Samples
TPD1E10B09DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		(A1, A2, A6, BJ)	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPD1E10B09 :**

- Automotive : [TPD1E10B09-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

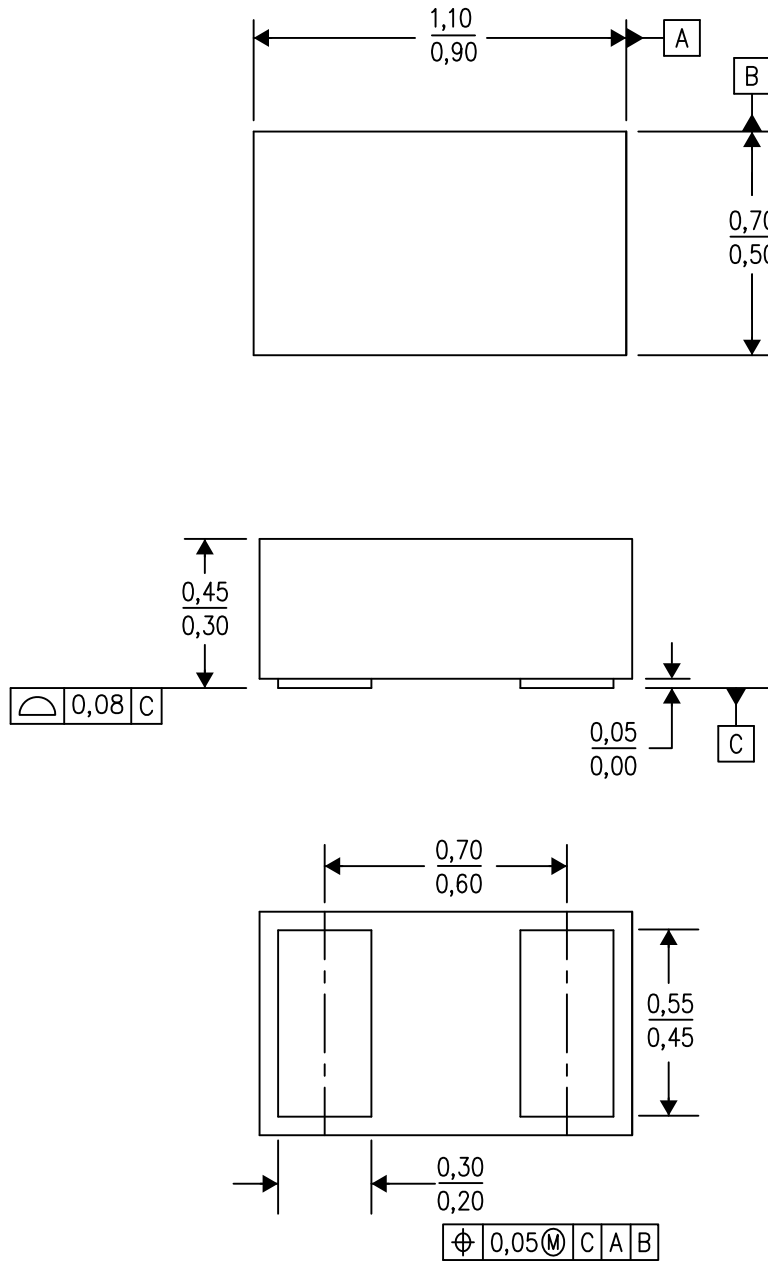

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B09DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E10B09DPYT	X1SON	DPY	2	250	205.0	200.0	33.0
TPD1E10B09DPYT	X1SON	DPY	2	250	189.0	185.0	36.0



DPY (R-PX1SON-N2)

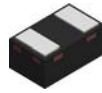
PLASTIC SMALL OUTLINE NO-LEAD



4211012/D 08/14

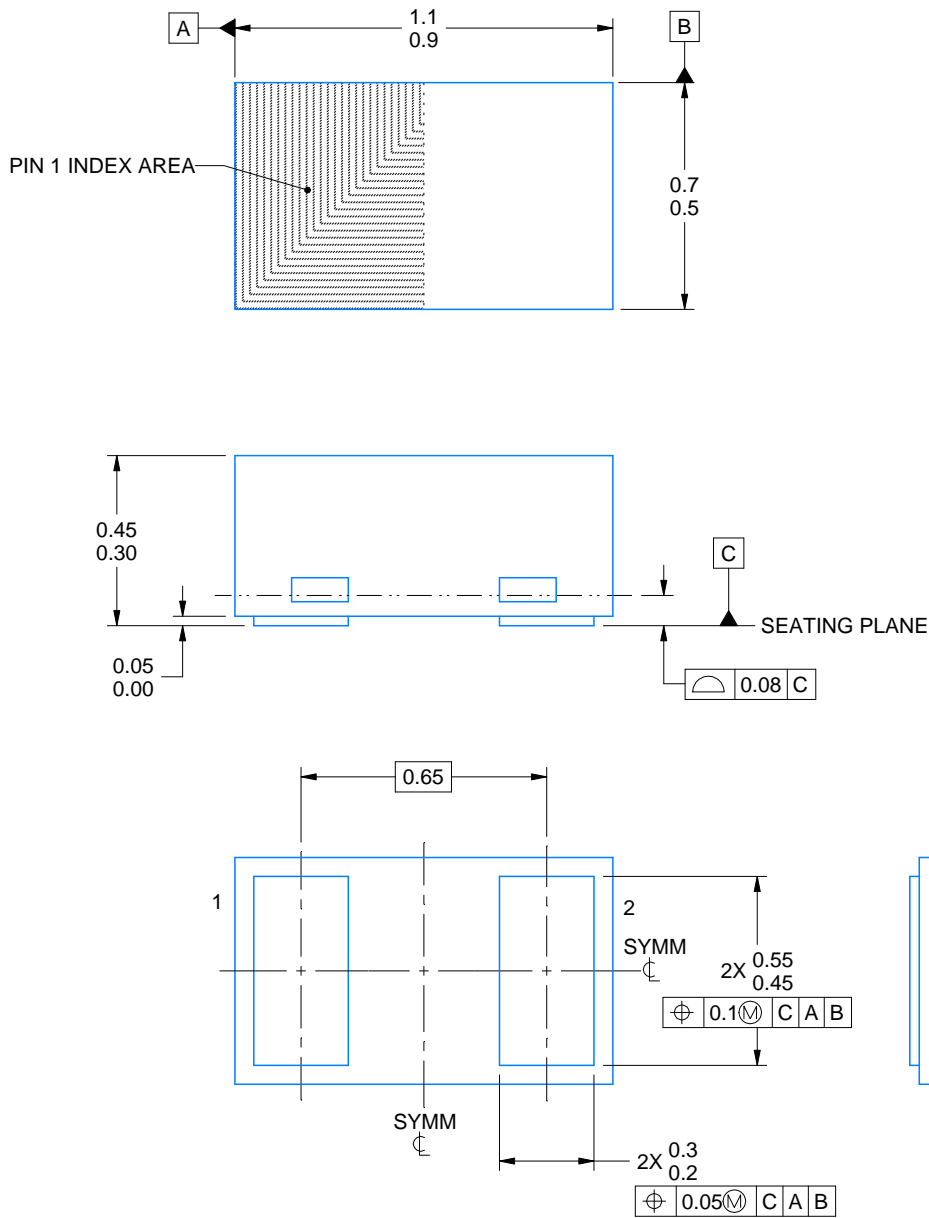
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - SON (Small Outline No-Lead) package configuration.

DPY0002A



**PACKAGE OUTLINE**  
**X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



4224561/B 03/2021

NOTES:

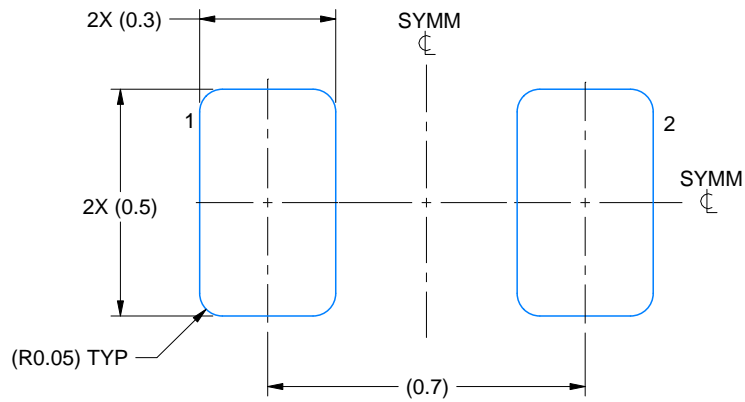
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

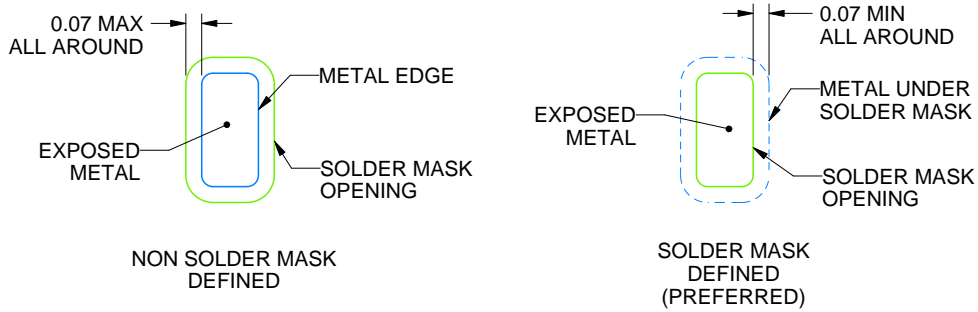
DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:60X



SOLDER MASK DETAILS

4224561/B 03/2021

NOTES: (continued)

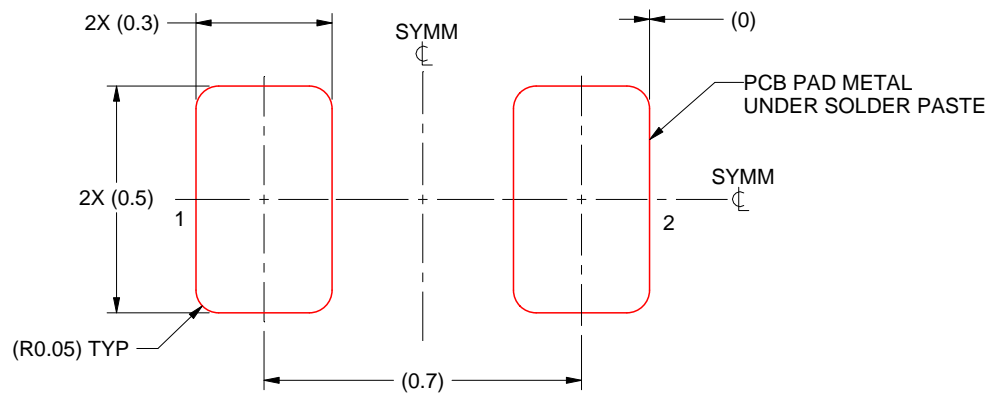
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated