UC1834-DIE High Efficiency Linear Regulator

1 Features

- Equally Usable for Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Undervoltage and Overvoltage Fault Alert With Programmable Delay

2 Applications

- Wireless LAN
- Programmable Logic Controller
- Motor Control and Drives
- Solar Energy Systems
- Sonar, Ultrasound

3 Description

The UC1834-DIE integrated circuit is optimized for the design of low input-output differential linear regulator. A high-gain amplifier and sink or source drive outputs facilitate high-output current designs, which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, the UC1834-DIE has a fault monitoring circuit which senses both undervoltage and overvoltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the overvoltage case, a crowbar output is activated. An overvoltage latch maintains the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input, which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

Ordering Information(1)

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
UC1834	TD	Bare die in waffle pack(2)	UC1834VTD1	80
			UC1834VTD2	10

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

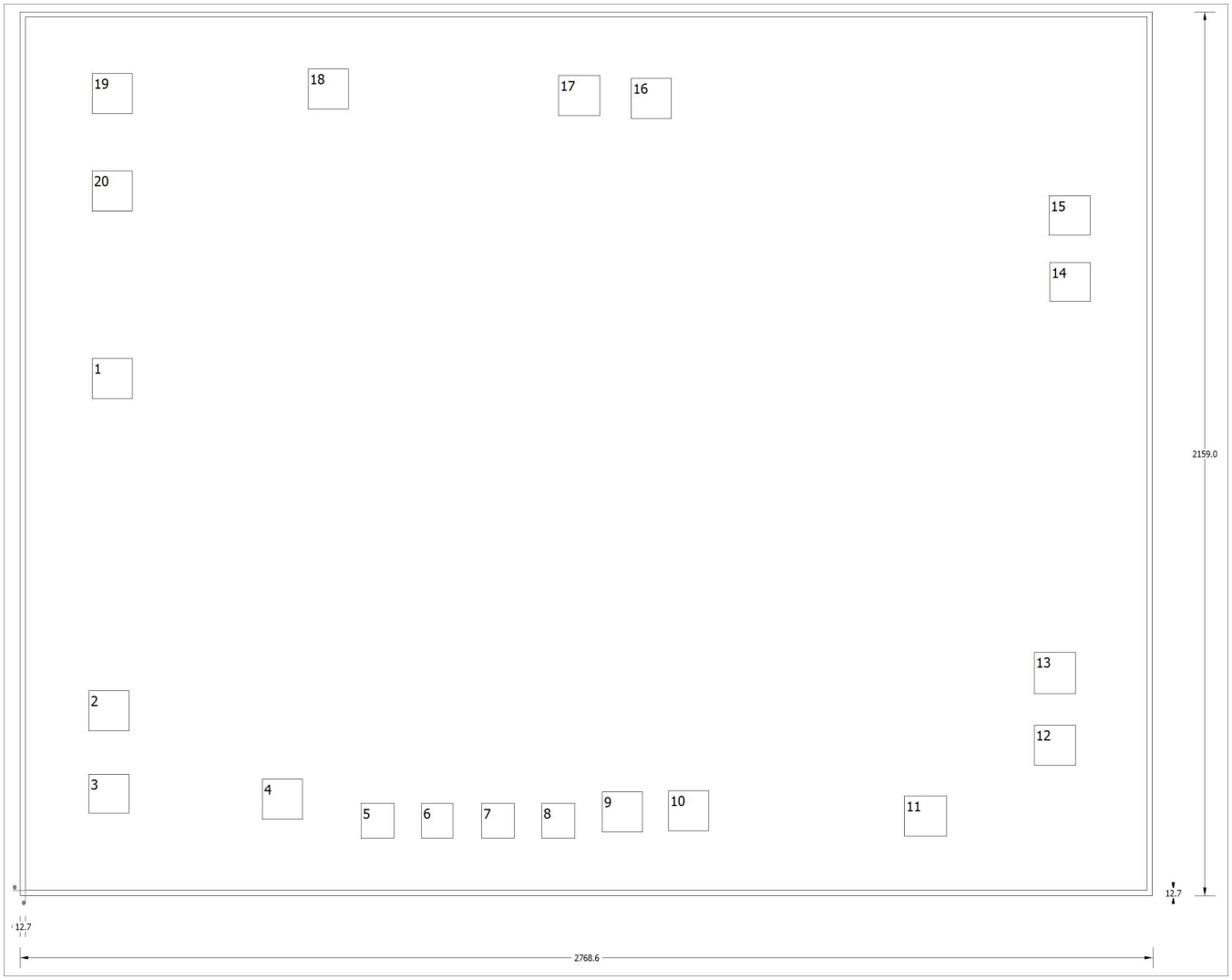
(2) Processing is per the Texas Instruments space production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils	Silicon with backgrind	Floating	AlCu2%	2000 nm



Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN+	1	162.56	1201.42	261.62	1300.48
–2.0-V reference	2	154.94	388.62	254	487.68
1.5-V reference	3	154.94	187.96	254	284.48
Threshold adj.	4	579.12	172.72	678.18	271.78
N/C	5	820.42	127	901.7	213.36
N/C	6	967.74	127	1046.48	213.36
N/C	7	1115.06	127	1196.34	213.36
N/C	8	1262.38	127	1343.66	213.36
VIN–	9	1409.7	142.24	1508.76	241.3
Sense–	10	1572.26	144.78	1671.32	243.84
Sense+	11	2148.84	132.08	2252.98	231.14
Non-inverting input	12	2466.34	304.8	2567.94	403.86
Inverting input	13	2466.34	480.06	2567.94	581.66
Fault alert	14	2504.44	1437.64	2603.5	1534.16
Fault delay	15	2501.9	1600.2	2603.5	1696.72
Driver sink	16	1480.82	1884.68	1579.88	1983.74
Driver source	17	1303.02	1892.3	1404.62	1991.36
Compensation/shutdown	18	690.88	1907.54	789.94	2006.6
Overvoltage latch output/reset	19	162.56	1897.38	261.62	1996.44
Crowbar gate	20	162.56	1658.62	261.62	1757.68

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1834VTD1	ACTIVE			0	80	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples
UC1834VTD2	ACTIVE			0	10	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC1834-DIE :

- Space : UC1834-SP

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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