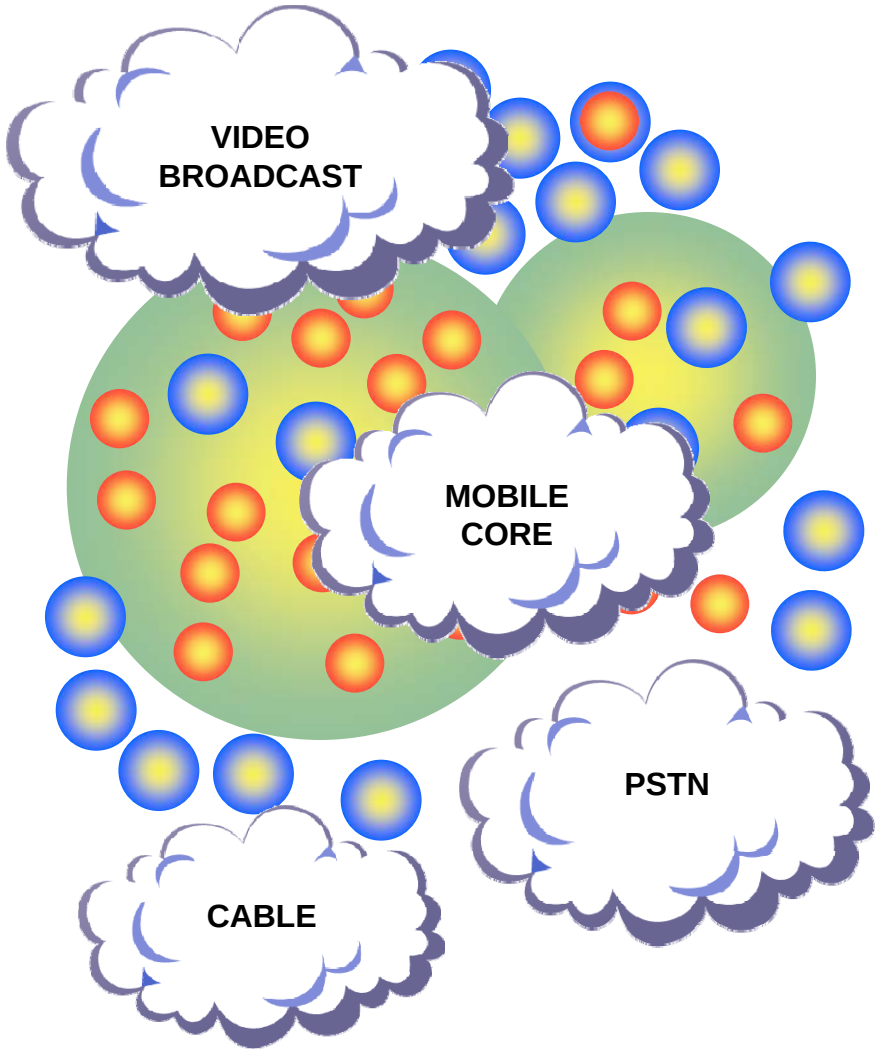
Multicore, Multilayer SoC

New multicore system-on-a-chip architecture for communications infrastructure equipment

February 15, 2010

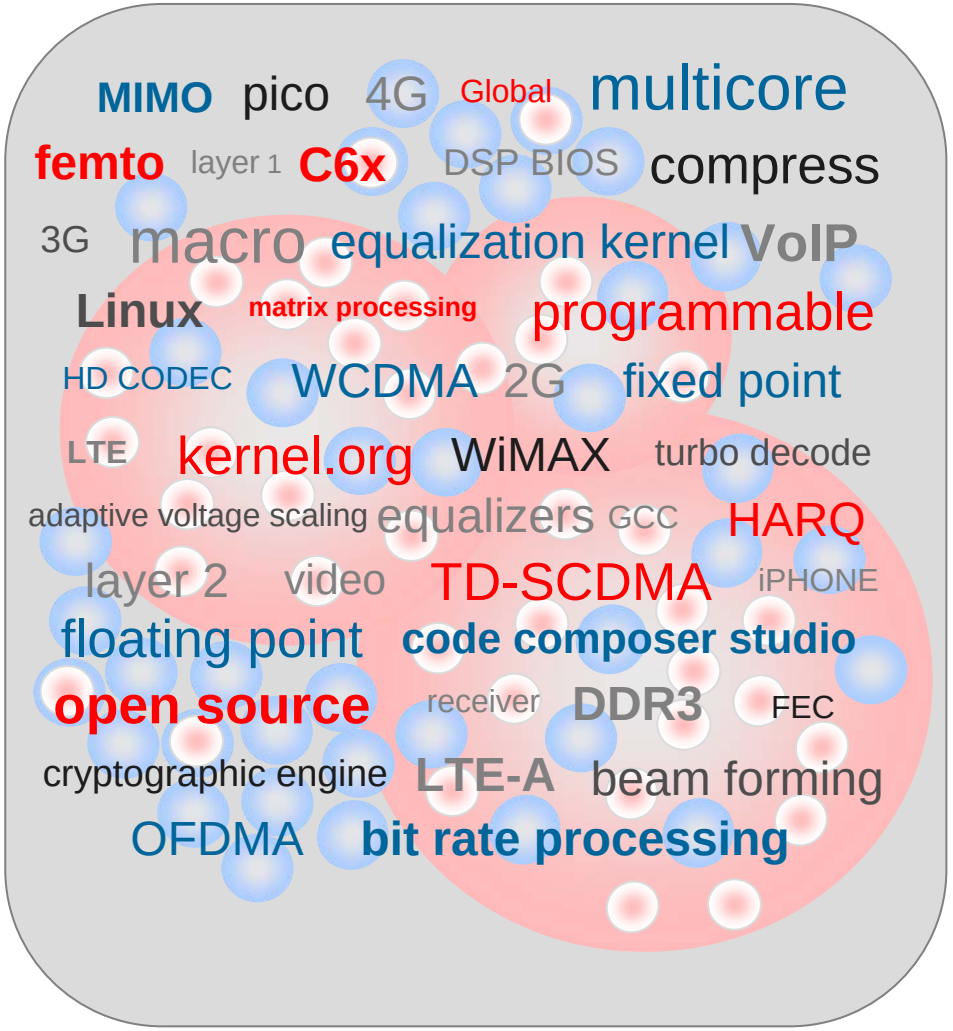
Communications infrastructure focus



- **Increase capacity & reduce power/MHz**
  - Heterogeneous networks
  - Advanced receivers
  - Maximum spectral efficiency
  - Enhanced voice & video solution density
- **Reduce costs**
  - Reduce wireless cost per bit
  - Reduce cost per channel for multimedia gateways
  - Reduce power consumption
- **All-IP focus**
  - Border gateways
  - LTE gateways

Impacts on infrastructure equipment
Paradigm shift for OEMs

- **Reduced power consumption**
  - *Lower power 24/7*
  - Low power static, dynamic solutions
- **Heterogeneous networks**
  - *Small cell solutions*
  - Require scalable hardware & software platforms
- **Advanced receivers**
  - *MIMO capabilities*
  - Require optimized matrix processing environments
- **Maximum spectral efficiency**
  - *LTE scheduling paradigm*
  - Requires low latency, compute intensive processing environments
- **Reduced cost/bit**
  - *Opex/Capex implications*
  - Cost optimized platforms
- **Voice/video convergence**
  - Maximize solution density
  - Low latency voice & video processing



What is TI announcing?

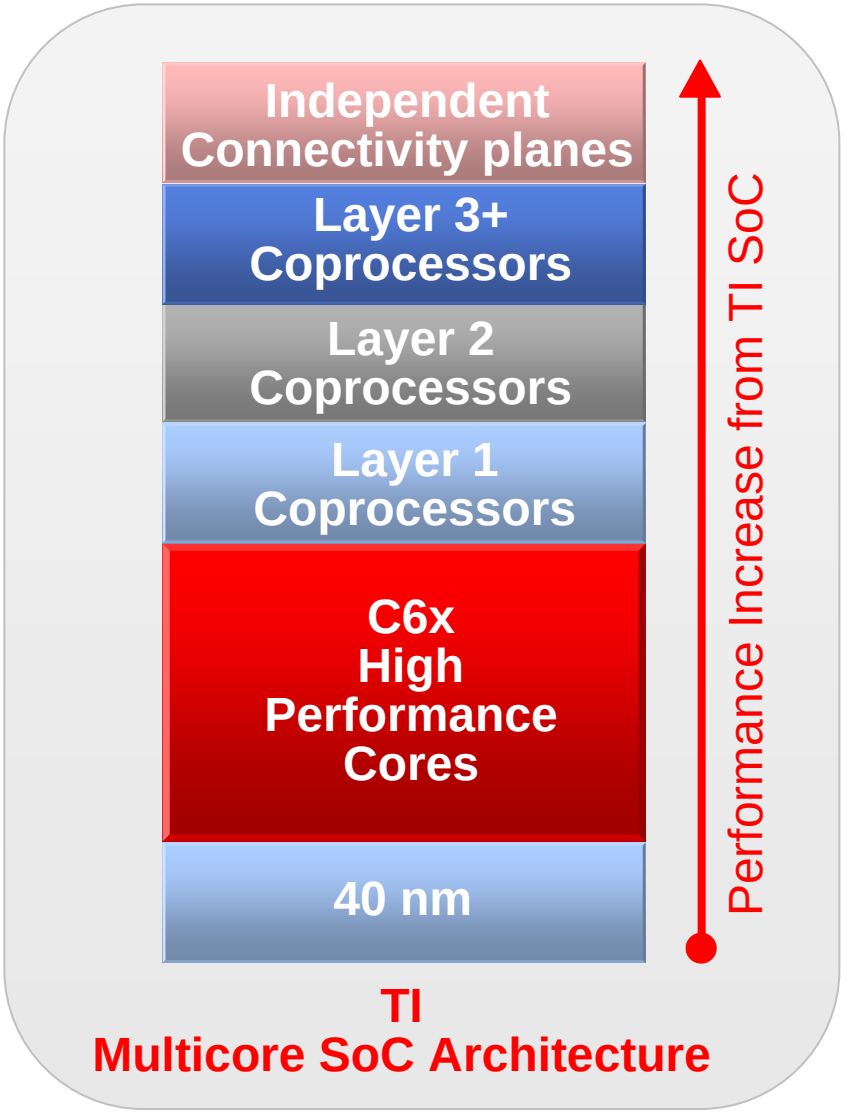
A new multicore SoC architecture that offers vendors a common platform to accelerate development of communications infrastructure products - wireless base stations, media gateways, networking & video infrastructure equipment

- Industry's **highest performing** CPU -- up to 1.2GHz, 256 GMACS/128 GFLOPS
- Integrated **fixed & floating point processing** -- simplifies programming of complex algorithms
- Programmable platform -- **flexibility** for emerging standards
- C6x **software compatibility** & **scalability** -- macro, pico, femto from a single software investment
- Latest technology -- **cost, performance & power optimized**
- Product family will include range of devices starting with:
  - A four-core device for wireless base stations
  - An eight-core device for media gateway & networking applications
  - Flexibility to include multiple core types and expandable to include device clusters

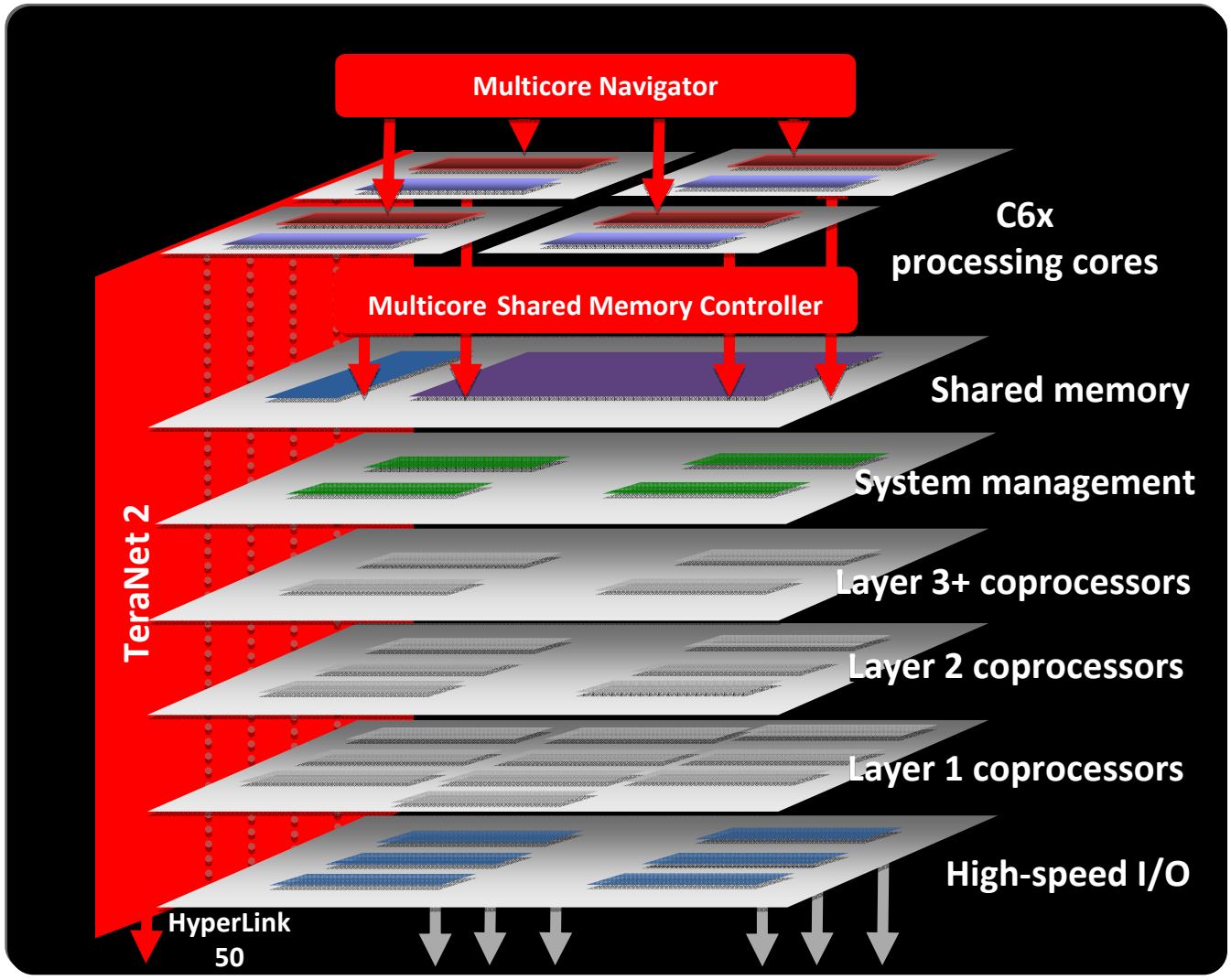
TI multicore system-on-a-chip

New performance requirements drive new solutions

- Process node scale
  - Traditional performance gains
- C6x core innovations
- Coprocessors
  - Layer 1
  - Layer 2
  - Layer 3+
- Independent intra-chip connectivity planes



TI multicore SoC architecture



TI multicore SoC elements

The first network on chip infrastructure to unleash full multicore entitlement

- **Multicore Navigator**
  - Network on chip management element leveraging 8192 task oriented queues to optimize data flow
  - Fast, efficient, scalable
  - Packet/Message based leveraging Host/Buffer Descriptors model
- **TeraNet 2**
  - An on-chip networked switching hierarchy
  - Nearly 2 terabit per second non-blocking network backbone interconnecting cores coprocessors and peripherals
- **Multicore Shared Memory Controller**
  - Provides direct core to memory access
  - No need to traverse TeraNet 2
- **HyperLink 50**
  - Provides a chip level interconnect allowing open to span multiple chips
  - Multicore Shared Memory Controller
- **Coprocessors**
  - Accelerators for Layer 1, 2, 3+

TI leads the market with development tools

Simplifying multicore processor design

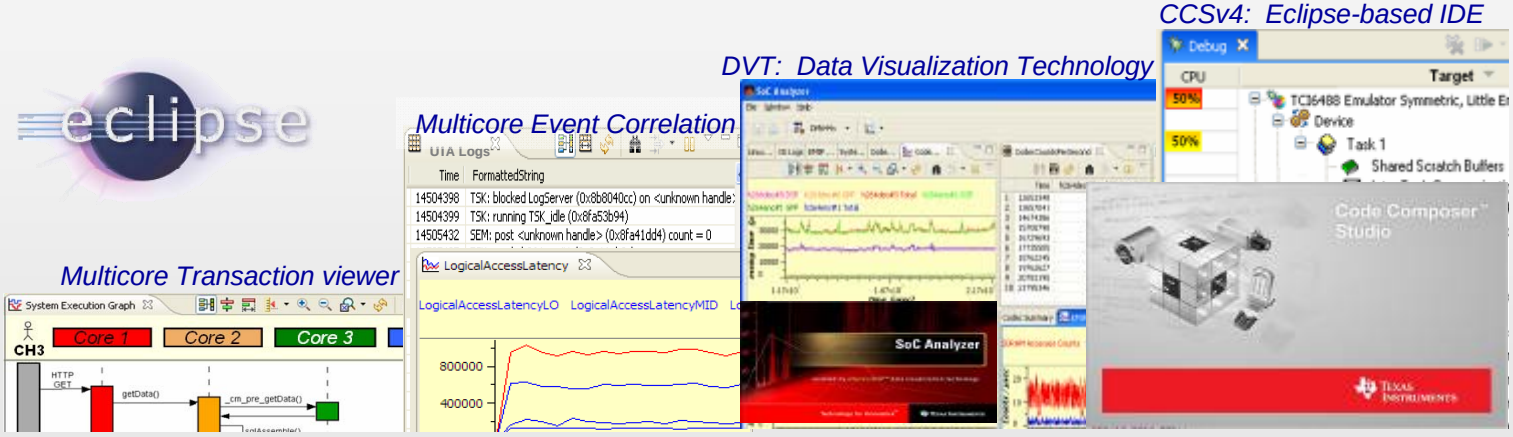
- Highest compiler efficiency
  - Customers can deliver products with more value
    - e.g. more capacity per Hz
  - Less need to optimize
- Best debug and analysis tools
  - Solid code gets to the field faster
  - Field issues are resolved quicker

CCSv4: Eclipse-based IDE

DVT: Data Visualization Technology

Multicore Event Correlation

Multicore Transaction viewer



Jump start software

Commercial operating systems

- High performance TI tool chain
- Professional support
- Legacy software compatibility
- DSP programming model
- Highly optimized code

GSM-EDGE, WCDMA-HSPA HSPA+, WiMAX, and LTE Software Libraries

Voice & Video Gateway Software Developer's Kits, Voice & Video Codecs

Reduce risk and accelerate development time

TI's Multicore, Multilayer Solutions

- Innovative TI multicore SoC architecture
  - Optimized for high performance, cost effective, power efficient processing for communications infrastructure equipment
- TI tools and software
  - Protects customers' investment in C6x software and operating environments
  - Jump start development
  - Jump start field enhancements

SPRT548

The first network on chip infrastructure to unleash full multicore entitlement

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