DLPC300 Programmer’s Guide

User's Guide

Literature Number: DLPU004B
November 2011–Revised July 2013

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About This Manual

This document specifies the command and control interface to the 0.3 WVGA chipset. It also defines all applicable commands, default settings, and control register bit definitions to communicate with the 0.3 WVGA chipset.

Related Documents from Texas Instruments

- DLP 0.3 WVGA Chipset: DLP 0.3 WVGA Chipset Data Manual, DLPZ005
- DLPC300 Data Sheet: DLP Digital Controller for DLP3000 DMD, DLPS023
- DLP3000 Data Sheet: DLP 0.3 WVGA DDR Series 220 DMD, DLPS022

If You Need Assistance

See the DLP and MEMS TI E2E Community support forums.

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Interface Protocol

This chapter describes the interface protocol between the DLPC300 and a host processor.

1.1 I²C Interface

The DLPC300 controller uses the I²C protocol to exchange commands and data with a host processor. The I²C protocol is a two-wire serial data bus that conforms to the NXP I²C specification, up to 400 kHz. One wire, SCL, serves as a serial clock, while the second wire, SDA, serves as serial data. Several different devices can be connected together in an I²C bus. Each device is software addressable by a unique address. Communication between devices occurs in a simple master-to-slave relationship.

1.1.1 I²C Transaction Structure

All I²C transactions are composed of a number of bytes, combined in the following order:

START Condition, Slave Address Byte + R/W Bit, Sub-Address Byte, N-Data Bytes, STOP Condition

where N in "N-Data Bytes" varies based on the sub-address.

1.1.1.1 I²C START Condition

All I²C transactions begin with a START condition. A START condition is defined by a high to low transition on the SDA line, while the SCL line is high.

1.1.1.2 DLPC300 Slave Address

The DLPC300 offers two different slave addresses. The I2C_ADDR_SEL pin of the DPLC300 provides the ability to select an alternate set of 7-bit I²C slave addresses. If I2C_ADDR_SEL pin is low, then the DLPC300 slave address is 0x1B. If I2C_ADDR_SEL pin is high, then the DLPC300 slave address is 0x1D. Because the first 8-bit I²C packet includes the 7-bit slave address followed by a read (high) or write (low) bit, a read command to the DLPC300 concatenates the slave address with a 0. A write command to the DLPC300 concatenates the slave address with a 1. Thus, when I2C_ADDR_SEL is low, the DLPC300 first byte packet of an I²C command is 0x36 for write and 0x37 for read. When I2C_ADDR_SEL is high, the DLPC300 first byte packet of an I²C command is 0x3A for write and 0xB7 for read.

1.1.1.3 DLPC300 Sub-Address and Data Bytes

The DLPC300 sub-address corresponds to the byte address of the DLPC300 registers described in Section A.1. Each register address requires a certain number of data bytes, typically 4. Thus, a register address is followed by up to four data bytes. These bytes contain the value read or written into this register.

1.1.1.4 I²C STOP Condition

All I²C transactions end with a STOP condition. A STOP condition is defined by a low to high transition on the SDA line while the SCL line is high.

1.1.1.5 Example Read Transaction Sequence

To read the DLPC300 register address 0x15, the host must perform the following steps. First, the host sends a START condition followed by the DLPC300 address with the read/write bit cleared (0x36). Then, the host writes a sub-address 15h, with a data field that contains the address of the desired register. Then, the host issues another I²C START condition followed by the DLPC300 address with the read/write bit set. Then the host waits for four bytes to be transferred by the DLPC300. After the DLPC300 transfers four bytes, the host must issue a STOP condition to terminate the register read access.

An example of reading register 4h whose contents are 00000000h would follow this sequence:

S 36 14 04 P

S 37 00 00 00 00 P

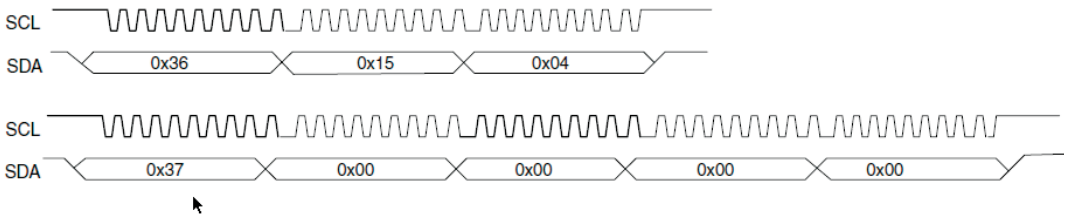


Figure 1-1. I²C Read Register Sequence

1.1.1.6 Example Register Write Transaction Sequence

To write a DLPC300 register, the host must perform the following steps.

First, the host sends a START condition followed by the DLPC300 address with the read/write bit cleared (0x36). Then, the host sends the DLPC300 register address and four bytes for the data to write into the DLPC300 register. The transaction ends when the hosts sends a STOP condition. All register-write transactions must include one byte for the register address and 4 bytes for data. An example of writing to register 0x04 write with data x00000000 is as follows:

S 36 04 00 00 00 00 P

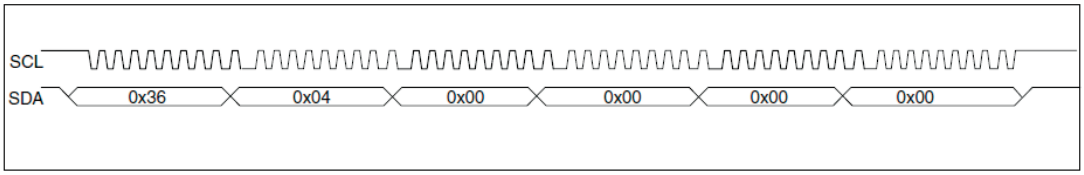


Figure 1-2. I²C Write Register Sequence

Chipset Registers and I²C Commands

This chapter lists the DLPC300 configuration registers and control commands.

NOTE: **Momentary Image Corruption During Command Writes**. Certain commands may cause brief visual artifacts in the display image under some circumstances. Command data values may always be read without impacting displayed image. To avoid momentary corruption of image due to a command, disable the LEDs prior to the command write, then reenable the LEDs after all commands have been issued.

The following sections list the supported configuration registers and control commands. In the *Type* column, 'wr' type is writeable. Data can also be read back through the I²C interface for 'wr' type bits. Type *r* is read-only. Write to read-only fields is ignored. Type *I* is interrupt.

Type *s* signifies a special latched status bit. Reading a 1 from an s bit means that the hardware signal associated with that bit has gone active since the last *clear* of that status bit. Writing a 1 to an s bit clears the status bit. The bit then reads zero until the next active condition of the hardware associated with the status bit.

The Reset column in all of the following command tables is the default value in the command register immediately after power up. These values may be overwritten after power up.

NOTE: **Reserved bits and registers.** When writing to valid registers, all bits marked as unused or reserved should be set to zero unless specified otherwise. Registers marked as reserved should not be accessed.

2.1 Chipset Configuration Registers

The DLPC300 has the following set of configuration registers:

- Interrupt Status Registers
- Main Status Register
- General Purpose Register
- mDDR Memory BIST Status Register

2.1.1 Interrupt Status Register (I²C: 0x00/0x01)

The Interrupt Status Register provides DLPC300 interrupt status information. Note: The Interrupt Status Register is mapped to two addresses: x000 and x001. Reading either address returns the same value. Writing a 1 to a bit in this register clears the interrupt. When a bit is read, the state of the interrupt is not clear. Reading a 0 indicates that the interrupt is not active. Reading a 1 indicates that the interrupt occurred.

Table 2-1. Interrupt Status Register

BIT(S)	DESCRIPTION	RESET	TYPE
0	Sequencer-abort status flag 0 = No abort 1 = Sequencer abort has occurred.	b0	i

Table 2-1. Interrupt Status Register (continued)

BIT(S)	DESCRIPTION	RESET	TYPE
1	DMD reset-waveform-controller overrun-error flag 0 = No error has occurred. 1 = Reset-waveform-controller overrun has occurred.	b0	i
2	DMD reset controller reset-block-error flag 0 = No error has occurred. 1 = Multiple overlapping bias/reset operations are accessing the same DMD block.	b0	i
3	DMD reset controller I/F overrun-error flag 0 = No error has occurred. 1 = Overlapping DMD reset requests have been detected and cannot be supported across the serial interface.	b0	i
4	Formatter read-buffer overflow 0 = No error has occurred 1 = Formatter read buffer has overflowed	b0	i
5	Formatter (CMB) starvation error 0 = No error has occurred. 1 = Formatter (CMB) starvation error has occurred.	b0	i
6	Reserved	b0	i
7	Flash memory controller FIFO error 0 = No error has occurred. 1 = Flash memory controller FIFO errors occurred.	b0	i
8	Flash memory controller DMA abort 0 = No error has occurred. 1 = Flash memory controller DMA abort has occurred.	b0	i
9	Formatter (CMB) multiple error 0 = No error has occurred. 1 = Formatter (CMB) multiple error occurred.	b0	i
10	Formatter (CMB) command error 0 = No error has occurred. 1 = Formatter (CMB) command error occurred.	b0	i
11	Formatter (CMB) queue warning 0 = No error has occurred. 1 = Formatter (CMB) queue warning occurred.	b0	i
12	mDDR memory controller BP-write FIFO overflow 0 = No error has occurred. 1 = mDDR memory controller BP-write FIFO overflowed.	b0	i
13	mDDR memory controller FB-write FIFO overflow no data 0 = No error has occurred. 1 = mDDR memory controller FB-write FIFO overflowed.	b0	i
14	Scaler line-count error 0 = No error has occurred. 1 = The number of lines in a frame was less than expected.	b0	i
15	Scaler pixel-count error 0 = No error has occurred. 1 = The number of pixels in a line was less than expected.	b0	i
16	Reserved	b0	i
17	Reserved	b0	i

Table 2-1. Interrupt Status Register (continued)

BIT(S)	DESCRIPTION	RESET	TYPE
18	LED timeout error 0 = No error has occurred 1 = LED timeout error has occurred (in effect, a given color has been continuously enabled for > 18 ms).	b0	i

2.1.2 Main Status Register (I^2C: 0x03)

The Main Status Register provides instantaneous DLPC300 status information. The DMA status bit should be polled following the initiation of a flash memory controller DMA operation to determine when it is complete, as no other flash memory controller operation can be requested during a DMA transaction or the DMA is aborted. Bits 10 and 11 can be polled following the release of reset, for I^2C applications only, to determine when auto-initialization is complete. When bit 10 is cleared and bit 11 is set, initialization is complete. Also, the DLPC300 sets INIT_DONE high during auto-initialization. On completion of the auto-initialization, the DLPC300 sets INIT_DONE low.

Table 2-2. Main Status Register

BIT(S)	DESCRIPTION	RESET	TYPE
7:0	Device ID, for DLPC300 ID = 0x8A	0x8A	s
8	DMA status 0 = Current operation is complete. 1 = Busy	b0	s
9	Reserved	X	s
10	Indicates the flash controller is performing initialization 0 = Initialization complete 1 = Flash controller performing initialization	b0	s
11	Indicates when auto-initialization is complete 0 = Auto-initialization is in progress. 1 = Auto-initialization is complete (or was bypassed).	b1	s
12	Indicates LED timeout status 0 = No timeout has occurred. 1 = LED timeout error has occurred (in effect, a given color has been continuously enabled for > 18 ms).	b0	s

2.1.3 General Purpose Register (I^2C: 0x30)

This is a General Purpose R/W Storage Register. The value written has no affect on DLPC300 operation. It provides system applications to store firmware revision or other information that is accessible from an external host.

Table 2-3. General Purpose Register

BIT(S)	DESCRIPTION	RESET	TYPE
5:0	6-bit General Purpose R/W Register	x00	wr

2.1.4 mDDR Memory BIST Status Register (I^2C: 0x9B)

This register provides mDDR Memory Built-In-Self-Test (BIST) Status information.

Table 2-4. mDDR Memory BIST Status Register

BIT(S)	DESCRIPTION	RESET	TYPE
0	Memory Controller BIST ERROR 0= No BIST errors are detected 1= An error is detected during mDDR Memory BIST execution	b0	r
1	Memory Controller BIST DONE 0= BIST is in progress (if enabled) 1= BIST is complete	b0 b0	r r

2.2 Chipset Control I²C Commands

The DLPC300 has the following set of I²C control commands:

Chipset configuration and control

Parallel interface configuration and control

Input source control

Image rotation and flip control

Image processing control

LED driver control

Sleep mode control

DLP display sequence control

I²control commands are accepted in any order, except when special sequencing is required (for example, setting up the flash). Each control command is validated for sub-address and parameter errors as it is received. Commands failing validation are ignored. On power up, it is necessary to wait for DLPC300 to complete its initialization before sending it any I²C transactions. The INIT_DONE pin signals when initialization is complete (see the DLPC300 Data Sheet).

2.2.1 Chipset Configuration and Control I²C Commands

2.2.1.1 Software Reset (I²C: 0x1F)

This command issues a software reset to the DLPC300, regardless of the argument sent. This command provides a back-up recovery mechanism. Prior to issuing a Software Reset command, it is recommended that a DMD PARK (I²C: 0x2D) command be applied first, followed by a 500 µs wait interval before issuing the reset.

Table 2-5. Software Reset Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Software Reset: 0 – Software Reset is recognized (bit value is don't care) 1 – Software Reset is recognized (bit value is don't care)	d0	wr

2.2.1.2 Display Frame Rate Control

The display frame rate must always be periodic. It is driven by the frame rate attribute of the selected DLP® display sequence. For the best motion video performance, the display frame rate and the DLP® display sequence should be chosen to match an integer multiple of the source frame rate, and the sequence-sync-mode parameter (0x1E) should be set to the lock-to-VSYNC mode. This is used in BT.656 and parallel bus applications, as these sources are assumed to always possess a periodic source frame rate.

2.2.1.2.1 Video Frame Rate Control (I²C: 0x19)

The Video Frame Rate parameter defines the periodic frame rate of the source. BT.656 and parallel bus applications are assumed always to possess a periodic source frame rate. Splash and test-pattern-generation applications should be assumed always to possess a non-periodic source frame rate. The default value is programmed for a 60-Hz frame rate.

Table 2-6. Video Frame Rate Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
11:0	Defines the free-run sequence rate of the CPUVSYNC/TE_SYNC output signal Range is 30 Hz to 72 Hz (default = x0859, 60 Hz) Value (decimal) = (1,000,000 / Freq(Hz)) / 7.8 Example; f = 60 Hz, Value = (1,000,000/60) / 7.8 = 2137 (decimal) = x0859 (hex)	x859	wr

2.2.1.3 YCrCb Source Control

When YCrCB pixel data format is sent as input to the DLPC300, the DLPC300 settings must be configured to match the color space and sampling attributes of the source. This is accomplished through the Source Color Space and Sampling Control Register and the YCrCb to RGB Control Register.

2.2.1.3.1 Source Color Space and Sampling Control (I²C: 0xC3)

This register must be configured to match the color space and sampling attributes of the source.

Table 2-7. Source Color Space and Sampling Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Reserved Set to zero	b0	wr
1	YCrCb 4:2:2 to 4:4:4 chroma interpolation function enable(1) (2) 0 = Function disabled 1 = Function enabled	b0	wr
2	YCrCb to RGB color space conversion function enable(3) (4) 0 = Function disabled 1 = Function enabled	b0	wr
5:3	Reserved Must be set to zero	b000	wr

(1) 4:2:2 to 4:4:4 chroma interpolation is only valid for YCrCb source
(2) The partial-image horizontal-start address must be EVEN for YCrCb 4:2:2 source data.
(3) When enabled, YCrCb to RGB Control Register (I²C: 0xA4) and the YCrCb 4:2:2 to 4:4:4 chroma interpolation parameter (I²C: 0xC3) must be set appropriately.
(4) Both the YCrCb 4:2:2 to 4:4:4 chroma interpolation parameter and the YCrCb to RGB color space conversion parameter must be set for BT.656 operation.

2.2.1.3.2 YCrCb To RGB Control (I²C: 0xA4)

This register must be configured to match the attributes on a YCrCb source. This register only applies when YCrCb to RGB color space conversion (I²C: 0xC3) is enabled.

Table 2-8. YCrCb To RGB Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	YCrCb to RGB color space select 0 = BT.601 color space 1 = BT.709 color space	b0	wr

Table 2-8. YCrCb To RGB Control Command (continued)

BIT(S)	DESCRIPTION	RESET	TYPE
1	YCrCb to RGB dynamic range select 0 = YCrCb source with 0–255 dynamic range on all three components 1 = YCrCb source with 16 to 240 Y and –112 to 112 CrCb	b1	wr
2	YCrCb to RGB input luma offset select 0 = YCrCb input luma offset = 0 1 = YCrCb input luma offset = –16	b1	wr
3	YCrCb to RGB input chroma offset binary select 0 = YCrCb chroma is input as a signed value. (Set input chroma offset to 0) 1 = YCrCb chroma is input as an offset binary value. (Set input chroma offset to –128)	b1	wr

2.2.1.3.3 Chroma Channel Swap (I²C: 0x33)

This register applies to both 4:2:2 and 4:4:4 YCrCb data sources. It allows the Cr and Cb chroma data received from the source to be swapped. The reference Cb/Cr order for a YCrCb 4:2:2 input is assumed to be Cb/Cr. Thus, setting this changes the order to Cr/Cb. For YCrCb 4:4:4 this bit also swaps the input channels.

Table 2-9. Chroma Channel Swap Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Chroma Channel Cr/Cb Swap 0 = Chroma Channel Swap disabled (for YCrCb 4:2:2 input = Cb/Cr) 1 = Chroma Channel Swap enabled (for YCrCb 4:2:2 input = Cr/Cb)	b0	wr

2.2.1.4 Display Buffer Swap Freeze (I²C: 0xA3)

When reconfiguring the chipset through a series of commands that change the input source or operating mode, the Display Buffer Swap Freeze command is recommended to prevent temporary artifacts from reaching the display. When the buffer swap is frozen, the last display image continues to be displayed.

Table 2-10. Display Buffer Swap Freeze Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Display Buffer Swap Freeze (a.k.a. Memory Buffer Swap Disable). 0 = Enable Buffer Swapping (Default) 1 = Disable Buffer Swapping (Freeze)	b0	wr

2.2.1.5 DMD Control

2.2.1.5.1 Display Curtain Control (I²C: 0xA6)

This register provides image curtain control. When enabled, the image curtain displays a solid field on the entire DMD display regardless of DLPC300 source configurations. It does however require that the sequence is running. The Display Curtain Control provides an alternate method of masking temporary source corruption from reaching the display due to on-the-fly reconfiguration. It is also useful for optical test and debug support.

Table 2-11. Display Curtain Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
3:0	Display Curtain Enable (All undefined values are reserved) x0 = Curtain disabled x1 = Curtain enabled	x0	wr
7:4	Display Curtain Color Select (All undefined values are reserved) x0 = Black x3 = Yellow (Red + Green) x1 = Red x5 = Magenta (Red + Blue) x2 = Green x6 = Cyan (Green + Blue) x4 = Blue x7 = White	x0	wr

2.2.1.5.2 DMD Bus Swap Control (I²C: 0xA7)

The DMD Bus Swap Control command reverses the bit-ordering of the DMD data bits output by the DLPC300 to potentially facilitate simpler PCB routing.

Table 2-12. DMD Bus Swap Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	DMD Bus Swap Control 0 = Swap disabled 1 = Swap enabled (Output DMD data bus bit-order is reversed)	b0	wr

2.2.1.5.3 DMD PARK (I²C: 0x2D)

The DMD PARK command provides a software programmable alternative to using the PWRGOOD signal. If PWRGOOD is tied HIGH, the DMD PARK command can be used to warn the DLPC300 is impending DMD power loss such that it can PARK the DMD mirrors and avoid reliability degradation. Note that for proper power-up/down sequencing refer to Chapter 4

Table 2-13. DMD PARK Command

BIT(S)	DESCRIPTION	RESET	TYPE6
0	DMD Park Control(1) 0 = Unpark the DMD (Default) 1 = Park the DMD	b0	wr

(1) This park operation does not reject the DMD_PWR_EN output, therefore DMD power remains on.

2.2.2 Parallel Interface Configuration and Control

The following commands are unique to operating the parallel interface.

2.2.2.1 Parallel Interface Polarity Control (I²C: 0xAF)

The Parallel Interface Polarity Control command controls the polarity of the HSYNC, VSYNC, clock, and data signals of the parallel interface. These parameters must be configured to match the attributes of the input signals to the DLPC300 parallel interface.

Table 2-14. Parallel Interface Polarity Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Reserved Must be set = 0	b0	wr
1	Defines the polarity of the incoming HSYNC signal: 0 = Active-low pulse 1 = Active-high pulse	b0	wr
2	Defines the polarity of the incoming VSYNC signal: 0 = Active-low pulse 1 = Active-high pulse	b0	wr
3	Pixel clock polarity 0 = Data sample on rising edge 1 = Data sample on falling edge	b0	wr
4	DATEN polarity 0 = Active-low 1 = Active-high	b0	wr

2.2.2.2 Vertical Sync Line Delay (I²C: 0x23)

The Vertical Sync Line Delay controls an adjustable delay on VSYNC. This delay is sometimes needed if the vertical front porch is too short. This VSYNC Line Delay command is only applicable to the parallel interface and BT.656 interface.

Table 2-15. Vertical Sync Line Delay Command

BIT(S)	DESCRIPTION	RESET	TYPE
4:0	Vertical Sync Line Delay (VSLD) – Range is 0-15 lines. Should be set following these contstraints: 6 - VFP (min 0) ≤ VSLD ≤ VBP – 2 (max 15) where VFP = vertical front porch (in lines) and VBP = vertical back porch (in lines)	x05	wr

2.2.2.3 Auto Framing Function

Auto framing supports the automatic generation of a data-valid (DATEN) signal for sources that do not provide data-valid. It requires vertical and horizontal back-porch timing to be consistent from frame to frame with zero variation. Horizontal and vertical back-porch framing parameters (registers 0xB0–0xB1) should be defined before enabling the function (register 0xAE). This feature should not be used for still-image operation if the horizontal and vertical syncs are being sent in the absence of data. Otherwise, auto framing would continue to frame the data even though there is not data present. Note that auto framing is only valid for parallel interface sources.

2.2.2.3.1 Auto Framing Function Enable (I²C: 0xAE)

Table 2-16. Auto Framing Function Enable Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Auto Framing Function Enable 0 = Auto generation of the DATEN signal is disabled. 1 = Auto generation of the DATEN signal is enabled.	b0	wr

2.2.2.3.2 Auto Framing Horizontal Back Porch (I²C: 0xB0)

Table 2-17. Auto Framing Horizontal Back Porch Command

BIT(S)	DESCRIPTION	RESET	TYPE
11:0	Expected input horizontal back porch blanking. The number of clocks between input HSYNC active edge and first clock of active data. Only applicable when *Auto Framing Function Enable* = 1.	x000	wr

2.2.2.3.3 Auto Framing Vertical Back Porch (I²C: 0xB1)

Table 2-18. Auto Framing Vertical Back Porch Command

BIT(S)	DESCRIPTION	RESET	TYPE
11:0	Expected input vertical back porch blanking. The number of vertical back porch blanks that defines the index of the first non-blanking (active data) line. Applicable when *Auto Framing Function Enable* = 1 (to feed image framing) or the BT.656 source is selected.	d23	wr

2.2.2.3.4 Custom Framing Commands

Custom framing is applicable to the parallel interface only. It provides the option to define a subset of active frame data using pixel and line counts relative to the source-data enable signal (DATEN). In other words, this feature allows the source image to be cropped as the first step in the processing chain.

2.2.2.3.4.1 First Active Line in the Frame (I²C: 0x29)

Table 2-19. First Active Line in the Frame Command

BIT(S)	DESCRIPTION	RESET	TYPE
10:0	First Active Line in the Frame (relative to active lines) image crop control 0-based (0 = first line, 1 = second line, etc.), default = 0 (no left cropping)	x000	wr

2.2.2.3.4.2 Last Active Line in the Frame (I²C: 0x2A)

Table 2-20. Last Active Line in the Frame Command

BIT(S)	DESCRIPTION	RESET	TYPE
10:0	Last Active Line in the Frame (relative to active lines) image crop control 1-based (N = N, except 0 = line 1024), default = 0 (no right cropping)	x000	wr

2.2.2.3.4.3 First Active Pixel in the Line (I²C: 0x2B)

Table 2-21. First Active Pixel in the Line Command

BIT(S)	DESCRIPTION	RESET	TYPE
10:0	First Active Pixel in the Line (relative to active pixels) image crop control 0-based (0 = first line, 1 = second line, etc.), default = 0 (no top cropping)	x000	wr

2.2.2.3.4.4 Last Active Pixel in the Line (I ²C: 0x2C)

Last Active Pixel in the Line (relative to active pixels) is relative to the uncropped source (in effect, First Active Pixel in the Line does not affect this parameter).

Table 2-22. Last Active Pixel in the Line Command

BIT(S)	DESCRIPTION	RESET	TYPE
10:0	Last Active Pixel in the Line (relative to active pixels) image crop control 1-based (N = N, except 0 = line 1024), default = 0 (no bottom cropping)	x000	wr

2.2.3 Input Source Control

The Input Source Selection determines the input source for the DLPC300 data display.

2.2.3.1 Input Source Selection: (I ²C: 0x0B)

Table 2-23. Input Source Selection Command

BIT(S)	DESCRIPTION	RESET	TYPE
2:0	Select the input source and interface mode: 0 = Parallel interface with 16-bit, 18-bit, or 24-bit RGB or YCrCb data formats 1 = Internal test pattern; command 0x11 is used to select the test pattern type. 2 = Splash screen. Splash screens are single-frame, still images stored in flash that are uploaded on command. 3 = Reserved 4 = BT.656 interface. Supports only NTSC and PAL input resolutions. YCrCb to RGB color space conversion and 4:2:2 to 4:4:4 chroma interpolation (both controlled via I ²C: 0xC3) must be enabled when BT.656 is selected. 5 = Reserved 6 = Reserved 7 = Reserved	X2	wr

2.2.3.2 Input Resolution: (I² C: 0x0C)

Table 2-24 shows the supported input and output resolutions for the DLP3000 0.3 WVGA DMD. Yellow highlighting indicates the displayed image does not fill the entire DMD. Gray highlighting means the mode is not supported.

Table 2-24. Input Resolution Command

BIT(S)	DESCRIPTION					RESET	TYPE
4:0	Select the input resolution [1] :					d1	wr
	Input Resolution Options [2] (decimal)	Source Resolution		Display Non-Rotated		Display Rotated	
		H	V	H	V	H	V
	0 = QVGA portrait [3]	240	320	360	480	640	480
	1 = QVGA landscape [3]	320	240	640	480		
	2 = QWVGA portrait [3]	240	427			853	480
	3 = QWVGA landscape [4]	427	240	853	480		
	4 = 2:3 VGA Portrait [3]	430	640	322	480	714	480
	5 = 3:2 VGA Landscape [3]	640	430	716	480		
	6 = VGA portrait [3]	480	640	360	480	640	480
	7 = VGA landscape [3]	640	480	640	480		
	8 = WVGA-720 portrait [3]	480	720	320	480	720	480
	9 = WVGA-720 landscape [3]	720	480	720	480		
	10 = WVGA-752 portrait [3]	480	752	306	480	752	480
	11= WVGA-752 landscape [3]	752	480	752	480		
	12 = WVGA-800 portrait [3]	480	800	288	480	800	480
	13 = WVGA-800 landscape [3]	800	480	800	480		
	14 = WVGA-852 portrait [3]	480	852	270	480	853	480
	15 = WVGA-852 landscape	852	480	853	480		
	16 = WVGA-853 portrait [3]	480	853	270	480	853	480
	17 = WVGA-853 landscape [4]	853	480	853	480		
	18 = WVGA-854 portrait [3]	480	853	270	480	853	480
	19 = WVGA-854 landscape	854	480	853	480		
	20 = WVGA-864 portrait [3]	480	854	270	480	853	480
	21 = WVGA-864 landscape	864	480	853	480		
	22 = Reserved						
	23 = NTSC landscape [3] [5]	720	240	640	480		
	24 = Reserved [3]						
	25 = PAL landscape	720	288	640	480		
	26 = Reserved	360	640	270	480	853	480
	27 = Reserved	640	360	853	480		
	28 = Reserved						
	29 = WVGA-854 Landscape input / VGA OUTPUT [3]	854	480	640	480		
	30–34 = Reserved						
	35 = 1:1 Mirror-mapping landscape [6]	608	684	608	684		
	Others = Reserved						

(1) See Section 2.2.3.3 for input source resolution restrictions.

(2) Unless otherwise noted, all display resolutions are the Manhattan equivalent. A note with Dia corresponds to diamond equivalent.

(3) Horizontal display resolutions less than 853 are centered with black borders.

(4) The DLPC300 does not support an odd number of active, full-image, pixels per line in partial-buffer mode. Thus 427 × 480 and 853 × 480 resolutions are not supported for partial-buffer mode.

(5) BT.656 source port only. Interlaced.

(6) 1:1 mapping means that each pixel in the image corresponds to single mirror in the 0.3" DMD device. Therefore, a typical image generated with a Manhattan pixel must be compacted horizontally to transform them for the diamond pixel. To compact horizontally, the half pixel shift between vertical rows is simply removed. Prior to horizontal compacting, it is assumed that the diamond image has the same phase as the DMD. Specifically, the top line (along with all other odd lines) of the diamond image is assumed to be shifted a half-pixel to the right relative to the second line (and all other even lines) of the diamond image. This diamond phase orientation also requires that the Long-Axis Image Flip parameter (I²C: 0x0F) and Short-Axis Image Flip parameter (I²C: 0x10) be set to the same value.

2.2.3.2.1 Internal Test Patterns Select: (I2C: 0x11)

When the internal test pattern is selected as input, the Internal Test Patterns Select defines the test pattern displayed on the screen. These test patterns are internally generated and injected into the beginning of the DLPC300 image processing path. Therefore, all image processing is performed on the test images. All command registers should be set up as if the test images are input from an RGB 8:8:8 external source and the Input Resolution should be set to the value listed in the table. No other input resolutions are supported.

For a typical WVGA DMD test pattern usage, the following command settings and sequence should be used:

Input Source and Interface Mode: 0x0B = 0x1 (Internal test patterns)

Input Resolution: 0x0C = 0x13 (WVGA landscape 854h*480v)

Pixel Format: 0x0D = 0x2 (RGB888)

Table 2-25. Internal Test Patterns Select Command

BIT(S)	DESCRIPTION		RESET	TYPE
3:0	Internal Test Patterns Select:		xD	wr
		Required Source Resolution		
	Options	**WVGA DMD**		
	0x0 – Fine checkerboard (WVGA DMD - 14x8 checkerboard)	854 x 480		
	0x1 - Solid black			
	0x2 - Solid white			
	0x3 - Solid green			
	0x4 - Solid blue			
	0x5 - Solid red			
	0x6 - Vertical lines (1-white, 7-black)			
	0x7 - Horizontal lines (1-white, 7-black)			
	0x8 - Vertical lines (1-white, 1-black)			
	0x9 - Horizontal lines (1-white, 1-black)			
	0xA - Diagonal lines			
	0xB - Vertical gray ramps			
	0xC - Horizontal gray ramps			
	0xD - ANSI 4x4 checkerboard	852 x 480		

2.2.3.3 Input Pixel Data Format: (I ²C: 0x0D)

When the parallel interface is selected, the Input Pixel Data Format command (I ²C: 0x0D) defines the pixel data format input into the DLPC300.

Table 2-26. Input Pixel Data Format Command

BIT(S)	DESCRIPTION					RESET	TYPE
3:0	Select the pixel format					d2	wr
		Pixel Formats Supported vs Source Type					
		Parallel	Test Pattern	Splash	CPU	BT.656	
	0 = RGB565 transferred on a 16-bit bus (1)	Y	no	Y	Y	no	
	1 = RGB666 or 4:4:4 YCrCb666 transferred on an 18-bit bus (2)	Y	no	no	Y	no	
	2 = RGB888 or 4:4:4 YCrCb888 on a 24-bit bus or 4:2:2 YCrCb880 on a 24-bit bus (2) (3)	Y	Y	no	Y	Y	
	3 = RGB565 transferred on an 8-bit bus (4)	no	no	no	Y	no	
	4 = RGB888 or 4:4:4 YCrCb888 transferred on an 8-bit bus(1 pixel over 3 clocks) (4) (2)	no	no	no	Y	no	
	5 = RGB888 or 4:4:4 YCrCb888 transferred on a 16-bit bus(2 pixels over 3 clocks) (4) (2)	no	no	no	Y	no	
	6 = RGB666 transferred on an 8-bit bus (1 pixel over 3 clocks) (4)	no	no	no	Y	no	
	7 = RGB666 transferred on a 16-bit bus (2 pixels over 3 clocks) (4)	no	no	no	Y	no	
	8 = 4:2:2 YCr/Cb transferred on a 16-bit bus (8-bit Y and 8-bits Cr/Cb) (4) (2)	no	no	no	Y	no	
	9 = 4:2:2 YCr/Cb transferred on an 8-bit bus (8-bit Y and 8-bits Cr/Cb) (1 pixel over 2 clocks) (4) (2)	no	no	no	Y	no	
	Other = Reserved	n/a	n/a	n/a	n/a	n/a	

(1) This parameter is ignored for test-pattern and splash applications. Internal test patterns are assumed to be RGB888 regardless of this pixel-format setting. Splash is assumed to be RGB565 regardless of this pixel-format setting.
(2) RGB vs YCrCb source selection is made via I ²C address 0xC3.
(3) Although the BT.656 source selection is option 2, YCrCb888 on a 24-bit bus, data is only input on the 8 LSBs of the 24-bit PDATA bus.
(4) The horizontal width must be even when using data formats 3–9. Thus the 427 × 240 and 853 × 480 source resolutions are not supported for these data formats.

2.2.4 Image Rotation and Flip

The DLPC300 supports rotation and inversion of images to handle portrait, landscape, rear-, and front-projection configurations.

2.2.4.1 Image Rotation Control: (I²C: 0x0E)

The Image Rotation Control defines whether the input image is displayed without rotation or be rotated by –90º on the DLP3000 DMD. This command is used when the portrait image is to be displayed as landscape. This command is not applicable for landscape source images. If this parameter is changed while displaying a still image, the input still image should be resent. If the image is not re-sent, the output image might be slightly corrupted. Figure 2-1 shows example of an image rotation.

Table 2-27. Image Rotation Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Image rotation (only used if input is portrait, should be set to 0 if input is landscape) 0 = No rotation (image centered on DMD and padded with black bars) 1 = –90º rotation (input portrait is scaled and rotated on DMD)	d0	wr

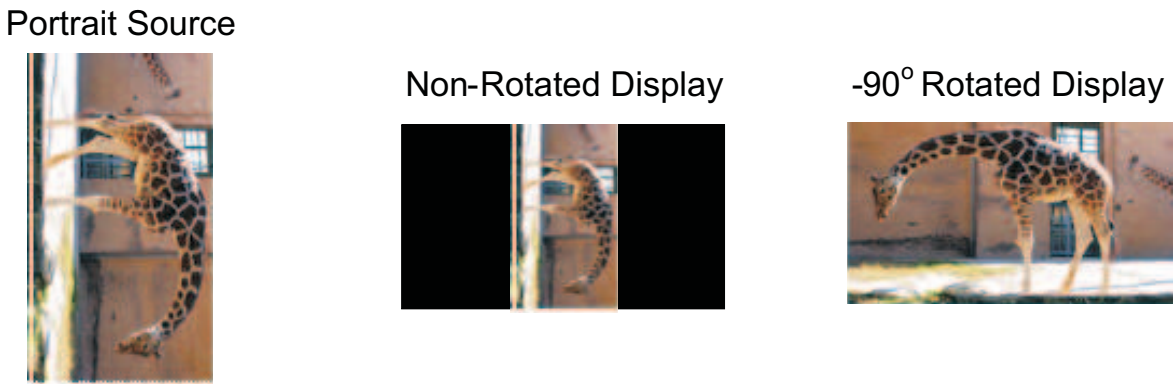


Figure 2-1. Image Rotation Example

2.2.4.2 Long Axis Image Flip: (I²C: 0x0F)

The Long-Axis Image Flip defines whether the input image is flipped across the long axis of the DMD. If this parameter is changed while displaying a still image, the input still image should be re-sent. If the image is not re-sent, the output image might be slightly corrupted. Figure 2-2 shows an example of an image flip.

Table 2-28. Long Axis Image Flip Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Flips image along the long side of the DMD: 0 = Disable flip 1 = Enable flip	d0	wr

Figure 2-2. Image Long-Axis Flip Example

2.2.4.3 Short Axis Image Flip: (I²C: 0x10)

The Short-Axis Image Flip defines whether the input image is flipped across the short axis of the DMD. If this parameter is changed while displaying a still image, the input still image should be resent. If the image is not re-sent, the output image might be slightly corrupted. Figure 2-3 shows an example of an image flip.

Table 2-29. Short Axis Image Flip Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	Flips image along the short side of the DMD: 0 - Disable flip 1 - Enable flip	d0	wr

Figure 2-3. Image Short-Axis Flip Example

2.2.5 Image Processing Control

2.2.5.1 Temporal Dither Control: (I²C: 0x7E)

This command enables or disables temporal dithering. Temporal Dither Control should be disabled for any non-periodic source or any periodic source with a frame rate slower than 50 Hz. Otherwise, temporal dither should be enabled to improve image quality.

Table 2-30. Temporal Dither Control Command

BIT(S)	DESCRIPTION	RESET	TYPE
1:0	Temporal Dither Control(1) 0 – Enable temporal dithering 1 – Reserved 2 – Disable temporal dithering 3 – Reserved	b10	wr

(1) A special CMT table is required in order to disable spatial dithering. This parameter only controls temporal dithering.

2.2.5.2 Automatic Gain Control Function

The Automatic Gain Control (AGC) function helps to maintain maximum perceived display brightness. The following parameters control AGC operation. These parameters are source frame rate dependent and must be updated accordingly.

2.2.5.2.1 Auto Gain Control Function Enable (I²C: 0x50)

Auto Gain Control (AGC) Function Enable is intended for use with motion video sources.

Table 2-31. Auto Gain Control Function Enable Command

BIT(S)	DESCRIPTION	RESET	TYPE
2:0	AGC Function Enable 0–5 – Reserved 6 – AGC disabled 7 – AGC enabled	b110	wr

2.2.5.2.2 AGC Step Size Increment (I²C: 0x52)

Table 2-32. AGC Step Size Increment Command

BIT(S)	DESCRIPTION	RESET	TYPE
11:0	Step size for gain increase for brightness decreases Recommended value = 60/ source frame rate Default: b1 (60 Hz recommended value)	d1	wr

2.2.5.2.3 AGC Step Size Decrement (I²C: 0x53)

Table 2-33. AGC Step Size Decrement Command

BIT(S)	DESCRIPTION	RESET	TYPE
11:0	Step size for gain decrease for brightness increases Recommended value = 60/ source frame rate Default: d1 (60 Hz recommended value)	d1	wr

2.2.5.2.4 AGC Leap Size Decrement (I²C: 0x54)

Table 2-34. AGC Leap Size Decrement Command

BIT(S)	DESCRIPTION	RESET	TYPE
11:0	Largest gain decrement amount for drastic brightness increases Recommended value = 20 + (1200/ source frame rate) Default: d40 (60 Hz recommended value)	d40	wr

2.2.5.3 Color Coordinate Adjustment (CCA) Function

The Color Coordinate Adjustment (CCA) function modifies the color coordinates of the incoming image. This allows the color coordinates and color gain to be adjusted for R, G, B, and W (Y, C, and M are not programmable). Upon hardware reset, the CCA function is disabled, and the coefficients are set to a unity matrix. Note that, the format for all coefficients is u1.8 for all coefficients.

$$\begin{bmatrix} Red \\ Green \\ Blue \end{bmatrix} = \begin{bmatrix} C1R1 & C2R1 & C3R1 & C4R1 & C5R1 & C6R1 & C7R1 \\ C1R2 & C2R2 & C3R2 & C4R2 & C5R2 & C6R2 & C7R2 \\ C1R3 & C2R3 & C3R3 & C4R3 & C5R3 & C6R3 & C7R3 \end{bmatrix} \begin{bmatrix} Red \\ Green \\ Blue \\ Cyan \\ Magenta \\ Yellow \\ White \end{bmatrix}$$

2.2.5.3.1 CCA Function Enable (I²C: 0x5E)

Table 2-35. CCA Function Enable Command

BIT(S)	DESCRIPTION	RESET	TYPE
0	CCA Function Enable 0 – CCA disabled 1 – CCA enabled	d1	wr

2.2.5.3.2 CCA C1R1 Coefficient (I²C: 0x5F)

Table 2-36. CCA C1R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 1 row 1 coefficient (RED)	x100	wr

2.2.5.3.3 CCA C1R2 Coeff (I²C: 0x60)

Table 2-37. CCA C1R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 1 row 2 coefficient (RED)	x000	wr

2.2.5.3.4 CCA C1R3 Coeff (I²C: 0x61)

Table 2-38. CCA C1R3 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 1 row 3 coefficient (RED)	x000	wr

2.2.5.3.5 CCA C2R1 Coeff (I²C: 0x62)

Table 2-39. CCA C2R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 2 row 1 coefficient (GREEN)	x000	wr

2.2.5.3.6 CCA C2R2 Coeff (I²C: 0x63)

Table 2-40. CCA C2R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 2 row 2 coefficient (GREEN)	X100	wr

2.2.5.3.7 CCA C2R3 Coeff (I²C: 0x64)

Table 2-41. CCA C2R3 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 2 row 3 coefficient (GREEN)	x000	wr

2.2.5.3.8 CCA C3R1 Coeff (I²C: 0x65)

Table 2-42. CCA C3R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 3 row 1 coefficient (BLUE)	x000	wr

2.2.5.3.9 CCA C3R2 Coeff (I²C: 0x66)

Table 2-43. CCA C3R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 3 row 2 coefficient (BLUE)	x000	wr

2.2.5.3.10 CCA C3R3 Coeff (I²C: 0x67)

Table 2-44. CCA C3R3 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 3 row 3 coefficient (BLUE)	x100	wr

2.2.5.3.11 CCA C4R1 Coeff (Hard Coded – Not Programmable)

Table 2-45. CCA C4R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 4 row 1 coefficient (CYAN)	x000	wr

2.2.5.3.12 CCA C4R2 Coeff (Hard Coded – Not Programmable)

Table 2-46. CCA C4R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 4 row 2 coefficient (CYAN)	x100	wr

2.2.5.3.13 CCA C4R3 Coeff (Hard Coded – Not Programmable)

Table 2-47. CCA C4R3 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 4 row 3 coefficient (CYAN)	x100	wr

2.2.5.3.14 CCA C5R1 Coeff (Hard Coded – Not Programmable)

Table 2-48. CCA C5R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 5 row 1 coefficient (MAGENTA)	x100	wr

2.2.5.3.15 CCA C5R2 Coeff (Hard Coded – Not Programmable)

Table 2-49. CCA C5R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 5 row 2 coefficient (MAGENTA)	x000	wr

2.2.5.3.16 CCA C5R3 Coeff (Hard Coded – Not Programmable)

Table 2-50. CCA C5R3 CCoefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 5 row 3 coefficient (MAGENTA)	x100	wr

2.2.5.3.17 CCA C6R1 Coeff (Hard Coded – Not Programmable)

Table 2-51. CCA C6R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 6 row 1 coefficient (YELLOW)	x100	wr

2.2.5.3.18 CCA C6R2 Coeff (Hard Coded – Not Programmable)

Table 2-52. CCA C6R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 6 row 2 coefficient (YELLOW)	x100	wr

2.2.5.3.19 CCA C6R3 Coeff (Hard Coded – Not Programmable)

Table 2-53. CCA C6R3 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE
8:0	Column 6 row 3 coefficient (YELLOW)	x000	wr

2.2.5.3.20 CCA C7R1 Coeff (I²C: 0x71)

Table 2-54. CCA C7R1 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE00
8:0	Column 7 row 1 coefficient (WHITE)	x100	wr

2.2.5.3.21 CCA C7R2 Coeff (I²C: 0x72)

Table 2-55. CCA C7R2 Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE01
8:0	Column 7 row 2 coefficient (WHITE)	x100	wr

2.2.5.3.22 CCA C7R3 Coeff (I²C: 0x73)

Table 2-56. CCA C7R Coefficient

BIT(S)	DESCRIPTION	RESET	TYPE02
8:0	Column 7 row 3 coefficient (WHITE)	x100	wr

2.2.6 LED Driver Control

LED driver operation is a function of the LED_ENABLE input, individual red, green and blue LED-enable software-control parameters, and the white-point correction function. The recommended order for initializing LED drivers is to:

1. Assert the appropriate LED_ENABLE input HIGH.
2. Program the individual red, green and blue LED driver currents.
3. Enable the individual LED enable outputs
4. Turn ON the DLP® display sequence
5. Simultaneously turn ON the red, green and blue LED enables.
6. Turn ON white-point correction (as desired).

The LED-current software-control parameters define PWM values that drive corresponding LED current. The white-point correction function, when enabled, continually monitors LED intensity, via external sensor, and automatically adjusts these PWM values to maintain a constant white point. Due to LED manufacturing variations, a Pico Projector manufacturing calibration step is recommended to set the initial white-point correction of each unit. When the white-point correction function is not enabled, the red, green and blue LED driver-current parameters, listed following, must be used to set the drive for each LED.

CAUTION

Careful control of LED current is needed to prevent damage to LEDs. Follow all LED manufacturer recommendations and maintain LED current levels within recommended operating conditions. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, etc.). Therefore, the recommended and absolute-maximum settings vary greatly.

2.2.6.1 LED Enable Outputs

DLPC300 offers two sets of pins to control the LED enables:

- LED_SEL_0 and LED_SEL_1
- RED_EN, GREEN_EN, BLUE_EN

After reset, the LED_SEL_0 and LED_SEL_1 are active, but the individual LED enables (RED_EN, GREEN_EN, and BLUE_EN) are not active. To output the individual LED enables, the LED Enable and Buffer Control Registers 1 and 2 must be configured through an I²C command.

2.2.6.1.1 LED Enable and Buffer Control Register 1 (I²C: 0x4B)

LED Enable and Buffer Control Register 1 controls the output of RED_EN, PATTERN_INVERT, BUFFER_SWAP, and READ_BUF0 pins.

Table 2-57. LED Enable and Buffer Control Register 1

BIT(S)	DESCRIPTION	RESET	TYPE03
7:0	Enable READ_BUF0 output: 0x00 = Disable READ_BUF0 output, pin is always driven low 0x24 = Enable READ_BUF0 output. Pin is driven by internal buffer logic	d0	wr
15:8	Enable BUFFER_SWAP output: 0x00 = Disable BUFFER_SWAP output, pin is always driven low 0x16 = Enable BUFFER_SWAP output. Pin is driven by internal buffer logic.	d0	wr
23:16	Enable PATTERN_INVERT output: 0x00 = Disable PATTERN_INVERT output, pin is always driven low 0x15 = Enable PATTERN_INVERT output. Pin is driven by internal buffer logic	d0	wr
31:24	Enable RED_EN output: 0x00 = Disable RED_EN output, pin is always driven low 0x14 = EnableRED_EN output. Pin is driven by internal LED circuits	d0	wr

2.2.6.1.2 LED Enable and Buffer Control Register 2 (I²C: 0x4C)

LED Enable and Buffer Control Register 2 controls the output of READ_BUF1, OUTPUT_TRIGGER, BLUE_EN, and GREEN_EN pins.

Table 2-58. LED Enable and Buffer Control Register 2

BIT(S)	DESCRIPTION	RESET	TYPE04
7:0	Enable GREEN_EN output: 0x00 = Disable GREEN_EN output, pin is always driven low 0x13 = Enable GREEN_EN output. Pin is driven by internal LED circuits	d0	wr
15:8	Enable BLUE_EN output: 0x00 = Disable BLUE_EN output, pin is always driven low 0x12 = Enable BLUE_EN output. Pin is driven by internal LED circuits	d0	wr
23:16	Enable OUTPUT_TRIGGER output: 0x00 = Disable OUTPUT_TRIGGER output, pin is always driven low 0x11 = Enable OUTPUT_TRIGGER output. Pin is driven by internal buffer logic	d0	wr
31:24	Enable READ_BUF1 output: 0x00 = Disable READ_BUF1 output, pin is always driven low 0x25 = Enable READ_BUF1 output. Pin is driven by internal buffer logic	d0	wr

2.2.6.2 RGB LED Driver Enable (I²C: 0x16)

This parameter enables or disables the red, blue, and green LEDs.

Table 2-59. RGB LED Driver Enable Command

BIT(S)	DESCRIPTION	RESET	TYPE05
0	Enable red LED: 0 = Disable red LED 1 = Enable red LED	d0	wr
1	Enable green LED: 0 = Disable green LED 1 = Enable green LED	d0	wr
2	Enable blue LED: 0 = Disable blue LED 1 = Enable blue LED	d0	wr

2.2.6.3 Red LED Driver Current (I²C: 0x12)

This parameter controls the pulse duration of the red LED PWM modulation output pin. The resolution is 11 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0 to 100% in 1/1024 steps. A setting of 0x400 gives the minimum PWM setting. The LED current is a function of the specific LED driver design.

Using the RGB LED enable pins to gate the time the LED is on during video frames impacts the total LED current and average power.

CAUTION

Care should be taken when using this command. Improper use of this command can lead to damage to the system. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, etc.). Therefore, recommended and absolute-maximum settings vary greatly.

Table 2-60. Red LED Driver Current Command

BIT(S)	DESCRIPTION	RESET	TYPE06
10:0	Red LED current PWM value Valid range is: 0x000 (0% duty cycle → LEDs are 100% ON) to 0x400 (100% duty cycle → LEDs are 0% ON) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus varies by design.	d1023	wr

2.2.6.4 Green LED Driver Current (I²C: 0x13)

This parameter controls the pulse duration of the green LED PWM modulation output pin. The resolution is 11 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0 to 100% in 1/1024 steps. A setting of 0x400 gives the minimum PWM setting. The LED current is a function of the specific LED driver design.

Using the RGB LED enable pins to gate the time the LED is on during video frames impacts the total LED current and average power.

CAUTION

Care should be taken when using this command. Improper use of this command can lead to damage to the system. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, etc.). Therefore, recommended and absolute-maximum settings vary greatly.

Table 2-61. Green LED Driver Current Command

BIT(S)	DESCRIPTION	RESET	TYPE07
10:0	Green LED current PWM value Valid range is: 0x000 (0% duty cycle → LEDs are 100% ON) to 0x400 (100% duty cycle → LEDs are 0% ON) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus varies by design.	d1023	wr

2.2.6.5 Blue LED Driver Current (I²C: 0x14)

This parameter controls the pulse duration of the blue LED PWM modulation output pin. The resolution is 11 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0 to 100% in 1/1024 steps. A setting of 0x400 gives the minimum PWM setting. The LED current is a function of the specific LED driver design.

Using the RGB LED enable pins to gate the time the LED is on during video frames impacts the total LED current and average power.

CAUTION

Care should be taken when using this command. Improper use of this command can lead to damage to the system. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, etc.). Therefore, recommended and absolute-maximum settings vary greatly.

Table 2-62. Blue LED Driver Current Command

BIT(S)	DESCRIPTION	RESET	TYPE08
10:0	Blue LED current PWM value Valid range is: 0x000 (0% duty cycle → LEDs are 100% ON) to 0x400 (100% duty cycle → LEDs are 0% ON) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus varies by design.	d1023	wr

2.2.7 Sleep Mode

2.2.7.1 Interface Sleep Control (I²C: 0x1D)

Interface sleep mode places all the source interfaces (parallel, BT.656, internal test patterns, and splash screen) in a low-power state. This mode is useful for saving power for still-image applications where updates are infrequent. Interface sleep control is ONLY usable when sequence sync mode = 0 (in effect, free-run). Interface Sleep Control must be disabled when sequence sync mode = 1. Interface sleep mode should only be enabled after all data for the last frame to be displayed has been transferred to the DLPC300, and must be disabled prior to sending any new data.

Table 2-63. Interface Sleep Control Command

BIT(S)	DESCRIPTION	RESET	TYPE09
0	Interface Sleep Control 0 = Interface sleep mode disabled – interfaces active 1 = Interface sleep mode enabled – all data I/F operations shut down (Commands can still be transferred.)	d0	wr

2.2.8 Internal Pattern Generator

The DLPC300 can generate a set of 15 vertical 1-bit monochrome patterns with its internal pattern generator. Up to 32 of these vertical patterns can be arranged in any order with or without inversion. The inversion of a pattern converts the black regions to white and the white regions to black. Table 2-64 describes the available patterns. Pattern numbers 0 through 10 form a set of gray coded patterns. Pattern numbers 11 through 14 can be used for auto-focus.

Table 2-64. Internally Generated Patterns

Pattern Number	Description	Starting Color	Right Border Pixel Width	Vertical Stripe Pixel Width	Repetitions of Vertical Stripes	Left Border Pixel Width
0x0	All Black	Black	608	0	0	0
0x1	50% Black, 50% White	Black	304	304	1	0

Table 2-64. Internally Generated Patterns (continued)

Pattern Number	Description	Starting Color	Right Border Pixel Width	Vertical Stripe Pixel Width	Repetitions of Vertical Stripes	Left Border Pixel Width
0x2	512 pixel-wide Black Centered Stripe	White	48	512	1	48
0x3	256 pixel-wide White Centered Stripe	Black	176	256	1	176
0x4	128 pixel-wide Black and White Stripes	White	112	128	3	112
0x5	64 pixel-wide Black and White Stripes	Black	16	64	9	16
0x6	32 pixel-wide Black and White Stripes	White	32	32	17	32
0x7	16 pixel-wide Black and White Stripes	White	8	16	37	8
0x8	8 pixel-wide Black and White Stripes	White	4	8	75	4
0x9	4 pixel-wide Black and White Stripes	White	2	4	151	2
0xA	2 pixel-wide Black and White Stripes	White	1	2	303	1
0xB	304 pixel-wide White Centered Stripe	Black	152	304	1	152
0xC	152 pixel-wide White Centered Stripe	Black	228	152	1	228
0xD	76 pixel-wide White Centered Stripe	Black	266	76	1	266
0xE	38 pixel-wide White Centered Stripe	Black	285	38	1	285

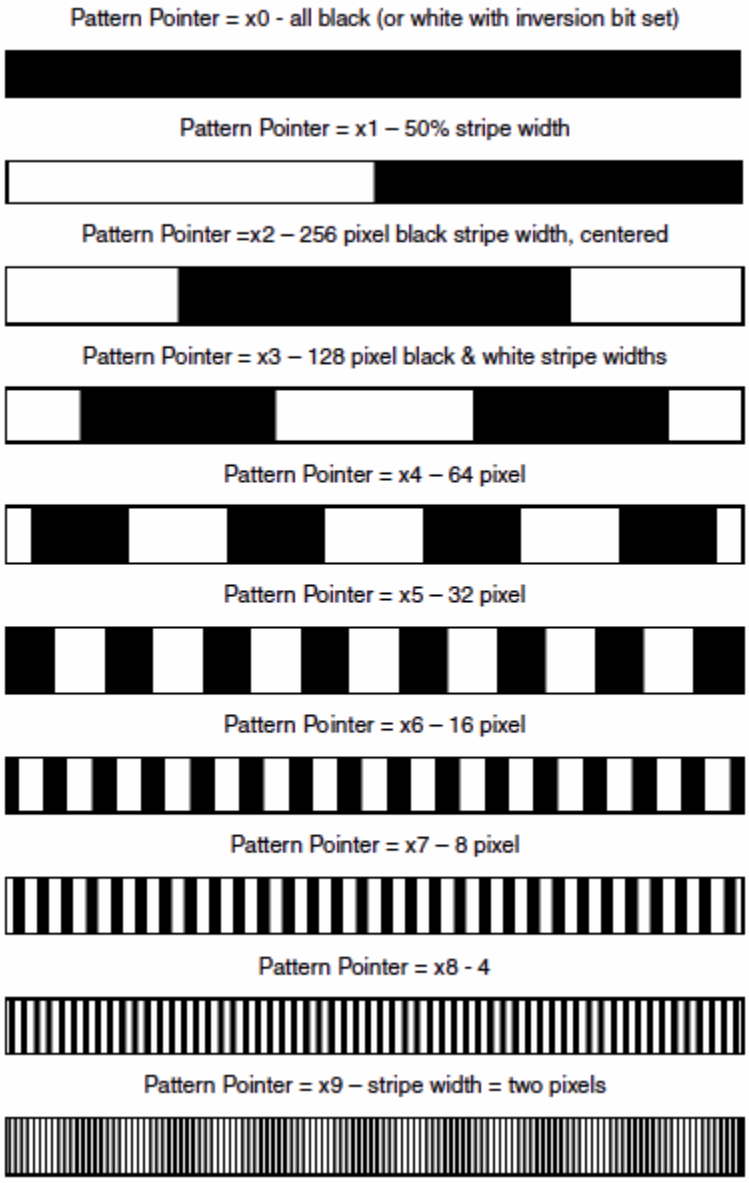


Figure 2-4. Gray Coded Patterns

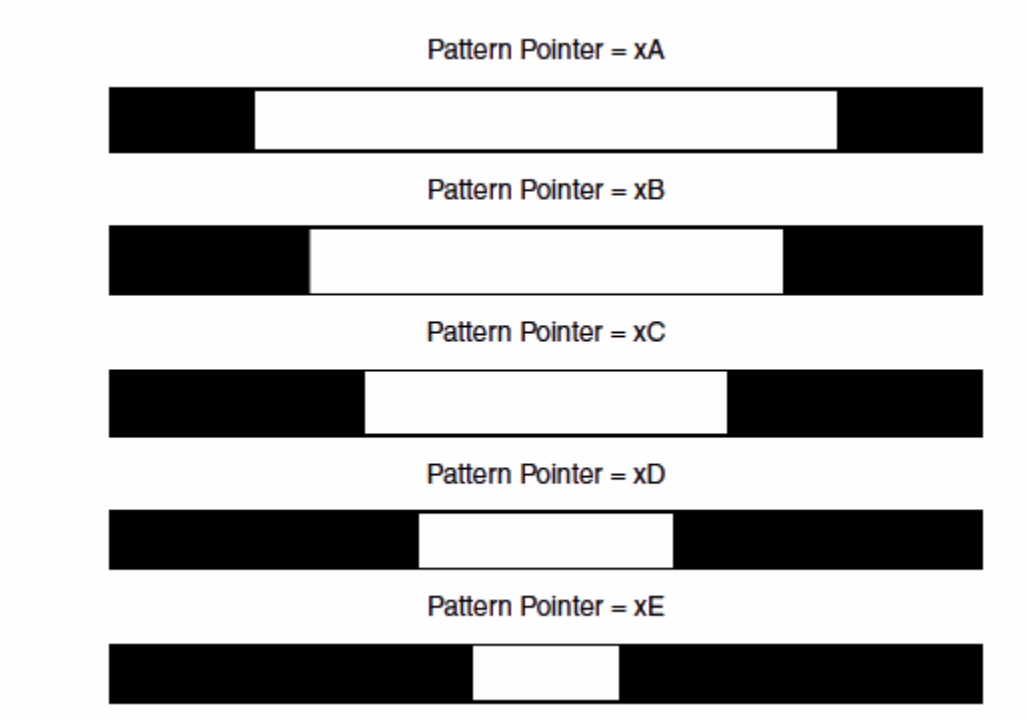


Figure 2-5. Additional Patterns

2.2.8.1 Pattern Generator Enable Register (I²C: 0xCF)

Table 2-65 depicts the Internal Pattern Generator Enable Register for pattern number 0 through pattern number 32.

Table 2-65. Internal Generator Enable Register

BIT(S)	DESCRIPTION	RESET	TYPE10
0	Enables internal pattern generator 0: Disables internal pattern generator 1: Enables internal pattern generator	b0	wr
3:1	Reserved	b0	r
8:4	Indicates set of patterns displayed in sequence 0: Pattern number 1 only 1: Pattern number 1 through pattern number 2 2: Pattern number 1 through pattern number 3 3: Pattern number 1 through pattern number 4 … 32: Pattern number 1 through pattern number 32	b00000	wr
31:9	Reserved	b0	r

2.2.8.2 Pattern Generator Control Registers for Patterns 1-8 (I²C: 0xD0)

Table 2-66 depicts the Internal Pattern Generator Control Register for pattern number 0 through pattern number 8.

Table 2-66. Internal Generator Control Register for Pattern Number 1–Pattern Number 8

BIT(S)	DESCRIPTION	RESET	TYPE11
3:0	Selects internally generated pattern to display on pattern number 1 0–15: See Table 2-64	b0	wr
7:4	Selects internally generated pattern to display on pattern number 2 0–15: See Table 2-64	b0	wr
11:8	Selects internally generated pattern to display on pattern number 3 0–15: See Table 2-64	b0	wr
15:12	Selects internally generated pattern to display on pattern number 4 0–15: See Table 2-64	b0	wr
19:16	Selects internally generated pattern to display on pattern number 5 0–15: See Table 2-64	b0	wr
23:20	Selects internally generated pattern to display on pattern number 6 0–15: See Table 2-64	b0	wr
27:24	Selects internally generated pattern to display on pattern number 7 0–15: See Table 2-64	b0	wr
31:28	Selects internally generated pattern to display on pattern number 8 0–15: See Table 2-64	b0	wr

2.2.8.3 Pattern Generator Control Registers for Patterns 9-16 (I²C: 0xD1)

Table 2-67 depicts the Internal Pattern Generator Control Register for pattern number 9 through pattern number 16.

Table 2-67. Internal Generator Control Register for Pattern Number 9–Pattern Number 16

BIT(S)	DESCRIPTION	RESET	TYPE12
3:0	Selects internally generated pattern to display on pattern number 9 0–15: See Table 2-64	b0	wr
7:4	Selects internally generated pattern to display on pattern number 10 0–15: See Table 2-64	b0	wr
11:8	Selects internally generated pattern to display on pattern number 11 0–15: See Table 2-64	b0	wr
15:12	Selects internally generated pattern to display on pattern number 12 0–15: See Table 2-64	b0	wr
19:16	Selects internally generated pattern to display on pattern number 13 0–15: See Table 2-64	b0	wr
23:20	Selects internally generated pattern to display on pattern number 14 0–15: See Table 2-64	b0	wr
27:24	Selects internally generated pattern to display on pattern number 15 0–15: See Table 2-64	b0	wr
31:28	Selects internally generated pattern to display on pattern number 16 0–15: See Table 2-64	b0	wr

2.2.8.4 Pattern Generator Control Registers for Patterns 17-24 (I²C: 0xD2)

Table 2-68 depicts the Internal Pattern Generator Control Register for pattern number 17 through pattern number 24.

Table 2-68. Internal Generator Control Register for Pattern Number 17–Pattern Number 24

BIT(S)	DESCRIPTION	RESET	TYPE13
3:0	Selects internally generated pattern to display on pattern number 17 0–15: See Table 2-64	b0	wr
7:4	Selects internally generated pattern to display on pattern number 18 0–15: See Table 2-64	b0	wr
11:8	Selects internally generated pattern to display on pattern number 19 0–15: See Table 2-64	b0	wr
15:12	Selects internally generated pattern to display on pattern number 20 0–15: See Table 2-64	b0	wr
19:16	Selects internally generated pattern to display on pattern number 21 0–15: See Table 2-64	b0	wr
23:20	Selects internally generated pattern to display on pattern number 22 0–15: See Table 2-64	b0	wr
27:24	Selects internally generated pattern to display on pattern number 23 0–15: See Table 2-64	b0	wr
31:28	Selects internally generated pattern to display on pattern number 24 0–15: See Table 2-64	b0	wr

2.2.8.5 Pattern Generator Control Registers for Patterns 25-32 (I²C: 0xD3)

Table 2-69 depicts the Internal Pattern Generator Control Register for pattern number 25 through pattern number 32.

Table 2-69. Internal Generator Control Register for Pattern Number 25–Pattern Number 32

BIT(S)	DESCRIPTION	RESET	TYPE`4
3:0	Selects internally generated pattern to display on pattern number 25 0–15: See Table 2-64	b0	wr
7:4	Selects internally generated pattern to display on pattern number 26 0–15: See Table 2-64	b0	wr
11:8	Selects internally generated pattern to display on pattern number 27 0–15: See Table 2-64	b0	wr
15:12	Selects internally generated pattern to display on pattern number 28 0–15: See Table 2-64	b0	wr
19:16	Selects internally generated pattern to display on pattern number 29 0–15: See Table 2-64	b0	wr
23:20	Selects internally generated pattern to display on pattern number 30 0–15: See Table 2-64	b0	wr
27:24	Selects internally generated pattern to display on pattern number 31 0–15: See Table 2-64	b0	wr
31:28	Selects internally generated pattern to display on pattern number 32 0–15: See Table 2-64	b0	wr

2.2.8.6 Pattern Generator Inversion Control Register (I²C: 0xD4)

Table 2-70 depicts the Internal Pattern Generator Inversion Control Register.

Table 2-70. Internal Generator Inversion Control Register

BIT(S)	DESCRIPTION	RESET	TYPE`5
0	Inverts pattern number 1 0: Pattern not inverted 1: Pattern inverted	b0	wr
1	Inverts pattern number 2 0: Pattern not inverted 1: Pattern inverted	b0	wr
2	Inverts pattern number 3 0: Pattern not inverted 1: Pattern inverted	b0	wr
3	Inverts pattern number 4 0: Pattern not inverted 1: Pattern inverted	b0	wr
4	Inverts pattern number 5 0: Pattern not inverted 1: Pattern inverted	b0	wr
5	Inverts pattern number 6 0: Pattern not inverted 1: Pattern inverted	b0	wr
6	Inverts pattern number 7 0: Pattern not inverted 1: Pattern inverted	b0	wr
7	Inverts pattern number 8 0: Pattern not inverted 1: Pattern inverted	b0	wr
8	Inverts pattern number 9 0: Pattern not inverted 1: Pattern inverted	b0	wr
9	Inverts pattern number 10 0: Pattern not inverted 1: Pattern inverted	b0	wr
10	Inverts pattern number 11 0: Pattern not inverted 1: Pattern inverted	b0	wr
11	Inverts pattern number 12 0: Pattern not inverted 1: Pattern inverted	b0	wr
12	Inverts pattern number 13 0: Pattern not inverted 1: Pattern inverted	b0	wr
13	Inverts pattern number 14 0: Pattern not inverted 1: Pattern inverted	b0	wr
14	Inverts pattern number 15 0: Pattern not inverted 1: Pattern inverted	b0	wr
15	Inverts pattern number 16 0: Pattern not inverted 1: Pattern inverted	b0	wr

Table 2-70. Internal Generator Inversion Control Register (continued)

BIT(S)	DESCRIPTION	RESET	TYPE`5
16	Inverts pattern number 17 0: Pattern not inverted 1: Pattern inverted	b0	wr
17	Inverts pattern number 18 0: Pattern not inverted 1: Pattern inverted	b0	wr
18	Inverts pattern number 19 0: Pattern not inverted 1: Pattern inverted	b0	wr
19	Inverts pattern number 20 0: Pattern not inverted 1: Pattern inverted	b0	wr
20	Inverts pattern number 21 0: Pattern not inverted 1: Pattern inverted	b0	wr
21	Inverts pattern number 22 0: Pattern not inverted 1: Pattern inverted	b0	wr
22	Inverts pattern number 23 0: Pattern not inverted 1: Pattern inverted	b0	wr
23	Inverts pattern number 24 0: Pattern not inverted 1: Pattern inverted	b0	wr
24	Inverts pattern number 25 0: Pattern not inverted 1: Pattern inverted	b0	wr
25	Inverts pattern number 26 0: Pattern not inverted 1: Pattern inverted	b0	wr
26	Inverts pattern number 27 0: Pattern not inverted 1: Pattern inverted	b0	wr
27	Inverts pattern number 28 0: Pattern not inverted 1: Pattern inverted	b0	wr
28	Inverts pattern number 29 0: Pattern not inverted 1: Pattern inverted	b0	wr
29	Inverts pattern number 30 0: Pattern not inverted 1: Pattern inverted	b0	wr
30	Inverts pattern number 31 0: Pattern not inverted 1: Pattern inverted	b0	wr

Table 2-70. Internal Generator Inversion Control Register (continued)

BIT(S)	DESCRIPTION	RESET	TYPE`5
31	Inverts pattern number 32 0: Pattern not inverted 1: Pattern inverted	b0	wr

2.2.9 Sequencer Control

The following registers control the video sequencer.

2.2.9.1 Sequencer Control: (I²C: 0x82)

Table 2-71 enables or disables the sequencer.

Table 2-71. Sequence Control Command

BIT(S)	DESCRIPTION	RESET	TYPE16
0	Sequencer Control Enable 0 = Disable sequence 1 = Enable sequence	d0	wr
1	Sequencer Vector Increment Enable 0 = Sequencer Vector Increment set to 1 1 = Sequencer Vector Increment dictated by sequence sub-vector number. (Typical operating mode)	d0	wr

2.2.9.2 Sequence Sync Mode (I²C: 0x1E)

The Sequence Sync Mode command defines whether or not the DLP® display frame rate needs to be independent of the source frame or synchronized with the source frame rate.

When the source frame rate is non-periodic, such as when a still image updates in response to user control, the DLP® display frame rate needs to be independent from the source such that the display can be refreshed at a regular rate. To do this, the Sequence Sync Mode must be set to free-run mode. In this mode, the DLP® display frame rate is defined directly by the frame rate attribute of the selected DLP® display sequence.

When the source frame rate is periodic, such as from a motion video or graphics source, the DLP® display frame rate needs to be synchronized to the source such that motion artifacts are minimized. To do this the Sequence Sync Mode must be set to lock-to-VSYNC mode where VSYNC is the applicable vertical sync signal. For BT.656 applications, the VSYNC signal is encoded into the data stream. For parallel interface applications, the VSYNC input pin drives source synchronization. The DLPC300 provides the ability to synchronize the DLP® display frame rate to an integer multiple of the source frame rate over a range of 1x to 12x. A multiple that is greater than one provides the option to increase the display frame rate when the source frame rate is slow and would result in an undesirably low display refresh rate. In all display modes, the DLP® display frame rate is defined by the frame rate attribute of the selected DLP® display sequence. However, the source frame rate is assume to be DLP® display frame rate divided by N (where N is a programmable integer multiplier).

Table 2-72. Sequence Sync Mode Command

BIT(S)	DESCRIPTION	RESET	TYPE17
0	Sequence Sync Mode[1] 0 - Free-run (The display is asynchronous with respect to the source) 1 - Lock-to-VSYNC (The display is synchronous with the source)	d0	wr

(1) The only valid image inputs for using *lock-to-VSYNC* mode are:
Parallel I/F input frames that are periodic and equal to the video frame rate programmed in the Video Frame Rate Register (0x19).
NTSC inputs (periodic at 60 Hz) from a video decoder device, like TVP515x.
PAL/SECAM inputs (periodic at 50 Hz) from a video decoder device, like TVP515x.
Internal test patterns.
Free-run mode must be selected in these cases:
Parallel I/F for frame rates that are < 5 Hz or non sub-multiples of the video frame rate programmed in the Video Frame Rate Register (0x19).
Parallel I/F for frame rates that are not periodic.
Splash screens.

2.2.9.3 Sequence Vector Setup: (I²C: 0x83)

The Sequence Vector Setup selects the desired sequence to run from on-chip memory. Two parameters are used to describe a sequence: sequence vector and sub-vector. The sequence vector indicates the starting vector offset location while the sub-vector defines the number of times the sequence is repeated in a VSYNC period. Refer to Section 2.3 for supported sequences, vectors, and sub-vectors.

Table 2-73. Sequence Vector Setup Command

BIT(S)	DESCRIPTION	RESET	TYPE18
7:0	Sequence start vector select See start vector column of Table 2-80 and Table 2-80	x00	wr
15:8	Number of sequence sub-vectors 0 = A value of zero is illegal See sub-vector column of Table 2-80 and Table 2-80. When Sequence Vector Increment Enable is set, this parameter defines the number of times the sequence is repeated for each VSYNC input.	x02	wr

2.2.10 Compound I²C Commands

To upload a new sequence from SPI flash firmware, a compound I²C command must be issued. The compound I²C command allows the execution of several time consuming operations in a sequence of I²C commands. A compound I²C command sequence consists of:

1. Poll the Handshake Register (0x3A) and wait until processor is not busy.
2. Write the Data Register (0x39) with the command arguments.
3. Set busy status in the Handshake Register (0x3A).
4. Write a Command Register (0x38) with the command to be executed.
5. Poll the Handshake Register (0x3A) to wait for processor not busy.

To avoid potential corruption, no other I²C transactions, except to the Data and Handshake Registers should be sent to the DLPC300 until the completion of the prior compound I²C command processing. This restriction is necessary to allow sufficient time to complete these compound I²C commands. To determine when the current compound I²C command processing has completed, the host must poll the Handshake Register and wait for the command busy flag to be cleared.

2.2.10.1 Compound I²C Command Handshake Register (I²C: 0x3A)

The Handshake Register provides a compound I²C command busy flag that can be polled to help manage compound I²C command processing. The intent of this flag is to ensure a new command is not sent until processing of the prior command is complete and that any associated data is properly transferred. The command busy flag is set by the host before writing a new command to the Compound I²C Command Register. This flag will remain set until the previous compound I²C command completes processing. When this flag is set, the host understands that the previous command execution is not complete. When this flag is cleared, all processing associated with the previous compound I²C command is complete. The host is expected to poll the Compound I²C Command Handshake Register and must not send a new command until the busy flag is cleared. If a new compound I²C command is received before completion of the previous compound I²C command, the previous compound I²C command aborts, setting a corresponding error in the Compound I²C Command Error Status Register. Then, the new command is processed. To prevent the host from waiting for a cleared flag indefinitely, the host should have a timeout.

After a write command is received, the DLPC300 processor clears the busy flag after reading the data from the Compound I²C Command Data Register and writing it to the appropriate destination.

After a read command is received, the DLPC300 processor clears the busy flag after fetching the requested data and writing it to the Compound I²C Command Data Register. The host is expected to wait for the busy flag to clear before sending the next command.

Table 2-74. Compound I²C Command Handshake Register

BIT(S)	DESCRIPTION	RESET	TYPE20
0	Compound I²C Command Handshake busy flag (This flag is set by the host before any writes to the Compound I²C Command Register. This flag is cleared by the DLPC300 processor when it completes the previous compound I²C command. The host is expected to wait for this busy flag to be cleared before sending the next command.) 0 = Compound I²C command processing is idle and ready to accept a new command. 1 = A compound I²C command has been issued and is being processed (indicates that command processing is not complete and any command received during this time will abort processing of the prior command in order to process the new command).	b0	wr

2.2.10.2 Compound I²C Command Data Register (I²C: 0x39)

The Compound I²C Command Data Register accepts a parameter associated with the compound I²C command.

Table 2-75. Compound I²C Command Data Register

BIT(S)	DESCRIPTION	RESET	TYPE19
7:0	Compound I²C Command Data	d0	wr

2.2.10.3 Compound I²C Command Command Register (I²C: 0x38)

The Compound I²C Command Command Register accepts a set of commands processed by the DLPC300 processor. These commands are 8-bit commands received via the I²C bus that perform more than simple register read/ write operations. Most commands must also be accompanied by compound I²C command data. For commands that require a compound I²C command data value, the data value must be written prior to writing the compound I²C command.

Table 2-76. Compound I²C Command Command Register

BIT(S)	DESCRIPTION	RESET	TYPE
7:0	Compound I²C Command Command	d0	wr

2.2.10.4 Compound I²C Command Definitions

Table 2-77 provides a list of supported compound I²C commands and their corresponding op-codes (options and operations).

Table 2-77. Compound I²C Command Definitions

Command	Description	Value
0xC1	Loads a new display sequence from SPI flash	0–7, 13–16 for external video sequence (See Table 2-80) 17–31 for internal video sequences with optional FPGA (See Table 2-80)

2.3 Display Sequences

A DLP® display sequence consists of several parameters which dictate the loading of the DMD and the control of PWM to the LEDs. To upload a display sequence, a compound I²C command must be issue to read the sequence from SPI flash firmware, load into the DLPC300 processor memory, and configure the DLPC300 processor to this sequence. Section 2.2.10 describes the compound I²C command sequence. Once a particular sequence is loaded into the DLPC300 processor memory, the Sequence Vector Setup selects the vector of the sequence to execute.

DLPC300 supports two main video output modes: streaming data through the 24-bit RGB parallel bus or displaying preloaded images from the DLPC300 mDDR display buffer. The video output modes operate on a per-frame basis where the DLPC300 takes the input data and appropriately allocates it in a frame. For example, a 24-bit RGB input image is allocated into a 60 Hz frame by dividing each color (red, green, and blue) into specific percentages of the frame (See Table 2-80). Therefore, for 40% red, 45% green, and 15% blue ratio; the red, green, and blue colors have a 6.67 ms, 7.5 ms, and 2.54 ms time slot allocated, respectively. Because each color has an 8-bit depth, each color time slot is further divided into bit-planes, as shown in Figure 2-6. A bit-plane is the two-dimensional arrangement of one bit extracted from all the pixels in the full color 2D image.

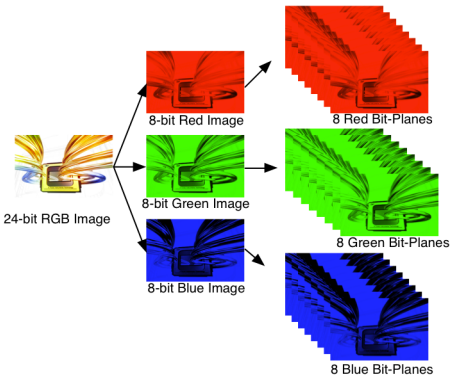


Figure 2-6. Bit-Planes of a 24-bit RGB Image

The length of each bit-plane in the time slot is weighted by the corresponding power of 2 of its binary representation. This provides a binary pulse-width modulation of the image. In the 24-bit RGB streaming input, Figure 2-7 shows that each color time slot is divided into eight bit-planes. The sum of all bit weighs in the color time slot equal 255, with each bit-plane weighted by its binary representation.

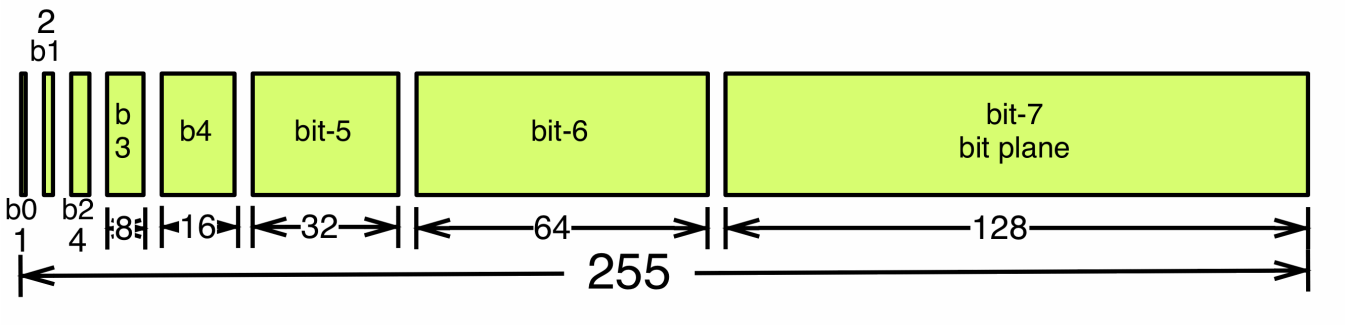


Figure 2-7. Bit Partition in a Frame for an 8-bit Monochrome Image

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane and shining light on them. With the binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on and illuminated. For a 24-bit RGB frame image input to the DLPC300, the DLPC300 creates 24 bit-planes, stores them on the mDDR, and sends them to the DLP3000 DMD on the next frame, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC300 controls the time this bit-plane is exposed to light. The time a bit plane is illuminated is directly proportional to the intensity of the bit-plane. To improve image quality in video frames, these bit-planes, time slots, and color frames are intertwined and interleaved with spatial-temporal algorithms by the DLPC300.

For other applications where this image enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The bit-depth of the pattern is then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed. For structured light applications this mechanism provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object.

As shown in Figure 2-8, the DLPC300 stores four 24-bit frames in the mDDR. This portion of mDDR serves as the DLP3000 display buffer. The 96 bit-plane display buffer is arranged in a circular buffer style. Two signals from the DPLC300: D_BUF [1:0] indicate the buffer currently in use by the DLPC300, meaning that the last bit-plane addition to the buffer replaces the oldest stored bit-plane. While the DLPC300 fills one buffer, the DLPC300 can read a previously filled buffer and load it into the DLP3000 DMD array. The DLPC300 takes 215 µs to load the first bit-plane into the DMD array. The DLPC300 takes 135 µs to rotate buffers. Therefore, for every 24-bit planes there is an additional 135 µs delay to rotate the buffer.

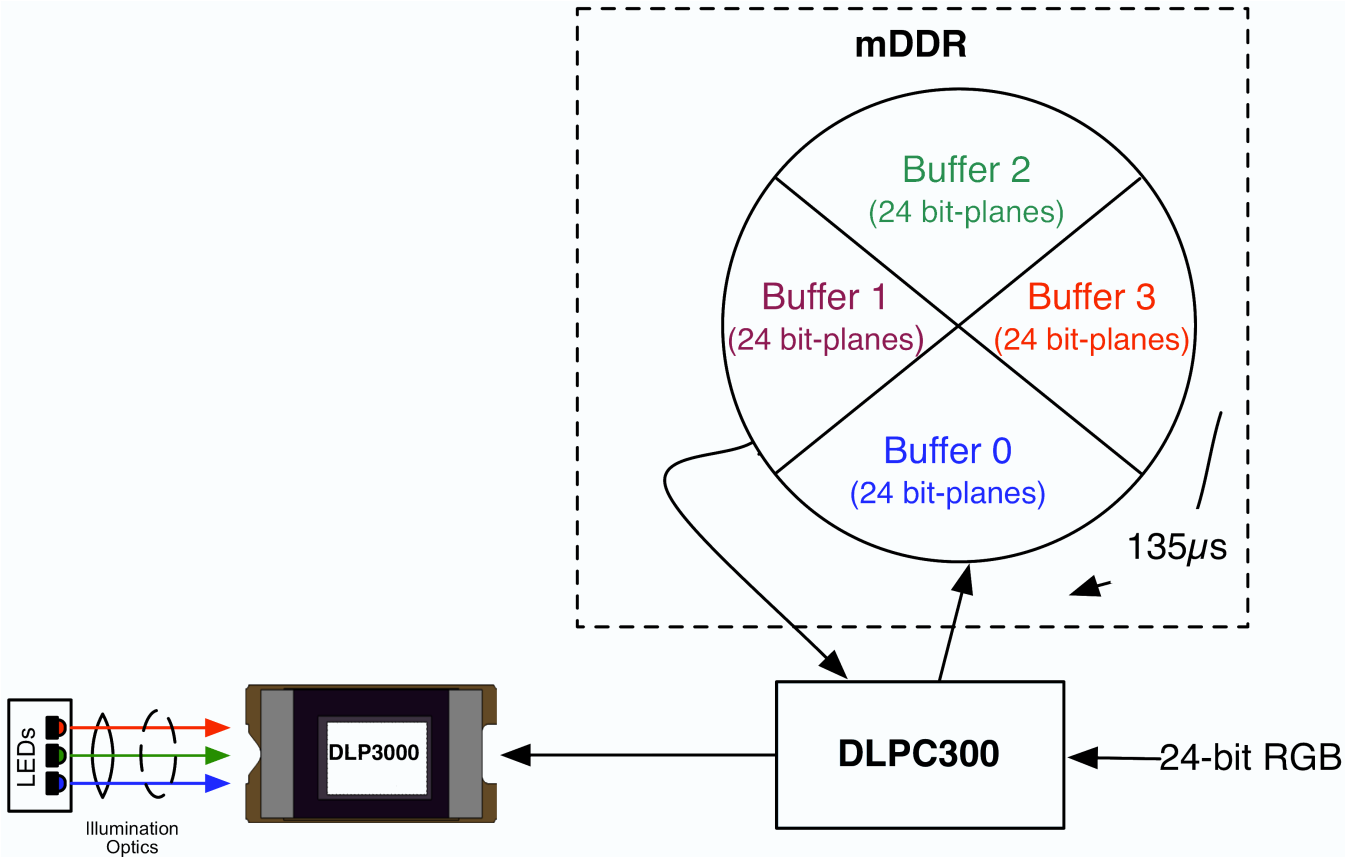


Figure 2-8. DLP3000 Frame Buffer

Note that the displayed image is frame delayed in relation to the data streamed through the 24-bit RGB parallel bus, as shown in Figure 2-9. In this figure, R0 corresponds to the red portion of Image 0, G0 corresponds to the green portion of Image 0, and B0 corresponds to the blue portion of Image 0. R1 corresponds to the red portion of Image 1, G1 corresponds to the green portion of Image 1, and B1 corresponds to the blue portion of Image 1, etc.

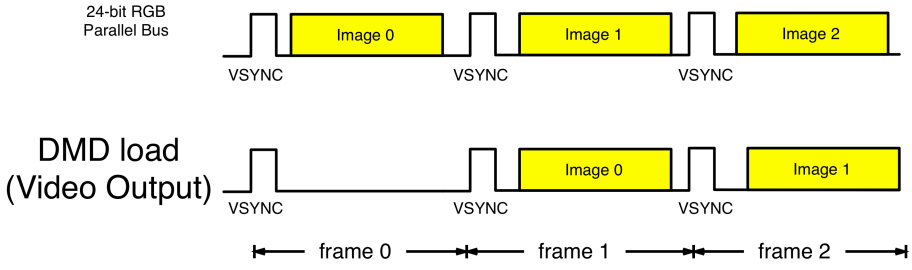


Figure 2-9. Frame Delay Between RGB Input and Video Output

2.3.1 Video Modes

DLPC300 utilizes display sequences to support two main video output modes:

- Video mode with external input from 24-bit RGB parallel port
- Structured light mode
  - External video input from 24-bit RGB parallel port
  - Internal video from preloaded patterns with optional FPGA

– Internal video from internally generated patterns

In the following sections, the video sequences that support video input from 24-bit RGB parallel port are classified as external video sequences. The video sequences that support video from preloaded patterns are classified as internal video sequences.

2.3.1.1 External Video Sequence

The external video sequence supports 3-, 6-, 12-, 16-, 18-, or 24-bit RGB images, as well as, 1-, 2-, 3-, 4-, 5-, 6- ,7-, or 8-bit monochrome images at up to 60 Hz frame rate. These external video sequences take data streamed through the 24-bit RGB parallel bus at a pre-selected frame rate of 15, 30, 40/45, or 60 Hz. The 16-, 18-, and 24-bit external video sequences are typical of projection systems, while the 3-, 6-, and 12-bit RGB and the monochrome video sequences are typically used in structure light applications. Table 2-78 depicts the video sequences and maximum pattern rates.

Table 2-78. External Video Sequences and Pattern Rates

EXTERNAL VIDEO SEQUENCE		NUMBER OF PATTERNS PER FRAME	FRAME RATE	PATTERN RATE
Monochrome	1 bit per pixel	24	15, 30, 40, or 60 Hz	24 × Frame Rate
	2 bits per pixel	12		12 × Frame Rate
	3 bits per pixel	8	15, 30, 45, or 60 Hz	8 × Frame Rate
	4 bits per pixel	6	15, 30, 40, or 60 Hz	6 × Frame Rate
	5 bits per pixel	4	15, 30, 45, or 60 Hz	4 × Frame Rate
	6 bits per pixel	4		4 × Frame Rate
	7 bits per pixel	3	15, 30, 40, or 60 Hz	3 × Frame Rate
	8 bits per pixel	2	15, 30, 45, or 60 Hz	2 × Frame Rate
RGB	1-bit per color pixel (3-bit per pixel)	8		4 × Frame Rate
	2-bit per color pixel (6-bit per pixel)	4		3 × Frame Rate
	4-bit per color pixel (12-bit per pixel)	2		2 × Frame Rate
	5/6/5-bit RGB pixel (16-bit per pixel)	1		Frame Rate
	6-bit per color pixel (18-bit per pixel)			
	8-bit per color pixel (24-bit per pixel)			

2.3.1.1.1 16-, 18-, and 24-bit External Video Sequence

The 16-, 18-, and 24-bit external video sequence takes as input 16-, 18-, or 24-bit red, green, and blue (RGB) data at up to 60 Hz frame rate in resolutions ranging from QVGA to WVGA (Table 2-24). To improve image quality, the DLPC300 offers several image-enhancement functions: AGC, CCA, and Spatial-Temporal Multiplexing (Dithering).

To change into video mode, follow the procedure shown in Table 2-79

Table 2-79. Steps to Configure DLPC300 for Video Mode with External Input from 24-bit RGB Parallel Port

Step	Description		I²C Address	Value
1	Turn off the LEDs by disabling the red, green, and blue LED enables:	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000000
		If using RED_EN pin	0x4B	0x00151624
		If using GREEN_EN and BLUE_EN pin	0x4C	0x25110000
2	Disable the sequencer by clearing the sequencer enable bit		0x82	0x00000000
3	Enable video processing functions:	Enable Auto Gain Control Function	0x50	0x00000007
		Enable Temporal Dither Control	0x7E	0x00000000
		Enable Color Coordinate Adjustment	0x5E	0x00000001
4	Make input source attribute changes, as needed	Set Input Source Selection	0x0B	appropriate value from Section 2.2.3.1
		Set Input Resolution	0x0C	appropriate value from Section 2.2.3.2
		Set Input Pixel Data Format	0x0D	appropriate value from Section 2.2.3.3
5	Lock sequence to input sync VSYNC		0x1E	0x00000001
6	Set up the sequence vector		0x83	appropriate value [(Sub-Vector) << 8 | (Start Vector)] from Table 2-80
7	Load new sequence from SPI flash by sending the following I²C compound commands:	Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
		Write the Data Register with the compound command to load a new sequence number	0x39	appropriate sequence number from Table 2-80
		Set busy status in Handshake Register	0x3A	0x00000001
		Write the Command Register with the compound command to load a new sequence number	0x38	0x000000C1
		Poll the Handshake Register and wait until processor is not busy	0x3A	is = 000?
8	Enable the sequencer by setting the sequencer enable bit		0x82	0x00000001
9	Turn on the LEDs by enabling the red, green, and blue LED enables	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000003
		If using RED_EN pin	0x4B	0x14151624
		If using BLUE_EN and GREEN_EN pin	0x4C	0x25111213

Table 2-80 shows the 24-bit RBG video sequences for 60 and 50 Hz frame rates. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus, as shown in Figure 2-9.

Table 2-80. DLPC300 16-, 18-, and 24-bit RGB External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
16-, 18-, and 24-bit RGB (8-bit per color) video sequence with 40% red, 45% green, and 15% blue	50	0	0	1
16-, 18-, and 24-bit RGB (8-bit per color) video sequence with 35% red, 45% green, and 20% blue		1	0	1
16-, 18-, and 24-bit RGB (8-bit per color) video sequence with 40% red, 45% green, and 15% blue	60	2	0	1
16-, 18-, and 24-bit RGB (8-bit per color) video sequence with 35% red, 45% green, and 20% blue		3	0	1

2.3.1.1.2 Pixel Accurate External Video Sequences

In structure light applications, pixel accuracy is highly desired. For accurate pixel to DMD-pixel mapping, set the resolution to 608×684 and bypass the video processing functions with the procedure shown in Table 2-81

Table 2-81. Steps to Configure DLPC300 for Pixel Accurate Video Mode with External Input from 24-bit RGB Parallel Port

Step	Description		I^2C address	Value
1	Turn off the LEDs by disabling the red, green, and blue LED enables:	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000000
		If using RED_EN pin	0x4B	0x00151624
		If using GREEN_EN and BLUE_EN pin	0x4C	0x25110000
2	Disable the sequencer by clearing the sequencer enable bit		0x82	0x00000000
3	Disable video processing functions:	Disable Auto Gain Control Function	0x50	0x00000006
		Disable Temporal Dither Control	0x7E	0x00000002
		Disable Color Coordinate Adjustment	0x5E	0x00000000
4	Make input source attributes changes, as needed	Set Input Source Selection	0x0B	appropriate value from Section 2.2.3.1
		Set Input Resolution	0x0C	0x00000023
		Set Input Pixel Data Format	0x0D	appropriate value from Section 2.2.3.3
5	Lock sequence to input sync VSYNC		0x1E	0x00000001
6	Set up the sequence vector		0x83	appropriate value [(Sub-Vector) << 8 | (Start Vector)] from Table 2-82 through Table 2-103

Table 2-81. Steps to Configure DLPC300 for Pixel Accurate Video Mode with External Input from 24-bit RGB Parallel Port (continued)

Step	Description		I^2C address	Value
7	Load new sequence from SPI flash by sending the following I^2C compound commands:	Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
		Write the Data Register with the compound command to load a new sequence number	0x39	appropriate sequence number from Table 2-80
		Set busy status in Handshake Register	0x3A	0x00000001
		Write the Command Register with the compound command to load a new sequence number	0x38	0x000000C1
		Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
8	Enable the sequencer by setting the sequencer enable bit		0x82	0x00000001
9	Turn on the LEDs by enabling the red, green, and blue LED enables	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000003
		If using RED_EN pin	0x4B	0x14151624
		If using BLUE_EN and GREEN_EN pin	0x4C	0x25111213

2.3.1.1.2.1 12-bit RGB External Video Sequences

Table 2-82 shows the 12-bit RGB external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of two images in one frame to produce two images per frame rate. The DMD display with respect to the output trigger is shown in Figure 2-10. Each image is composed of 4-bits per color with a corresponding trigger input or output. In this figure, R0 corresponds to the bit 0 plane of the red portion of the image, G0 corresponds to the bit 0 plane of the green portion of the image, and B0 corresponds to the bit 0 plane of the blue portion of the image. R1 corresponds to the bit-plane of the first bit of the red portion of the image, G1 corresponds to the bit-plane of the first bit of the green portion of the image, and B0 corresponds to the bit-plane of the first bit of the blue portion of the image. R2 corresponds to the bit-plane of the second bit of the red portion of the image, G2 corresponds to the bit-plane of the second bit of the green portion of the image, and B2 corresponds to the bit-plane of the second bit of the blue portion of the image, and so forth.

Table 2-82. DLPC300 12-bit RGB External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
12-bit RGB (4-bit per color) video sequence	60	13	30	1
	45		42	1
	30		43	1
	15		44	1

Table 2-83. DLPC300 12-bit RGB External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
12-bit RGB (4-bit per color) video sequence	60	13	30	1
	45		42	1
	30		43	1
	15		44	1

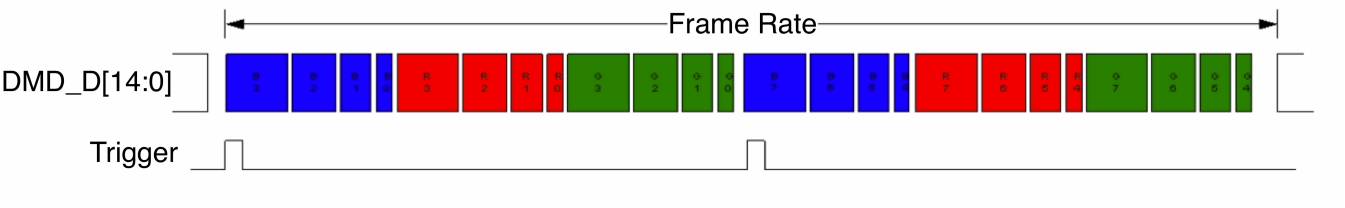


Figure 2-10. 12-bit RGB External Video

To provide more than one image per frame rate, Table 2-84 describes the mapping between the DLPC300 pin and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is two images behind the currently loaded image.

Table 2-84. DLPC300 24-bit RGB Input Pin to 12-bit RGB Image Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Red [3:0]	1	Red [3:0]
Green [3:0]		Green [3:0]
Blue [3:0]		Blue [3:0]
Red [7:4]	2	Red [3:0]
Green [7:4]		Green [3:0]
Blue [7:4]		Blue [3:0]

2.3.1.1.2.2 6-bit RGB External Video Sequences

Figure 2-11 shows the 6-bit RGB external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of four images in one frame to produce a frame rate of four images per frame. The DMD display with respect to the output trigger is shown in Table 2-85. Each image is composed of 2-bits per color with a corresponding trigger input or output.

Table 2-85. DLPC300 6-bit RGB External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
6-bit RGB (2-bit per color) video sequence	60	13	15	1
	45		27	1
	30		28	1
	15		29	1

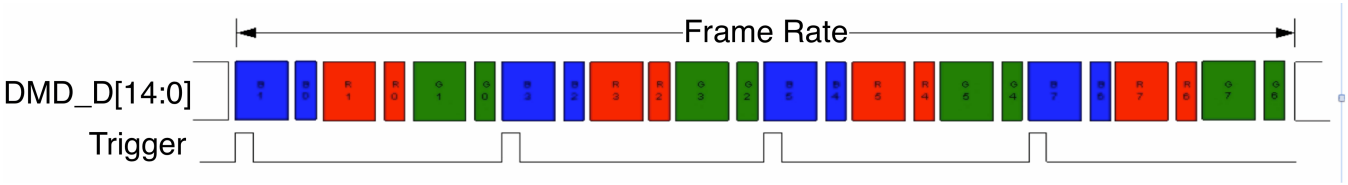


Figure 2-11. 6-bit RGB External Video

To provide more than one image per frame rate, Table 2-86 describes the mapping between the DLPC300 pin and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is four images behind the currently loaded image.

Table 2-86. DLPC300 24-bit RGB Input Pin to 6-bit RGB Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Red [1:0]	1	Red [1:0]
Green [1:0]		Green [1:0]
Blue [1:0]		Blue [1:0]
Red [3:2]	2	Red [1:0]
Green [3:2]		Green [1:0]
Blue [3:2]		Blue [1:0]
Red [5:4]	3	Red [1:0]
Green [5:4]		Green [1:0]
Blue [5:4]		Blue [1:0]
Red [7:6]	4	Red [1:0]
Green [7:6]		Green [1:0]
Blue [7:6]		Blue [1:0]

2.3.1.1.2.3 3-bit RGB External Video

Table 2-87 shows the 3-bit RGB external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of eight images in one frame to produce a frame rate of eight images per frame. The DMD display with respect to the output trigger is shown in Figure 2-12. Each image is composed of 1-bit per color with a corresponding trigger input or output.

Table 2-87. DLPC300 3-bit RGB External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
3-bit RGB (1-bit per color) video sequence	60	13	0	1
	45		12	1
	30		13	1
	15		14	1

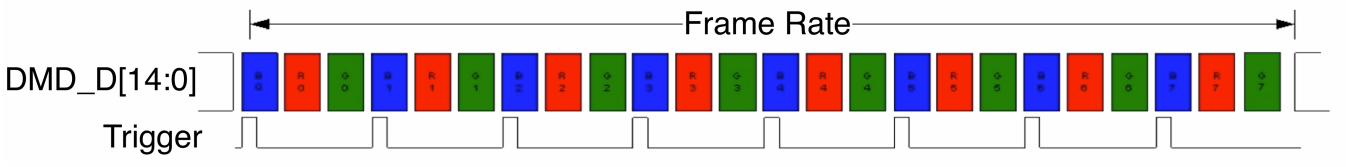


Figure 2-12. 3-bit RGB External Video

To provide more than one image per frame rate, Table 2-88 describes the mapping between the DLPC300 pin and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is eight images behind the currently loaded image.

Table 2-88. DLPC300 24-bit RGB Input Pin to 3-bit RGB Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Red [0]	1	Red [0]
Green [0]		Green [0]
Blue [0]		Blue [0]
Red [1]	2	Red [0]
Green [1]		Green [0]
Blue [1]		Blue [0]
Red [2]	3	Red [0]
Green [2]		Green [0]
Blue [2]		Blue [0]
Red [3]	4	Red [0]
Green [3]		Green [0]
Blue [3]		Blue [0]
Red [4]	5	Red [0]
Green [4]		Green [0]
Blue [4]		Blue [0]
Red [5]	6	Red [0]
Green [5]		Green [0]
Blue [5]		Blue [0]
Red [6]	7	Red [0]
Green [6]		Green [0]
Blue [6]		Blue [0]
Red [7]	8	Red [0]
Green [7]		Green [0]
Blue [7]		Blue [0]

2.3.1.1.2.4 8-bit Monochrome External Video

Table 2-89 shows the 8-bit monochrome external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of two images in one frame to produce images at twice the frame rate.

Table 2-89. DLPC300 8-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
8-bit monochrome video sequence	60	16	15	1
	45		27	1
	30		28	1
	15		29	1

The DMD display with respect to the output trigger is shown in Figure 2-13. Each image is composed of an 8-bit monochrome with a corresponding trigger input or output.

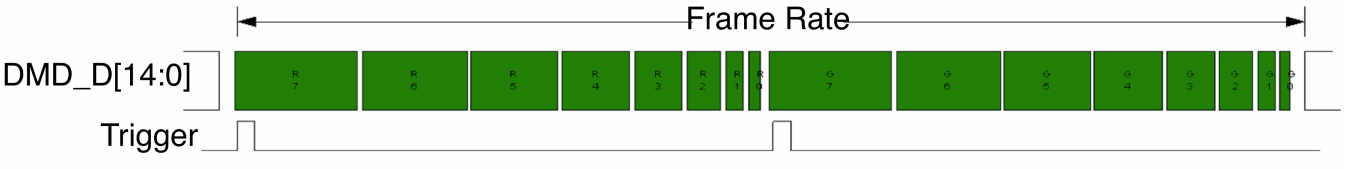


Figure 2-13. 8-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-90 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is two images behind the currently loaded image.

Table 2-90. DLPC300 24-bit RGB Input Pin to 8-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Red [7:0]	1	Monochrome [7:0]
Green [7:0]	2	Monochrome [7:0]
Blue [7:0]		Not used

2.3.1.1.2.5 7-bit Monochrome External Video

Table 2-91 shows the 7-bit monochrome external video sequences for 15, 30, 40, and 60 Hz frame rates. These sequences support the input of three images in one frame to produce images at three times the frame rate.

Table 2-91. DLPC300 7-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
7-bit monochrome video sequence	60	16	0	1
	40		12	1
	30		13	1
	15		14	1

The DMD display with respect to the output trigger is shown in Figure 2-14. Each image is composed of a 7-bit monochrome with a corresponding trigger input or output.

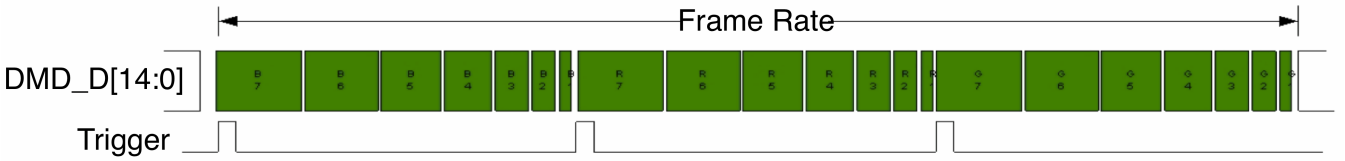


Figure 2-14. 7-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-92 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that pins Blue [0], Red [0], and Green [0] of the DLPC300 24-bit RGB parallel bus are not used. Furthermore, the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is three images behind the currently loaded image.

Table 2-92. DLPC300 24-bit RGB Input Pin to 7-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [7:1]	1	Monochrome [6:0]
Red [7:1]	2	Monochrome [6:0]
Green [7:1]	3	Monochrome [6:0]

2.3.1.1.2.6 6-bit Monochrome External Video

Table 2-93 shows the 6-bit monochrome external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of four images in one frame to produce images at four times the frame rate.

Table 2-93. DLPC300 6-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
6-bit monochrome video sequence	60	15	15	1
	40		27	1
	30		28	1
	15		29	1

The DMD display with respect to the output trigger is shown in Figure 2-15. Each image is composed of a 6-bit monochrome with a corresponding trigger input or output.

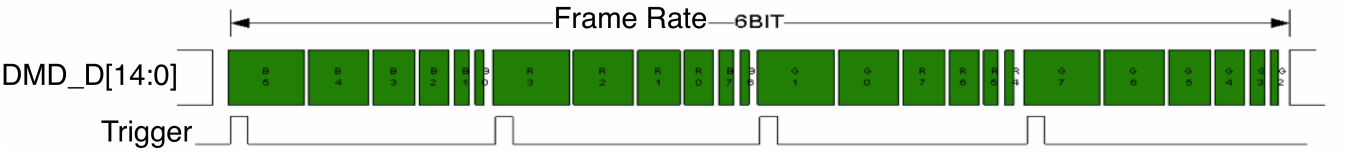


Figure 2-15. 6-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-94 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is four images behind the currently loaded image.

Table 2-94. DLPC300 24-bit RGB Input Pin to 6-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [5:0]	1	Monochrome [5:0]
Red [3:0], Blue [7:6]	2	Monochrome [5:0]
Green [1:0], Red [7:4]	3	Monochrome [5:0]
Green [7:2]	4	Monochrome [5:0]

2.3.1.1.2.7 5-bit Monochrome External Video

Table 2-95 shows the 5-bit monochrome external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of four images in one frame to produce images at four times the frame rate.

Table 2-95. DLPC300 5-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
5-bit monochrome video sequence	60	15	0	1
	45		12	1
	30		13	1
	15		14	1

The DMD display with respect to the output trigger is shown in Figure 2-16. Each image is composed of a 5-bit monochrome with a corresponding trigger input or output.

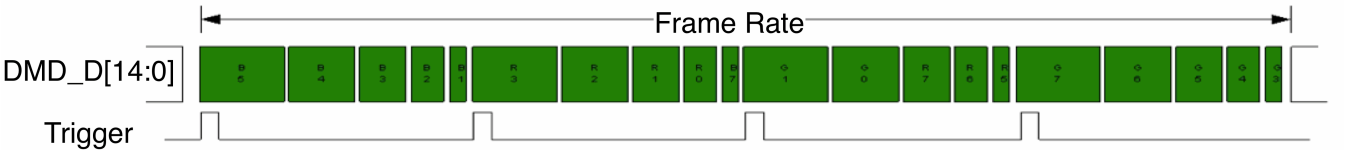


Figure 2-16. 5-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-96 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that pins Blue [6], Blue [0], Red [4], and Green [2] of the DLPC300 24-bit RGB parallel bus are not used. Furthermore, the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is four images behind the currently loaded image.

Table 2-96. DLPC300 24-bit RGB Input Pin to 5-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [5:1]	1	Monochrome [4:0]
Red [3:0], Blue [7]	2	Monochrome [4:0]
Green [1:0], Red [7:5]	3	Monochrome [4:0]
Green [7:3]	4	Monochrome [4:0]

2.3.1.1.2.8 4-bit Monochrome External Video

Table 2-97 shows the 4-bit monochrome external video sequences for 15, 30, 40, and 60 Hz frame rates. These sequences support the input of six images in one frame to produce images at six times the frame rate.

Table 2-97. DLPC300 4-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
4-bit monochrome video sequence	60	14	45	1
	40		57	1
	30		58	1
	15		59	1

The DMD display with respect to the output trigger is shown in Figure 2-18. Each image is composed of a 4-bit monochrome with a corresponding trigger input or output.

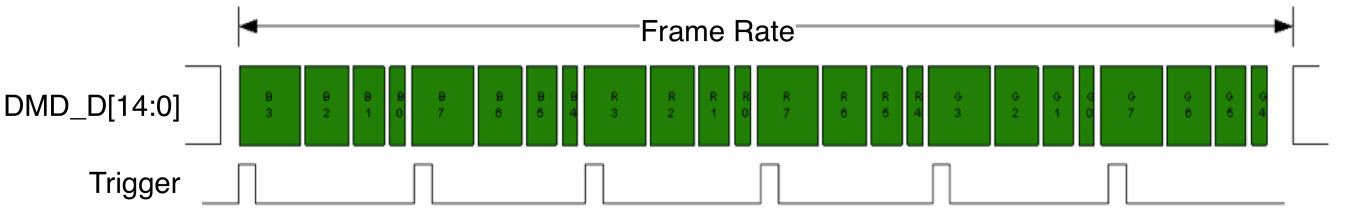


Figure 2-17. 4-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-98 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is six images behind the currently loaded image.

Table 2-98. DLPC300 24-bit RGB Input Pin to 4-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [3:0]	1	Monochrome [3:0]
Blue [7:4]	2	Monochrome [3:0]
Red [3:0]	3	Monochrome [3:0]
Red [7:4]	4	Monochrome [3:0]
Green [3:0]	5	Monochrome [3:0]
Green [7:4]	6	Monochrome [3:0]

2.3.1.1.2.9 3-bit Monochrome External Video

Table 2-99 shows the 3-bit monochrome external video sequences for 15, 30, 45, and 60 Hz frame rates. These sequences support the input of eight images in one frame to produce images at eight times the frame rate.

Table 2-99. DLPC300 3-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
3-bit monochrome video sequence	60	14	30	1
	45		42	1
	30		43	1
	15		44	1

The DMD display with respect to the output trigger is shown in Figure 2-18. Each image is composed of a 3-bit monochrome with a corresponding trigger input or output.

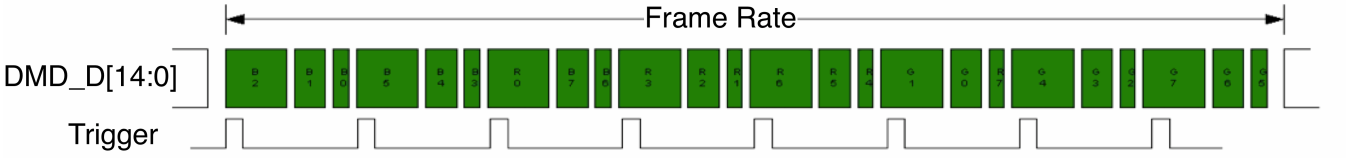


Figure 2-18. 3-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-100 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is eight images behind the currently loaded image.

Table 2-100. DLPC300 24-bit RGB Input Pin to 3-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [2:0]	1	Monochrome [2:0]
Blue [5:3]	2	Monochrome [2:0]
Red [0], Blue [7:6]	3	Monochrome [2:0]
Red [3:1]	4	Monochrome [2:0]
Red [6:4]	5	Monochrome [2:0]
Green [1:0], Red [7]	6	Monochrome [2:0]
Green [4:2]	7	Monochrome [2:0]
Green [7:5]	8	Monochrome [2:0]

2.3.1.1.2.10 2-bit Monochrome External Video

Table 2-101 shows the 2-bit monochrome external video sequences for 15, 30, 40, and 60 Hz frame rates. These sequences support the input of 12 images in one frame to produce images at 12 times the frame rate.

Table 2-101. DLPC300 2-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
2-bit monochrome video sequence	60	14	15	1
	40		27	1
	30		28	1
	15		29	1

The DMD display with respect to the output trigger is shown in Figure 2-19. Each image is composed of a 2-bit monochrome with a corresponding trigger input or output.

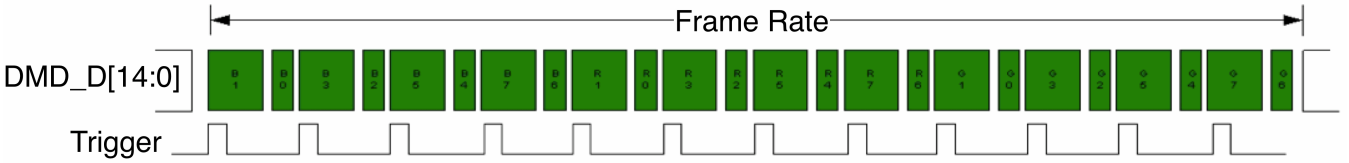


Figure 2-19. 2-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-102 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Therefore, the displayed image is 12 images behind the currently loaded image.

Table 2-102. DLPC300 24-bit RGB Input Pin to 2-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [1:0]	1	Monochrome [1:0]
Blue [3:2]	2	Monochrome [1:0]
Blue [5:4]	3	Monochrome [1:0]
Blue [7:6]	4	Monochrome [1:0]
Red [1:0]	5	Monochrome [1:0]
Red [3:2]	6	Monochrome [1:0]
Red [5:4]	7	Monochrome [1:0]
Red [7:6]	8	Monochrome [1:0]
Green [1:0]	9	Monochrome [1:0]
Green [3:2]	10	Monochrome [1:0]
Green [5:4]	11	Monochrome [1:0]
Green [7:6]	12	Monochrome [1:0]

2.3.1.1.2.11 1-bit Monochrome External Video

Table 2-103 shows the 1-bit monochrome external video sequences for 15, 30, 40, and 60 Hz frame rates. These sequences support the input of 24 images in one frame to produce images at 24 times the frame rate.

Table 2-103. DLPC300 1-bit Monochrome External Video Sequences

Description	Frame Rate (Hz)	Sequence Number	Start Vector	Sub-Vector
1-bit monochrome video sequence	60	14	0	1
	40		12	1
	30		13	1
	15		14	1

The DMD display with respect to the output trigger is shown in Figure 2-20. Each image is composed of a 3-bit monochrome with a corresponding trigger input or output.

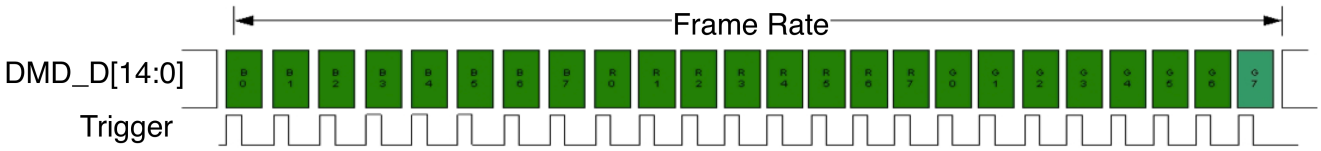


Figure 2-20. 1-bit Monochrome External Video

To provide more than one image per frame rate, Table 2-104 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that the displayed image is a frame delayed in relation to the data streamed through the 24-bit RGB parallel bus. Thus, the displayed image is 24 images behind the currently loaded image.

Table 2-104. DLPC300 24-bit RGB Input Pin to 1-bit Monochrome Image Bit Mapping

DLPC300 RGB Input Pins	Image Number	Image Bit Mapping
Blue [0]	1	Monochrome [0]
Blue [1]	2	Monochrome [0]
Blue [2]	3	Monochrome [0]
Blue [3]	4	Monochrome [0]
Blue [4]	5	Monochrome [0]
Blue [5]	6	Monochrome [0]
Blue [6]	7	Monochrome [0]
Blue [7]	8	Monochrome [0]
Red [0]	9	Monochrome [0]
Red [1]	10	Monochrome [0]
Red [2]	11	Monochrome [0]
Red [3]	12	Monochrome [0]
Red [4]	13	Monochrome [0]
Red [5]	14	Monochrome [0]
Red [6]	15	Monochrome [0]
Red [7]	16	Monochrome [0]
Green [0]	17	Monochrome [0]
Green [1]	18	Monochrome [0]
Green [2]	19	Monochrome [0]
Green [3]	20	Monochrome [0]
Green [4]	21	Monochrome [0]
Green [5]	22	Monochrome [0]
Green [6]	23	Monochrome [0]
Green [7]	24	Monochrome [0]

2.3.1.2 Internal Video Sequence with Optional FPGA

The internal video sequence supports 1-, 2-, 3-, 4-, 5-, 6- ,7, or 8-bit monochrome images. This mode utilizes custom display sequences with an optional FPGA to display monochrome patterns at higher speeds than the external video sequence. The DLPC300 in conjunction with an optional FPGA achieve higher speeds by preloading the images into the DLPC300 mDDR. Once the images are preloaded, the DLPC300 loads the images into the DMD while the FPGA rotates the display buffer on every 24th bit-plane.

With the optional FPGA, the maximum pattern frame rate can be calculated with the following equation for all modes, except for the 1-bit internal video sequence:

$$Pattern\ Rate = \begin{cases} \dfrac{1}{\left(\begin{matrix}Pattern\\ Exposure\ Period\end{matrix}\right)+\left(\begin{matrix}Bit\ Plane\\ Load\ Time\end{matrix}\right)} & ;if\left[\left(\begin{matrix}\text{Number of}\\ \text{Images}\end{matrix}\right)\times\left(\begin{matrix}\text{Bit}\\ \text{Depth}\end{matrix}\right)\right]\le 24 \\ \dfrac{1}{\left(\begin{matrix}Pattern\\ Exposure\ Period\end{matrix}\right)+\left(\begin{matrix}Bit\ Plane\\ Load\ Time\end{matrix}\right)+\left(\begin{matrix}Buffer\ Rotate\\ Overhead\end{matrix}\right)} & ;if\left[\left(\begin{matrix}\text{Number of}\\ \text{Images}\end{matrix}\right)\times\left(\begin{matrix}\text{Bit}\\ \text{Depth}\end{matrix}\right)\right]> 24 \end{cases} \quad (1)$$

where:

typical DMD first bit-plane load time = 215 µs

typical buffer rotate overhead = 135 µs

refer to Table 2-107 through Table 2-114 for supported exposure times.

Table 2-105 shows the maximum pattern rate that can be achieved by using a single FPGA internal buffer in continuous mode. In 1-bit internal video sequence mode, the DMD load is pipelined with the exposure time for the fastest rate possible.

Table 2-105. Internal Video Sequence and Maximum Pattern Rates with Optional FPGA

COLOR MODE		MAXIMUM NUMBER OF PATTERNS	MAXIMUM PATTERN RATE
Monochrome	1 bit per pixel	96	4000 Hz
	2 bits per pixel	48	1100 Hz
	3 bits per pixel	32	590 Hz
	4 bits per pixel	24	550 Hz
	5 bits per pixel	16	450 Hz
	6 bits per pixel	16	365 Hz
	7 bits per pixel	12	210 Hz
	8 bits per pixel	12	115 Hz

The mDDR accommodates four 608×684 24-bit RGB images or 96 bit-plane (24 bit-planes/image × 4 images). These internal video sequences are typically used in structure light applications where pixel accuracy is desired. For accurate pixel-to-DMD-pixel mapping, set the resolution to 608×684, bypass the video processing functions, and preload the images with the procedure shown in Table 2-106.

Table 2-106. Steps to Configure DLPC300 for Pixel Accurate Video Mode with Preloaded Images with Optional FPGA

Step	Description		I^2C address	Value
1	Turn off the LEDs by disabling the red, green, and blue LED enables:	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000000
		If using RED_EN pin	0x4B	0x00151624
		If using GREEN_EN and BLUE_EN pin	0x4C	0x25110000
2	Disable the sequencer by clearing the sequencer enable bit		0x82	0x00000000

Table 2-106. Steps to Configure DLPC300 for Pixel Accurate Video Mode with Preloaded Images with Optional FPGA (continued)

Step	Description		I^2C address	Value
3	Disable video processing functions:	Disable Auto Gain Control Function	0x50	0x00000006
		Disable Temporal Dither Control	0x7E	0x00000002
		Disable Color Coordinate Adjustment	0x5E	0x00000000
4	Make input source attributes changes, as needed	Set Input Source Selection	0x0B	appropriate value from Section 2.2.3.1
		Set Input Resolution	0x0C	0x00000023
		Set Input Pixel Data Format	0x0D	appropriate value from Section 2.2.3.3
5	Lock sequence to input sync VSYNC		0x1E	0x00000001
6	Set up the sequence vector		0x83	appropriate value [(Sub-Vector) << 8 | (Start Vector)] from Table 2-107 through Table 2-114
7	Load new sequence from SPI flash by sending the following I^2C compound commands:	Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
		Write the Data Register with the compound command to load a new sequence number	0x39	appropriate sequence number from Table 2-80
		Set busy status in Handshake Register	0x3A	0x00000001
		Write the Command Register with the compound command to load a new sequence number	0x38	0x000000C1
		Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
8	preload the images to the display buffer by filling one buffer at a time	Freeze the display buffer swap.	0xA3	0x00000001
		Load a single display buffer by sending data through the DLPC300 24-bit RGB parallel bus.		
		Enable the display buffer swap to rotate the buffer.	0xA3	0x000000
		If more than 24 bit-planes are needed, rotate the buffer by generating a VSYNC with two horizontal blank lines.		
		Repeat this process until the necessary buffers are filled. Note that each buffer can only accommodate 24 bit-planes. A total of 96 bit-planes can be preloaded.		
8	Enable the sequencer by setting the sequencer enable bit		0x82	0x00000003

Table 2-106. Steps to Configure DLPC300 for Pixel Accurate Video Mode with Preloaded Images with Optional FPGA (continued)

Step	Description		I^2C address	Value
9	Turn on the LEDs by enabling the red, green, and blue LED enables	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000003
		If using RED_EN pin	0x4B	0x14151624
		If using BLUE_EN and GREEN_EN pin	0x4C	0x25111213

2.3.1.2.1 8-bit Internal Video Sequence with Optional FPGA

Table 2-107 shows the 8-bit monochrome internal video sequence for exposure times ranging from 8.33 µs to 20 ms, at 500 µs increment. These sequences display up to 12 preloaded images once or continuously cycling through all the images.

Table 2-107. DLPC300 8-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 8-bit internal pattern sequence	8333	30	0	4
	9000		4	4
	9500		8	4
	10000		12	4
	10500		16	4
	11000		20	4
	11500		24	4
	12000		28	4
	12500		32	4
	13000		36	4
	13500		40	4
	14000		44	4
	14500	31	0	4
	15000		4	4
	15500		8	4
	16000		12	4
	16500		16	4
	17000		20	4
	17500		24	4
	18000		28	4
	18500		32	4
	19000		36	4
	19500		40	4
	20000		44	4

To load the images, Table 2-90 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents.

2.3.1.2.2 7-bit Internal Video Sequence with Optional FPGA

Table 2-108 shows the 7-bit monochrome internal video sequence for exposure times ranging from 4.5 µs to 20 ms, at 500 µs increment. These sequences display up to 12 preloaded images once or continuously cycling through all preloaded images.

Table 2-108. DLPC300 7-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 7-bit internal pattern sequence	4500	28	0	4
	5000		4	4
	5500		8	4
	6000		12	4
	6500		16	4
	7000		20	4
	7500		24	4
	8000		28	4
	8500		32	4
	9000		36	4
	9500		40	4
	10000		44	4
	10500		48	4
	11000		52	4
	11500		56	4
	12000		60	4
	12500		64	4
	13000	29	0	4
	13500		4	4
	14000		8	4
	14500		12	4
	15000		16	4
	15500		20	4
	16000		24	4
	16500		28	4
	17000		32	4
	17500		36	4
	18000		40	4
	18500		44	4
	19000		48	4
	19500		52	4
	20000		56	4

To load the images, Table 2-92 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that pins Blue [0], Red [0], and Green [0] of the 24-bit RGB parallel bus are not used.

2.3.1.2.3 6-bit Internal Video Sequence with Optional FPGA

Table 2-109 shows the 6-bit monochrome internal video sequence for exposure times ranging from 2.5 µs to 20 ms, at 500 µs increment. These sequences display up to 16 preloaded images once or continuously cycling through all preloaded images.

Table 2-109. DLPC300 6-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 6-bit internal pattern sequence	2500	26	0	5
	3000		5	5
	3500		10	5
	4000		15	5
	4500		20	5
	5000		25	5
	5500		30	5
	6000		35	5
	6500		40	5
	7000		45	5
	7500		50	5
	8000		55	5
	8500		60	5
	9000		65	5
	9500		70	5
	10000		75	5
	10500		80	5
	11000	27	0	5
	11500		5	5
	12000		10	5
	12500		15	5
	13000		20	5
	13500		25	5
	14000		30	5
	14500		35	5
	15000		40	5
	15500		45	5
	16000		50	5
	16500		55	5
	17000		60	5
	17500		65	5
	18000		70	5
	18500		75	5
	19000		80	5
	19500		85	5
	20000		90	5

To load the images, Table 2-94 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents.

2.3.1.2.4 5-bit Internal Video Sequence with Optional FPGA

Table 2-110 shows the 6-bit monochrome internal video sequence for exposure times ranging from 2 µs to 20 ms, at 500 µs increment. These sequences display up to 16 preloaded images once or continuously cycling through all preloaded images.

Table 2-110. DLPC300 5-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 5-bit internal pattern sequence	2000	24	0	5
	2500		5	5
	3000		10	5
	3500		15	5
	4000		20	5
	4500		25	5
	5000		30	5
	5500		35	5
	6000		40	5
	6500		45	5
	7000		50	5
	7500		55	5
	8000		60	5
	8500		65	5
	9000		70	5
	9500		75	5
	10000		80	5
	10500		85	5
	11000	25	0	5
	11500		5	5
	12000		10	5
	12500		15	5
	13000		20	5
	13500		25	5
	14000		30	5
	14500		35	5
	15000		40	5
	15500		45	5
	16000		50	5
	16500		55	5
	17000		60	5
	17500		65	5
	18000		70	5
	18500		75	5
	19000		80	5
	19500		85	5
	20000		90	5

To load the images, Table 2-96 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents. Note that pins Blue [6], Blue [0], Red [4], and Green [2] of the DLPC300 24-bit RGB parallel bus are not used.

2.3.1.2.5 4-bit Internal Video Sequence with Optional FPGA

Table 2-111 shows the 4-bit monochrome internal video sequence for exposure times ranging from 1.6 µs to 20 ms, at 500 µs increment. These sequences display up to 24 preloaded images once or continuously cycling through all preloaded images.

Table 2-111. DLPC300 4-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 4-bit internal pattern sequence	1600	22	0	7
	2000		7	7
	2500		14	7
	3000		21	7
	3500		28	7
	4000		35	7
	4500		42	7
	5000		49	7
	5500		56	7
	6000		63	7
	6500		70	7
	7000		77	7
	7500		84	7
	8000		91	7
	8500		98	7
	9000		105	7
	9500		112	7
	10000		119	7
	10500		126	7
	11000	23	0	7
	11500		7	7
	12000		14	7
	12500		21	7
	13000		28	7
	13500		35	7
	14000		42	7
	14500		49	7
	15000		56	7
	15500		63	7
	16000		70	7
	16500		77	7
	17000		84	7
	17500		91	7
	18000		98	7
	18500		105	7
	19000		112	7
	19500		119	7
	20000		126	7

To load the images, Table 2-98 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents.

2.3.1.2.6 3-bit Internal Video Sequence with Optional FPGA

Table 2-112 shows the 3-bit monochrome internal video sequence for exposure times ranging from 1.47 µs to 20 ms, at 500 µs increment. These sequences display up to 32 preloaded images once or continuously cycling through all preloaded images.

Table 2-112. DLPC300 3-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 3-bit internal pattern sequence	1470	20	0	9
	2000		9	9
	2500		18	9
	3000		27	9
	3500		36	9
	4000		45	9
	4500		54	9
	5000		63	9
	5500		72	9
	6000		81	9
	6500		90	9
	7000		99	9
	7500		108	9
	8000		117	9
	8500		126	9
	9000		135	9
	9500		144	9
	10000		153	9
	10500		162	9
	11000		171	9
	11500		180	9
	12000		189	9
	12500	21	0	9
	13000		9	9
	13500		18	9
	14000		27	9
	14500		36	9
	15000		45	9
	15500		54	9
	16000		63	9
	16500		72	9
	17000		81	9
	17500		90	9
	18000		99	9
	18500		108	9
	19000		117	9
	19500		126	9
	20000		135	9

To load the images, Table 2-100 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents.

2.3.1.2.7 2-bit Internal Video Sequence with Optional FPGA

Table 2-113 shows the 2-bit monochrome internal video sequence for exposure times ranging from 0.666 µs to 20 ms, at 500 µs increment. These sequences display up to 48 preloaded images once or continuously cycling through all preloaded images.

Table 2-113. DLPC300 2-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time (µs)	Sequence Number	Start Vector	Sub-Vector
Monochrome 2-bit internal pattern sequence	666	18	0	13
	1000		13	13
	1500		26	13
	2000		39	13
	2500		52	13
	3000		65	13
	3500		78	13
	4000		91	13
	4500		104	13
	5000		117	13
	5500		143	13
	6000		143	13
	6500		156	13
	7000		169	13
	7500		182	13
	8000		195	13
	8500		208	13
	9000		221	13
	9500		234	13
	10000	19	0	13
	10500		13	13
	11000		26	13
	11500		39	13
	12000		52	13
	12500		65	13
	13000		78	13
	13500		91	13
	14000		104	13
	14500		117	13
	15000		130	13
	15500		143	13
	16000		156	13
	16500		169	13
	17000		182	13
	17500		195	13
	18000		208	13
	19000		221	13
	20000		234	13

To load the images, Table 2-102 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents.

2.3.1.2.8 1-bit Internal Video Sequence with Optional FPGA

Table 2-114 shows the 1-bit monochrome internal video sequence for exposure times ranging from 0 µs to 20 ms. These sequences display up to 96 preloaded images once or continuously cycling through all preloaded images.

In contrast to the other internal monochrome video sequence modes, the 1-bit internal video sequence exposure time is controlled by the FPGA instead of the display sequence. This allows the pipelining of the DMD load with exposure time for the fastest rate possible. Basically, while the DLPC300 is loading the DMD array, the previous pattern is being exposed.

Table 2-114. DLPC300 1-bit Internal Video Sequence with Optional FPGA

Description	Exposure Time	Sequence Number	Start Vector	Sub-Vector2 0
Monochrome 1-bit internal pattern sequence	250 µs–2 sec	17	0	25
Monochrome 1-bit internal pattern sequence with inversion (one pattern followed by its inverted pattern)			25	49
Monochrome 1-bit internal inverted pattern sequence (displays the inverted pattern of the loaded pattern)			74	33

To load the images, Table 2-104 describes the mapping between the DLPC300 24-bit RGB parallel bus pins and the display sequence expected image contents.

2.3.1.3 Internal Video from Internally Generated Patterns

The internal video sequence from internally generated patterns supports 1-bit monochrome images. Each pattern is a 1-bit (black and white, no gray shades) vertical stripe pattern. The internal pattern generator supports up to a 32 frame deep repeating pattern set. Each pattern has a register setting that allows selection from 15 patterns and an inversion mask setting. The inversion mask indicates if the pattern is inverted, meaning that black regions become white, white becomes black.

To change into video mode, follow the procedure shown in Table 2-115

Table 2-115. Steps to Configure DLPC300 for Internal Video Mode with Internally Generated 1-bit Vertical Patterns

Step	Description		I^2C address	Value
1	Turn off the LEDs by disabling the red, green, and blue LED enables:	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000000
		If using RED_EN pin	0x4B	0x00151624
		If using GREEN_EN and BLUE_EN pin	0x4C	0x25110000
2	Disable the sequencer by clearing the sequencer enable bit		0x82	0x00000000
3	Disable video processing functions:	Disable Auto Gain Control Function	0x50	0x00000006
		Disable Temporal Dither Control	0x7E	0x00000002
		Disable Color Coordinate Adjustment	0x5E	0x00000000
4	Make input source attributes changes, as needed	Set Input Source Selection	0x0B	appropriate value from Section 2.2.3.1
		Set Input Resolution	0x0C	0x00000023
		Set Input Pixel Data Format	0x0D	appropriate value from Section 2.2.3.3
5	Lock sequence to input sync VSYNC		0x1E	0x00000001
6	Set up internally generated patterns	Setup pattern generator	0xD0, 0xD1, 0xD2, 0xD3, 0xD4	appropriate value from
		Enable pattern generator	0xCF	appropriate value from
7	Set up the sequence vector		0x83	appropriate value [(Sub-Vector) << 8 | (0x4B)] from Table 2-107 through Table 2-114

Table 2-115. Steps to Configure DLPC300 for Internal Video Mode with Internally Generated 1-bit Vertical Patterns (continued)

Step	Description		I^2C address	Value
8	Load new sequence from SPI flash by sending the following I^2C compound commands:	Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
		Write the Data Register with the compound command to load a new sequence number	0x39	appropriate sequence number from Table 2-80
		Set busy status in Handshake Register	0x3A	0x00000001
		Write the Command Register with the compound command to load a new sequence number	0x38	0x000000C1
		Poll the Handshake Register and wait until processor is not busy	0x3A	is = 0x00?
8	preload the images to the display buffer by filling one buffer at a time	Freeze the display buffer swap.	0xA3	0x00000001
		Load a single display buffer by sending data through the DLPC300 24-bit RGB parallel bus.		
		Enable the display buffer swap to rotate the buffer.	0xA3	0x000000
		If more than 24 bit-planes are needed, rotate the buffer by generating a VSYNC with two horizontal blank lines.		
		Repeat this process until the necessary buffers are filled. Note that each buffer can only accommodate 24 bit-planes. A total of 96 bit-planes can be preloaded.		
9	Enable the sequencer by setting the sequencer enable bit		0x82	0x00000003
10	Turn on the LEDs by enabling the red, green, and blue LED enables	If using LED_SEL_0 and LED_SEL_1 pin	0x16	0x00000003
		If using RED_EN pin	0x4B	0x14151624
		If using BLUE_EN and GREEN_EN pin	0x4C	0x25111213

Sample Display Options

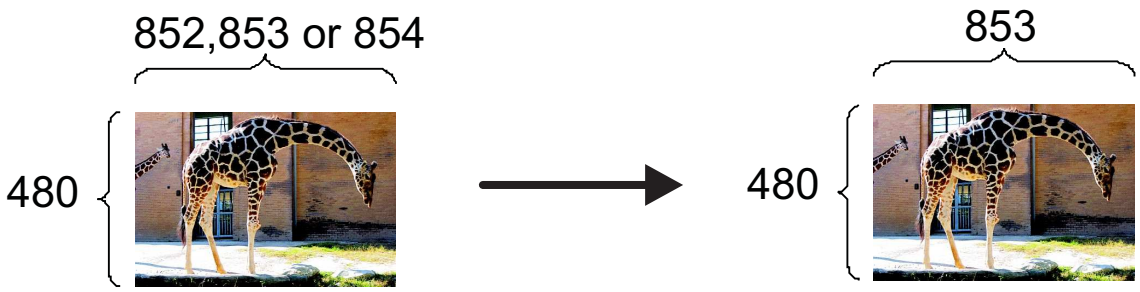
This chapter provides a variety of example of display options for various input image resolutions and orientations.

3.1 Sample Display Options for various Input Image Resolutions and Orientations

The following sections provide a sample of the display options for various input image resolutions and orientations. This includes only a subset of available source options.

3.1.1 Landscape WVGA (852x480, 853x480 or 854x480) source to WVGA (853x480)

Scale Factor: Uniform

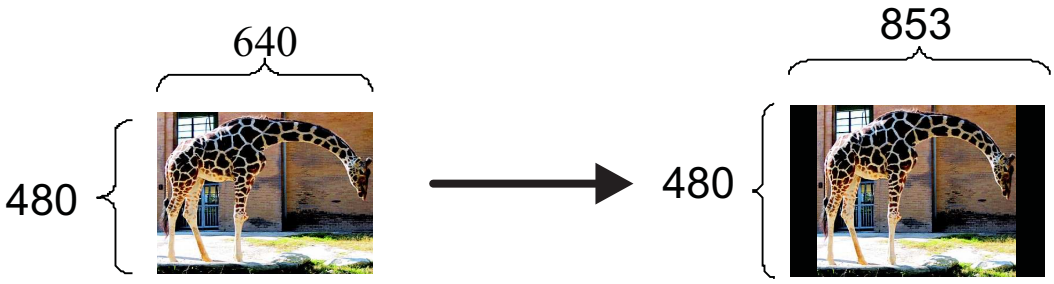


Commands: Image Resolution: WVGA Landscape (Addr x0C=xF,x11,x13)
Image Rotation: No Rotation (Addr x0E=x0)

Note that other WVGA resolutions such as 720x480, 752x480 and 800x480 are uniformly scaled and displayed with vertical black bars similar to a VGA source (as shown in the next paragraph).

3.1.2 Landscape VGA Source to WVGA

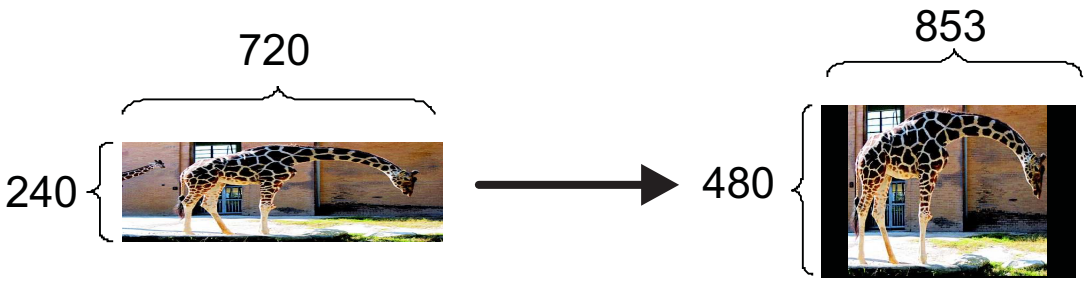
Scale Factor: Uniform



Commands: Image Resolution: VGA Landscape (Addr x0C=x7)
Image Rotation: No Rotation (Addr x0E=x0)

3.1.3 Landscape NTSC Source to WVGA

Scale Factor: Non-Uniform

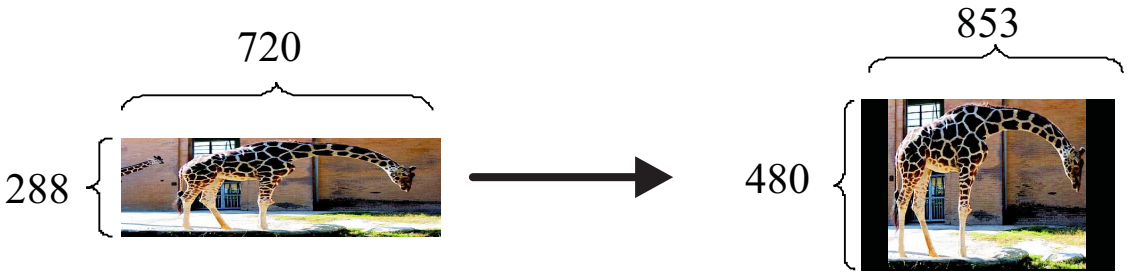


Commands:	**Image Resolution:**	**NTSC Landscape**	**(Addr x0C=x17)**
	Image Rotation:	**No Rotation**	**(Addr x0E=x0)**

The TVP5151 video decoder outputs a 720x240 a image size for each 60 Hz NTSC field. The image is only 240 lines tall because every other line is missing due to interlacing. The DLPC300 scales the field to create a full frame of data to display on the DMD at a 60 Hz frame rate. The scaling operation achieves a low-cost method of de-interlacing.

3.1.4 Landscape PAL/SECAM Source to WVGA

Scale Factor: Non-Uniform



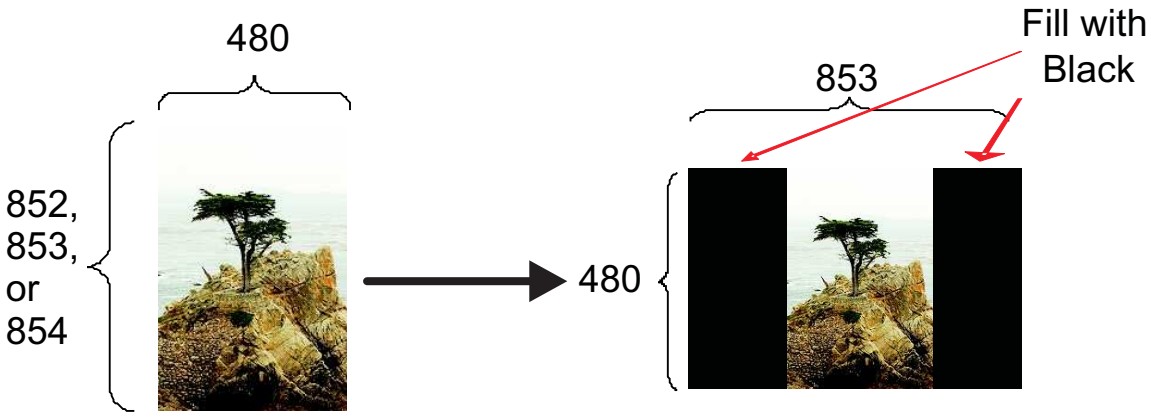
Commands:	**Image Resolution:**	**PAL/SECAM Landscape**	**(Addr x0C=x19)**
	Image Rotation:	**No Rotation**	**(Addr x0E=x0)**

The TVP5151 video decoder outputs a 720x288 image size for each 60 Hz PAL or SECAM field. The image is only 288 lines tall because every other line is missing due to interlacing. The DLPC300 scales the field to create a full frame of data to display on the DMD at a 50Hz frame rate. The scaling operation achieves a low-cost method of de-interlacing.

3.1.5 Portrait WVGA (852x480, 853x480 or 854x480) Source to WVGA (853x480)

For normal image:

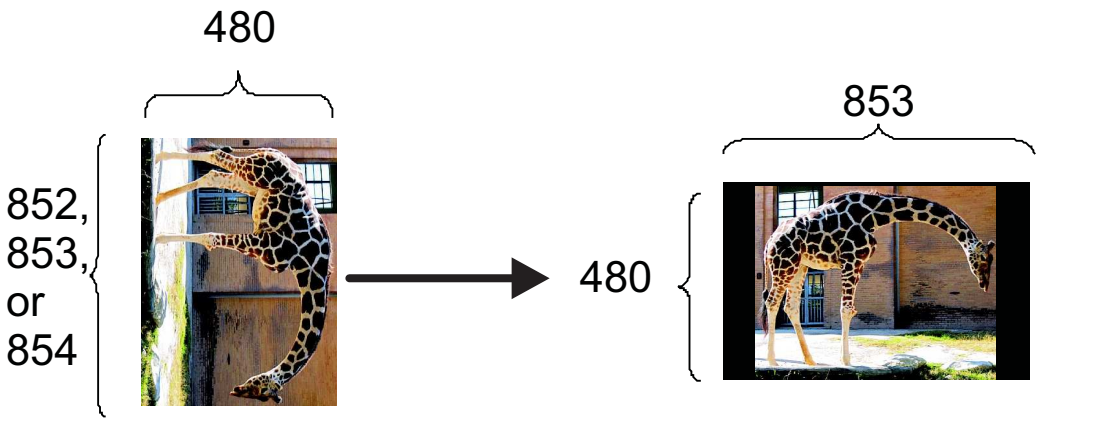
Scale Factor: Uniform



Commands: Image Resolution: WVGA Portrait (Addr x0C=xE,x10,x12)
Image Rotation: No Rotation (Addr x0E=x0)

For rotated image:

Scale Factor: Uniform

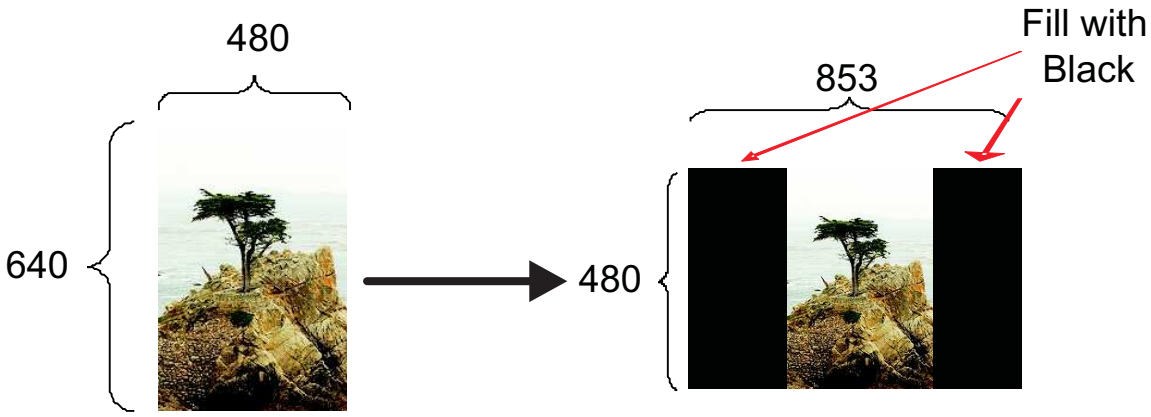


Commands: Image Resolution: WVGA Portrait (Addr x0C=xE,x10,x12)
Image Rotation: Rotation (-90 degrees) (Addr x0E=x1)

3.1.6 Portrait VGA Source to WVGA

For normal image:

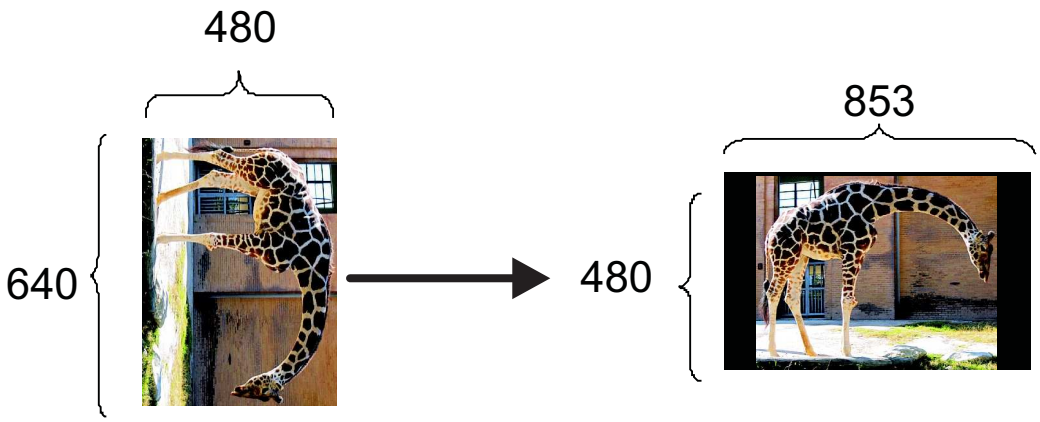
Scale Factor: Uniform



Commands: Image Resolution: VGA Portrait (Addr x0C=x6)
Image Rotation: No Rotation (Addr x0E=x0)

For rotated image:

Scale Factor: Uniform



Commands: Image Resolution: VGA Portrait (Addr x0C=x6)
Image Rotation: Rotation (-90 degrees) (Addr x0E=x1)

Power-Up/Down and Initialization Considerations

This chapter describes the initial power-up and power-down considerations, as well as, other initialization considerations.

4.1 Power Up

The DLPC300 is initialized and ready to process commands 0.1 seconds after the signal $\overline{\text{RESET}}$ is driven high. Detailed power-up timing is given in the DLPC300 Datasheet.

4.2 Power Down

No commands are required at power down of the DLPC300. The DC power supplies must be turned off, and PWRGOOD must be set low, according to the timing in the DLPC300 Datasheet.

4.3 Power-Up Auto-Initialization

Upon release of system reset, the DLPC300 executes an auto-initialization routine that is automatically uploaded from flash. This initialization process consists of setting specific register configurations, uploading specific configuration tables (such as sequence, CMT, etc.), running mDDR Memory BIST, displaying a defined splash screen for a fixed amount of time and then running a configuration batch file to program the DLPC300. The goal of the auto-initialization process is to allow the DLPC300 to fully configure itself for default operation with no external I^2C control.

An *auto-initialization* status flag, INIT_DONE, is held high to indicate that auto initialization is in progress. It is set low when auto-initialization is complete. Subsequently, INIT_DONE is configured as an output interrupt signal that outputs an active high pulse when an error condition exists.

Mode Transition and System Reconfiguration Requirements

This chapter describes the procedures to handle mode transitions and system reconfiguration.

5.1 Mode Transition and System Reconfiguration Requirements

Reconfiguring the system is a process that could result in artifacts or corrupted data being displayed, if not properly handled. Reconfiguration generally includes such operations as source selection changes, operational mode changes, and feature selection changes. In general, if a change could potentially cause some form of undesirable artifact, thus proper transition procedures must be followed to minimize the artifact.

These procedures apply to CPU mode changes (partial buffer to non partial image mode, etc.), source attributes changes (channel, resolution and format), and display attributes changes (rotation and flip). However, the DLPC300 ICP processor manages some transitions internally, such as, the DLP® display sequence changes, sequence synchronization mode (free-run to lock-to-VSYNC or vice versa) changes, and CMT table changes.

In general, to avoid undesirable artifacts either turn off the LEDs (resulting in the display turned off), blank the screen (a.k.a. put up a *curtain*), or freeze the last displayed image. By turning off the LEDs, visible affects resulting from data-path reconfiguration are hidden from the viewer.

The following is the generalized procedure that should be followed for CPU mode changes (partial buffer to non partial image mode etc), LUT changes, source attribute changes (channel, resolution and format) and display attributes changes (rotation and flip). This procedure freezes the image in the formatter buffer. By freezing the formatter buffer before making any changes, the formatter buffer image does not swap during frame boundaries and expose intermediate parameter changes to the viewer.

Step 1. Freeze the formatter display buffer by setting freeze/buffer swap disable bit to 1 (I^2C address 0xA3)

1. The formatter continues to display the last image.
2. In general it is recommended to wait for at least one frame (20 ms) before freezing the formatter to allow the last frame to propagate to the display.
3. If it is desired to display a black screen instead of the last displayed image set the curtain enable bit to 1 (I^2C address 0xA6). Note that this is the recommended operation for a long-side flip.

Step 2. Do the necessary system reconfiguration

1. If needed, load the new CMT tables through I^2C.
2. Make input source attribute changes, as desired:
   - I^2C address 0x0B for Input Source Selection
   - I^2C address 0x0C for input source resolution
   - I^2C address 0x0D for Input Pixel Data Format
3. Make display attributes changes, as desired:
   - I^2C address 0x0E for Image Rotation Control
   - I^2C address 0x0F and 0x10 for Image Flip Control

Step 3. If the last displayed image was a still image then the still image must be re-sent before unfreezing

Step 4. Wait for at least 20 ms (1–50 Hz frame timing) before unfreezing the display buffer to allow a completely new image to propagate to the formatter input buffer.

Step 5. Unfreeze the display buffer by setting the freeze/buffer swap disable bit to 0 (I^2C address 0xA3)

1. The unfreeze operation is synchronized to the vertical sync to avoid tearing.

Register Quick Reference

This appendix provides a quick reference summary of all available registers.

A.1 Register Quick Reference

Table A-1. Register Quick Reference

I²C Address	Description	Type	Reset Value	Default Action
0x00	Interrupt Clear Register	I	n/a	
0x01	Interrupt Set Register	I	n/a	
0x03	Main Status Registers	RO	0x8	
0x0B	Input Source Selection	RW	0x2	Splash
0x0C	Input Resolution Selection	RW	0x1	QVGA Landscape
0x0D	Pixel Data Format Select	RW	0x2	RGB888
0x0E	Image Rotation Control	RW	0x0	No rotate
0x0F	Long-Axis Image Flip Control	RW	0x0	Disabled
0x10	Short-Axis Image Flip Control	RW	0x0	Disabled
0x11	Internal Test Pattern Select	RW	0xD	Checkerboard
0x12	Red LED Driver Current	RW	0x03FF	Min current
0x13	Green LED Driver Current	RW	0x03FF	Min current
0x14	Blue LED Driver Current	RW	0x03FF	Min current
0x15	RESERVED for I²C Read			
0x16	RGB LED Driver Enable	RW	0x0	Disabled
0x19	Video Frame Rate	RW	0x0859	60Hz
0x1D	Interface Sleep Control	RW	0x0	Interface active
0x1E	Sequence Sync Mode	RW	0x0	Free-run
0x1F	Software Reset	RW	0x0	Not in reset
0x23	Vertical Sync Line Delay	RW	0x5	Delay = 5 lines
0x29	Auto Framing-First Active Line in the Frame	RW	0x0	n/a
0x2A	Auto Framing-Last Active Line in the Frame	RW	0x0	n/a
0x2B	Auto Framing-First Active Pixel in the Line	RW	0x0	n/a
0x2C	Auto Framing-Last Active Pixel in the Line	RW	0x0	n/a
0x2D	DMD Park Control	RW	0x0	Disabled
0x30	Firmware Revision	RW	0x0	
0x33	Chroma Channel Swap	RW	0x0	Chroma Channel Swap enabled
0x38	Compound Command Command	RW	0x0	
0x39	Compound Command Data	RW	0x0	
0x3A	Compound Command Handshake	RW	0x0	
0x4B	LED Enable and Buffer Control Register 1	RW	0x0	Disable READ_BUF0, BUFFER_SWAP, PATTERN_INVERT, and RED_EN outputs and drive pins low
0x4C	LED Enable and Buffer Control Register 2	RW	0x0	Disable GREEN_EN, BLUE_EN, OUTPUT_TRIGGER, and READ_BUF1 outputs and drive pins low
0x50	AGC Control	RW	0x6	AGC disabled
0x52	AGC Step Size Increment	RW	0x1	60 Hz
0x53	AGC Step Size Decrement	RW	0x1	60 Hz
0x54	AGC Leap Size Decrement	RW	0x28	60 Hz

Table A-1. Register Quick Reference (continued)

I^2C Address	Description	Type	Reset Value	Default Action
0x5E	CCA Control	RW	0x1	CCA enabled
0x5F	CCA Parameter-Red 1	RW	0x100	
0x60	CCA Parameter-Red 2	RW	0x0	
0x61	CCA Parameter-Red 3	RW	0x0	
0x62	CCA Parameter-Green 1	RW	0x0	
0x63	CCA Parameter-Green 2	RW	0x100	
0x64	CCA Parameter-Green 3	RW	0x0	
0x65	CCA Parameter-Blue 1	RW	0x0	
0x66	CCA Parameter-Blue 2	RW	0x0	
0x67	CCA Parameter-Blue 3	RW	0x100	
0x71	CCA Parameter-White 1	RW	0x100	
0x72	CCA Parameter-White 2	RW	0x100	
0x73	CCA Parameter-White 3	RW	0x100	
0x7E	Temporal Dither Control	RW	0x2	Dither disabled
0x82	Sequencer Control	RW	0x0	
0x83	Sequence Vector Setup	RW	0x0	SEQ VECT = 0, 2 sub-vectors per SEQ
0x9B	mDDR Memory BIST Status	RO	0x0	
0xA3	Display Buffer Swap Freeze	RW	0x0	UnFrozen
0xA4	YCrCb To RGB Control	RW	0xE	BT.601
0xA6	Display Image Curtain Control	RW	0x0	Curtain disabled
0xA7	DMD Bus Swap Enable	RW	0x0	Disabled
0xAE	Auto Framing Function Enable	RW	0x0	Disabled
0xAF	Parallel Bus Polarity Control	RW	0x10	
0xB0	Auto Framing-Horizontal Back Porch Select	RW	0x 0	
0xB1	Auto Framing-Vertical Back Porch Select	RW	0x17	
0xC3	Source Color Space and Sampling Control	RW	0x0	RGB, 4:4:4
0xCF	Pattern Generator Enable Register	RW	0x0	Internal Pattern Generator disabled
0xD0	Pattern Generator Control Registers for Patterns 1–8	RW	0x0	Display pattern 0
0xD1	Pattern Generator Control Registers for Patterns 9–16	RW	0x0	Display pattern 0
0xD2	Pattern Generator Control Registers for Patterns 17–24	RW	0x0	Display pattern 0
0xD3	Pattern Generator Control Registers for Patterns 25–32	RW	0x0	Display pattern 0
0xD4	Pattern Generator Inversion Control Register	RW	0x0	Patterns not inverted

REVISION A HISTORY

Changes from Original (November, 2011) to A Revision **Page**

- Added section "Internal Pattern Generator" 29
- Added section "Sequencer Control" 37
- Added section "Compound I²C Commands" 38
- Added section "Display Sequences" 40
- Added Appendix A with new I2C registers. 75

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

REVISION B HISTORY

Changes from A Revision (May 2012) to B Revision **Page**

- Changed GPIO4_INTF to INIT_DONE in the Main Status Register (I²C: 0x03) section 9
- Changed GPIO4_INTF to INIT_DONE in the Chipset Control I²C Commands section 10
- Changed GPIO4_INTF to INIT_DONE in the Power-Up Auto-Initialization section 72

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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