INA188
Precision, Zero-Drift, Rail-to-Rail Out, High-Voltage Instrumentation Amplifier

1 Features

- Excellent DC Performance:
  - Low Input Offset Voltage: 55 µV (max)
  - Low Input Offset Drift: 0.2 µV/°C (max)
  - High CMRR: 104 dB, G ≥ 10 (min)
- Low Input Noise:
  - 12 nV/√Hz at 1 kHz
  - 0.25 μV_{PP} (0.1 Hz to 10 Hz)
- Wide Supply Range:
  - Single Supply: 4 V to 36 V
  - Dual Supply: ±2 V to ±18 V
- Gain Set with a Single External Resistor:
  - Gain Equation: G = 1 + (50 kΩ / R_G)
  - Gain Error: 0.007%, G = 1
  - Gain Drift: 5 ppm/°C (max) G = 1
- Input Voltage: (V–) + 0.1 V to (V+) – 1.5 V
- RFI-Filtered Inputs
- Rail-to-Rail Output
- Low Quiescent Current: 1.4 mA
- Operating Temperature: –55°C to +150°C
- SOIC-8 and DFN-8 Packages

2 Applications

- Bridge Amplifiers
- ECG Amplifiers
- Pressure Sensors
- Medical Instrumentation
- Portable Instrumentation
- Weigh Scales
- Thermocouple Amplifiers
- RTD Sensor Amplifiers
- Data Acquisition

3 Description

The INA188 is a precision instrumentation amplifier that uses TI proprietary auto-zeroing techniques to achieve low offset voltage, near-zero offset and gain drift, excellent linearity, and exceptionally low-noise density (12 nV/√Hz) that extends down to dc.

The INA188 is optimized to provide excellent common-mode rejection of greater than 104 dB (G ≥ 10). Superior common-mode and supply rejection supports high-resolution, precise measurement applications. The versatile three op-amp design offers a rail-to-rail output, low-voltage operation from a 4-V single supply as well as dual supplies up to ±18 V, and a wide, high-impedance input range. These specifications make this device ideal for universal signal measurement and sensor conditioning (such as temperature or bridge applications).

A single external resistor sets any gain from 1 to 1000. The INA188 is designed to use an industry-standard gain equation: G = 1 + (50 kΩ / R_G). The reference pin can be used for level-shifting in single-supply operation or for an offset calibration.

The INA188 is specified over the temperature range of –40°C to +125°C .

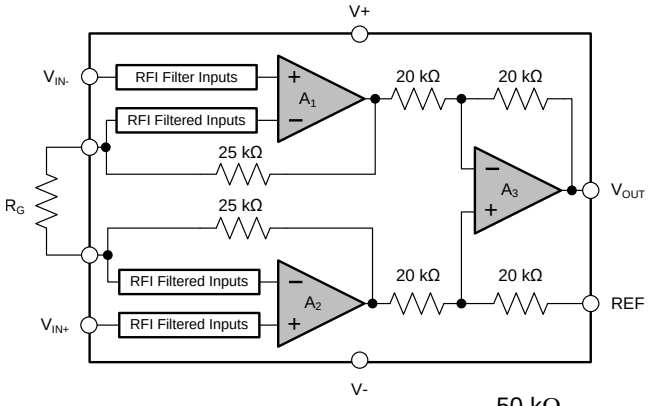
Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
INA188	SOIC (8)	4.90 mm × 3.91 mm
INA188	WSON (8)(2)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The DRJ package (WSON-8) is a preview device.

Simplified Schematic



$$V_{OUT} = (V_{IN+} - V_{IN-}) \times G + V_{REF} \qquad G = 1 + \frac{50\ k\Omega}{R_G}$$

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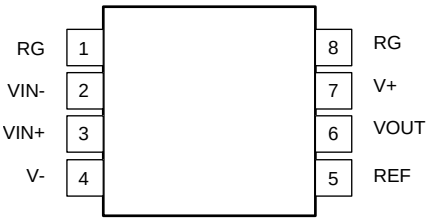
4 Revision History

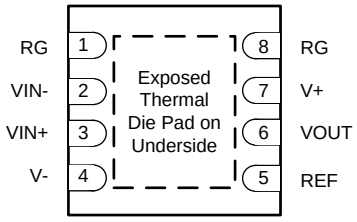
DATE	REVISION	NOTES
September 2015	*	Initial release.

5 Pin Configuration and Functions

D Package
SOIC-8
Top View



DRJ Package
WSON-8
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
RG	1, 8	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
V–	4	—	Negative supply
V+	7	—	Positive supply
VIN–	2	I	Negative input
VIN+	3	I	Positive input
VOUT	6	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply		±20	V
			40 (single supply)	
	Current		±10	mA
	Analog input range(2)	(V–) – 0.5	(V+) + 0.5	V
Output short-circuit(3)			Continuous	
Temperature	Operating range, T_A	–55	150	°C
	Junction, T_J		150	
	Storage temperature, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	4 (±2)		36 (±18)	V
	Specified temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA188		UNIT
		D (SOIC)	DRG (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	145	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80	75	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68	39	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32	14	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68	105	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

At T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT(1)						
V_{OSI}	Input stage offset voltage	At RTI(2)		±25	±55	µV
		At RTI, T_A = –40°C to +125°C		±0.08	±0.2	µV/°C
V_{OSO}	Output stage offset voltage	At RTI		±60	±170	µV
		At RTI, T_A = –40°C to +125°C		±0.2	±0.35	µV/°C
V_{OS}	Offset voltage	At RTI		±25 ±60 / G	±55 ±170 / G	µV
		At RTI, T_A = –40°C to +125°C			±0.2 ±0.35 / G	µV/°C
PSRR	Power-supply rejection ratio	G = 1, V_S = 4 V to 36 V, V_{CM} = V_S / 2		±0.7	±2.25	µV/V
		G = 10, V_S = 4 V to 36 V, V_{CM} = V_S / 2		±0.6		
		G = 100, V_S = 4 V to 36 V, V_{CM} = V_S / 2		±0.45		
		G = 1000, V_S = 4 V to 36 V, V_{CM} = V_S / 2		±0.3	±0.8	
	Long-term stability			1(3)		µV
	Turn-on time to specified V_{OSI}			See the *Typical Characteristics*		
z_{id}	Differential input impedance			100 || 6		GΩ || pF
z_{ic}	Common-mode input impedance			100 || 9.5		
V_{CM}	Common-mode voltage range	The input signal common-mode range can be calculated with this tool	(V–) + 0.1		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	G = 1, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	84	90		dB
		G = 10, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	104	110		
		G = 100, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	118	130		
		G = 1000, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	118	130		
INPUT BIAS CURRENT						
I_{IB}	Input bias current			±850	±2500	pA
		T_A = –40°C to +125°C		See Figure 10		pA/°C
I_{OS}	Input offset current			±850	±2500	pA
		T_A = –40°C to +125°C		See Figure 11		pA/°C
INPUT VOLTAGE NOISE						
e_{NI}	Input voltage noise	f = 1 kHz, G = 100, R_S = 0 Ω		12.5		nV/√Hz
		f = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		0.25		$µV_{PP}$
e_{NO}	Output voltage noise	f = 1 kHz, G = 100, R_S = 0 Ω		118		nV/√Hz
		f = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		2.5		$µV_{PP}$
i_N	Input current noise	f = 1 kHz		440		fA/√Hz
		f = 0.1 Hz to 10 Hz		10		pA_{PP}
GAIN						
G	Gain equation			1 + (50 kΩ / R_G)		V/V
	Gain range		1		1000	V/V
E_G	Gain error	G = 1, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.007%	±0.025%	
		G = 10, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.05%	±0.20%	
		G = 100, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.06%	±0.20%	
		G = 1000, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.2%	±0.50%	
	Gain versus temperature	G = 1, T_A = –40°C to +125°C		1	5	ppm/°C
		G > 1(4), T_A = –40°C to +125°C		15	50	
	Gain nonlinearity	G = 1, V_O = –10 V to +10 V		3	8	ppm
		G > 1, V_O = –10 V to +10 V		See Figure 42 to Figure 45		

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G).
(2) RTI = Referred-to-input.
(3) 300-hour life test at 150°C demonstrated a randomly distributed variation of approximately 1 µV.
(4) Does not include effects of external resistor R_G.

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

At T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
	Output voltage swing from rail(5)		R_L = 10 kΩ(5)		220	250	mV
	Capacitive load drive				1		nF
I_{SC}	Short-circuit current		Continuous to common		±18		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB		G = 1		600		kHz
			G = 10		95		
			G = 100		15		
			G = 1000		1.5		
SR	Slew rate		G = 1, V_S = ±18 V, V_O = 10-V step		0.9		V/µs
			G = 100, V_S = ±18 V, V_O = 10-V step		0.17		
t_S	Settling time	To 0.1%	G = 1, V_S = ±18 V, V_{STEP} = 10 V		50		µs
			G = 100, V_S = ±18 V, V_{STEP} = 10 V		400		
		To 0.01%	G = 1, V_S = ±18 V, V_{STEP} = 10 V		60		µs
			G = 100, V_S = ±18 V, V_{STEP} = 10 V		500		
	Overload recovery		50% overdrive		75		µs
REFERENCE INPUT							
R_{IN}	Input impedance				40		kΩ
	Voltage range			V–		V+	V
POWER SUPPLY							
	Voltage range	Single		4		36	V
		Dual		±2		±18	
I_Q	Quiescent current		V_{IN} = V_S / 2		1.4	1.6	mA
			T_A = –40°C to +125°C			1.8	
TEMPERATURE RANGE							
	Specified temperature range			–40		125	°C
	Operating temperature range			–55		150	°C

(5) See *Typical Characteristics* curves, *Output Voltage Swing vs Output Current* (Figure 19 to Figure 22).

6.6 Electrical Characteristics: V_S = ±2 V to < ±4 V (V_S = 4 V to < 8 V)

At T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1, unless otherwise noted. Specifications not shown are identical to the *Electrical Characteristics* table for V_S = ±2 V to ±18 V (V_S = 8 V to 36 V).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT(1)						
V_{OSI}	Input stage offset voltage	At RTI(2)		±25	±55	µV
		At RTI, T_A = –40°C to +125°C		±0.08	±0.2	µV/°C
V_{OSO}	Output stage offset voltage	At RTI		±60	±170	µV
		At RTI, T_A = –40°C to +125°C		±0.2	±0.35	µV/°C
V_{OS}	Offset voltage	At RTI		±25 ±60 / G	±55 ±170 / G	µV
		At RTI, T_A = –40°C to +125°C			±0.2 ±0.35 / G	µV/°C
	Long-term stability			1(3)		µV
	Turn-on time to specified V_{OSI}			See the *Typical Characteristics*		
z_{id}	Differential input impedance			100 || 6		GΩ || pF
z_{ic}	Common-mode input impedance			100 || 9.5		GΩ || pF
V_{CM}	Common-mode voltage range	V_O = 0 V, the input signal common-mode range can be calculated with this tool	(V–)		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	G = 1, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	80	90		dB
		G = 10, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	94	110		dB
		G = 100, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	102	120		dB
		G = 1000, at dc to 60 Hz, V_{CM} = (V–) + 1.0 V to (V+) – 2.5 V	102	120		dB
INPUT BIAS CURRENT						
I_{IB}	Input bias current			±850	±2500	pA
		T_A = –40°C to +125°C		See Figure 10		pA/°C
I_{OS}	Input offset current			±850	±2500	pA
		T_A = –40°C to +125°C		See Figure 11		pA/°C
INPUT VOLTAGE NOISE						
e_{NI}	Input voltage noise	f = 1 kHz, G = 100, R_S = 0 Ω		12.5		nV/√Hz
		f = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		0.25		$µV_{PP}$
e_{NO}	Output voltage noise	f = 1 kHz, G = 100, R_S = 0 Ω		118		nV/√Hz
		f = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω		2.5		$µV_{PP}$
i_N	Input current noise	f = 1 kHz		430		fA/√Hz
		f = 0.1 Hz to 10 Hz		10		pA_{PP}
GAIN						
G	Gain equation			1 + (50 kΩ / R_G)		V/V
	Gain range		1		1000	V/V
E_G	Gain error	G = 1, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.007%	±0.05%	
		G = 10, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.07%	±0.2%	
		G = 100, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.07%	±0.2%	
		G = 1000, (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		±0.25%	±0.5%	
	Gain versus temperature	G = 1, T_A = –40°C to +125°C		1	5	ppm/°C
		G > 1(4), T_A = –40°C to +125°C		15	50	ppm/°C
	Gain nonlinearity	G = 1, V_O = (V–) + 0.5 V ≤ V_O ≤ (V+) – 1.5 V		3	8	ppm

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G).
(2) RTI = Referred-to-input.
(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.
(4) Does not include effects of external resistor R_G.

Electrical Characteristics: V_S = ±2 V to < ±4 V (V_S = 4 V to < 8 V) (continued)

At T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1, unless otherwise noted. Specifications not shown are identical to the *Electrical Characteristics* table for V_S = ±2 V to ±18 V (V_S = 8 V to 36 V).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
	Output voltage swing from rail(5)		R_L = 10 kΩ		220	250	mV
	Capacitive load drive				1		nF
I_{SC}	Short-circuit current		Continuous to common		±18		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB		G = 1		600		kHz
			G = 10		95		
			G = 100		15		
			G = 1000		1.5		
SR	Slew rate		G = 1, V_S = 5 V, V_O = 4-V step		0.9		V/µs
			G = 100, V_S = 5 V, V_O = 4-V step		0.17		
t_S	Settling time	To 0.1%	G = 1, V_S = 5 V, V_{STEP} = 4 V		50		µs
			G = 100, V_S = 5 V, V_{STEP} = 4 V		400		
		To 0.01%	G = 1, V_S = 5 V, V_{STEP} = 4 V		60		µs
			G = 100, V_S = 5 V, V_{STEP} = 4 V		500		
	Overload recovery		50% overdrive		75		µs
REFERENCE INPUT							
R_{IN}	Input impedance				40		kΩ
	Voltage range			V–		V+	V
POWER SUPPLY							
	Voltage range	Single		4		36	V
		Dual		±2		±18	
I_Q	Quiescent current		V_{IN} = V_S / 2		1.4	1.6	mA
			T_A = –40°C to +125°C			1.8	
TEMPERATURE RANGE							
	Specified temperature range			–40		125	°C
	Operating temperature range			–55		150	°C

(5) See *Typical Characteristics* curves, *Output Voltage Swing vs Output Current* (Figure 19 to Figure 22).

6.7 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

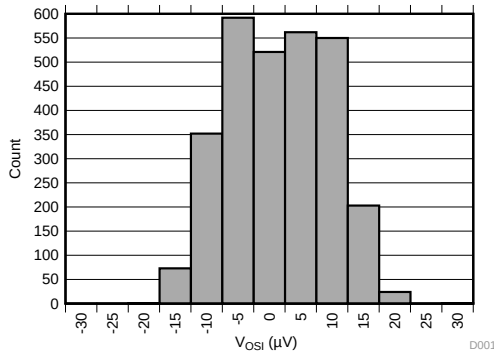


Figure 1. Input Voltage Offset Distribution

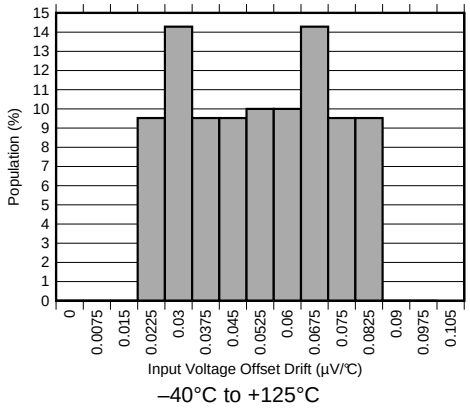


Figure 2. Input Voltage Offset Drift Distribution

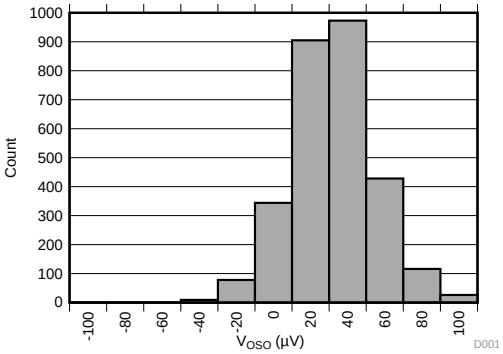


Figure 3. Output Voltage Offset Distribution

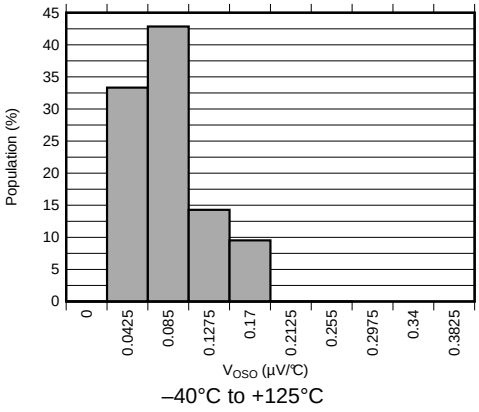


Figure 4. Output Voltage Offset Drift Distribution

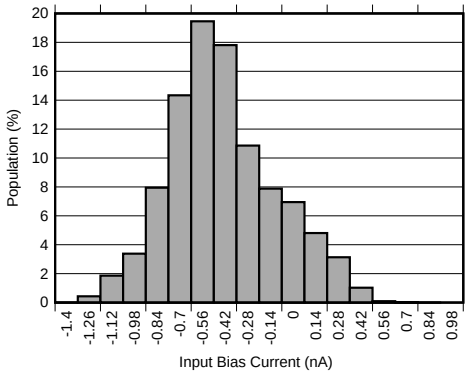


Figure 5. Input Bias Current Distribution

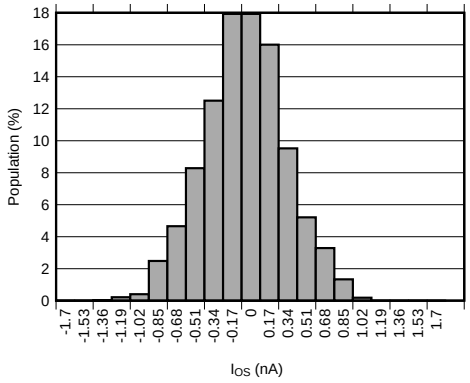


Figure 6. Input Offset Current Distribution

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

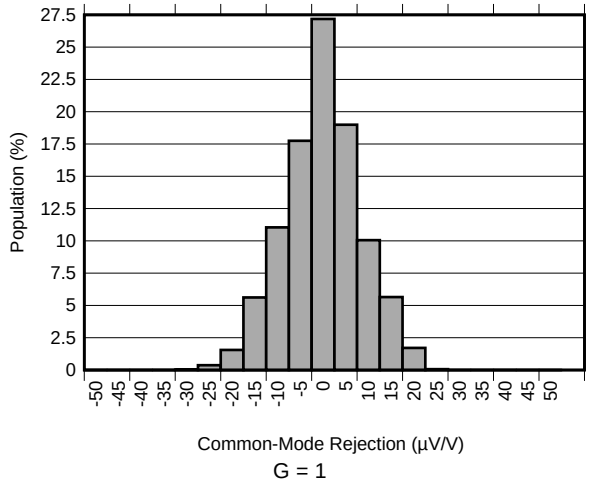


Figure 7. CMRR Distribution

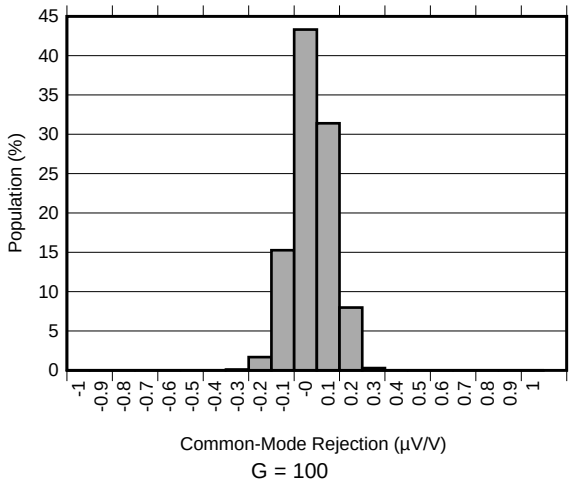


Figure 8. CMRR Distribution

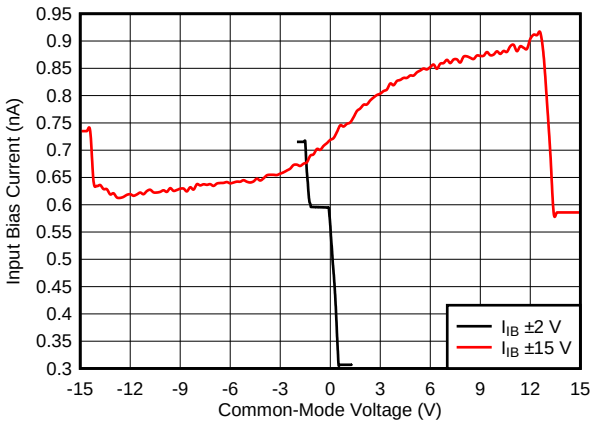


Figure 9. Input Bias Current vs Common-Mode Voltage

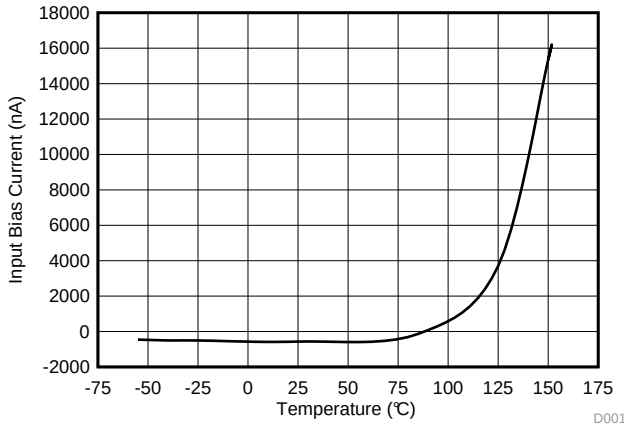


Figure 10. Input Bias Current vs Temperature

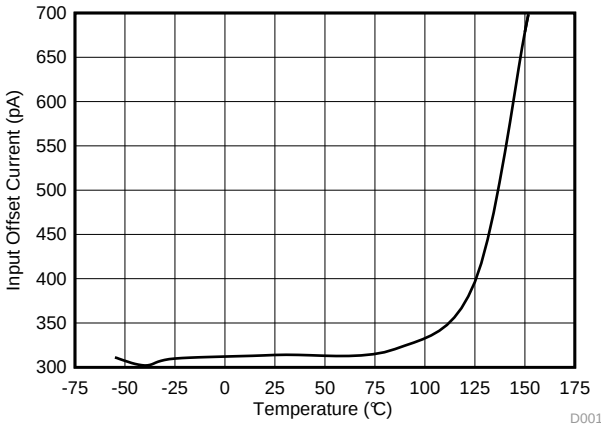


Figure 11. Input Offset Current vs Temperature

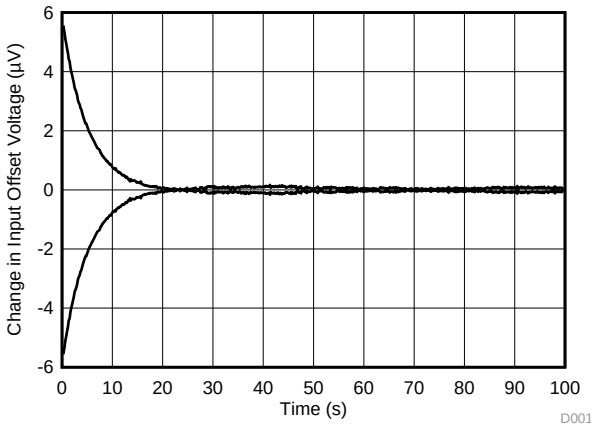


Figure 12. Change in Input Offset Voltage vs Warm-Up Time

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

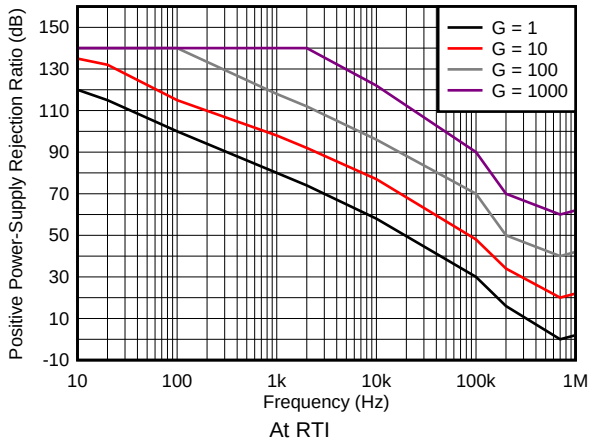


Figure 13. Positive PSRR vs Frequency

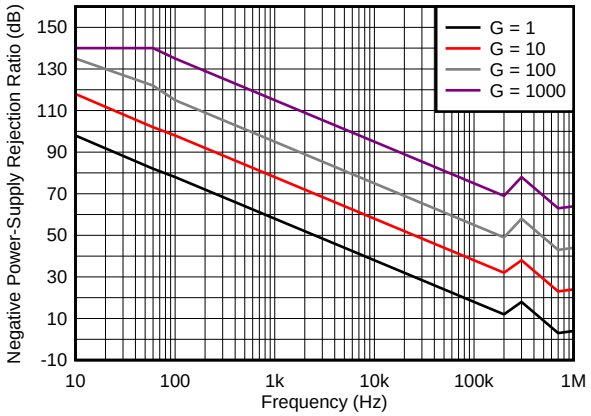


Figure 14. Negative PSRR vs Frequency

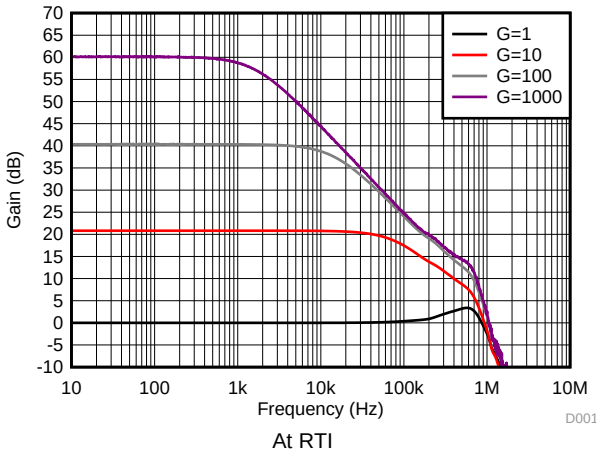


Figure 15. Gain vs Frequency

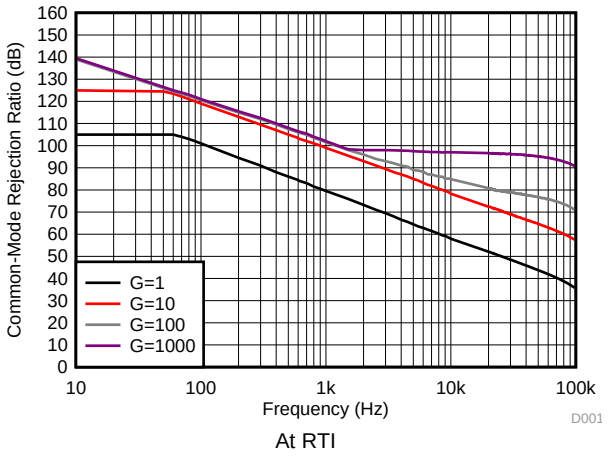


Figure 16. CMRR vs Frequency

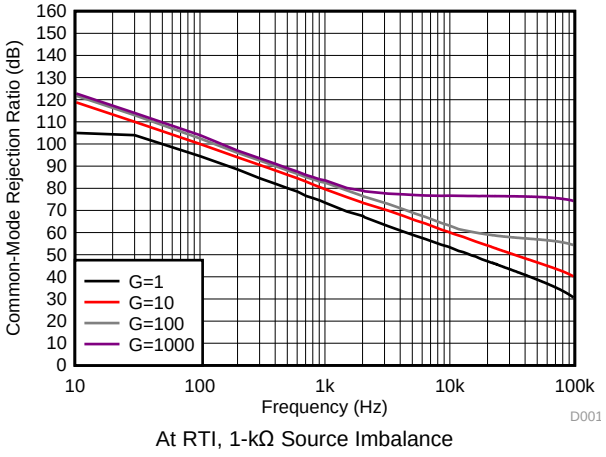


Figure 17. CMRR vs Frequency

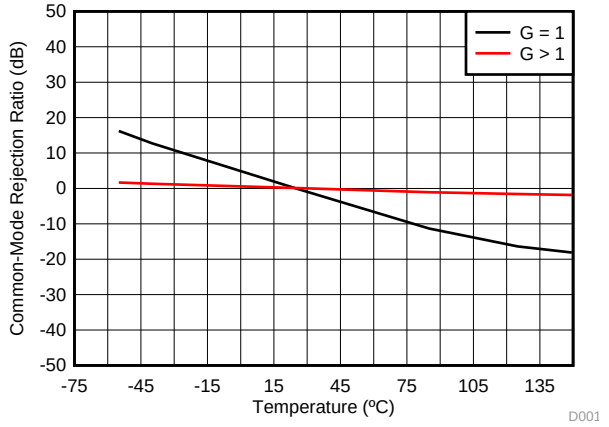
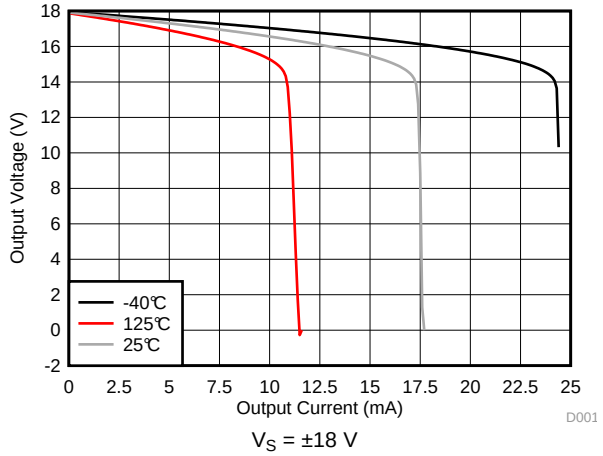


Figure 18. Common-Mode Rejection Ratio vs Temperature

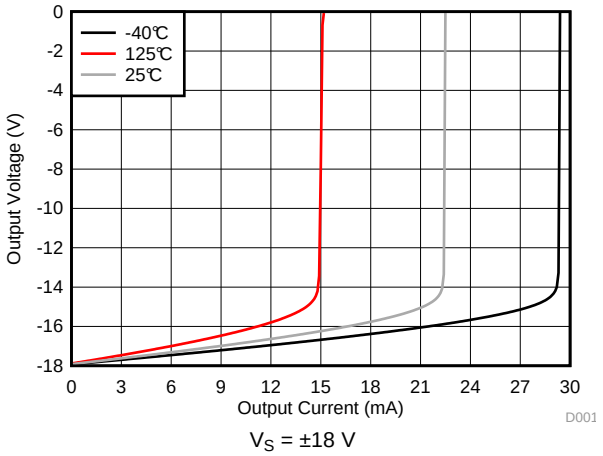
Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.



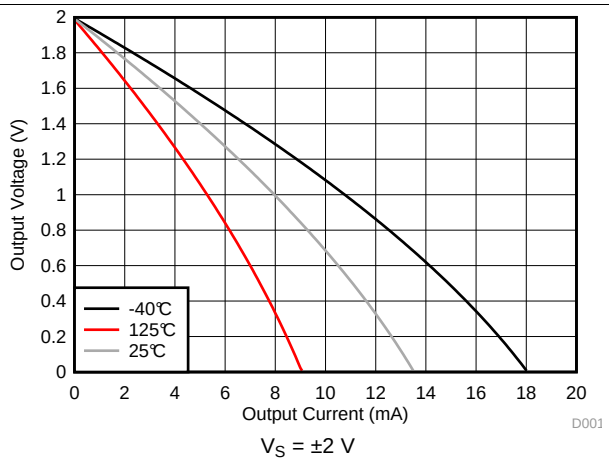
V_S = ±18 V

Figure 19. Positive Output Voltage Swing vs Output Current



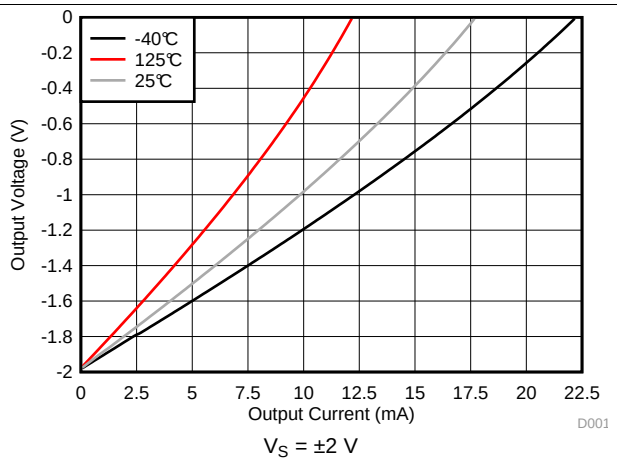
V_S = ±18 V

Figure 20. Negative Output Voltage Swing vs Output Current



V_S = ±2 V

Figure 21. Positive Output Voltage Swing vs Output Current



V_S = ±2 V

Figure 22. Negative Output Voltage Swing vs Output Current

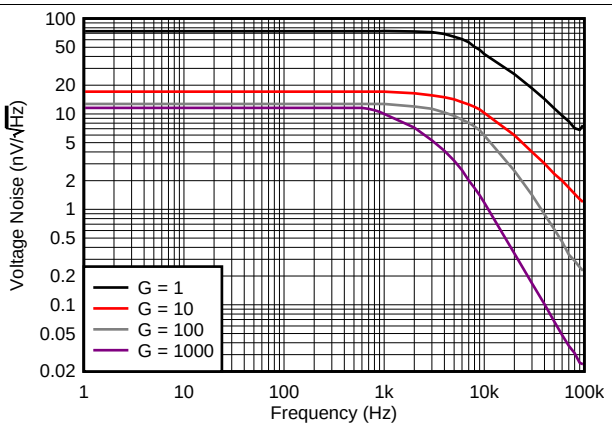
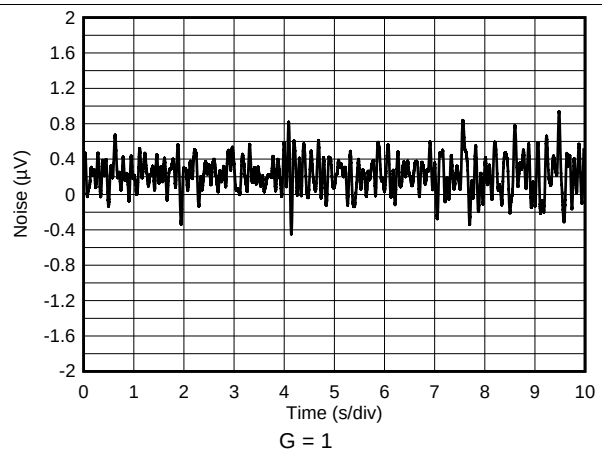


Figure 23. Voltage Noise Spectral Density vs Frequency



G = 1

Figure 24. 0.1-Hz to 10-Hz RTI Voltage Noise

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

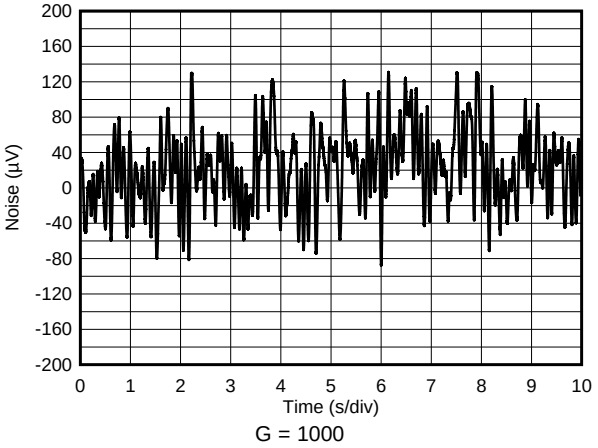


Figure 25. 0.1-Hz to 10-Hz RTI Voltage Noise

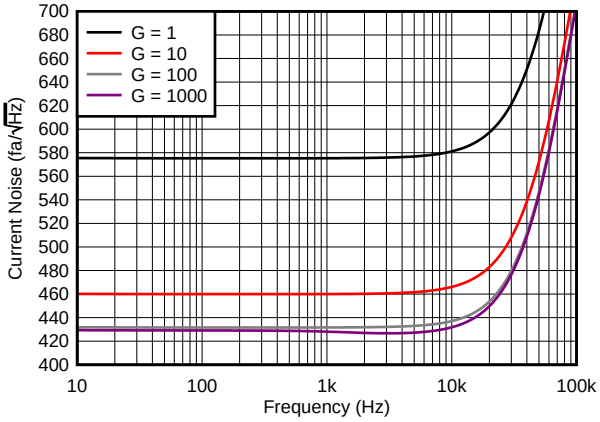


Figure 26. Current Noise Spectral Density vs Frequency

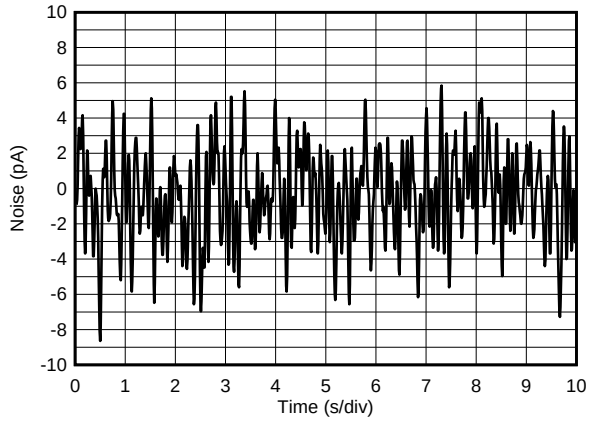


Figure 27. 0.1-Hz to 10-Hz RTI Current Noise

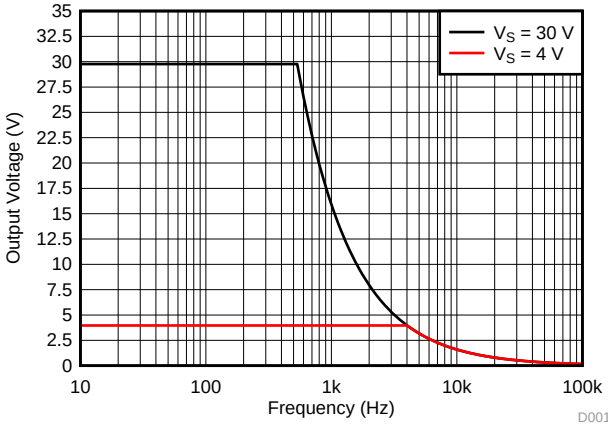


Figure 28. Large-Signal Response vs Frequency

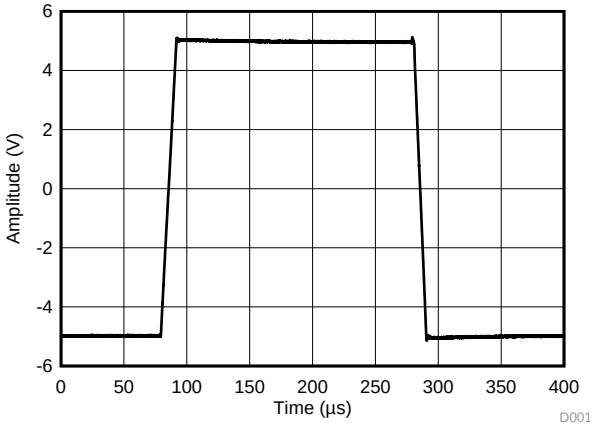


Figure 29. Large-Signal Pulse Response

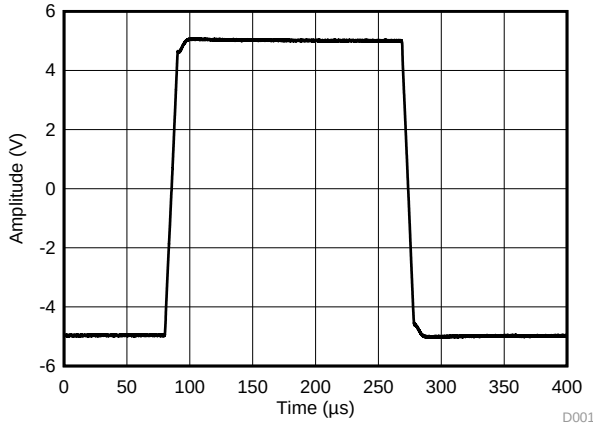
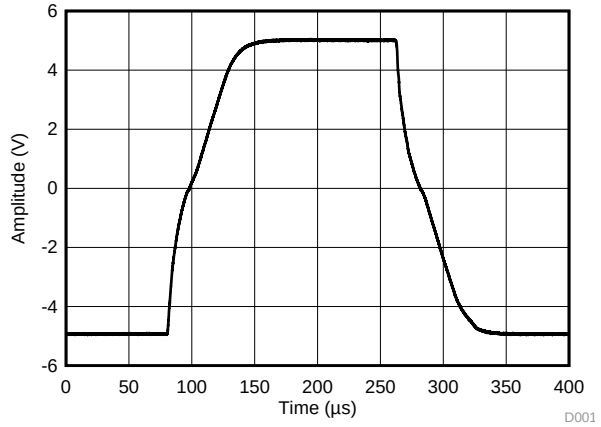


Figure 30. Large-Signal Pulse Response

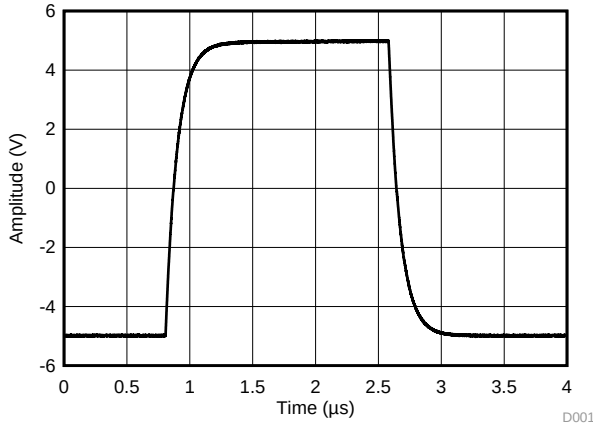
Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.



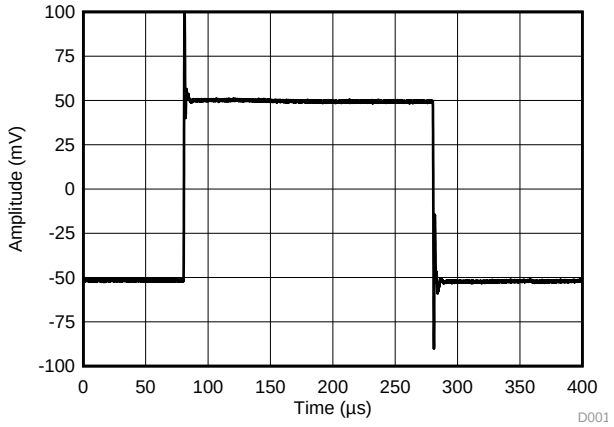
R_L = 10 kΩ, C_L = 100 pF, G = 100

Figure 31. Large-Signal Pulse Response



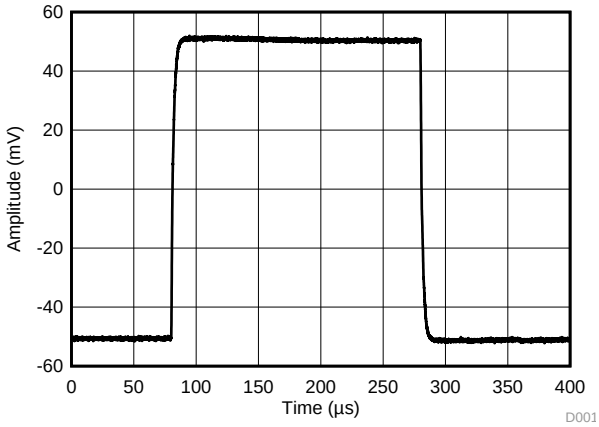
R_L = 10 kΩ, C_L = 100 pF, G = 1000

Figure 32. Large-Signal Pulse Response



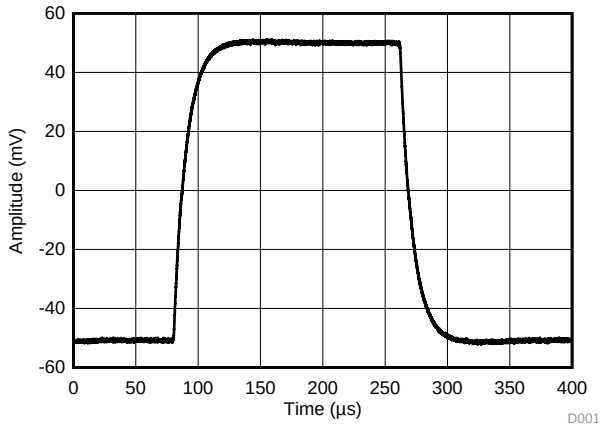
R_L = 10 kΩ, C_L = 100 pF, G = 1

Figure 33. Small-Signal Pulse Response



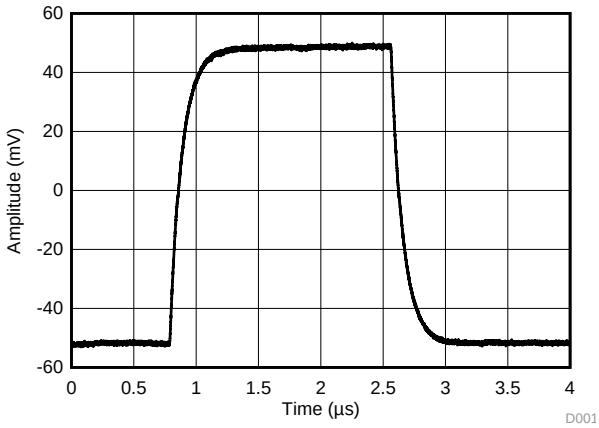
R_L = 10 kΩ, C_L = 100 pF, G = 10

Figure 34. Small-Signal Pulse Response



R_L = 10 kΩ, C_L = 100 pF, G = 100

Figure 35. Small-Signal Pulse Response



R_L = 10 kΩ, C_L = 100 pF, G = 1000

Figure 36. Small-Signal Pulse Response

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

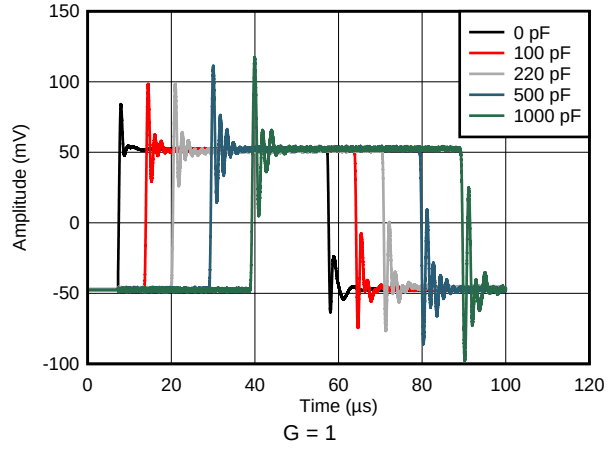


Figure 37. Small-Signal Response vs Capacitive Load

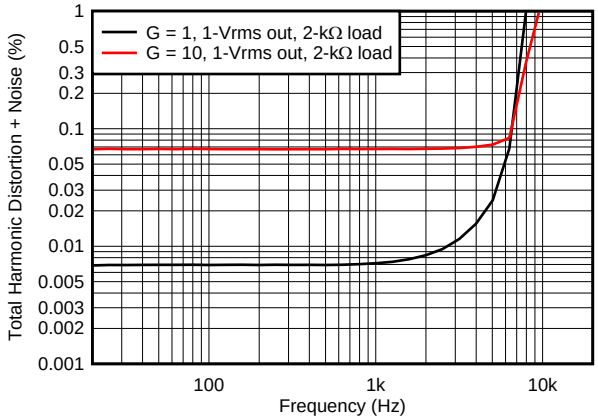


Figure 38. Total Harmonic Distortion + Noise vs Frequency

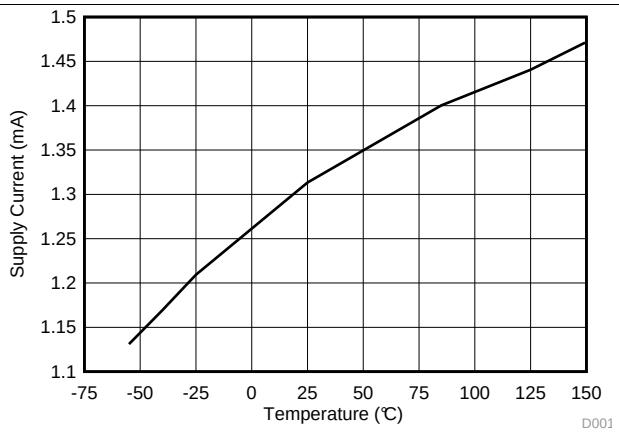


Figure 39. Supply Current vs Temperature

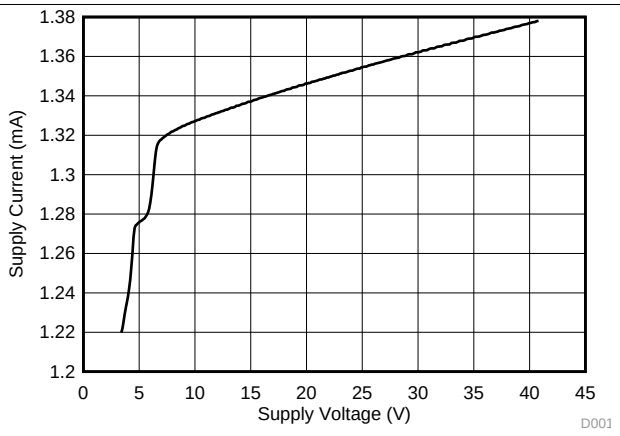


Figure 40. Supply Current vs Supply Voltage

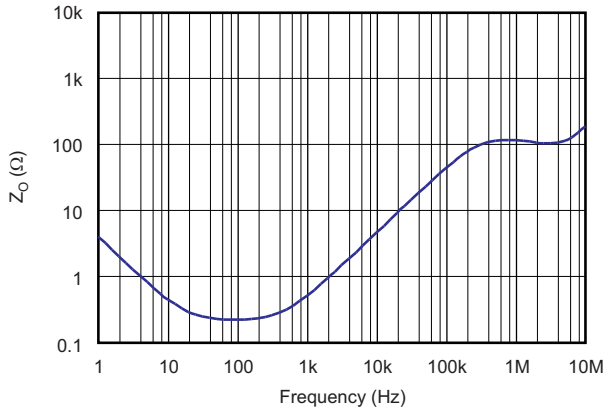


Figure 41. Open-Loop Output Impedance

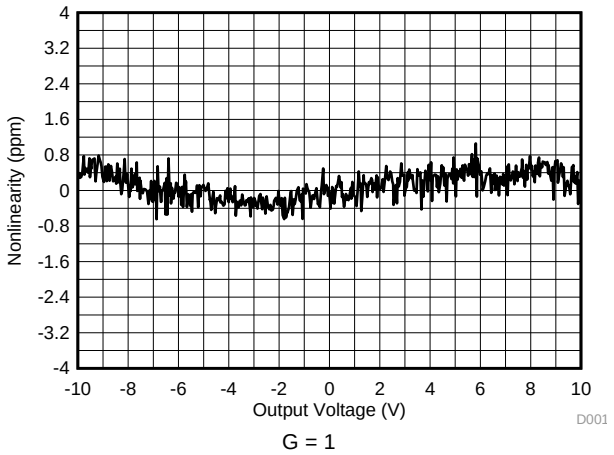


Figure 42. Gain Nonlinearity

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

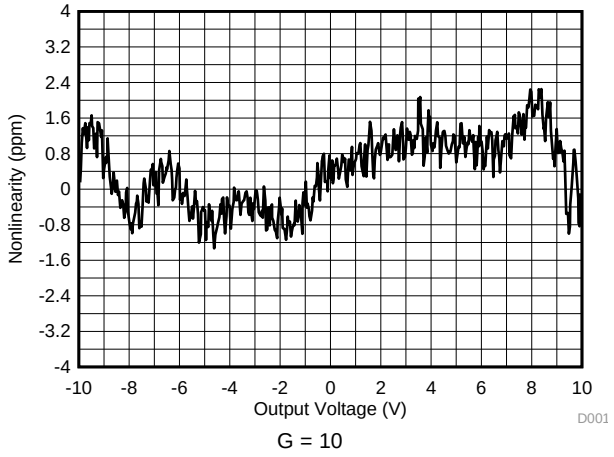


Figure 43. Gain Nonlinearity

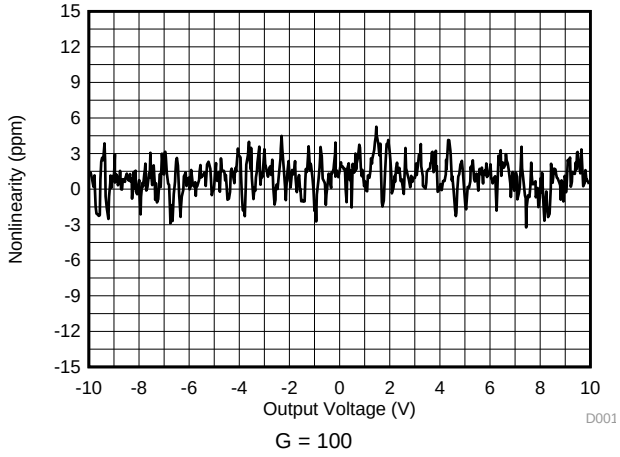


Figure 44. Gain Nonlinearity

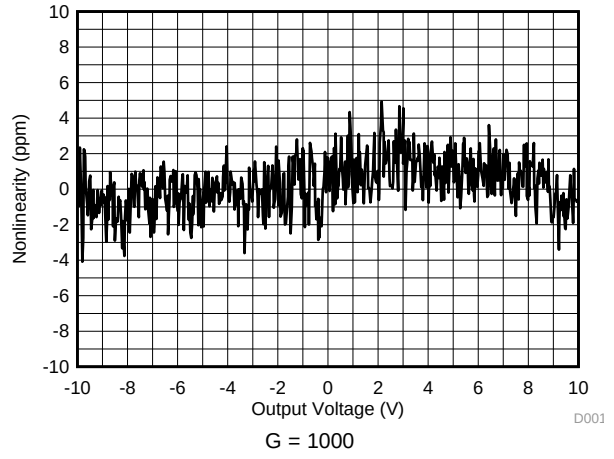


Figure 45. Gain Nonlinearity

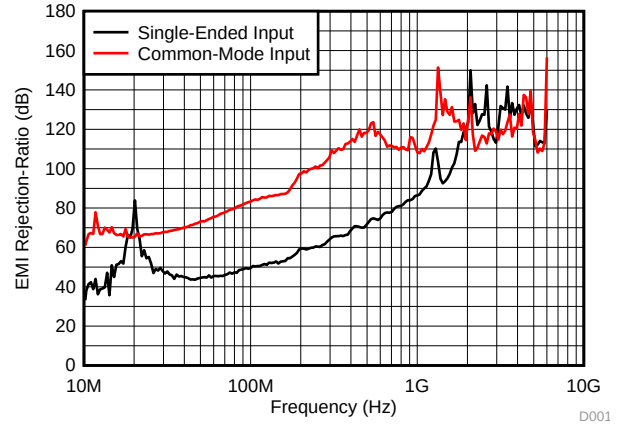


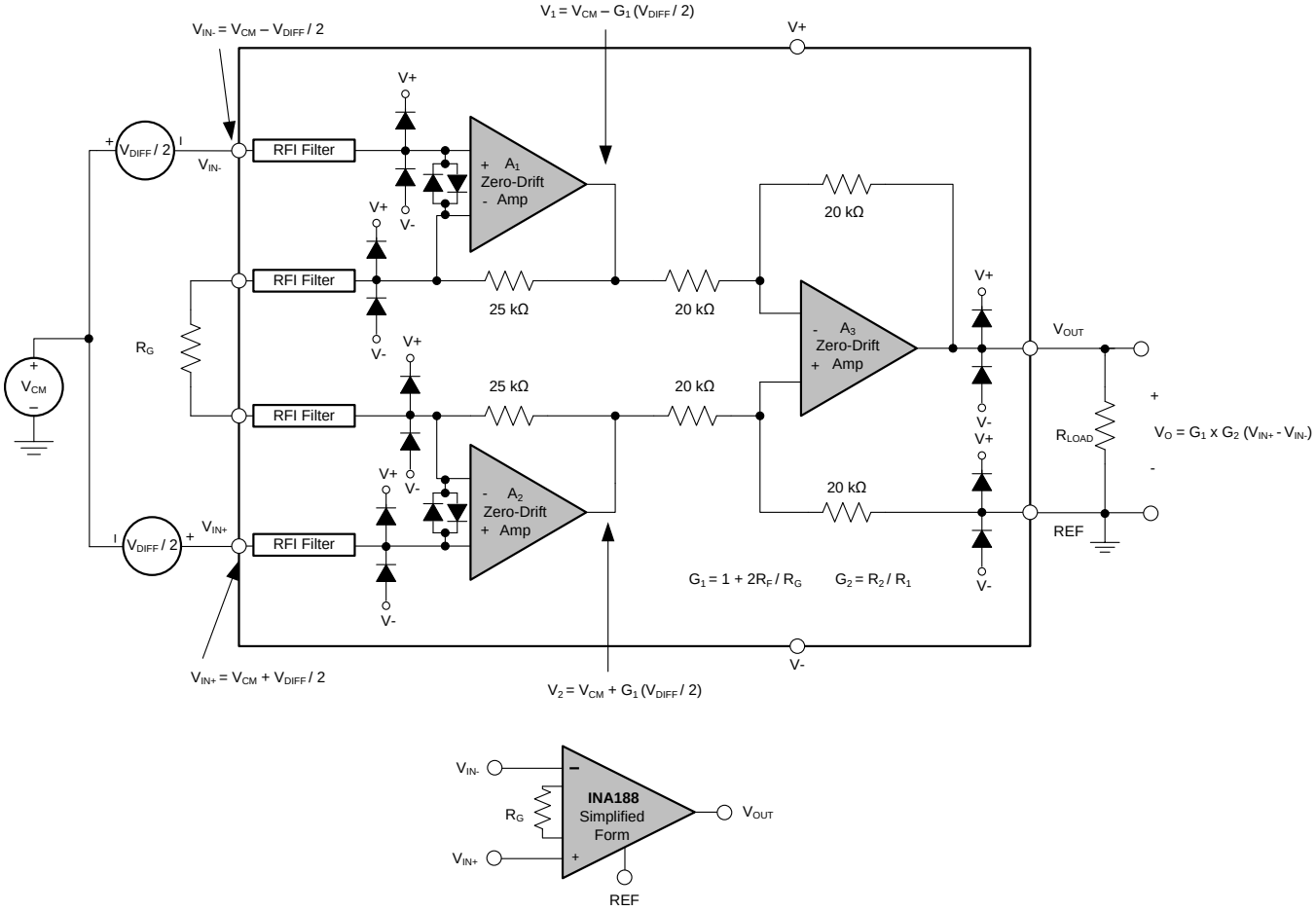
Figure 46. EMIRR

7 Detailed Description

7.1 Overview

The INA188 is a monolithic instrumentation amplifier (INA) based on the 36-V, precision zero-drift OPA188 (operational amplifier) core. The INA188 also integrates laser-trimmed resistors to ensure excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding dc precision and makes the INA188 ideal for many high-voltage industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inside the INA188

The *Functional Block Diagram* section provides a detailed diagram for the INA188, including the ESD protection and radio frequency interference (RFI) filtering. Instrumentation amplifiers are commonly represented in a simplified form, as shown in Figure 47.

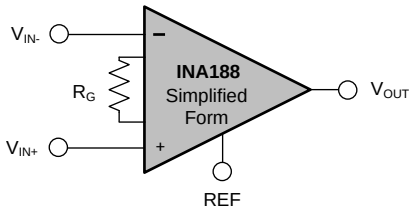


Figure 47. INA Simplified Form

A brief description of the internal operation is as follows:

The differential input voltage applied across R_G causes a signal current to flow through the R_G resistor and both R_F resistors. The output difference amplifier (A_3) removes the common-mode component of the input signal and refers the output signal to the REF pin.

The equations shown in the *Functional Block Diagram* section describe the output voltages of A_1 and A_2. Understanding the internal node voltages is useful to avoid saturating the device and to ensure proper device operation.

7.3.2 Setting the Gain

The gain of the INA188 is set by a single external resistor, R_G, connected between pins 1 and 8. The value of R_G is selected according to Equation 1:

$$G = 1 + \frac{50\ k\Omega}{R_G} \tag{1}$$

Table 1 lists several commonly-used gains and resistor values. The 50-kΩ term in Equation 1 comes from the sum of the two internal 25-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA188.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	50k	49.9k
5	12.5k	12.4k
10	5.556k	5.49k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9

(1) NC denotes no connection. When using the SPICE model, the simulation does not converge unless a resistor is connected to the R_G pins; use a very large resistor value.

7.3.2.1 Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be determined from Equation 1.

The best gain drift of 5 ppm/°C can be achieved when the INA188 uses G = 1 without R_G connected. In this case, gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 20-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor R_G. The low temperature coefficient of the internal feedback resistors significantly improves the overall temperature stability of applications using gains greater than 1 V/V over competing alternate solutions.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see *Typical Characteristics* curve, Figure 17.

7.3.3 Zero Drift Topology

7.3.3.1 Internal Offset Correction

Figure 48 shows a simple representation of the proprietary zero-drift architecture for one of the three amplifiers that comprise the INA188. These high-precision input amplifiers enable very low dc error and drift as a result of a modern chopper technology with an embedded synchronous filter that removes nearly all chopping noise. The chopping frequency is approximately 750 kHz. This amplifier is zero-corrected every 3 µs using a proprietary technique. This design has no aliasing.

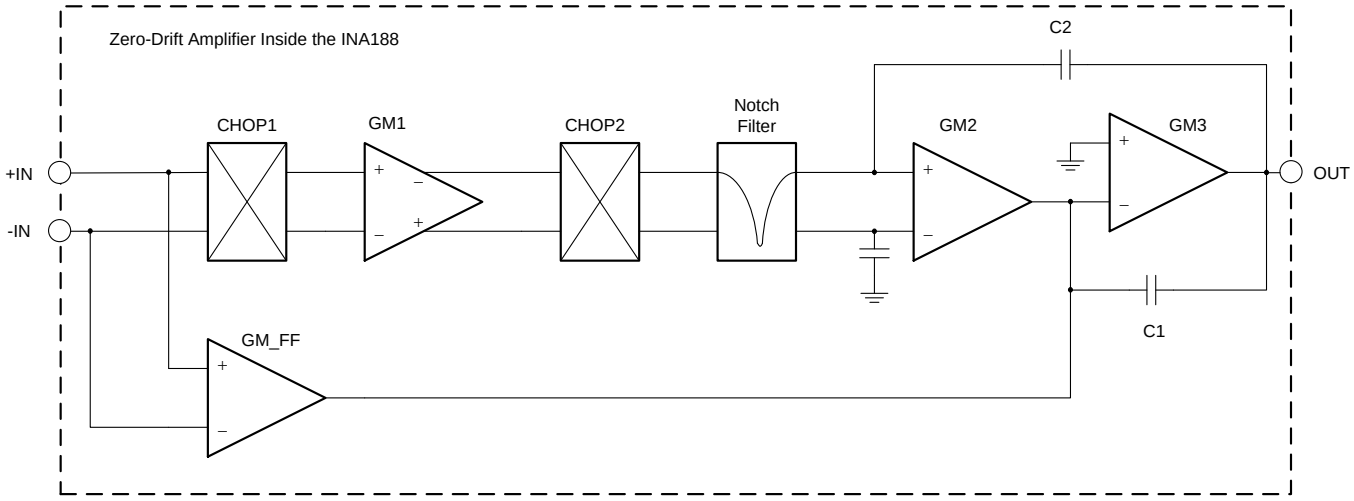


Figure 48. Zero-Drift Amplifier Functional Block Diagram

7.3.3.2 Noise Performance

This zero-drift architecture reduces flicker (1/f) noise to a minimum, and therefore enables the precise measurement of small dc-signals with high resolution, accuracy, and repeatability. The auto-calibration technique used by the INA188 results in reduced low-frequency noise, typically only 12 nV/$\sqrt{\text{Hz}}$ (at G = 100). The spectral noise density is detailed in Figure 53. Low-frequency noise of the INA188 is approximately 0.25 μV_{PP} measured from 0.1 Hz to 10 Hz (at G = 100).

7.3.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers, such as the INA188, use switching on their inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents them from being amplified; however, the pulses can be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter (such as an RC network).

7.3.4 EMI Rejection

The INA188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources (such as wireless communications) and densely-populated boards with a mix of analog signal-chain and digital components. The INA188 is specifically designed to minimize susceptibility to EMI by incorporating an internal low-pass filter. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system, as well as incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing. Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum, extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the INA188 ability to reject EMI. Figure 49 and Figure 50 show the INA188 EMIRR graph for both differential and common-mode EMI rejection across this frequency range. Table 2 shows the EMIRR values for the INA188 at frequencies commonly encountered in real-world applications. Applications listed in Table 2 can be centered on or operated near the particular frequency shown.

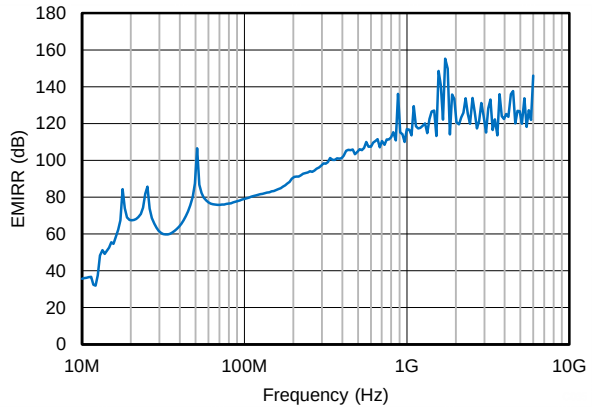


Figure 49. Common Mode EMIRR Testing

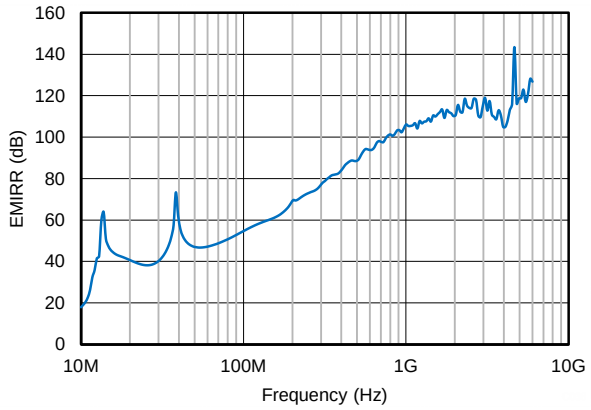


Figure 50. Differential Mode (VIN+) EMIRR Testing

Table 2. INA188 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL (IN-P) EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	83 dB	101 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	103 dB	118 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	112 dB	125 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	114 dB	123 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	110 dB	121 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	119 dB	123 dB

7.3.5 Input Protection and Electrical Overstress

Designers often ask questions about the capability of an amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal ESD protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. The *Functional Block Diagram* section illustrates the ESD circuits contained in the INA188. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines. This protection circuitry is intended to remain inactive during normal circuit operation.

The input pins of the INA188 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent the input circuitry from being damaged. If the input signal voltage can exceed the power supplies by more than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. This current limiting can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

7.3.6 Input Common-Mode Range

The linear input voltage range of the INA188 input circuitry extends from 100 mV inside the negative supply voltage to 1.5 V below the positive supply, and maintains 84-dB (minimum) common-mode rejection throughout this range. The common-mode range for most common operating conditions is best calculated using the INA common-mode range calculating tool. The INA188 can operate over a wide range of power supplies and V_{REF} configurations, thus providing a comprehensive guide to common-mode range limits for all possible conditions is impractical.

The most commonly overlooked overload condition occurs when a circuit exceeds the output swing of A_1 and A_2, which are internal circuit nodes that cannot be measured. Calculating the expected voltages at the output of A_1 and A_2 (see the *Functional Block Diagram* section) provides a check for the most common overload conditions. The designs of A_1 and A_2 are identical and the outputs can swing to within approximately 250 mV of the power-supply rails. For example, when the A_2 output is saturated, A_1 can continue to be in linear operation, responding to changes in the noninverting input voltage. This difference can give the appearance of linear operation but the output voltage is invalid.

7.4 Device Functional Modes

7.4.1 Single-Supply Operation

The INA188 can be used on single power supplies of 4 V to 36 V. Use the output REF pin to level shift the internal output voltage into a linear operating condition. Ideally, connecting the REF pin to a potential that is mid-supply avoids saturating the output of the input amplifiers (A_1 and A_2). Actual output voltage swing is limited to 250 mV above ground when the load is referred to ground. The typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 19 to Figure 22) illustrates how the output voltage swing varies with output current. See the *Driving the Reference Pin* section for information on how to adequately drive the reference pin.

With single-supply operation, V_{IN+} and $V_{IN–}$ must both be 0.1 V above ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

Device Functional Modes (continued)

7.4.2 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. Figure 51 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF pin is summed at the output. The op amp buffer provides low impedance at the REF pin to preserve good common-mode rejection.

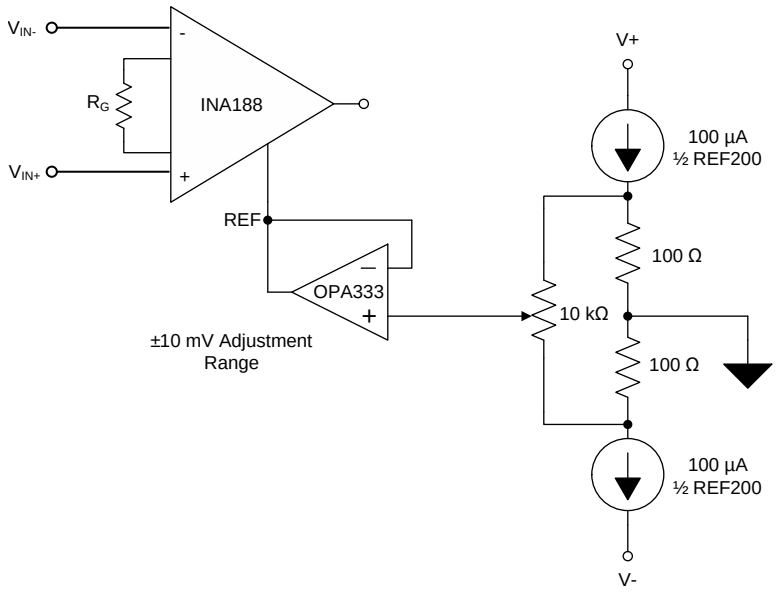


Figure 51. Optional Trimming of the Output Offset Voltage

Device Functional Modes (continued)

7.4.3 Input Bias Current Return Path

The input impedance of the INA188 is extremely high—approximately 20 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 750 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 52 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA188, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in Figure 52). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

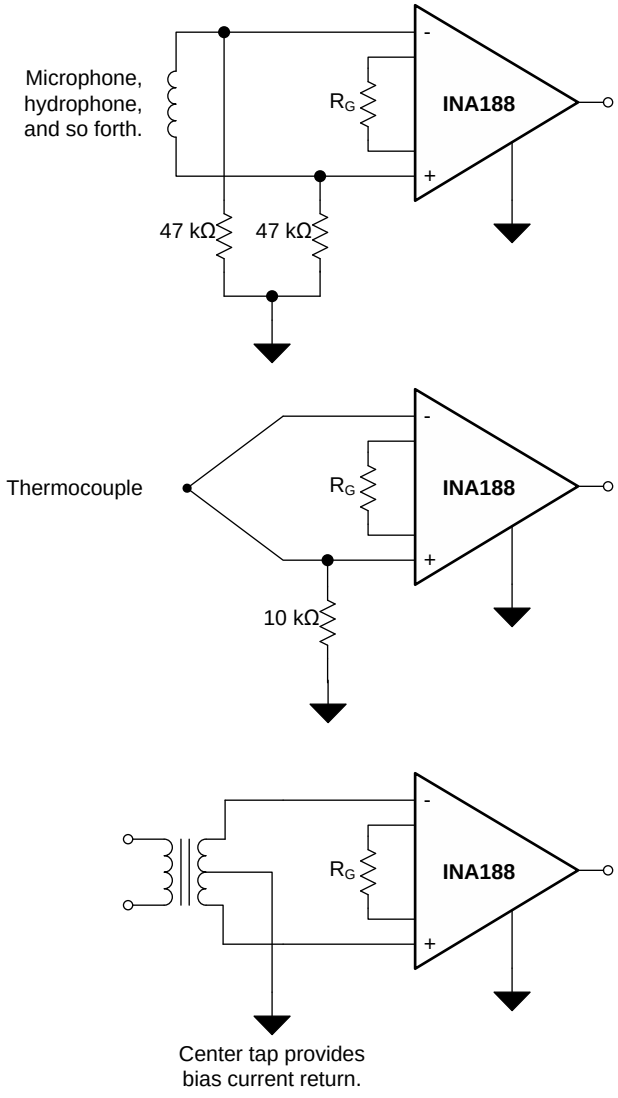


Figure 52. Providing an Input Common-Mode Current Path

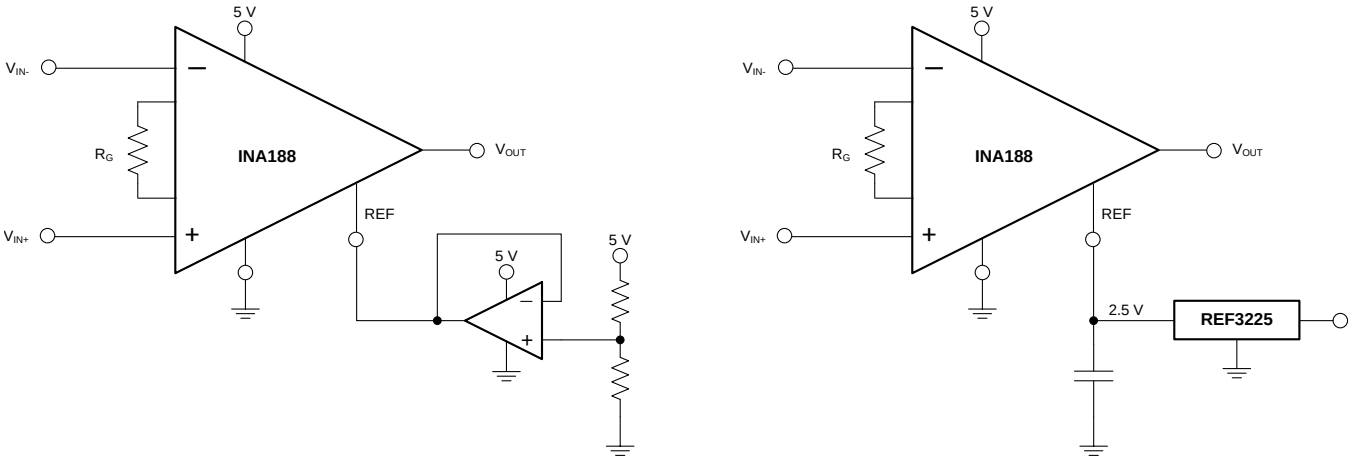
Device Functional Modes (continued)

7.4.4 Driving the Reference Pin

The output voltage of the INA188 is developed with respect to the voltage on the reference pin. Often, the reference pin (pin 5) is connected to the low-impedance system ground in dual-supply operation. In single-supply operation, offsetting the output signal to a precise mid-supply level (for example, 2.5 V in a 5-V supply environment) can be useful. To accomplish this, a voltage source can be tied to the REF pin to level-shift the output so that the INA188 can drive a single-supply analog-to-digital converter (ADC).

For best performance, keep the source impedance to the REF pin below 5 Ω. As illustrated in the *Functional Block Diagram* section, the reference pin is internally connected to a 20-kΩ resistor. Additional impedance at the REF pin adds to this 20-kΩ resistor. The imbalance in the resistor ratios results in degraded common-mode rejection ratio (CMRR).

Figure 53 shows two different methods of driving the reference pin with low impedance. The OPA330 is a low-power, chopper-stabilized amplifier, and therefore offers excellent stability over temperature. The OPA330 is available in a space-saving SC70 and an even smaller chip-scale package. The REF3225 is a precision reference in a small SOT23-6 package.



a) Level shifting using the OPA330 as a low-impedance buffer.

b) Level shifting using the low-impedance output of the REF3225.

Figure 53. Options for Low-Impedance Level Shifting

Device Functional Modes (continued)

7.4.5 Error Sources Example

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimizing these errors is important and can be done by choosing high-precision components (such as the INA188 that has improved specifications in critical areas that impact the precision of the overall system). Figure 54 shows an example application.

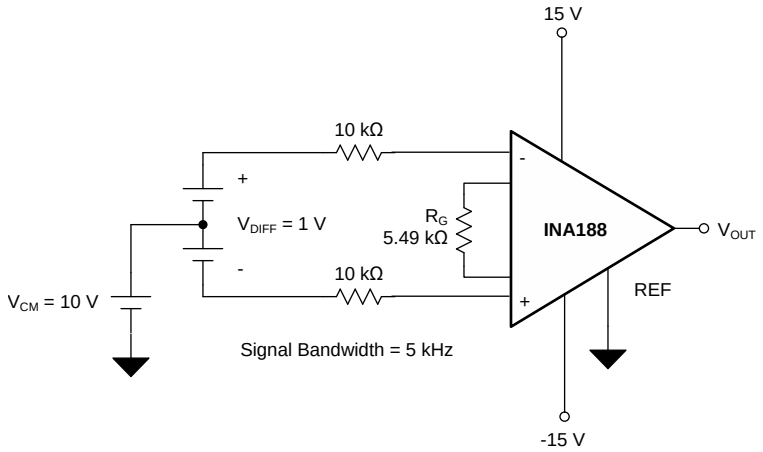


Figure 54. Example Application with G = 10 V/V and a 1-V Differential Voltage

Resistor-adjustable INAs such as the INA188 show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V) the gain error becomes a significant error source because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high-gain applications, gain drift is by far the largest error contributor compared to other drift errors, such as offset drift. The INA188 offers the lowest gain error over temperature in the marketplace for both G > 1 and G = 1 (no external gain resistor). Table 3 summarizes the major error sources in common INA applications and compares the two cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor). As explained in Table 3, although the static errors (absolute accuracy errors) in G = 1 are almost twice as great as compared to G = 10, there are much fewer drift errors because of the much lower gain error drift. In most applications, these static errors can readily be removed during calibration in production. All calculations refer the error to the input for easy comparison and system evaluation.

Device Functional Modes (continued)

Table 3. Error Calculation

ERROR SOURCE	ERROR CALCULATION	SPECIFICATION	G = 10 ERROR (ppm)	G = 1 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C				
Input offset voltage	V_{OSI} / V_{DIFF}	65 µV	65	65
Output offset voltage	V_{OSO} / (G × V_{DIFF})	180 µV	18	180
Input offset current	I_{OS} × maximum (R_{S+}, $R_{S–}$) / V_{DIFF}	5 nA	50	50
Common-mode rejection ratio	V_{CM} / ($10^{CMRR/20}$ × V_{DIFF})	104 dB (G = 10), 84 dB (G = 1)	20	501
Total absolute accuracy error (ppm)			153	796
DRIFT TO 105°C				
Gain drift	GTC × (T_A – 25)	35 ppm/°C (G = 10), 1 ppm/°C (G = 1)	2800	80
Input offset voltage drift	(V_{OSI_TC} / V_{DIFF}) × (T_A – 25)	0.15 µV/°C	12	12
Output offset voltage drift	[V_{OSO_TC} / (G × V_{DIFF})] × (T_A – 25)	0.85 µV/°C	6.8	68
Offset current drift	I_{OS_TC} × maximum (R_{S+}, $R_{S–}$) × (T_A – 25) / V_{DIFF}	60 pA/°C	48	48
Total drift error (ppm)			2867	208
RESOLUTION				
Gain nonlinearity		5 ppm of FS	5	5
Voltage noise (1 kHz)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left[\frac{e_{NO}}{G}\right]^2}$ × $\frac{6}{V_{DIFF}}$	e_{NI} = 18, e_{NO} = 110	9	47
Total resolution error (ppm)			14	52
TOTAL ERROR				
Total error (ppm)	Total error = sum of all error sources		3034	1056

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA188 measures a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The low offset drift in conjunction with no 1/f noise makes the INA188 suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.2 Typical Application

Figure 55 shows the basic connections required for operating the INA188. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. The output is referred to the output reference (REF) pin that is normally grounded. The reference pin must be a low-impedance connection to assure good common-mode rejection.

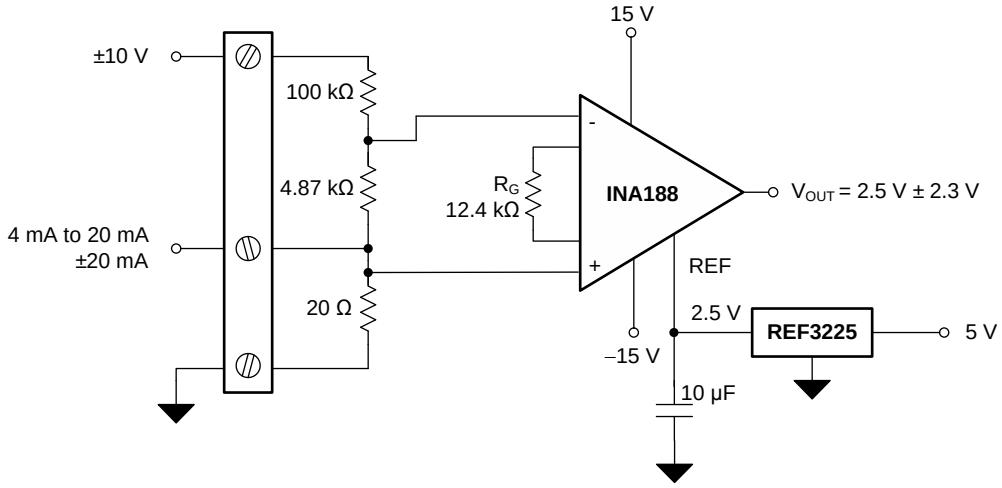


Figure 55. PLC Input (±10 V, 4 mA to 20 mA)

8.2.1 Design Requirements

For this application, the design requirements are:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

Typical Application (continued)

8.2.2 Detailed Design Procedure

The following steps must be applied for proper device functionality:

- For a 4-mA to 20-mA input, the maximum burden of 0.4 V must have a burden resistor equal to 0.4 / 0.02 = 20 Ω.
- To center the output within the 0-V to 5-V range, V_{REF} must equal 2.5 V.
- To keep the ±20-mA input linear within 0 V to 5 V, the gain resistor (R_G) must be 12.4 kΩ.
- To keep the ±10-V input within the 0-V to 5-V range, attenuation must be greater than 0.05.
- A 100-kΩ resistor in series with a 4.87-kΩ resistor provides 0.0466 attenuation of ±10 V, well within the ±2.5-V linear limits.

8.2.3 Application Curve

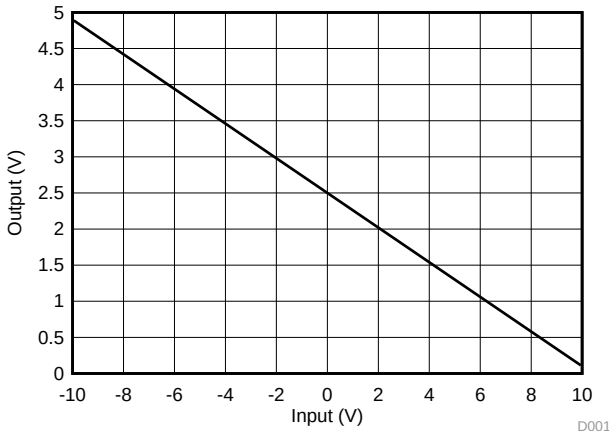


Figure 56. Plot of PLC Input Transfer Function

9 Power Supply Recommendations

The minimum power-supply voltage for the INA188 is ±2 V and the maximum power-supply voltage is ±18 V. This minimum and maximum range covers a wide range of power supplies. However, for optimum performance, ±15 V is recommended. A 0.1-µF bypass capacitor is recommended to be added at the input to compensate for the layout and power-supply source impedance.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Care must be taken to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 57, keeping R_G close to the pins minimizes parasitic capacitance.
- Keep the traces as short as possible.

10.2 Layout Example

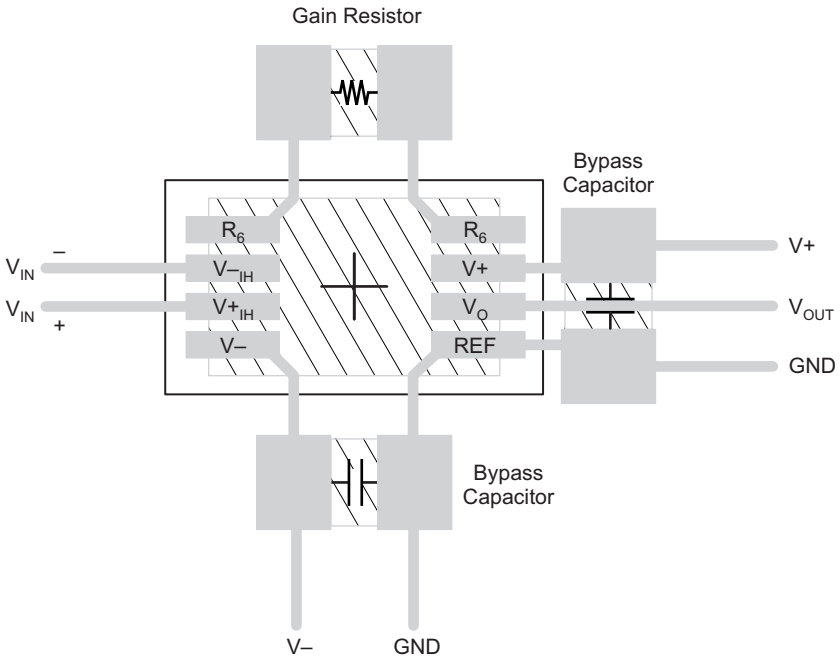


Figure 57. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Table 4. Table 1. Design Kits and Evaluation Modules

NAME	PART NUMBER	TYPE
DIP Adapter Evaluation Module	DIP-ADAPTER-EVM	Evaluation Module and Boards
Universal Instrumentation Amplifier Evaluation Module	INAEVM	Evaluation Module and Boards

Table 5. Table 2. Development Tools

NAME	PART NUMBER	TYPE
Calculate Input Common-Mode Range of Instrumentation Amplifiers	INA-CMV-CALC	Calculation Tools
SPICE-Based Analog Simulation Program	TINA-TI	Circuit Design and Simulation

11.2 Documentation Support

11.2.1 Related Documentation

OPA188 Data Sheet, SBOS642

OPA330 Data Sheet, SBOS432

REF3225 Data Sheet, SBVS058

Circuit Board Layout Techniques, SLOA089

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
PhotoMOS is a registered trademark of Panasonic Electric Works Europe AG.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA188ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA188	Samples
INA188IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA188	Samples
INA188IDRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

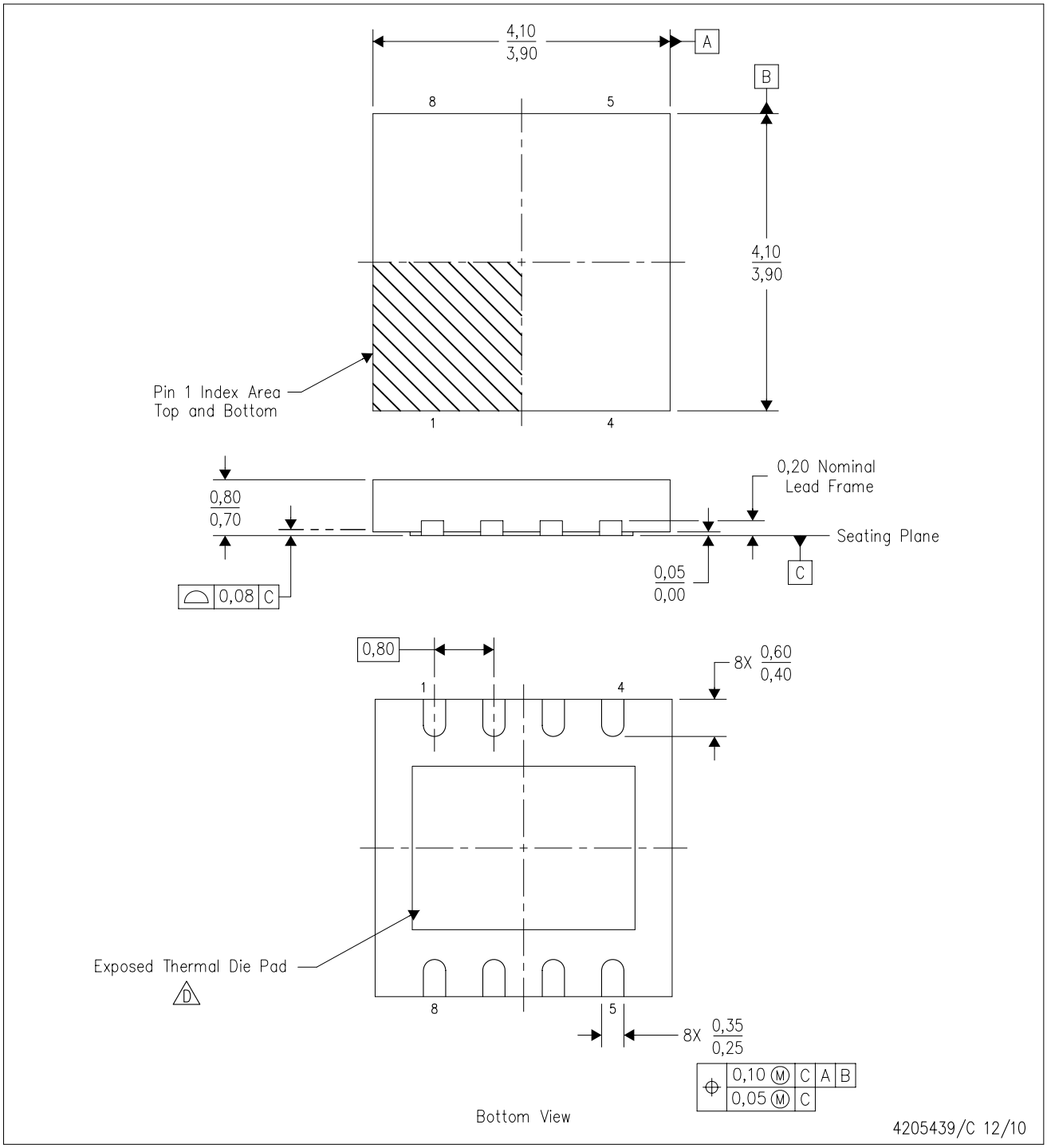
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

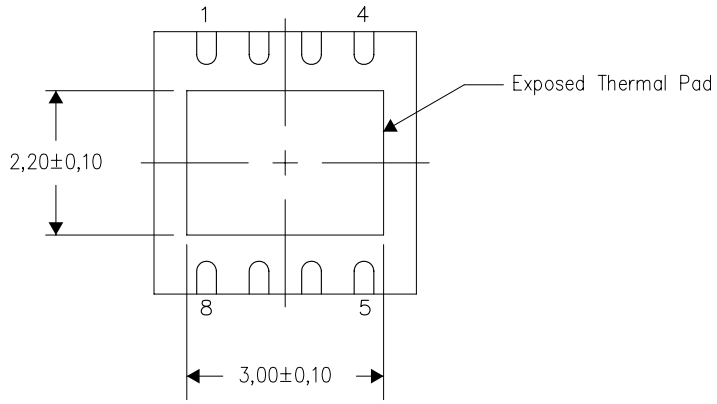
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



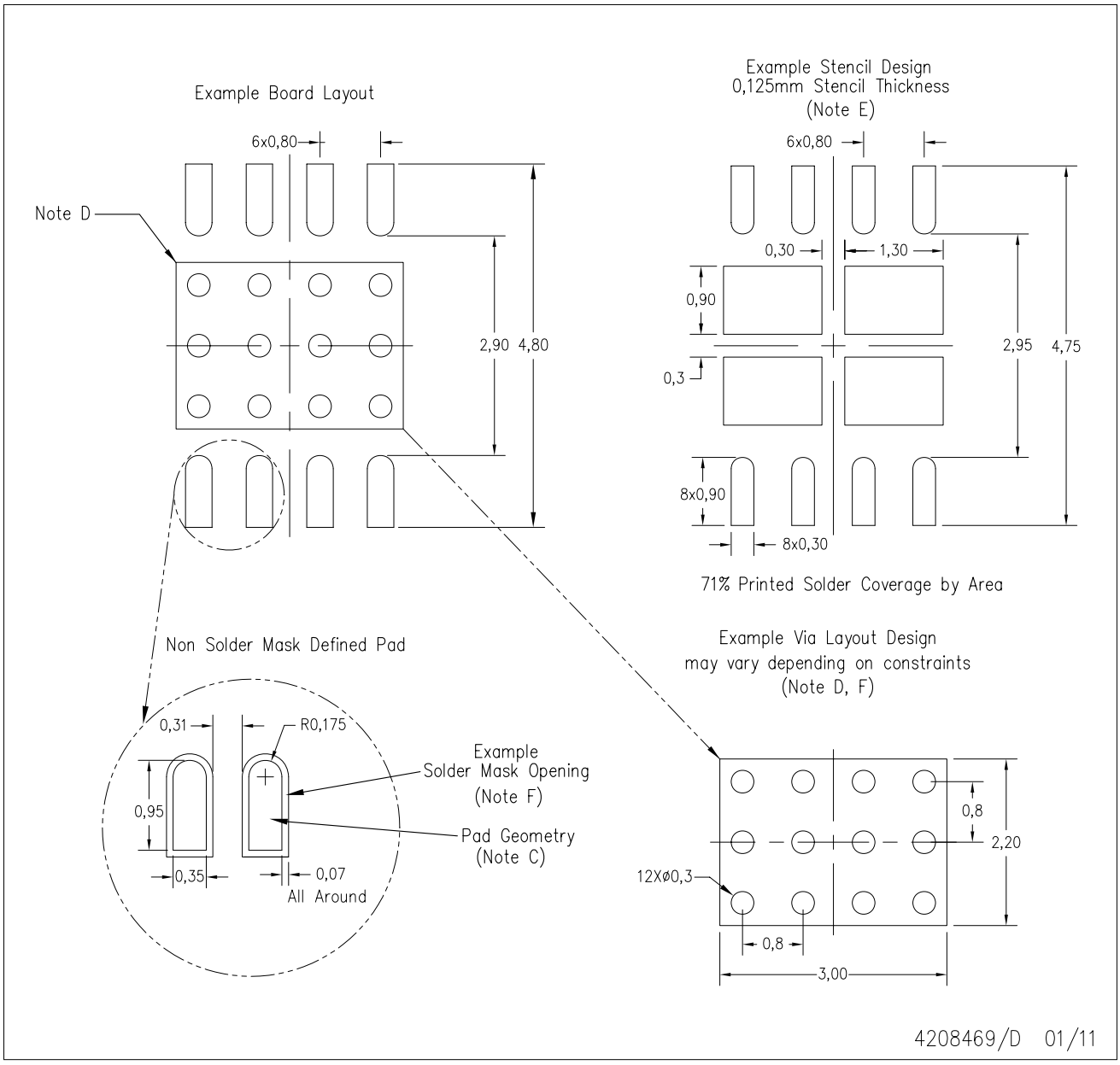
Bottom View

Exposed Thermal Pad Dimensions

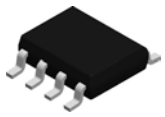
4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

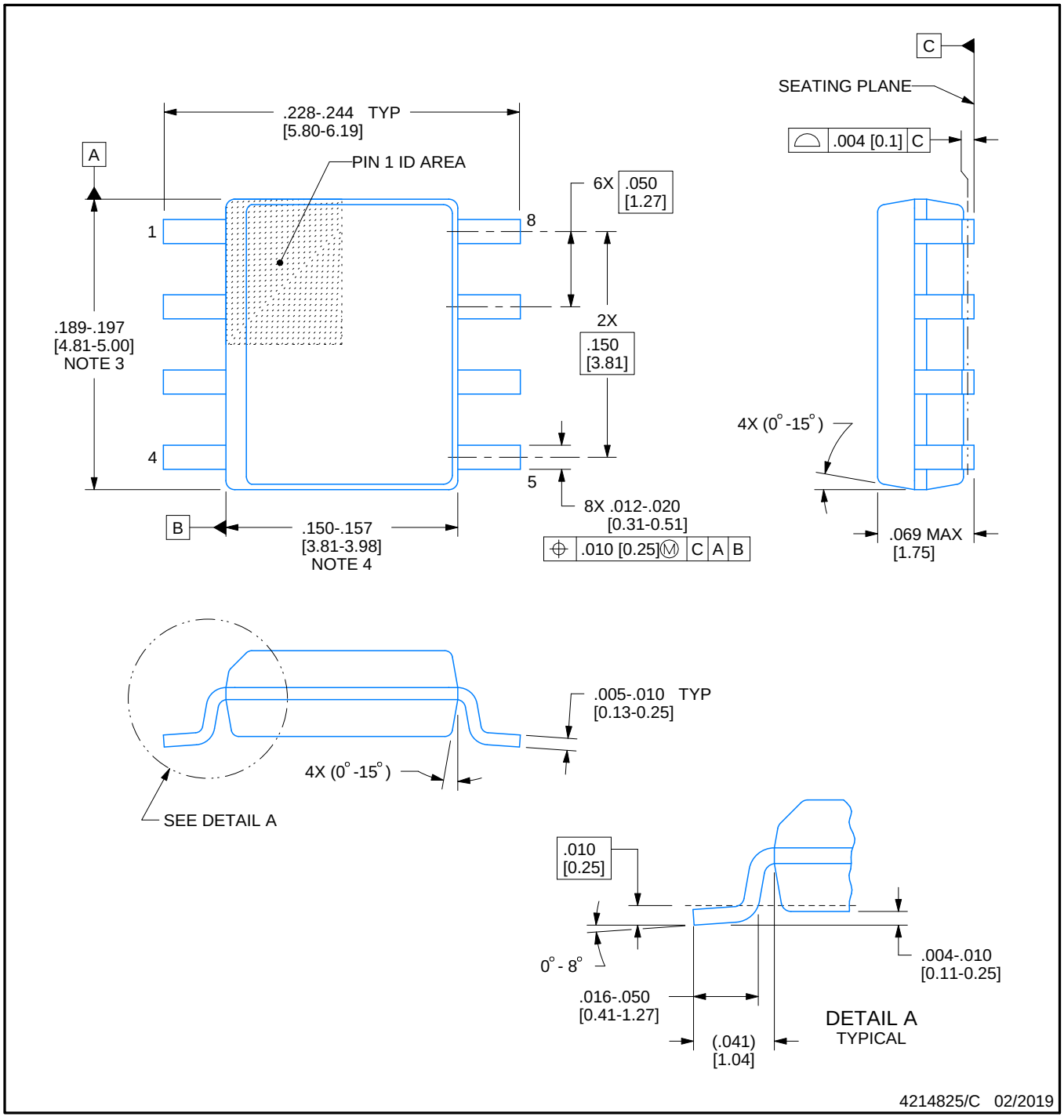


PACKAGE OUTLINE

D0008A

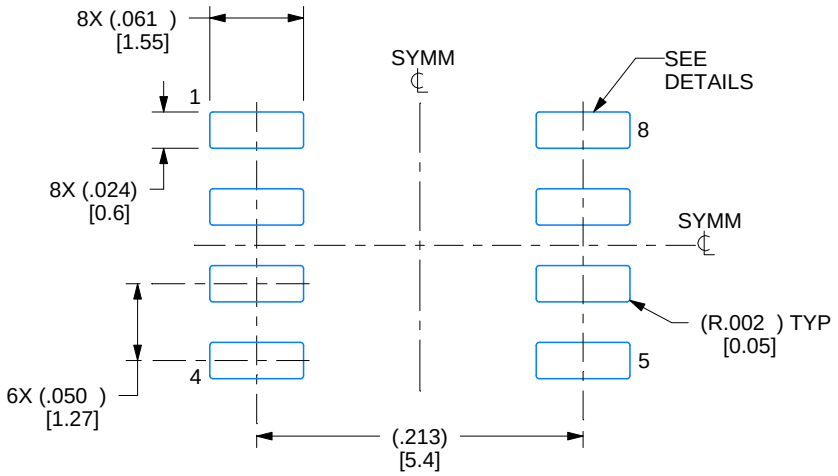
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

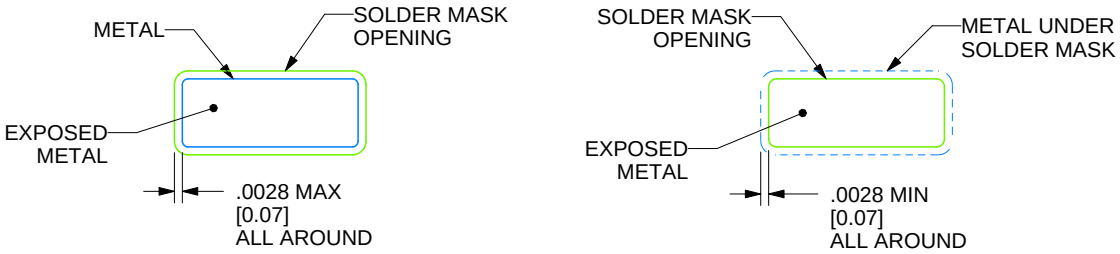


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

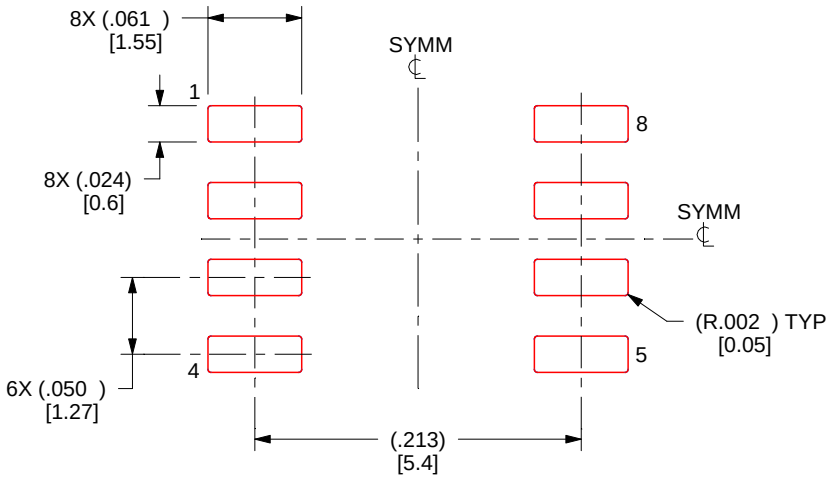
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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