

Migrating From the MSP430F2xx Family to the MSP430FR57xx Family

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ABSTRACT

This application report enables easy migration from MSP430F2xx Flash-based MCUs to the MSP430FR57xx family FRAM-based MCU. It covers programming, system, and peripheral considerations when migrating firmware. The purpose is to highlight differences between the two families. For more information on the usage of the MSP430FR57xx features, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)). Although the MSP430F2xx family is used as an example, similar considerations apply when migrating from MSP430F1xx/4xx families as well.

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1 Introduction

The purpose of this document is to highlight the key differences between the F2xx family and the FR57xx family to ensure a smooth migration. It is divided into:

- System-level considerations such as power management
- Changes when handling non-volatile memory
- Peripheral modifications

With respect to the instruction set, the MSP430FR57xx family is completely code compatible with all other MSP430™ families. The code migration is impacted only by register or peripheral feature changes; the instruction set remains the same.

2 In-System Programming of Non-Volatile Memory

2.1 Ferro-electric RAM (FRAM) Overview

Ferro-electric RAM (FRAM) is non-volatile memory that behaves and feels very similar to static RAM (SRAM); however, there are two significant differences.

- FRAM retains content on loss of power.
- The FRAM on the FR57xx device is limited to an access speed of 8 MHz.

In comparison to Flash memory, FRAM:

- Is very easy to program
- Requires no additional setup and preparation
- Memory is not segmented and each bit is individually erasable, writable, and addressable
- Does not require an erase before a write
- Allows low-power write accesses (does not require a charge pump)
- Can be written across the full voltage range (2.0 V-3.6 V) of the FR57xx device
- Can be written to at speeds > 8 MBps (maximum Flash write speed is ~14 kBps)
- Uses wait-states when accessed at speeds > 8 MHz

A single FRAM cell can be considered a dipole capacitor that consists of a film of ferroelectric material (ferroelectric crystal) between two electrode plates [1]. Storing a '1' or '0' (writing to FRAM) simply requires polarizing the crystal in a specific direction using an electric field. This makes FRAM very fast, easy to write to and capable of meeting high-endurance requirements. Reading from FRAM requires applying an electric field across the capacitor similar to a write. Depending on the state of the crystal, it may get re-polarized thereby emitting a large induced charge. This charge is then compared to a known reference to estimate the state of the crystal. The stored data bit '1' or '0' is inferred from the induced charge. In the process of reading the data, the crystal that is polarized in the direction of the applied field loses its current state. Therefore, every read needs to be accompanied by a write-back to restore the state of the memory location. In the MSP430FR57xx family, this is inherent to the nature of the FRAM memory and is completely transparent to the end user.

The FRAM controller also implements a safe write-back feature that allows the current read/write cycle to complete safely in the event of a power loss ensuring that there is no code corruption. This is accomplished by the FRAM low dropout (LDO) voltage regulator, which is internal to the chip and provides sufficient charge to complete the current write operation.

To the user, the experience of reading/writing to FRAM is the same as writing to RAM, simple and easy to use.

2.2 Protecting FRAM using the Memory Protection Unit

Since FRAM is very easy to re-program, it also makes it easy for erroneous code execution to overwrite application code unintentionally, just as it would if executing from RAM. In order to prevent this, a memory protection unit (MPU) is provided. It is recommended to setup boundaries between code and data memory to increase code security and protect against accidental writes/erasures. The MPU allows users to separate blocks of FRAM and assign unique privileges to each block based on the application's requirement. For example, if a memory block is assigned *read only* status, any write access to that block flags an error. This is useful for storing constant data or application code that is not expected to change over the device lifetime. For code examples on how to configure the MPU, the [MSP430FR5739](#) product folder or *MSP430FR573x, MSP430FR572x C Code Examples (IAR and CCS)* ([SLAC491](#)).

3 System Level Considerations

3.1 Power Management Module

The MSP430F2xx family of devices use a single voltage rail to power the chip, therefore, a single power rail supplies both the analog peripherals and the digital core on the chip. The MSP430FR57xx family, in keeping consistency with other F5xx family members, uses a split voltage supply. The external voltage supply on the DV_{CC} pin is fed to an internal low-dropout voltage regulator that supplies the CPU, memories, and digital modules while AV_{CC} supplies the I/O and analog modules (see Figure 1). However, unlike other F5xx family devices, the core voltage on FR57xx devices is pre-configured to a specific core setting (not user-configurable).

The power management module (PMM) manages all functions related to the core voltage and its supervision. Its primary functions are first to generate a supply voltage for the core logic, and second, to provide several mechanisms for the supervision of both the voltage supplied to the device (V_{CC}) and the voltage generated for the core (V_{CORE}).

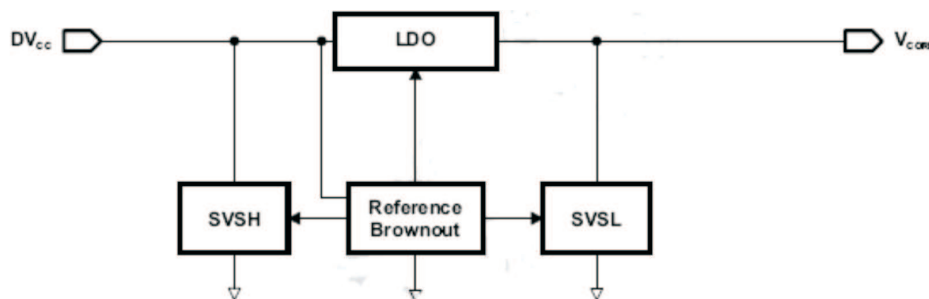


Figure 1. PMM Block Diagram

Using a split supply is especially advantageous as it allows the core to operate at a lower voltage, thereby, bringing significant power savings. It also ensures that the core receives a stable, regulated voltage over a wide supply range.

Since supply voltage supervision is an important aspect of providing a stable supply or a notification in case of power fail, the FR57xx supports two blocks: SVS high side (SVSH) and SVS low side (SVSL). SVSH handles the supervision of the external chip supply (V_{CC}) and SVSL supervises the core voltage (V_{CORE}).

The SVS function in the FR57xx PMM module is more flexible than the SVS module in the F2xx family because it provides the ability to either interrupt or reset the device in the case of a voltage-fail event. It is also responsible for holding the device in reset until the minimum V_{CC} is reached while the device is powering up.

Unlike the F2xx family, the SVS high side is automatically enabled in active and all low-power modes (except LPMx.5) by default. It cannot be turned off as it controls the device release from reset on a power-up and the device being placed in reset during a power down. The supervisor on the low side (SVSL) is kept on after a power cycle and when in active, LPM0 modes. It is turned off in LPM3 and LPM4 to conserve power. This is still a robust way to protect the device because it is expected that the core voltage is stable and regulated. Therefore, it is sufficient to monitor the high side during device operation.

When in debug mode, one of the main differences between the two families can be attributed to the PMM module. In the FR57xx family, the V_{CORE} regulator operates in two modes to conserve power: high performance (used in active LPM0/1) and low-power mode (LPM2/3/4). When the MSP430FR57xx device is in debug mode, it automatically forces the LDO to the high-performance mode regardless of the operating mode set by the application code. In an application, this might cause the device to behave differently than when operating in a stand-alone mode.

In conclusion, the main differences in power management between the F2xx and the FR57xx are summarized as:

- The FR57xx has a PMM module due to handling considerations required for a split supply.
- The SVS is now expanded to supervise both the rail voltage and the core voltage and can be configured to reset the device or provide an interrupt in a power fail event.

For most use cases the PMM can be left in its default state from power-up. For details on PMM configuration at power up, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

3.2 Clock System

The FR57xx clock system (CS) is similar to the F2xx basic clock system (BCS) in that it uses an internal digitally controlled oscillator (DCO) to provide pre-calibrated system clock frequencies.

The FR57xx also provides all of the same clock source options and system clocks as the F2xx family.

A significant difference with the FR57xx DCO is that it can be configured only to the factory provided calibrated frequencies and does not provide any in-between frequency steps that are possible with the F2xx DCO. [Table 1](#) shows a comparison.

While the MSP430FR57xx is capable of sourcing MCLK at frequencies up to 24 MHz, FRAM accesses are limited to 8 MHz automatically by the FRAM controller. Code execution from RAM, peripherals, DMA and accesses to peripherals and RAM can be carried out up to system frequencies of 24 MHz.

The internal digital oscillator of the ADC module in the F2xx family has been renamed MODOSC in the FR57xx family (similar to the F5xx family) and is not exclusive to the ADC module (used to generate system delays, timeouts, etc.).

The FR57xx CS supports a new feature termed *clocks-on-demand*. In the F2xx family, the availability of a system clock is impacted by entry into low-power modes. For example, SMCLK is turned off in LPM3; therefore, any peripheral such as a timer that uses SMCLK is inactive in LPM3. However, the FR57xx allows the LPM settings to be over-ridden by a clock request. As long as there is an active request for a clock from a peripheral, it remains ON, regardless of the LPM setting. The most visible effect is increased power consumption when porting code between families, and it is left to the user to disable any clock source requests that prevent the device from entering the required LPM. As an option, this feature can be disabled using the CSCCTL6 register (CLKREQEN bits). For more details, see the *Clock System* section in the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

Table 1. A Comparison Between FR57xx and F2xx Clock Systems

Parameter	FR57xx	F2xx
Max f_{SYSTEM}	24 MHz	16 MHz
DCO range	Calibrated frequencies only	0.06 MHz – 26 MHz
Production calibrated frequencies	5.33 MHz, 6.67 MHz, 8 MHz, 16 MHz, 20 MHz and 24 MHz	1 MHz, 8 MHz, 12 MHz and 16 MHz
Clocks on demand	Available	Not Available
Registers	CS0CTL-CS6CTL	DCOCTL, BCCTL1, BCCTL2, BCCTL3

The main differences in the clock system between the FR57xx and the F2xx families can be summarized as:

- The DCO can be configured to provide only six specific calibrated frequency settings; any clock sourced from the DCO is a factor of these frequencies.
- it is important to be aware of the clocks-on-demand feature and how it impacts your application when porting code to the FR57xx family.

3.3 Operating Mode, Wakeup and Reset

The various operating modes available in the two families and their features are compared in [Table 2](#).

Table 2. Comparison of Operating Modes

Parameter	FR57xx	F2xx
LPM0/1/2/3/4	Available	Available
LPM3.5	Available Wake up from Port, RTC interrupt	Not Available
LPM4.5	Available Wake up from Port interrupt	Not Available
Wakeup time from LPM0	2 μ s	2 μ s
Wakeup time from LPM1/2	20 μ s	2 μ s
Wakeup time from LPM3/4	100 μ s	2 μ s
Wakeup time from LPMx.5 and reset	500 μ s	Not Available

NOTE: The numbers presented in [Table 2](#) are an approximation. For actual numbers, see the device-specific data sheet.

The entry into LPM0-LPM4 remains the same in the FR57xx family as in the F2xx family. Two new low power modes introduced in the F5xx family and also present in the FR57xx family: LPM3.5 and LPM4.5. In both modes the V_{CORE} LDO is turned off, powering down the digital core, RAM, and peripherals. To wake up from LPM3.5, self-timed RTC interrupts or port interrupts are required; all other system interrupts are not available. Note that the RTC module on the FR57xx device is powered from the V_{CC} rail and can stay functional even when the core voltage is turned off. In LPM4.5, only port interrupts can wake up the device.

For more details on entry into and exit from these modes, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

One important difference between the families is the behavior on reset. There are multiple levels of reset across all MSP430 families such as PUC, POR and BOR. In the F2xx family, the program counter (PC) is reinitialized to the reset vector location on executing a PUC. In the case of a power cycle (POR), the PC is reinitialized once t_{DBOR} has elapsed. In the FR57xx family, the behavior on executing a PUC is the same as the F2xx family; that is, reinitialization of PC. A deeper level of reset such as POR or BOR, however, executes a boot code that is present in protected ROM. This boot code sets up the device and loads calibration settings that are essential to establish functionality. Therefore, in the FR57xx family, the time to start up from a POR/BOR may be longer than on an F2xx device. For start-up times, see the *MSP430FR573x, MSP430FR572x Mixed Signal Microcontroller Data Sheet* ([SLAS639](#)).

The FR57xx is also capable of initiating all levels of reset in software (in the F2xx family only a PUC was possible). This is done by setting the PMMSWBOR and PMMSWPOR bits in the PMM Control Register (PMMCTL0).

3.4 Interrupt Vectors

The MSP430FR57x uses an interrupt vector (IV) for any interrupt service routine that is sourced by multiple flags.

For example, in the F2xx family, the USCI TX interrupt sources the RX and TX interrupt flags and the USCI RX interrupt sources all the status flags. In the case of the FR57xx family, all these interrupt flags are captured using a single interrupt vector UCBxIV. This allows interrupt servicing to be more efficient and ensures a pre-defined latency when servicing the interrupts.

3.5 FRAM Controller

The MSP430 F2xx family Flash controller is replaced by the FRAM controller in the FR57xx family.

The FRAM controller uses a 2-way associative cache that has a 64-bit line size. The cache is a register file in static RAM that store pre-fetched instructions. For the remainder of this document, the term cache may be used interchangeably with static RAM or SRAM. The function of the FRAM controller is to pre-fetch four instruction words depending on the current PC location. The actual execution of these instructions is carried out in the cache. Once the end of the cache buffer is reached, the FRAM controller

preserves the four current words in one page of the cache and fetches the next four words. If a code discontinuity is encountered at the end of the second page of the cache, the cache is refreshed and the following four words of instruction are retrieved from FRAM. However, if at the end of the cache the application code loops back to a location already present in the cache, the relevant instruction is simply executed directly from the cache instead of re-fetching code from FRAM.

Note that only FRAM accesses are subject to the 8 MHz access limitation. When executing from SRAM, a system clock of up to 24 MHz can be used. Therefore, the cache is mostly useful in:

- Overcoming the 8 MHz limitation and increasing the system throughput
- Reducing overall active power by ensuring that most instructions are executed from SRAM

The cached execution of instructions in the FR57xx family is different from the F2xx family where instructions are directly executed from Flash with no pre-fetches or caching, providing a 1:1 relationship between MCLK and instruction execution. For example at MCLK = 16 MHz, 8 2-cycle instructions can be executed in 16 clocks. For the FR57xx family, this relationship is application-dependent. The 1:1 relationship holds true only up to MCLK = 8 MHz. For MCLK > 8 MHz, the number of inserted wait states (directly proportional to how many times FRAM is accessed) determines the MCLK to instruction execution ratio.

To provide another application example, with MCLK = 16 MHz a JMP \$ instruction (single cycle) is executed at the same rate in both families. This is because the FR57xx fetches this instruction and stores it in cache where it can be executed at the maximum MCLK speed. However, a loop that has more than four instruction words would require accessing the FRAM every time a cache refresh is needed. These FRAM accesses take place at MCLK/2 (that is, 8 MHz), which reduces the overall throughput of the system when compared to an F2xx device.

NOTE: The system speed and active power is directly impacted by the compiler optimization settings due to the caching mechanism. When using an FR57xx family device, always ensure that the compiler optimization setting is at least one level higher than the default. Increasing the optimization level ensures that register access is maximized and direct memory access (to FRAM) is reduced, which significantly improves system speed and power.

3.6 SYS Module

The MSP430FR57xx family of devices includes a SYS module that is useful in mapping reset sources. In the F2xx family, reset source flags such as WDT, Flash ACCVIFG, etc., are present in different registers requiring checks of multiple registers to determine the cause of reset. With the SYS module, the Reset Interrupt Vector Register (SYSRSTIV) can be accessed to determine the exact cause of reset as all system reset flags are reflected in this register. For a complete listing of all reset sources that map to the SYSRSTIV register, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

3.7 Useful Information on the FR57xx Family

This section includes miscellaneous useful tips when porting firmware between the families.

- The FR57xx device has the ability to activate an internal pull up on the reset line eliminating the need for an external reset resistor. For more details, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).
- The JTAG lock mechanism is now in software and does not require a high voltage physical fuse blow like the F2xx family. For more details, see the *JTAG Lock Mechanism via the Electronic Fuse* section in the *MSP430FR57xx Family User's Guide* ([SLAU272](#)). Also the JTAG can be optionally locked with a password stored in FRAM. A secure access from the tool chain is possible by providing this password, which eliminates the need to use the BSL while still securing JTAG access.
- The BSL is functionally similar to the F5xx family UART BSL, but is stored in protected ROM instead of Flash BSL.
- The TLV structure contains a unique die ID that is programmed at production for every device that can be used to serialize end products.

4 Peripheral Considerations

Some of the peripherals in the FR57xx family have new features or existing features that are implemented in a slightly different way. This section highlights the peripheral differences.

4.1 Watchdog Timer

With reference to the watchdog timer, the main difference between the two families lies in the fail-safe operation.

In the F2xx family, WDT is typically timed by ACLK, which is sourced by a crystal. If crystal failure occurs, WDT defaults to MCLK. If MCLK is also sourced by a crystal, the DCO is automatically activated.

In the FR57xx family, the WDT fail-safe defaults to VLO instead of the DCO.

4.2 Digital Input/Output

The main improvements in the FR57xx family, the general-purpose input/output (GPIO) pins are highlighted below:

- All GPIOs have internal, configurable pullup and pulldown resistors
- P3 and P4 ports are also interruptible (only P1, P2 in the 'F2xx family)
- JTAG functionality is multiplexed with GPIO pins on Port J

4.3 ADC10_B

The ADC10_B module in the FR57xx has been redesigned for lower power and also includes some new features. Some of the significant differences are:

- The ADC internal reference is no longer a part of the ADC module. For details on how to configure and use the reference, see the *REF Module* section in the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).
- The data transfer controller (DTC), that is used for automatic storage of conversion results in the F2xx family, has been replaced by the DMA in the FR57xx family.
- Up to 12 input channels are available externally
- The newly added window comparator allows the ADC module to provide interrupts only when specific thresholds have been reached
- An interrupt vector register with six interrupt flag sources including three from the window comparator function
- Increased options for controlling the sampling rate and the clock dividers
- ADC12OSC renamed to MODOSC in the FR57xx family

Some of the register names have changed to include the added functionality. For more information when porting firmware, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

4.4 Comparator (COMP_D)

The main differences between families with the COMP_D module are highlighted below:

- The Comp_D module connects the comparator output internally to the timer capture making it useful for applications such as cap-touch to measure the charge and discharge time of a capacitor without external connections.
- The comparator internal reference is sourced by the REF module.
- The internal voltage reference can be routed externally on a comparator pin
- The RC filter delay is selectable in software

Some of the register names have changed to include the added functionality. For more information when porting firmware, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

4.5 Enhanced Universal Serial Communication Interface (eUSCI)

A separate document is available that describes the changes necessary when migrating to the eUSCI module: *Migrating from the USCI Module to the eUSCI Module* ([SLAA522](#)).

5 Conclusion

This report addresses many of the key feature changes and new modules in the MSP430FR57xx family. While it was intended to be comprehensive, there may be a few minor differences between the F2xx and the FR57xx families that may not have been covered here. For details specific to a device, the device-specific datasheet is always the best source of information. For module functionality and usage, see the *MSP430FR57xx Family User's Guide* ([SLAU272](#)).

6 References

1. FRAM Technology Backgrounder – *An Overview of FRAM Technology Source*:
<http://www.ramtron.com>
2. *MSP430FR57xx Family User's Guide* ([SLAU272](#))
3. *MSP430x2xx Family User's Guide* ([SLAU144](#))
4. *MSP430F22x2, MSP430F22x4 Mixed Signal Microcontroller* data sheet ([SLAS504](#))
5. *MSP430FR573x, MSP430FR572x Mixed Signal Microcontroller* data sheet ([SLAS639](#))
6. SMBus Protocol Specification: <http://smbus.org/>
7. *Maximizing FRAM Write Speed on the MSP430FR5739* ([SLAA498](#))

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