Chapter 1

SLAU409F–August 2012–Revised March 2018

LCD_B Controller

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The most current version of the full user's guide is available here: http://www.ti.com/lit/pdf/slau208

The LCD_B controller drives static, 2-mux, 3-mux, or 4-mux LCDs. This chapter describes the LCD_B controller.

Topic **Page**

1.1 LCD_B Controller Introduction

The LCD_B controller directly drives LCD displays by creating the ac segment and common voltage signals automatically. The LCD_B controller can support static, 2-mux, 3-mux, and 4-mux LCD glasses.

The LCD_B controller features are:

- Display memory
- Automatic signal generation
- Configurable frame frequency
- Blinking of individual segments with separate blinking memory
- Regulated charge pump
- Contrast control by software
- Support for four types of LCDs
  - Static
  - 2-mux, 1/2 bias or 1/3 bias
  - 3-mux, 1/2 bias or 1/3 bias
  - 4-mux, 1/2 bias or 1/3 bias

The LCD_B controller block diagram for a configuration with a maximum of 160 segments is shown in Figure 1-1.

NOTE: Maximum LCD Segment Control

The maximum number of segment lines and memory registers available differs with device. See the device-specific data sheet for available segment pins and the maximum number of segments supported.

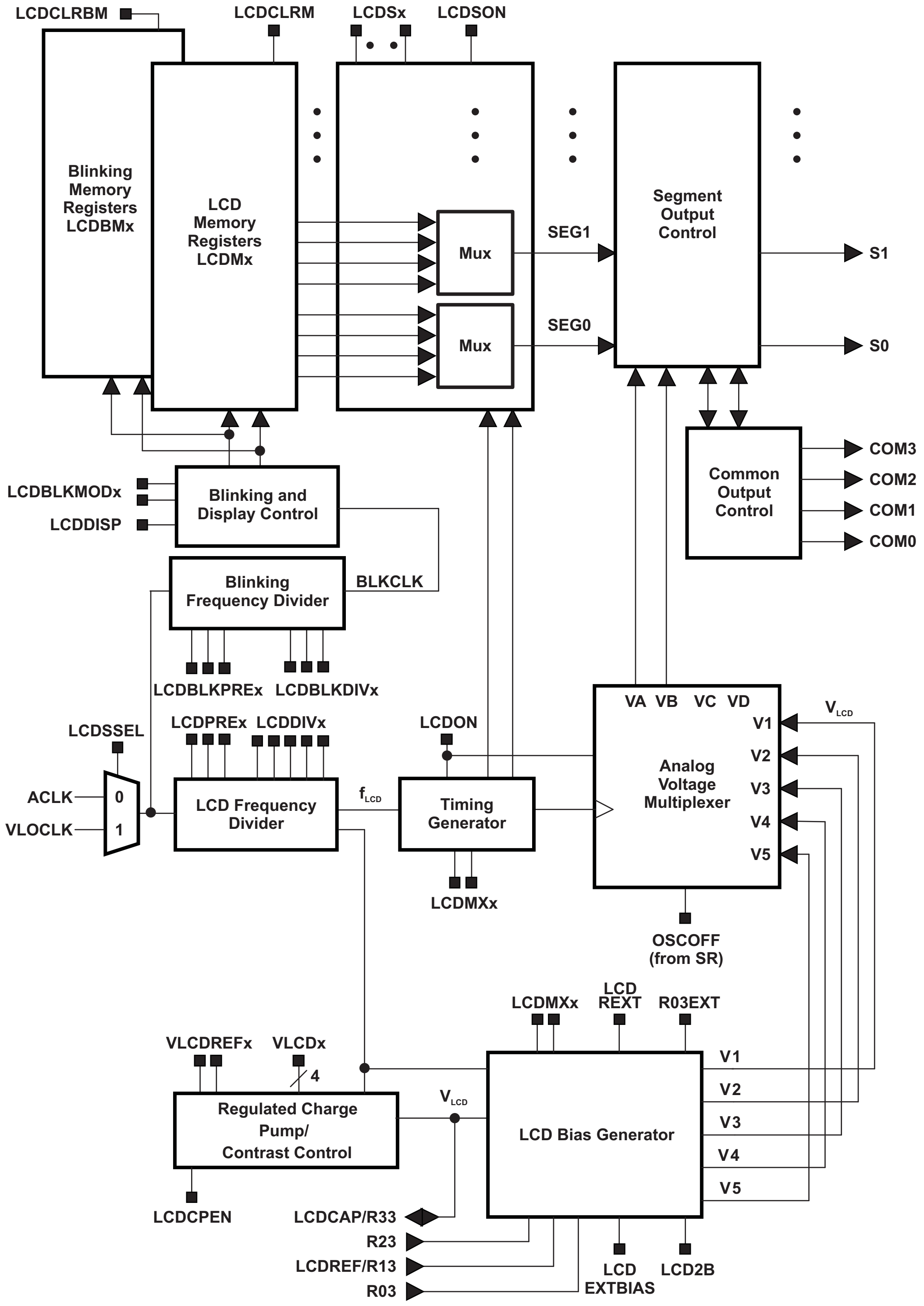


Figure 1-1. LCD_B Controller Block Diagram

1.2 LCD_B Controller Operation

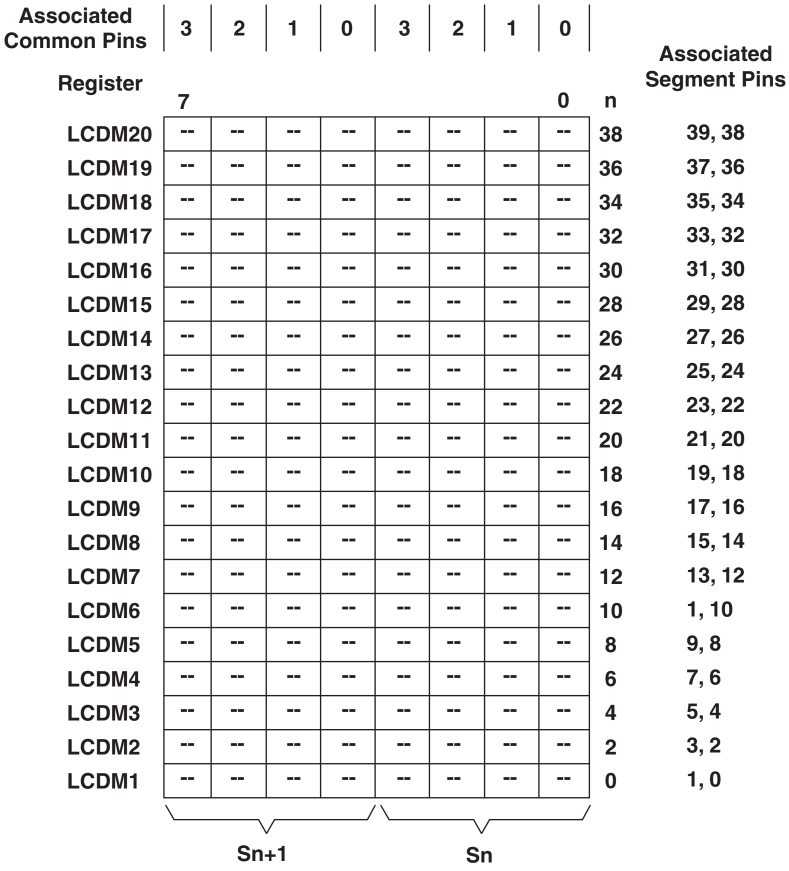
The LCD_B controller is configured with user software. The setup and operation of the LCD_B controller is discussed in the following sections.

1.2.1 LCD Memory

The LCD memory map for a device with a 160-segment maximum is shown in Figure 1-2. Each memory bit corresponds to one LCD segment or is not used, depending on the mode. To turn on an LCD segment, its corresponding memory bit is set.

The memory can also be accessed word-wise using the even addresses starting at LCDM1, LCDM3, etc.

Setting the bit LCDCLRM clears all LCD memory registers at the next frame boundary. It is reset automatically after the registers are cleared.



Associated Common Pins	3	2	1	0	3	2	1	0		Associated Segment Pins
Register	7							0	n	
LCDM20	--	--	--	--	--	--	--	--	38	39, 38
LCDM19	--	--	--	--	--	--	--	--	36	37, 36
LCDM18	--	--	--	--	--	--	--	--	34	35, 34
LCDM17	--	--	--	--	--	--	--	--	32	33, 32
LCDM16	--	--	--	--	--	--	--	--	30	31, 30
LCDM15	--	--	--	--	--	--	--	--	28	29, 28
LCDM14	--	--	--	--	--	--	--	--	26	27, 26
LCDM13	--	--	--	--	--	--	--	--	24	25, 24
LCDM12	--	--	--	--	--	--	--	--	22	23, 22
LCDM11	--	--	--	--	--	--	--	--	20	21, 20
LCDM10	--	--	--	--	--	--	--	--	18	19, 18
LCDM9	--	--	--	--	--	--	--	--	16	17, 16
LCDM8	--	--	--	--	--	--	--	--	14	15, 14
LCDM7	--	--	--	--	--	--	--	--	12	13, 12
LCDM6	--	--	--	--	--	--	--	--	10	1, 10
LCDM5	--	--	--	--	--	--	--	--	8	9, 8
LCDM4	--	--	--	--	--	--	--	--	6	7, 6
LCDM3	--	--	--	--	--	--	--	--	4	5, 4
LCDM2	--	--	--	--	--	--	--	--	2	3, 2
LCDM1	--	--	--	--	--	--	--	--	0	1, 0

Figure 1-2. LCD Memory - Example for 160 Segments Maximum

1.2.2 LCD Timing Generation

The LCD_B controller uses the f_{LCD} signal from the integrated clock divider to generate the timing for common and segment lines. With the LCDSSEL bit ACLK with a frequency between 30 kHz and 40 kHz or VLOCLK can be selected as clock source into the divider. The f_{LCD} frequency is selected with the LCDPREx and LCDDIVx bits. The resulting f_{LCD} frequency is calculated by:

$$f_{LCD} = \frac{f_{ACLK/VLOCLK}}{(LCDDIVx + 1) \times 2^{LCDPRE}}$$

The proper f_{LCD} frequency depends on the LCD's requirement for framing frequency and the LCD multiplex rate and is calculated by:

$$f_{LCD} = 2 \times mux \times f_{Frame}$$

For example, to calculate f_{LCD} for a 3-mux LCD, with a frame frequency of 30 Hz to 100 Hz:

f_{Frame} (from LCD data sheet) = 30 Hz to 100 Hz
$f_{LCD} = 2 \times 3 \times f_{Frame}$
$f_{LCD}(min) = 180$ Hz
$f_{LCD}(max) = 600$ Hz

With $f_{ACLK/VLOCLK}$ = 32768 Hz, LCDPREx = 011, and LCDDIVx = 10101:

$f_{LCD} = 32768 \text{ Hz} / ((21+1) \times 2^3) = 32768 \text{ Hz} / 176 = 186 \text{ Hz}$

With LCDPREx = 001 and LCDDIVx = 11011:

$f_{LCD} = 32768 \text{ Hz} / ((27+1) \times 2^1) = 32768 \text{ Hz} / 56 = 585 \text{ Hz}$

The lowest frequency has the lowest current consumption. The highest frequency has the least flicker.

1.2.3 Blanking the LCD

The LCD controller allows to blank the complete LCD. The LCDSON bit is ANDed with each segment's memory bit. When LCDSON = 1, each segment is on or off according to its bit value. When LCDSON = 0, each LCD segment is off.

1.2.4 LCD Blinking

The LCD_B controller also supports blinking. The blinking mode LCDBLKMODx = 01 allows to blink individual segments, with LCDBLKMODx = 10 all segments are blinking, and with LCDBLKMODx = 00 blinking is disabled.

1.2.4.1 Blinking Memory

To enable individual segments for blinking the corresponding bit in the blinking memory LCDBMx registers needs to be set. The memory uses the same structure as the LCD memory shown in Figure 1-2. Each memory bit corresponds to one LCD segment, or is not used, depending on the multiplexing mode LCDMXx. To enable blinking for a LCD segment, its corresponding memory bit is set.

The blinking memory can also be accessed word-wise using the even addresses starting at LCDBM1, LCDBM3, etc.

Setting the bit LCDCLRBM clears all blinking memory registers at the next frame boundary. It is automatically reset after the registers are cleared.

1.2.4.2 Blinking Frequency

The blinking frequency f_{BLINK} is selected with the LCDBLKPREx and LCDBLKDIVx bits. The same clock is used as selected for the LCD frequency f_{LCD}. The resulting f_{BLINK} frequency is calculated by:

$$f_{Blink} = \frac{f_{ACLK/VLO}}{(\text{LCDBLKDIVx} + 1) \times 2^{9+\text{LCDBLKPREx}}}$$

The divider generating the blinking frequency f_{BLINK} is reset while LCDBLKMODx = 00. After a blinking mode LCDBLKMODx = 01 or 10 is selected, the enabled segments or all segments go blank at the next frame boundary and stay off for half a BLKCLK period. Then they go active at the next frame boundary and stay on for another half BLKCLK period before they go blank again at a frame boundary.

NOTE: Blinking Frequency Restrictions

The blinking frequency must be smaller than the frame frequency, f_{Frame}.

The blinking frequency should be changed only when LCDBLKMODx = 00.

1.2.4.3 Dual Display Memory

The blinking memory can also be used as a secondary display memory when no blinking mode LCDBLKMODx = 01 or 10 is selected. The memory to be displayed can be selected either manually using the LCDDISP bit or automatically with LCDBLKMODx = 11.

With LCDDISP = 0 the LCD memory is selected, with LCDDISP = 1 the blinking memory is selected as display memory. Switching between the memories is synchronized to the frame boundaries.

With LCDBLKMODx = 11 the LCD controller switches automatically between the memories using the divider to generate the blinking frequency. After LCDBLKMODx = 11 is selected the memory to be displayed for the first half a BLKCLK period is the LCD memory. In the second half the blinking memory is used as display memory. Switching between the memories is synchronized to the frame boundaries.

1.2.5 LCD_B Voltage And Bias Generation

The LCD_B module allows selectable sources for the peak output waveform voltage, V1, as well as the fractional LCD biasing voltages V2 to V5. V_{LCD} may be sourced from V_{CC}, an internal charge pump, or externally.

All internal voltage generation is disabled if the selected clock source (ACLK or VLOCLK) is turned off (OSCOFF = 1) or the LCD_B module is disabled (LCDON = 0).

1.2.5.1 LCD Voltage Selection

V_{LCD} is sourced from V_{CC} when VLCDEXT = 0, VLCDx = 0, and VREFx = 0. V_{LCD} is sourced from the internal charge pump when VLCDEXT = 0, VLCDCPEN = 1, and VLCDx > 0. The charge pump is always sourced from DV_{CC}. The VLCDx bits provide a software selectable LCD voltage from 2.6 V to 3.44 V (typical) independent of DV_{CC}. See the device-specific data sheet for specifications.

When the internal charge pump is used, a 4.7-µF or larger capacitor must be connected between pin LCDCAP and ground. If no capacitor is connected and the charge pump is enabled, the LCDNOCAPIFG interrupt flag is set, and the charge pump is disabled to prevent damage to the device. The charge pump may be temporarily disabled by setting LCDCPEN = 0 with VLCDx > 0 to reduce system noise, or it can be automatically disabled during certain periods by setting the corresponding bits in the LCDBCPCTL register. In this case, the voltage present at the external capacitor is used for the LCD voltages until the charge pump is re-enabled.

NOTE: Capacitor Required For Internal Charge Pump

A 4.7-µF or larger capacitor must be connected from pin LCDCAP to ground when the internal charge pump is enabled. If no capacitor is connected, the LCDNOCAPIFG interrupt flag is set and the charge pump is disabled.

The internal charge pump may use an external reference voltage when VLCDREFx = 01 (and LCDREXT = 0 and LCDEXTBIAS = 0). In this case, the charge pump voltage is set to a multiply of the external reference voltage according to the VLCDx bits setting.

When VLCDEXT = 1, V_{LCD} is sourced externally from the LCDCAP, pin and the internal charge pump is disabled.

1.2.5.2 LCD Bias Generation

The fractional LCD biasing voltages, V2 to V5 can be generated internally or externally, independent of the source for V_{LCD}. The LCD bias generation block diagram is shown in Figure 1-3.

The internally generated bias voltages V2 to V4 are switched to external pins with LCDREXT = 1.

To source the bias voltages V2 to V4 externally, LCDEXTBIAS is set. This also disables the internal bias generation. Typically, an equally weighted resistor divider is used with resistors ranging from a few kΩ to 1 MΩ, depending on the size of the display. When using an external resistor divider, the V_{LCD} voltage may be sourced from the internal charge pump when VLCDEXT = 0 taking the maximum charge pump load current into account. V5 can also be sourced externally when R03EXT is set to control the contrast of the connected display by changing the voltage at the low end of the external resistor divider as shown in the left part of Figure 1-3.

When using an external resistor divider R33 may serve as a switched V_{LCD} output when VLCDEXT = 0. This allows the power to the resistor ladder to be turned off, eliminating current consumption when the LCD is not used. When VLCDEXT = 1, R33 serves as a V_{LCD} input.

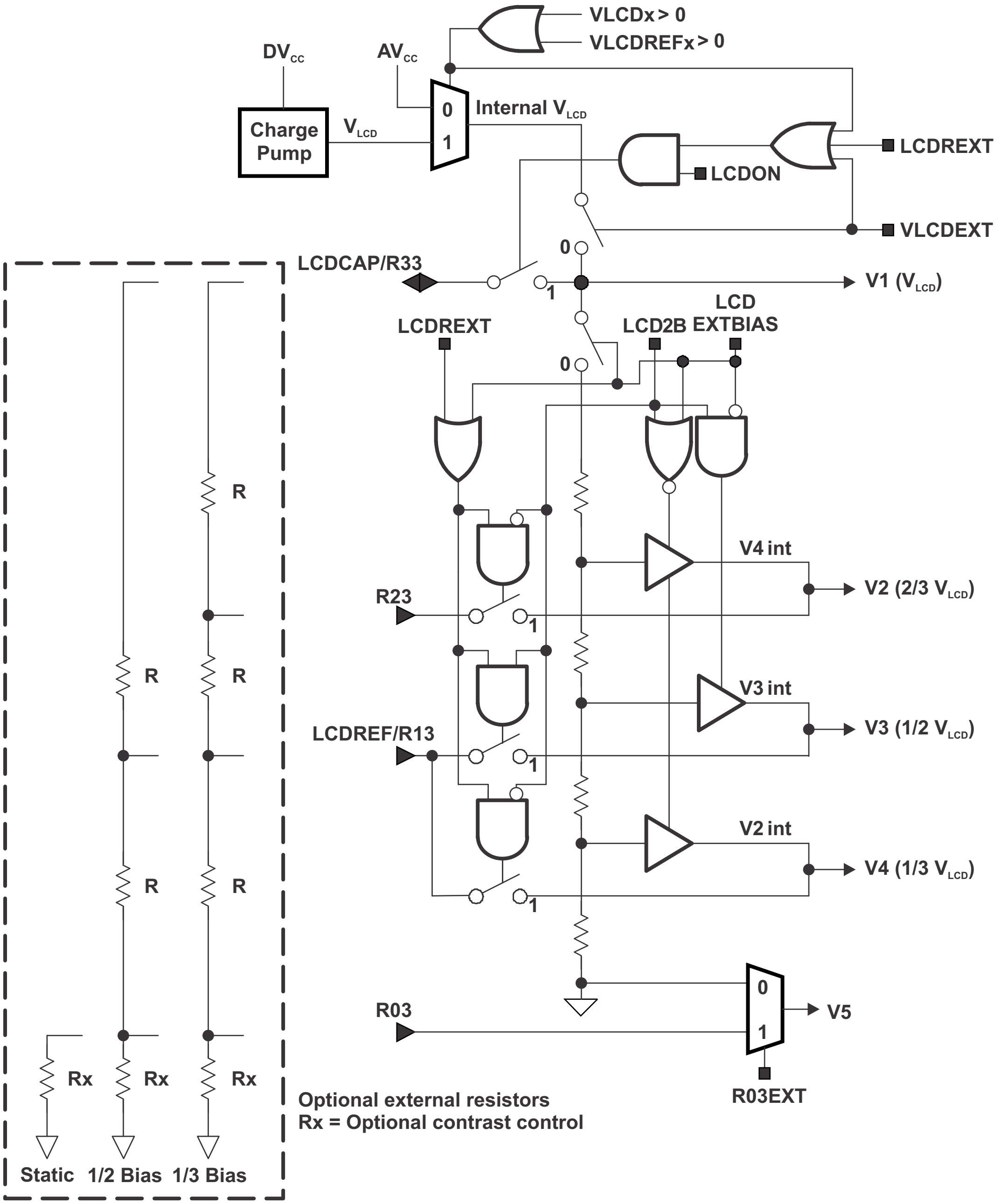


Figure 1-3. Bias Generation

The internal bias generator supports 1/2 bias LCDs when LCD2B = 1, and 1/3 bias LCDs when LCD2B = 0 in 2-mux, 3-mux, and 4-mux modes. In static mode, the internal divider is disabled.

Some devices share the LCDCAP, R33, and R23 functions. In this case, the charge pump cannot be used together with an external resistor divider with 1/3 biasing. When R03 is not available externally, V5 is always V_{SS}.

1.2.5.3 LCD Contrast Control

The peak voltage of the output waveforms together with the selected mode and biasing determine the contrast and the contrast ratio of the LCD. The LCD contrast can be controlled in software by adjusting the LCD voltage generated by the integrated charge pump using the VLCDx settings.

The contrast ratio depends on the used LCD display and the selected biasing scheme. Table 1-1 shows the biasing configurations that apply to the different modes together with the RMS voltages for the segments turned on ($V_{RMS,ON}$) and turned off ($V_{RMS,OFF}$) as functions of V_{LCD}. It also shows the resulting contrast ratios between the on and off states.

Table 1-1. LCD Voltage and Biasing Characteristics

Mode	Bias Config	LCDMx	LCD2B	COM Lines	Voltage Levels	$V_{RMS,OFF}$/ V_{LCD}	$V_{RMS,ON}$/ V_{LCD}	Contrast Ratio $V_{RMS,ON}$/ $V_{RMS,OFF}$
Static	Static	0	X	1	V1, V5	0	1	1/0
2-mux	1/2	1	1	2	V1, V3, V5	0.354	0.791	2.236
2-mux	1/3	1	0	2	V1, V2, V4, V5	0.333	0.745	2.236
3-mux	1/2	10	1	3	V1, V3, V5	0.408	0.707	1.732
3-mux	1/3	10	0	3	V1, V2, V4, V5	0.333	0.638	1.915
4-mux	1/2	11	1	4	V1, V3, V5	0.433	0.661	1.528
4-mux	1/3	11	0	4	V1, V2, V4, V5	0.333	0.577	1.732

A typical approach to determine the required V_{LCD} is by equating $V_{RMS,OFF}$ with a defined LCD threshold voltage, typically when the LCD exhibits approximately 10% contrast ($V_{th,10\%}$): $V_{RMS,OFF} = V_{th,10\%}$. Using the values for $V_{RMS,OFF}/V_{LCD}$ provided in the table results in $V_{LCD} = V_{th,10\%}/(V_{RMS,OFF}/V_{LCD})$. In the static mode, a suitable choice is V_{LCD} greater or equal than 3 times $V_{th,10\%}$.

In 3-mux and 4-mux mode typically a 1/3 biasing is used but a 1/2 biasing scheme is also possible. The 1/2 bias reduces the contrast ratio but the advantage is a reduction of the required full-scale LCD voltage V_{LCD}.

1.2.6 LCD Outputs

Some LCD segment, common, and Rxx functions are multiplexed with digital I/O functions. These pins can function either as digital I/O or as LCD functions.

The LCD segment functions, when multiplexed with digital I/O, are selected using the LCDSx bits in the LCDBPCTLx registers. The LCDSx bits select the LCD function for each segment line. When LCDSx = 0, a multiplexed pin is set to digital I/O function. When LCDSx = 1, a multiplexed pin is selected as LCD function.

The pin functions for COMx and Rxx, when multiplexed with digital I/O, are selected as described in the port schematic section of the device-specific datasheet. The COM1 to COM3 pins are shared with segment lines. If these pins are required as COM pins due to the selected LCD multiplexing mode the COM functionality takes precedence over the segment function that can be selected for those pins with the LCDSx bits as for all other segment pins.

See the port schematic section of the device-specific data sheet for details on controlling the pin functionality.

NOTE: LCDSx Bits Do Not Affect Dedicated LCD Segment Pins

The LCDSx bits only affect pins with multiplexed LCD segment functions and digital I/O functions. Dedicated LCD segment pins are not affected by the LCDSx bits.

1.2.7 LCD_B Interrupts

The LCD_B module has four interrupt sources available, each with independent enables and flags.

The four interrupt flags, namely LCDFRMIFG, LCDBLKOFFIFG, LCDBLKONIFG, and LCDNOCAPIFG, are prioritized and combined to source a single interrupt vector. The interrupt vector register LCDBIV is used to determine which flag requested an interrupt.

The highest priority enabled interrupt generates a number in the LCDBIV register (see register description). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled LCD_B interrupts do not affect the LCDBIV value.

Any read access of the LCDBIV register automatically resets the highest pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt. A write access to the LCDBIV register automatically resets all pending interrupt flags. In addition, all flags can be cleared via software.

The LCDNOCAPIFG indicates that no capacitor is present at the LCDCAP pin when the charge pump is enabled. Setting the LCDNOCAPIE bit enables the interrupt.

The LCDBLKONIFG is set at the BLKCLK edge synchronized to the frame boundaries that turns on the segments when blinking is enabled with LCDBLKMODx = 01 or 10. It is also set at the BLKCLK edge synchronized to the frame boundaries that selects the blinking memory as display memory when LCDBLKMODx = 11. It is automatically cleared when a LCD or blinking memory register is written. Setting the LCDBLKONIE bit enables the interrupt.

The LCDBLKOFFIFG is set at the BLKCLK edge synchronized to the frame boundaries that blanks the segments when blinking is enabled with LCDBLKMODx = 01 or 10. It is also set at the BLKCLK edge synchronized to the frame boundaries that selects the LCD memory as display memory when LCDBLKMODx = 11.It is automatically cleared when a LCD or blinking memory register is written. Setting the LCDBLKOFFIE bit enables the interrupt.

The LCDFRMIFG is set at a frame boundary. It is automatically cleared when a LCD or blinking memory register is written. Setting the LCDFRMIFGIE bit enables the interrupt.

1.2.7.1 LCDBIV Software Example

The following software example shows the recommended use of LCDBIV and the handling overhead. The LCDBIV value is added to the PC to automatically jump to the appropriate routine.

The numbers at the right margin show the necessary CPU cycles for each instruction. The software overhead for different interrupt sources includes interrupt latency and return-from-interrupt cycles but not the task handling itself.

```
; Interrupt handler for LCD_B interrupt flags.
LCDB_HND             ; Interrupt latency        6
   ADD &LCDBIV,PC    ; Add offset to Jump table  3
   RETI              ; Vector 0: No interrupt    5
   JMP LCDNOCAP_HND  ; Vector 2: LCDNOCAPIFG     2
   JMP LCDBLKON_HND  ; Vector 4: LCDBLKONIFG     2
   JMP LCDBLKOFF_HND ; Vector 6: LCDBLKOFFIFG    2
LCDFRM_HND           ; Vector 8: LCDFRMIFG
   ...    ; Task starts here
   RETI                                         5
LCDNOCAP_HND ; Vector 2: LCDNOCAPIFG
   ... ; Task starts here
   RETI                                         5
LCDBLKON_HND ; Vector 4: LCDBLKONIFG
   ... ; Task starts here
   RETI ; Back to main program                  5
LCDBLKOFF_HND ; Vector 6: LCDBLKOFFIFG
   ... ; Task starts here
   RETI ; Back to main program                  5
```

1.2.8 Static Mode

In static mode, each MSP430 segment pin drives one LCD segment and one common line, COM0, is used. Figure 1-4 shows some example static waveforms.

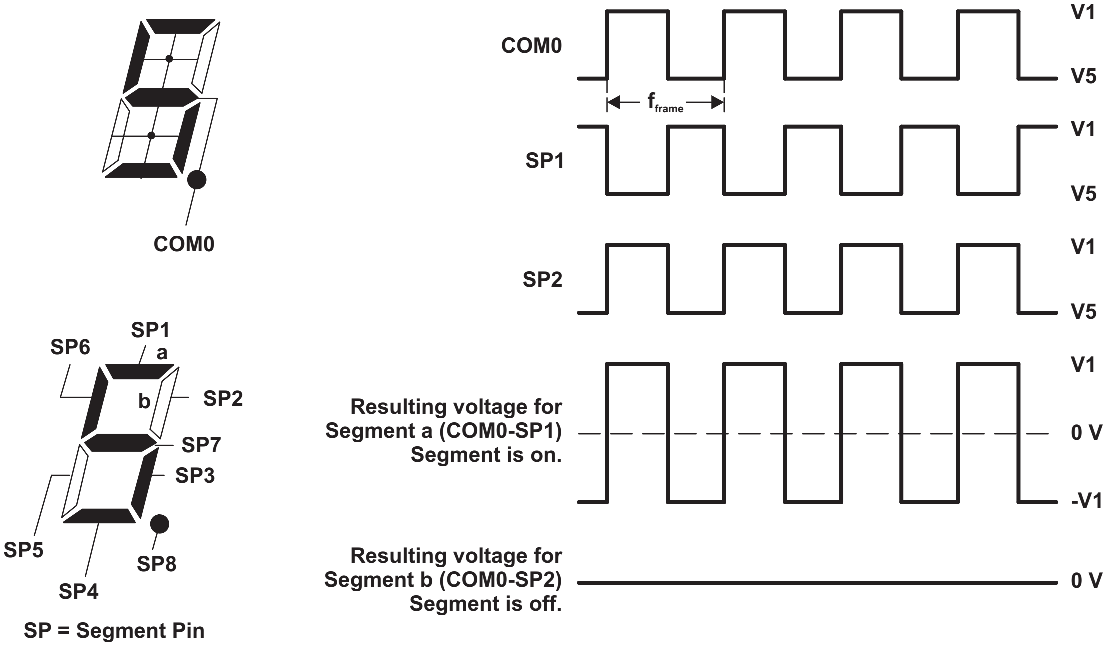
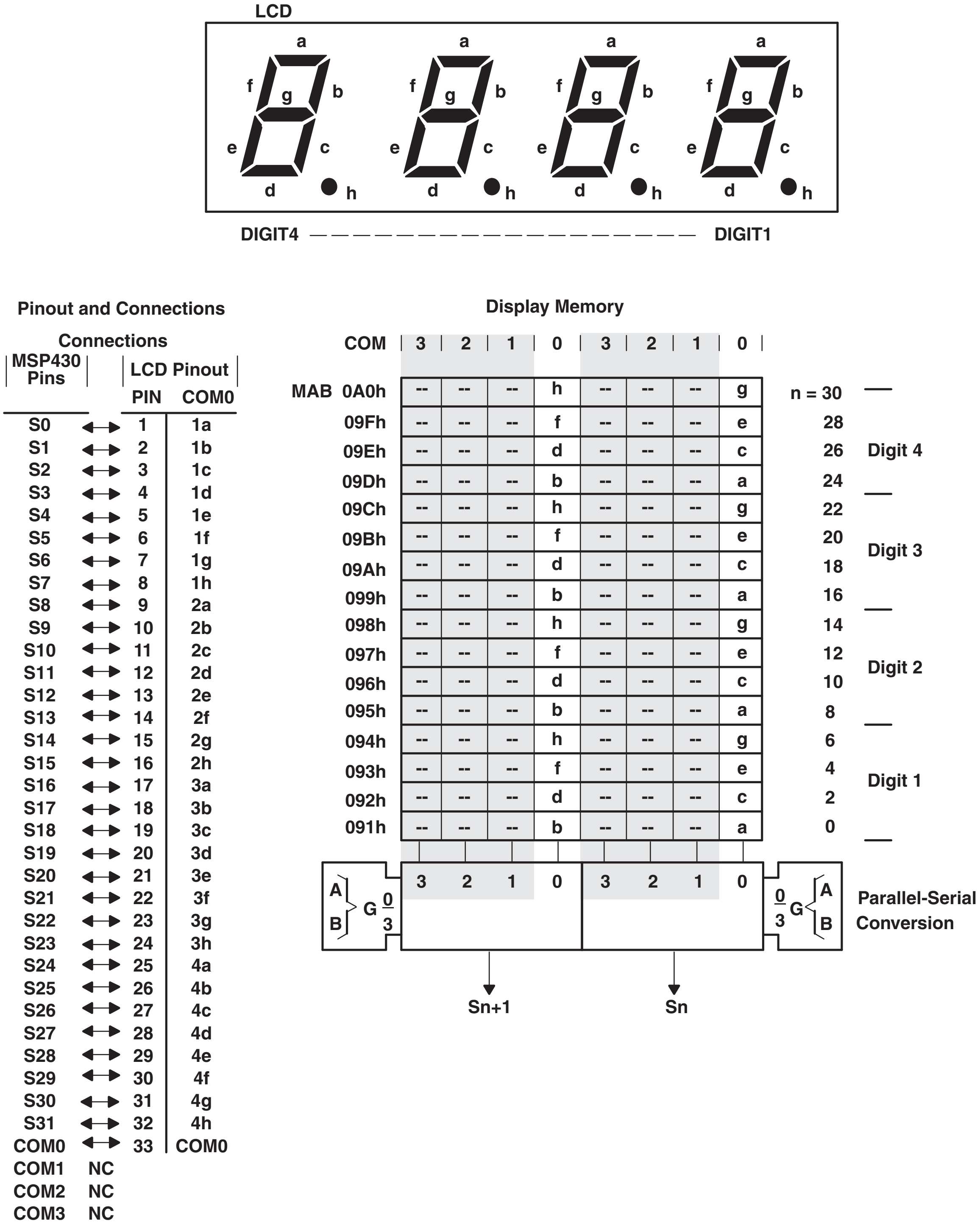

COM0
SP6
SP1
a
b
SP2
SP7
SP3
SP5
SP8
SP4
SP = Segment Pin
COM0
V1
V5
f_{frame}
SP1
V1
V5
SP2
V1
V5
Resulting voltage for Segment a (COM0-SP1) Segment is on.
V1
0 V
-V1
Resulting voltage for Segment b (COM0-SP2) Segment is off.
0 V

Figure 1-4. Example Static Waveforms

Figure 1-5 shows an example static LCD, pinout, LCD-to-MSP430 connections, and the resulting segment mapping. This is only an example. Segment mapping in a user's application depends on the LCD pinout and on the MSP430-to-LCD connections.



Connections

MSP430 Pins		LCD Pinout PIN	LCD Pinout COM0
S0	↔	1	1a
S1	↔	2	1b
S2	↔	3	1c
S3	↔	4	1d
S4	↔	5	1e
S5	↔	6	1f
S6	↔	7	1g
S7	↔	8	1h
S8	↔	9	2a
S9	↔	10	2b
S10	↔	11	2c
S11	↔	12	2d
S12	↔	13	2e
S13	↔	14	2f
S14	↔	15	2g
S15	↔	16	2h
S16	↔	17	3a
S17	↔	18	3b
S18	↔	19	3c
S19	↔	20	3d
S20	↔	21	3e
S21	↔	22	3f
S22	↔	23	3g
S23	↔	24	3h
S24	↔	25	4a
S25	↔	26	4b
S26	↔	27	4c
S27	↔	28	4d
S28	↔	29	4e
S29	↔	30	4f
S30	↔	31	4g
S31	↔	32	4h
COM0	↔	33	COM0
COM1	NC		
COM2	NC		
COM3	NC		

MAB	COM 3	2	1	0	3	2	1	0	n	
0A0h	--	--	--	h	--	--	--	g	n = 30	
09Fh	--	--	--	f	--	--	--	e	28	
09Eh	--	--	--	d	--	--	--	c	26	Digit 4
09Dh	--	--	--	b	--	--	--	a	24	
09Ch	--	--	--	h	--	--	--	g	22	
09Bh	--	--	--	f	--	--	--	e	20	Digit 3
09Ah	--	--	--	d	--	--	--	c	18	
099h	--	--	--	b	--	--	--	a	16	
098h	--	--	--	h	--	--	--	g	14	
097h	--	--	--	f	--	--	--	e	12	Digit 2
096h	--	--	--	d	--	--	--	c	10	
095h	--	--	--	b	--	--	--	a	8	
094h	--	--	--	h	--	--	--	g	6	
093h	--	--	--	f	--	--	--	e	4	Digit 1
092h	--	--	--	d	--	--	--	c	2	
091h	--	--	--	b	--	--	--	a	0	

Figure 1-5. Static LCD Example (MAB addresses need to be replaced with LCDMx)

1.2.8.1 Static Mode Software Example

```
; All eight segments of a digit are often located in four
; display memory bytes with the static display method.
;
a EQU 001h
b EQU 010h
c EQU 002h
d EQU 020h
e EQU 004h
f EQU 040h
g EQU 008h
h EQU 080h
; The register content of Rx should be displayed.
; The Table represents the 'on'-segments according to the
 ; content of Rx.
   MOV.B Table (Rx),RY ; Load segment information
                       ; into temporary memory.
                       ; (Ry) = 0000 0000 hfdb geca
   MOV.B Ry,&LCDn  ; Note:
                   ; All bits of an LCD memory
                   ; byte are written
   RRA Ry ; (Ry) = 0000 0000 0hfd bgec
   MOV.B Ry,&LCDn+1 ; Note:
                    ; All bits of an LCD memory
                    ; byte are written
   RRA Ry ; (Ry) = 0000 0000 00hf dbge
   MOV.B Ry,&LCDn+2 ; Note:
                    ; All bits of an LCD memory
                    ; byte are written
   RRA Ry ; (Ry) = 0000 0000 000h fdbg
   MOV.B Ry,&LCDn+3 ; Note:
                    ; All bits of an LCD memory
                    ; byte are written
   ........... ........... ; Table
   DB a+b+c+d+e+f ; displays "0"
   DB b+c; ; displays "1"
   ........... ...........
   DB ...........
```

1.2.9 2-Mux Mode

In 2-mux mode, each MSP430 segment pin drives two LCD segments and two common lines, COM0 and COM1, are used. Figure 1-6 shows some example 2-mux, 1/2 bias waveforms.

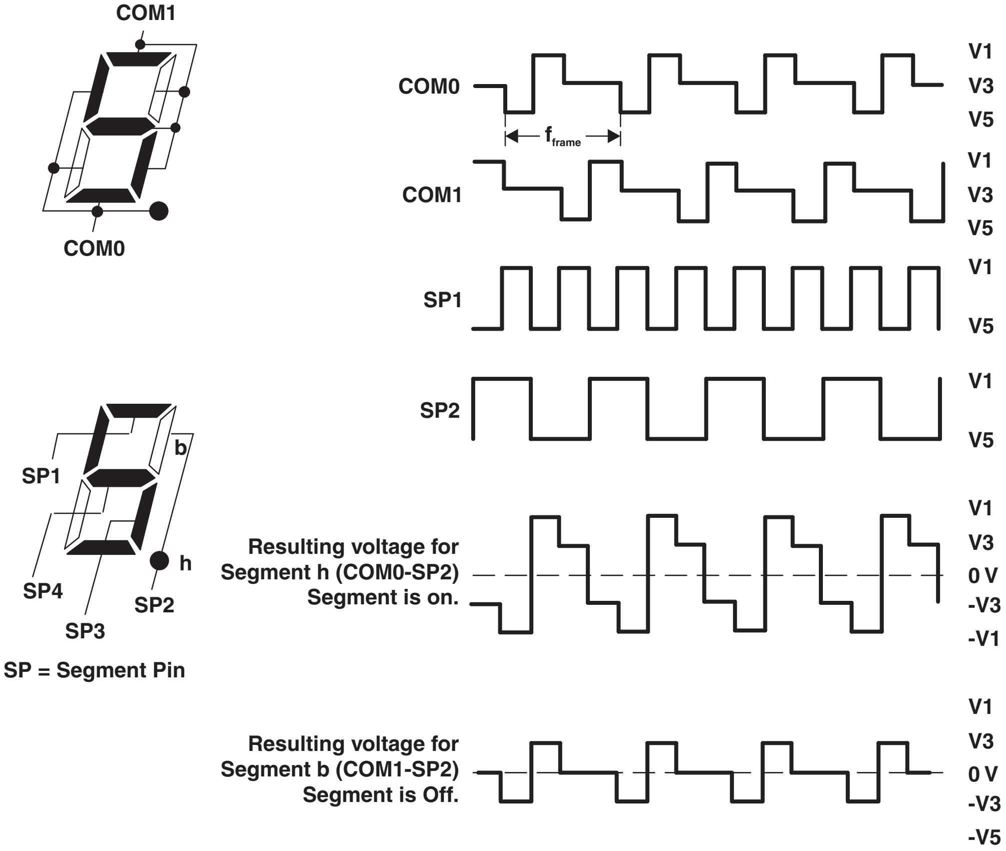
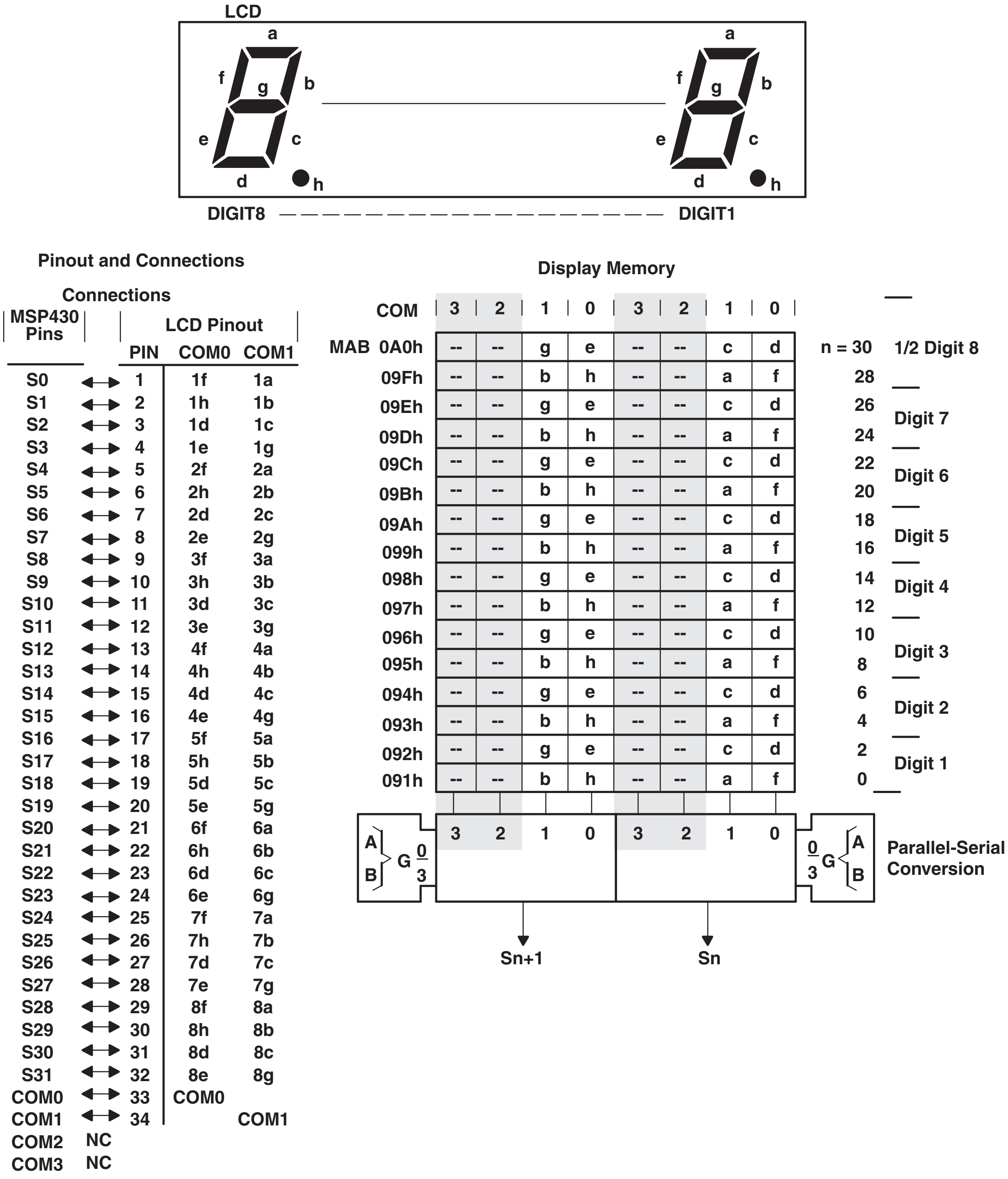

COM1
COM0
SP1
b
h
SP4
SP2
SP3
SP = Segment Pin
COM0
f_frame
COM1
SP1
SP2
Resulting voltage for Segment h (COM0-SP2) Segment is on.
Resulting voltage for Segment b (COM1-SP2) Segment is Off.
V1
V3
V5
V1
V3
V5
V1
V5
V1
V5
V1
V3
0 V
-V3
-V1
V1
V3
0 V
-V3
-V5

Figure 1-6. Example 2-Mux Waveforms

Figure 1-7 shows an example 2-mux LCD, pinout, LCD-to-MSP430 connections, and the resulting segment mapping. This is only an example. Segment mapping in a user's application completely depends on the LCD pinout and on the MSP430-to-LCD connections.



Pinout and Connections

Connections MSP430 Pins		LCD Pinout PIN	COM0	COM1
S0	↔	1	1f	1a
S1	↔	2	1h	1b
S2	↔	3	1d	1c
S3	↔	4	1e	1g
S4	↔	5	2f	2a
S5	↔	6	2h	2b
S6	↔	7	2d	2c
S7	↔	8	2e	2g
S8	↔	9	3f	3a
S9	↔	10	3h	3b
S10	↔	11	3d	3c
S11	↔	12	3e	3g
S12	↔	13	4f	4a
S13	↔	14	4h	4b
S14	↔	15	4d	4c
S15	↔	16	4e	4g
S16	↔	17	5f	5a
S17	↔	18	5h	5b
S18	↔	19	5d	5c
S19	↔	20	5e	5g
S20	↔	21	6f	6a
S21	↔	22	6h	6b
S22	↔	23	6d	6c
S23	↔	24	6e	6g
S24	↔	25	7f	7a
S25	↔	26	7h	7b
S26	↔	27	7d	7c
S27	↔	28	7e	7g
S28	↔	29	8f	8a
S29	↔	30	8h	8b
S30	↔	31	8d	8c
S31	↔	32	8e	8g
COM0	↔	33	COM0	
COM1	↔	34		COM1
COM2	NC			
COM3	NC			

COM	3	2	1	0	3	2	1	0		
MAB 0A0h	--	--	g	e	--	--	c	d	n = 30	1/2 Digit 8
09Fh	--	--	b	h	--	--	a	f	28	
09Eh	--	--	g	e	--	--	c	d	26	Digit 7
09Dh	--	--	b	h	--	--	a	f	24	
09Ch	--	--	g	e	--	--	c	d	22	Digit 6
09Bh	--	--	b	h	--	--	a	f	20	
09Ah	--	--	g	e	--	--	c	d	18	Digit 5
099h	--	--	b	h	--	--	a	f	16	
098h	--	--	g	e	--	--	c	d	14	Digit 4
097h	--	--	b	h	--	--	a	f	12	
096h	--	--	g	e	--	--	c	d	10	Digit 3
095h	--	--	b	h	--	--	a	f	8	
094h	--	--	g	e	--	--	c	d	6	Digit 2
093h	--	--	b	h	--	--	a	f	4	
092h	--	--	g	e	--	--	c	d	2	Digit 1
091h	--	--	b	h	--	--	a	f	0	
	3	2	1	0	3	2	1	0		

Figure 1-7. 2-Mux LCD Example (MAB addresses need to be replaced with LCDMx)

1.2.9.1 2-Mux Mode Software Example

```
; All eight segments of a digit are often located in two
; display memory bytes with the 2-mux display rate ;
a EQU 002h
b EQU 020h
c EQU 008h
d EQU 004h
e EQU 040h
f EQU 001h
g EQU 080h
h EQU 010h
; The register content of Rx should be displayed.
; The Table represents the 'on'-segments according to the
; content of Rx. ;
........... ...........
   MOV.B Table(Rx),Ry ; Load segment information into
                      ; temporary memory.
   MOV.B Ry,&LCDn ; (Ry) = 0000 0000 gebh cdaf
                      ; Note:
                      ; All bits of an LCD memory byte
                      ; are written
   RRA Ry ; (Ry) = 0000 0000 0geb hcda
   RRA Ry ; (Ry) = 0000 0000 00ge bhcd
   MOV.B Ry,&LCDn+1 ; Note:
                    ; All bits of an LCD memory byte
                    ; are written
   ........... ........... ...........
Table
   DB a+b+c+d+e+f   ; displays "0"
   ...........
   DB a+b+c+d+e+f+g ; displays "8"
   ........... ...........
   DB ........... ;
```

1.2.10 3-Mux Mode

In 3-mux mode, each MSP430 segment pin drives three LCD segments and three common lines (COM0, COM1, and COM2) are used.Figure 1-8 shows some example 3-mux, 1/3 bias waveforms.

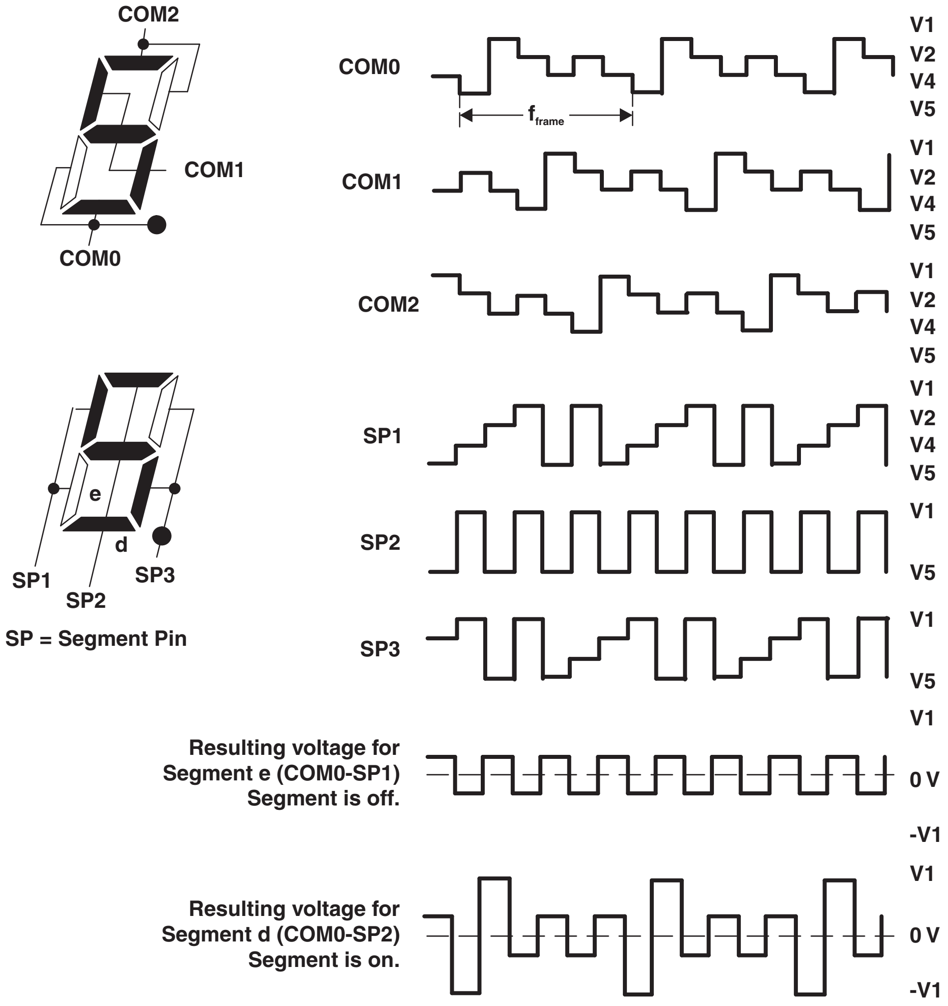
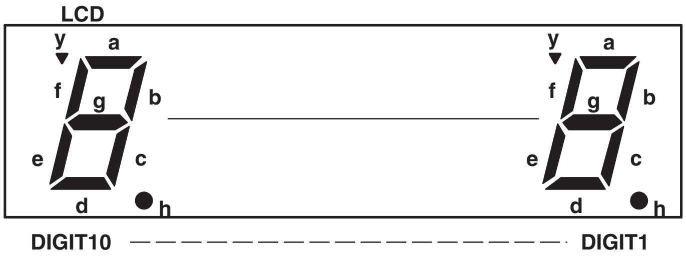


Figure 1-8. Example 3-Mux Waveforms

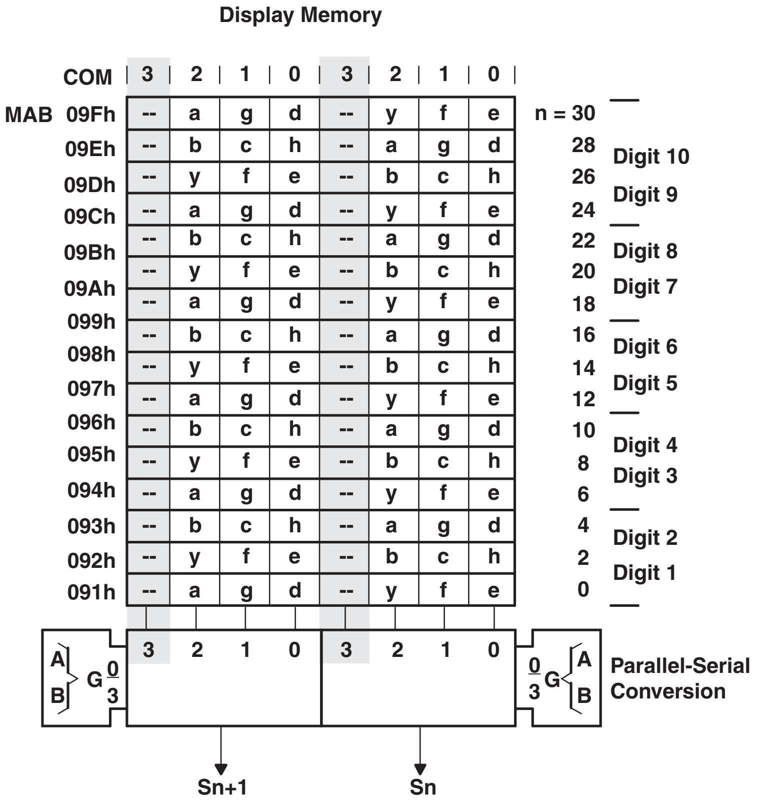
Figure 1-9 shows an example 3-mux LCD, pinout, LCD-to-MSP430 connections, and the resulting segment mapping. This is only an example. Segment mapping in a user's application depends on the LCD pinout and on the MSP430-to-LCD connections.



Pinout and Connections

MSP430 Pins	Connections	PIN	COM0	COM1	COM2
S0	↔	1	1e	1f	1y
S1	↔	2	1d	1g	1a
S2	↔	3	1h	1c	1b
S3	↔	4	2e	2f	2y
S4	↔	5	2d	2g	2a
S5	↔	6	2h	2c	2b
S6	↔	7	3e	3f	3y
S7	↔	8	3d	3g	3a
S8	↔	9	3h	3c	3b
S9	↔	10	4e	4f	4y
S10	↔	11	4d	4g	4a
S11	↔	12	4h	4c	4b
S12	↔	13	5e	5f	5y
S13	↔	14	5d	5g	5a
S14	↔	15	5h	5c	5b
S15	↔	16	6e	6f	6y
S16	↔	17	6d	6g	6a
S17	↔	18	6h	6c	6b
S18	↔	19	7e	7f	7y
S19	↔	20	7d	7g	7a
S20	↔	21	7h	7c	7b
S21	↔	22	8e	8f	8y
S22	↔	23	8d	8g	8a
S23	↔	24	8h	8c	8b
S24	↔	25	9e	9f	9y
S25	↔	26	9d	9g	9a
S26	↔	27	9h	9c	9b
S27	↔	28	10e	10f	10y
S28	↔	29	10d	10g	10a
S29	↔	30	10h	10c	10b
COM0	↔	31	COM0		
COM1	↔	32		COM1	
COM2	↔	33			COM2
COM3	NC				

Display Memory



COM	3	2	1	0	3	2	1	0		
MAB 09Fh	--	a	g	d	--	y	f	e	n = 30	
09Eh	--	b	c	h	--	a	g	d	28	Digit 10
09Dh	--	y	f	e	--	b	c	h	26	Digit 9
09Ch	--	a	g	d	--	y	f	e	24	
09Bh	--	b	c	h	--	a	g	d	22	Digit 8
	--	y	f	e	--	b	c	h	20	Digit 7
09Ah	--	a	g	d	--	y	f	e	18	
099h	--	b	c	h	--	a	g	d	16	Digit 6
098h	--	y	f	e	--	b	c	h	14	Digit 5
097h	--	a	g	d	--	y	f	e	12	
096h	--	b	c	h	--	a	g	d	10	Digit 4
095h	--	y	f	e	--	b	c	h	8	Digit 3
094h	--	a	g	d	--	y	f	e	6	
093h	--	b	c	h	--	a	g	d	4	Digit 2
092h	--	y	f	e	--	b	c	h	2	Digit 1
091h	--	a	g	d	--	y	f	e	0	

Figure 1-9. 3-Mux LCD Example (MAB addresses need to be replaced with LCDMx)

1.2.10.1 3-Mux Mode Software Example

```
; The 3-mux rate can support nine segments for each
; digit. The nine segments of a digit are located in
; 1 1/2 display memory bytes.
;
a EQU 0040h
b EQU 0400h
c EQU 0200h
d EQU 0010h
e EQU 0001h
f EQU 0002h
g EQU 0020h
h EQU 0100h
Y EQU 0004h
; The LSDigit of register Rx should be displayed.
; The Table represents the 'on'-segments according to the
; LSDigit of register of Rx.
; The register Ry is used for temporary memory
;
ODDDIG
   RLA Rx ; LCD in 3-mux has 9 segments per
              ; digit
              ; word table required for
              ; displayed characters.
   MOV Table(Rx),Ry ; Load segment information to
                    ; temporary mem.
                    ; (Ry) = 0000 0bch 0agd 0yfe
   MOV.B Ry,&LCDn ; write 'a, g, d, y, f, e' of
                  ; Digit n (LowByte)
   SWPB Ry ; (Ry) = 0agd 0yfe 0000 0bch
   BIC.B #07h,&LCDn+1 ; write 'b, c, h' of Digit n
                      ; (HighByte)
   BIS.B Ry,&LCDn+1
   .....
EVNDIG
   RLA Rx ; LCD in 3-mux has 9 segments per
          ; digit
          ; word table required for
          ; displayed characters.
   MOV Table(Rx),Ry ; Load segment information to
                    ; temporary mem.
                    ; (Ry) = 0000 0bch 0agd 0yfe
   RLA Ry ; (Ry) = 0000 bch0 agd0 yfe0
   RLA Ry ; (Ry) = 000b ch0a gd0y fe00
   RLA Ry ; (Ry) = 00bc h0ag d0yf e000
   RLA Ry ; (Ry) = 0bch 0agd 0yfe 0000
   BIC.B #070h,&LCDn+1
   BIS.B Ry,&LCDn+1 ; write 'y, f, e' of Digit n+1
                    ; (LowByte)
   SWPB Ry ; (Ry) = 0yfe 0000 0bch 0agd
   MOV.B Ry,&LCDn+2 ; write 'b, c, h, a, g, d' of
                    ; Digit n+1 (HighByte)
   ...........
Table
   DW a+b+c+d+e+f  ; displays "0"
   DW b+c          ; displays "1"
........... ...........
   DW a+e+f+g ; displays "F"
```

1.2.11 4-Mux Mode

In 4-mux mode, each MSP430 segment pin drives four LCD segments and all four common lines (COM0, COM1, COM2, and COM3) are used. Figure 1-10 shows some example 4-mux, 1/3 bias waveforms.

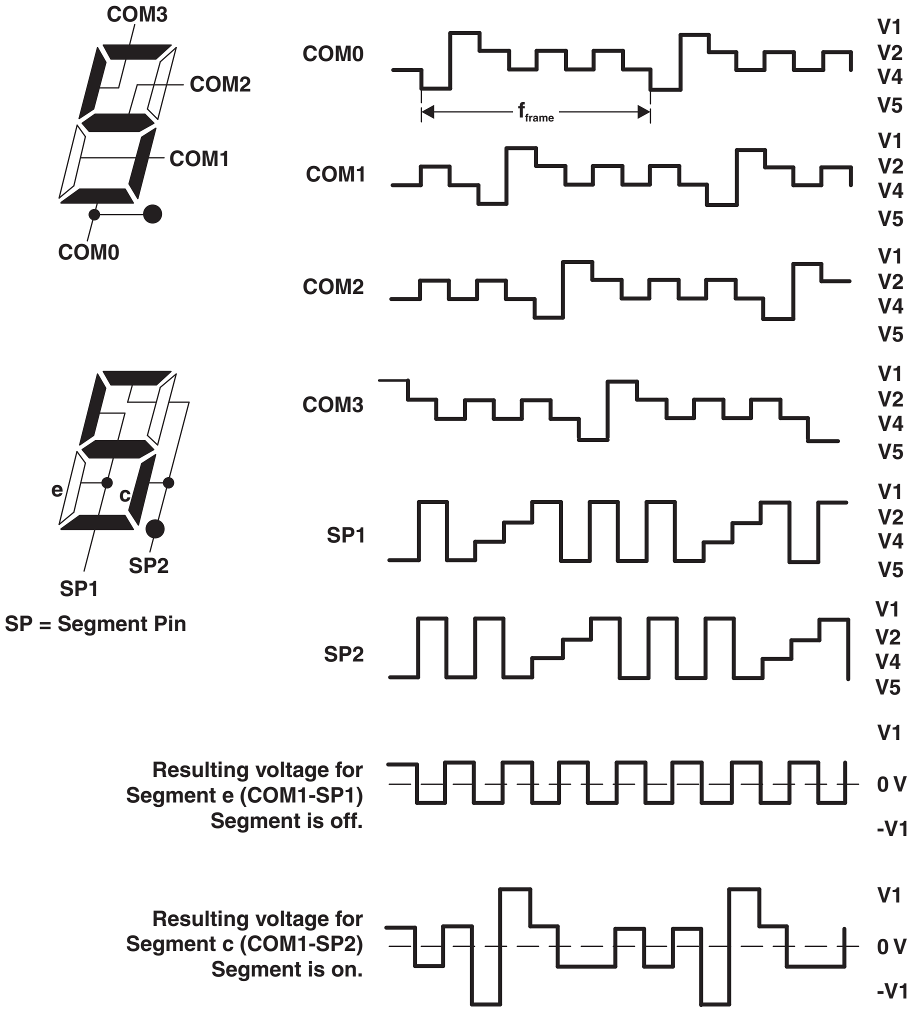
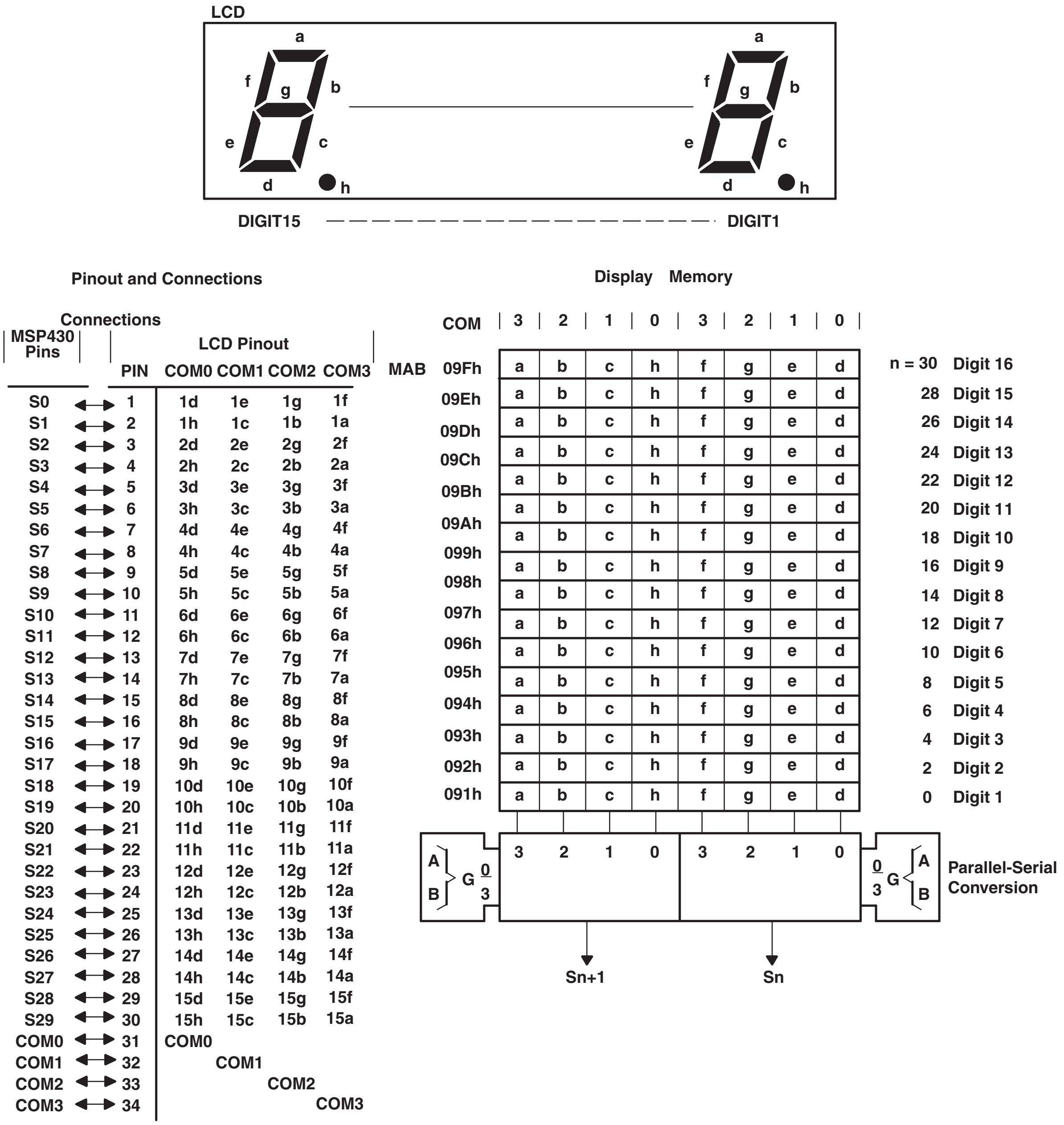

COM3
COM2
COM1
COM0
e
c
SP2
SP1
SP = Segment Pin
COM0
f_{frame}
COM1
COM2
COM3
SP1
SP2
V1
V2
V4
V5
Resulting voltage for Segment e (COM1-SP1) Segment is off.
V1
0 V
-V1
Resulting voltage for Segment c (COM1-SP2) Segment is on.
V1
0 V
-V1

Figure 1-10. Example 4-Mux Waveforms

Figure 1-11 shows an example 4-mux LCD, pinout, LCD-to-MSP430 connections, and the resulting segment mapping. This is only an example. Segment mapping in a user's application depends on the LCD pinout and on the MSP430-to-LCD connections.



Connections

MSP430 Pins		PIN	COM0	COM1	COM2	COM3
S0	◄─►	1	1d	1e	1g	1f
S1	◄─►	2	1h	1c	1b	1a
S2	◄─►	3	2d	2e	2g	2f
S3	◄─►	4	2h	2c	2b	2a
S4	◄─►	5	3d	3e	3g	3f
S5	◄─►	6	3h	3c	3b	3a
S6	◄─►	7	4d	4e	4g	4f
S7	◄─►	8	4h	4c	4b	4a
S8	◄─►	9	5d	5e	5g	5f
S9	◄─►	10	5h	5c	5b	5a
S10	◄─►	11	6d	6e	6g	6f
S11	◄─►	12	6h	6c	6b	6a
S12	◄─►	13	7d	7e	7g	7f
S13	◄─►	14	7h	7c	7b	7a
S14	◄─►	15	8d	8e	8g	8f
S15	◄─►	16	8h	8c	8b	8a
S16	◄─►	17	9d	9e	9g	9f
S17	◄─►	18	9h	9c	9b	9a
S18	◄─►	19	10d	10e	10g	10f
S19	◄─►	20	10h	10c	10b	10a
S20	◄─►	21	11d	11e	11g	11f
S21	◄─►	22	11h	11c	11b	11a
S22	◄─►	23	12d	12e	12g	12f
S23	◄─►	24	12h	12c	12b	12a
S24	◄─►	25	13d	13e	13g	13f
S25	◄─►	26	13h	13c	13b	13a
S26	◄─►	27	14d	14e	14g	14f
S27	◄─►	28	14h	14c	14b	14a
S28	◄─►	29	15d	15e	15g	15f
S29	◄─►	30	15h	15c	15b	15a
COM0	◄─►	31	COM0			
COM1	◄─►	32		COM1		
COM2	◄─►	33			COM2	
COM3	◄─►	34				COM3

MAB	COM 3	2	1	0	3	2	1	0		
09Fh	a	b	c	h	f	g	e	d	n = 30	Digit 16
09Eh	a	b	c	h	f	g	e	d	28	Digit 15
09Dh	a	b	c	h	f	g	e	d	26	Digit 14
09Ch	a	b	c	h	f	g	e	d	24	Digit 13
09Bh	a	b	c	h	f	g	e	d	22	Digit 12
09Ah	a	b	c	h	f	g	e	d	20	Digit 11
099h	a	b	c	h	f	g	e	d	18	Digit 10
098h	a	b	c	h	f	g	e	d	16	Digit 9
097h	a	b	c	h	f	g	e	d	14	Digit 8
096h	a	b	c	h	f	g	e	d	12	Digit 7
095h	a	b	c	h	f	g	e	d	10	Digit 6
094h	a	b	c	h	f	g	e	d	8	Digit 5
093h	a	b	c	h	f	g	e	d	6	Digit 4
092h	a	b	c	h	f	g	e	d	4	Digit 3
091h	a	b	c	h	f	g	e	d	2	Digit 2
	a	b	c	h	f	g	e	d	0	Digit 1

Figure 1-11. 4-Mux LCD Example (MAB addresses need to be replaced with LCDMx)

1.2.11.1 4-Mux Mode Software Example

```
; The 4-mux rate supports eight segments for each digit.
; All eight segments of a digit can often be located in
; one display memory byte
a EQU 080h
b EQU 040h
c EQU 020h
d EQU 001h
e EQU 002h
f EQU 008h
g EQU 004h
h EQU 010h
;
; The LSDigit of register Rx should be displayed.
; The Table represents the 'on'-segments according to the
; content of Rx.
;
   MOV.B Table(Rx),&LCDn ; n = 1 ..... 15
                         ; all eight segments are
                         ; written to the display
                         ; memory
........... ...........
Table
   DB a+b+c+d+e+f ; displays "0"
   DB b+c         ; displays "1"
........... ...........
   DB b+c+d+e+g   ; displays "d"
   DB a+d+e+f+g   ; displays "E"
   DB a+e+f+g     ; displays "F"
```

1.3 LCD_B Registers

The LCD_B registers are listed in Table 1-2 to Table 1-4. The LCD memory and blinking memory registers can also be accessed as word.

Table 1-2. LCD_B Registers

Offset	Acronym	Register Name	Type	Reset	Section
000h	LCDBCTL0	LCD_B control register 0	Read/write	0000h	Section 1.3.1
002h	LCDBCTL1	LCD_B control register 1	Read/write	0000h	Section 1.3.2
004h	LCDBBLKCTL	LCD_B blinking control register	Read/write	0000h	Section 1.3.3
006h	LCDBMEMCTL	LCD_B memory control register	Read/write	0000h	Section 1.3.4
008h	LCDBVCTL	LCD_B voltage control register	Read/write	0000h	Section 1.3.5
00Ah	LCDBPCTL0	LCD_B port control 0	Read/write	0000h	Section 1.3.6
00Ch	LCDBPCTL1	LCD_B port control 1	Read/write	0000h	Section 1.3.7
00Eh	LCDBPCTL2	LCD_B port control 2 (≥128 segments)	Read/write	0000h	Section 1.3.8
010h	LCDBPCTL3	LCD_B port control 3 (192 segments)	Read/write	0000h	Section 1.3.9
012h	LCDBCPCTL	LCD_B charge pump control	Read/write	0000h	Section 1.3.10
014h		Reserved			
016h		Reserved			
018h		Reserved			
01Ah		Reserved			
01Ch		Reserved			
01Eh	LCDBIV	LCD_B interrupt vector	Read/write	0000h	Section 1.3.11

Table 1-3. LCD_B Memory Registers[1]

Offset	Acronym	Register Name	Type	Reset
020h	LCDM1	LCD memory 1 (S1/S0)	Read/write	Unchanged
021h	LCDM2	LCD memory 2 (S3/S2)	Read/write	Unchanged
022h	LCDM3	LCD memory 3 (S5/S4)	Read/write	Unchanged
023h	LCDM4	LCD memory 4 (S7/S6)	Read/write	Unchanged
024h	LCDM5	LCD memory 5 (S9/S8)	Read/write	Unchanged
025h	LCDM6	LCD memory 6 (S11/S10)	Read/write	Unchanged
026h	LCDM7	LCD memory 7 (S13/S12)	Read/write	Unchanged
027h	LCDM8	LCD memory 8 (S15/S14)	Read/write	Unchanged
028h	LCDM9	LCD memory 9 (S17/S16)	Read/write	Unchanged
029h	LCDM10	LCD memory 10 (S19/S18)	Read/write	Unchanged
02Ah	LCDM11	LCD memory 11 (S21/S20)	Read/write	Unchanged
02Bh	LCDM12	LCD memory 12 (S23/S22)	Read/write	Unchanged
02Ch	LCDM13	LCD memory 13 (S25/S24)	Read/write	Unchanged
02Dh	LCDM14	LCD memory 14 (S27/S26)	Read/write	Unchanged
02Eh	LCDM15	LCD memory 15 (S29/S28, ≥128 segments)	Read/write	Unchanged
02Fh	LCDM16	LCD memory 16 (S31/S30, ≥128 segments)	Read/write	Unchanged
030h	LCDM17	LCD memory 17 (S33/S32, ≥128 segments)	Read/write	Unchanged
031h	LCDM18	LCD memory 18 (S35/S34, ≥128 segments)	Read/write	Unchanged
032h	LCDM19	LCD memory 19 (S37/S36, ≥160 segments)	Read/write	Unchanged
033h	LCDM20	LCD memory 20 (S39/S38, ≥160 segments)	Read/write	Unchanged
034h	LCDM21	LCD memory 21 (S41/S40, ≥160 segments)	Read/write	Unchanged
035h	LCDM22	LCD memory 22 (S43/S42, ≥160 segments)	Read/write	Unchanged
036h	LCDM23	LCD memory 23 (S45/S44, 192 segments)	Read/write	Unchanged
037h	LCDM24	LCD memory 24 (S47/S46, 192 segments)	Read/write	Unchanged
038h	LCDM25	LCD memory 25 (S49/S48, 192 segments)	Read/write	Unchanged
039h	LCDM26	LCD memory 26 (S50, 192 segments)	Read/write	Unchanged
03Ah		Reserved	Read/write	Unchanged
03Bh		Reserved	Read/write	Unchanged
03Ch		Reserved	Read/write	Unchanged
03Dh		Reserved	Read/write	Unchanged
03Eh		Reserved	Read/write	Unchanged
03Fh		Reserved	Read/write	Unchanged

[1] The LCD memory registers can also be accessed as word.

Table 1-4. LCD_B Blinking Memory Registers[1]

Offset	Acronym	Register Name	Type	Reset
040h	LCDBM1	LCD blinking memory 1	Read/write	Unchanged
041h	LCDBM2	LCD blinking memory 2	Read/write	Unchanged
042h	LCDBM3	LCD blinking memory 3	Read/write	Unchanged
043h	LCDBM4	LCD blinking memory 4	Read/write	Unchanged
044h	LCDBM5	LCD blinking memory 5	Read/write	Unchanged
045h	LCDBM6	LCD blinking memory 6	Read/write	Unchanged
046h	LCDBM7	LCD blinking memory 7	Read/write	Unchanged
047h	LCDBM8	LCD blinking memory 8	Read/write	Unchanged
048h	LCDBM9	LCD blinking memory 9	Read/write	Unchanged
049h	LCDBM10	LCD blinking memory 10	Read/write	Unchanged
04Ah	LCDBM11	LCD blinking memory 11	Read/write	Unchanged
04Bh	LCDBM12	LCD blinking memory 12	Read/write	Unchanged
04Ch	LCDBM13	LCD blinking memory 13	Read/write	Unchanged
04Dh	LCDBM14	LCD blinking memory 14	Read/write	Unchanged
04Eh	LCDBM15	LCD blinking memory 15 (≥128 segments)	Read/write	Unchanged
04Fh	LCDBM16	LCD blinking memory 16 (≥128 segments)	Read/write	Unchanged
050h	LCDBM17	LCD blinking memory 17 (≥128 segments)	Read/write	Unchanged
051h	LCDBM18	LCD blinking memory 18 (≥128 segments)	Read/write	Unchanged
052h	LCDBM19	LCD blinking memory 19 (≥160 segments)	Read/write	Unchanged
053h	LCDBM20	LCD blinking memory 20 (≥160 segments)	Read/write	Unchanged
054h	LCDBM21	LCD blinking memory 21 (≥160 segments)	Read/write	Unchanged
055h	LCDBM22	LCD blinking memory 22 (≥160 segments)	Read/write	Unchanged
056h	LCDBM23	LCD blinking memory 23 (190 segments)	Read/write	Unchanged
057h	LCDBM24	LCD blinking memory 24 (190 segments)	Read/write	Unchanged
058h	LCDBM25	LCD blinking memory 25 (190 segments)	Read/write	Unchanged
059h	LCDBM26	LCD blinking memory 26 (190 segments)	Read/write	Unchanged
05Ah		Reserved	Read/write	Unchanged
05Bh		Reserved	Read/write	Unchanged
05Ch		Reserved	Read/write	Unchanged
05Dh		Reserved	Read/write	Unchanged
05Eh		Reserved	Read/write	Unchanged
05Fh		Reserved	Read/write	Unchanged

[1] The LCD blinking memory registers can also be accessed as word.

1.3.1 LCDBCTL0 Register

LCD_B Control Register 0

Figure 1-12. LCDBCTL0 Register

15	14	13	12	11	10	9	8
LCDDIVx					LCDPREx		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDSSEL	Reserved		LCDMXx		LCDSON	Reserved	LCDON
rw-0	r0	r0	rw-0	rw-0	rw-0	r0	rw-0

Table 1-5. LCDBCTL0 Register Description

Bit	Field	Type	Reset	Description
15-11	LCDDIVx	RW	0h	LCD frequency divider. Together with LCDPREx the LCD frequency f_{LCD} is calculated as $f_{LCD} = f_{ACLK/VLO} / [(LCDDIVx + 1) \times 2^{LCDPREx}]$. Settings for this bit should be changed only while LCDON = 0. 00000b = Divide by 1 00001b = Divide by 2 ⋮ 11110b = Divide by 31 11111b = Divide by 32
10-8	LCDPREx	RW	0h	LCD frequency pre-scaler. Together with LCDDIVx the LCD frequency f_{LCD} is calculated as $f_{LCD} = f_{ACLK/VLO} / [(LCDDIVx + 1) \times 2^{LCDPREx}]$. Settings for this bit should be changed only while LCDON = 0. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 4 011b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Reserved - Defaults to divide by 32 111b = Reserved - Defaults to divide by 32
7	LCDSSEL	RW	0h	Clock source select for LCD and blinking frequency Settings for this bit should be changed only while LCDON = 0. 0b = ACLK (30 kHz to 40 kHz) 1b = VLOCLK
6-5	Reserved	R	0h	Reserved. Always reads as 0.
4-3	LCDMXx	RW	0h	LCD mux rate. These bits select the LCD mode. Settings for this bit should be changed only while LCDON = 0. 00b = Static 01b = 2-mux 10b = 3-mux 11b = 4-mux
2	LCDSON	RW	0h	LCD segments on. This bit supports flashing LCD applications by turning off all segment lines, while leaving the LCD timing generator and R33 enabled. 0b = All LCD segments are off. 1b = All LCD segments are enabled and on or off according to their corresponding memory location.
1	Reserved	R	0h	Reserved. Always reads as 0.
0	LCDON	RW	0h	LCD on. This bit turns the LCD_B module on or off. 0b = LCD_B module off 1b = LCD_B module on

1.3.2 LCDBCTL1 Register

LCD_B Control Register 1

Figure 1-13. LCDBCTL1 Register

15	14	13	12	11	10	9	8
Reserved				LCDNOCAPIE	LCDBLKONIE	LCDBLKOFFIE	LCDFRMIE
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				LCDNOCAPIFG	LCDBLKONIFG	LCDBLKOFFIFG	LCDFRMIFG
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0

Table 1-6. LCDBCTL1 Register Description

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0h	Reserved. Always reads as 0.
11	LCDNOCAPIE	RW	0h	No capacitance connected interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
10	LCDBLKONIE	RW	0h	LCD blinking interrupt enable, segments switched on 0b = Interrupt disabled 1b = Interrupt enabled
9	LCDBLKOFFIE	RW	0h	LCD blinking interrupt enable, segments switched off 0b = Interrupt disabled 1b = Interrupt enabled
8	LCDFRMIE	RW	0h	LCD frame interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
7-4	Reserved	R	0h	Reserved. Always reads as 0.
3	LCDNOCAPIFG	RW	0h	No capacitance connected interrupt flag. Set when charge pump is enabled but no capacitance is connected to LCDCAP pin. 0b = No interrupt pending 1b = Interrupt pending
2	LCDBLKONIFG	RW	0h	LCD blinking interrupt flag, segments switched on. Automatically cleared when data is written into a memory register. 0b = No interrupt pending 1b = Interrupt pending
1	LCDBLKOFFIFG	RW	0h	LCD blinking interrupt flag, segments switched off. Automatically cleared when data is written into a memory register. 0b = No interrupt pending 1b = Interrupt pending
0	LCDFRMIFG	RW	0h	LCD frame interrupt flag. Automatically cleared when data is written into a memory register. 0b = No interrupt pending 1b = Interrupt pending

1.3.3 LCDBBLKCTL Register

LCD_B Blink Control Register

Figure 1-14. LCDBBLKCTL Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCDBLKDIVx			LCDBLKPREx			LCDBLKMODx	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-7. LCDBBLKCTL Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved. Always reads as 0.
7-5	LCDBLKDIVx	RW	0h	Clock divider for blinking frequency. Together with LCDBLKPREx, the blinking frequency f_{BLINK} is calculated as $f_{BLINK} = f_{ACLK/VLO}$ / [(LCDBLKDIVx + 1) × $2^{9+LCDBLKPREx}$)]. Settings for this bit should be changed only while LCDBLKMODx = 00. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8
4-2	LCDBLKPREx	RW	0h	Clock pre-scaler for blinking frequency. Together with LCDBLKDIVx, the blinking frequency f_{BLINK} is calculated as $f_{BLINK} = f_{ACLK/VLO}$ / ((LCDBLKDIVx + 1) × $2^{9+LCDBLKPREx}$). Settings for this bit should be changed only while LCDBLKMODx = 00. 000b = Divide by 512 001b = Divide by 1024 010b = Divide by 2048 011b = Divide by 4096 100b = Divide by 8162 101b = Divide by 16384 110b = Divide by 32768 111b = Divide by 65536
1-0	LCDBLKMODx	RW	0h	Blinking mode 00b = Blinking disabled 01b = Blinking of individual segments as enabled in blinking memory register LCDBMx 10b = Blinking of all segments 11b = Switching between display contents as stored in LCDMx and LCDBMx memory registers.

1.3.4 LCDBMEMCTL Register

LCD_B Memory Control Register

Figure 1-15. LCDBMEMCTL Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved					LCDCLRBM	LCDCLRM	LCDDISP
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0

Table 1-8. LCDBMEMCTL Register Description

Bit	Field	Type	Reset	Description
15-3	Reserved	R	0h	Reserved. Always reads as 0.
2	LCDCLRBM	RW	0h	Clear LCD blinking memory Clears all blinking memory registers LCDBMx. The bit is automatically reset when the blinking memory is cleared. 0b = Contents of blinking memory registers LCDBMx remain unchanged 1b = Clear content of all blinking memory registers LCDBMx
1	LCDCLRM	RW	0h	Clear LCD memory Clears all LCD memory registers LCDMx. The bit is automatically reset when the LCD memory is cleared. 0b = Contents of LCD memory registers LCDMx remain unchanged 1b = Clear content of all LCD memory registers LCDMx
0	LCDDISP	RW	0h	Select LCD memory registers for display The bit is cleared in LCDBLKMODx = 01 and LCDBLKMODx = 10 and cannot be changed by software. When LCDBLKMODx = 11, this bit reflects the currently displayed memory but cannot be changed by software. When returning to LCDBLKMODx = 00 the bit is cleared. 0b = Display content of LCD memory registers LCDMx 1b = Display content of LCD blinking memory registers LCDBMx

1.3.5 LCDBVCTL Register

LCD_B Voltage Control Register

Figure 1-16. LCDBVCTL Register

15	14	13	12	11	10	9	8
Reserved			VLCDx				Reserved
r0	r0	r0	rw-0	rw-0	rw-0	rw-0	r0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCDREXT	R03EXT	LCDEXTBIAS	VLCDEXT	LCDCPEN	VLCDREFx		LCD2B
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-9. LCDBVCTL Register Description

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0h	Reserved. Always reads as 0.
12-9	VLCDx	RW	0h	Charge pump voltage select. LCDCPEN must be 1 for the charge pump to be enabled. V(CC) is used for V_{LCD} when VLCDx = 0000 and VLCDREFx = 00 and VLCDEXT = 0. If VLCDREFx = 00 or 10: 0000b = Charge pump disabled 0001b = V_{LCD} = 2.60 V 0010b = V_{LCD} = 2.66 V 0011b = V_{LCD} = 2.72 V 0100b = V_{LCD} = 2.78 V 0101b = V_{LCD} = 2.84 V 0110b = V_{LCD} = 2.90 V 0111b = V_{LCD} = 2.96 V 1000b = V_{LCD} = 3.02 V 1001b = V_{LCD} = 3.08 V 1010b = V_{LCD} = 3.14 V 1011b = V_{LCD} = 3.20 V 1100b = V_{LCD} = 3.26 V 1101b = V_{LCD} = 3.32 V 1110b = V_{LCD} = 3.38 V 1111b = V_{LCD} = 3.44 V If VLCDREFx = 01 or 11: 0000b = Charge pump disabled 0001b = V_{LCD} = 2.17 × V_{REF} 0010b = V_{LCD} = 2.22 × V_{REF} 0011b = V_{LCD} = 2.27 × V_{REF} 0100b = V_{LCD} = 2.32 × V_{REF} 0101b = V_{LCD} = 2.37 × V_{REF} 0110b = V_{LCD} = 2.42 × V_{REF} 0111b = V_{LCD} = 2.47 × V_{REF} 1000b = V_{LCD} = 2.52 × V_{REF} 1001b = V_{LCD} = 2.57 × V_{REF} 1010b = V_{LCD} = 2.62 × V_{REF} 1011b = V_{LCD} = 2.67 × V_{REF} 1100b = V_{LCD} = 2.72 × V_{REF} 1101b = V_{LCD} = 2.77 × V_{REF} 1110b = V_{LCD} = 2.82 × V_{REF} 1111b = V_{LCD} = 2.87 × V_{REF}
8	Reserved	R	0h	Reserved. Always reads as 0.

Table 1-9. LCDBVCTL Register Description (continued)

Bit	Field	Type	Reset	Description
7	LCDREXT	RW	0h	V2 to V4 voltage on external Rx3 pins. This bit selects the external connections for voltages V2 to V4 with internal bias generation (LCDEXTBIAS = 0). The bit is don't care if external biasing is selected (LCDEXTBIAS = 1). Settings for this bit should be changed only while LCDON = 0. 0b = Internally generated V2 to V4 are not switched to pins (LCDEXTBIAS = 0). 1b = Internally generated V2 to V4 are switched to pins (LCDEXTBIAS = 0).
6	R03EXT	RW	0h	V5 voltage select. This bit selects the external connection for the lowest LCD voltage. R03EXT is ignored if there is no R03 pin available. Settings for this bit should be changed only while LCDON = 0. 0b = V5 is V_{SS} 1b = V5 is sourced from the R03 pin
5	LCDEXTBIAS	RW	0h	V2 to V4 voltage select. This bit selects the generation for voltages V2 to V4. Settings for this bit should be changed only while LCDON = 0. 0b = V2 to V4 are generated internally. 1b = V2 to V4 are sourced externally and the internal bias generator is switched off.
4	VLCDEXT	RW	0h	V_{LCD} source select Settings for this bit should be changed only while LCDON = 0. 0b = V_{LCD} is generated internally. 1b = V_{LCD} is sourced externally.
3	LCDCPEN	RW	0h	Charge pump enable 0b = Charge pump disabled 1b = Charge pump enabled when V_{LCD} is generated internally (VLCDEXT = 0) and VLCDx > 0 or VLCDREFx > 0.
2-1	VLCDREFx	RW	0h	Charge pump reference select If LCDEXTBIAS = 1 or LCDREXT = 1 settings 01, 10 and 11 are not supported. Internal reference voltage used instead. Settings for this bit should be changed only while LCDON = 0. 00b = Internal reference voltage 01b = External reference voltage 10b = Internal reference voltage switched to external pin LCDREF/R13. 11b = Reserved. Defaults to external reference voltage.
0	LCD2B	RW	0h	Bias select. LCD2B is ignored when LCDMx = 00. 0b = 1/3 bias 1b = 1/2 bias

1.3.6 LCDBPCTL0 Register

LCD_B Port Control Register 0

Figure 1-17. LCDBPCTL0 Register

15	14	13	12	11	10	9	8
LCDS15	LCDS14	LCDS13	LCDS12	LCDS11	LCDS10	LCDS9	LCDS8
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDS7	LCDS6	LCDS5	LCDS4	LCDS3	LCDS2	LCDS1	LCDS0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-10. LCDBPCTL0 Register Description

Bit	Field	Type	Reset	Description
15-0	LCDSx	RW	0h	LCD segment line x enable This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0b = Multiplexed pins are port functions. 1b = Pins are LCD functions.

1.3.7 LCDBPCTL1 Register

LCD_B Port Control Register 1

Figure 1-18. LCDBPCTL1 Register

15	14	13	12	11	10	9	8
LCDS31	LCDS30	LCDS29	LCDS28	LCDS27	LCDS26	LCDS25	LCDS24
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDS23	LCDS22	LCDS21	LCDS20	LCDS19	LCDS18	LCDS17	LCDS16
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-11. LCDBPCTL1 Register Description

Bit	Field	Type	Reset	Description
15-0	LCDSx	RW	0h	LCD segment line x enable LCDS27 to LCDS31 are reserved on devices supporting a maximum of 96 segments. This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0b = Multiplexed pins are port functions. 1b = Pins are LCD functions.

1.3.8 LCDBPCTL2 Register

LCD_B Port Control Register 2 (≥ 128 Segments)

Figure 1-19. LCDBPCTL2 Register

15	14	13	12	11	10	9	8
LCDS47	LCDS46	LCDS45	LCDS44	LCDS43	LCDS42	LCDS41	LCDS40
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LCDS39	LCDS38	LCDS37	LCDS36	LCDS35	LCDS34	LCDS33	LCDS32
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-12. LCDBPCTL2 Register Description

Bit	Field	Type	Reset	Description
15-0	LCDSx	RW	0h	LCD segment line x enable LCDS35 to LCDS47 are reserved on devices supporting a maximum of 128 segments. LCDS43 to LCDS47 are reserved on devices supporting a maximum of 160 segments. This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. 0b = Multiplexed pins are port functions. 1b = Pins are LCD functions.

1.3.9 LCDBPCTL3 Register

LCD_B Port Control Register 2 (192 Segments)

Figure 1-20. LCDBPCTL3 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					LCDS50	LCDS49	LCDS48
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0

Table 1-13. LCDBPCTL3 Register Description

Bit	Field	Type	Reset	Description
15-3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	LCDSx	RW	0h	LCD segment line x enable This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. NOTE: Settings for LCDSx should be changed only while LCDON = 0. 0b = Multiplexed pins are port functions. 1b = Pins are LCD functions.

1.3.10 LCDBCPCTL Register

LCD_B Charge Pump Control Register

Figure 1-21. LCDBCPCTL Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
LCDCPDIS7	LCDCPDIS6	LCDCPDIS5	LCDCPDIS4	LCDCPDIS3	LCDCPDIS2	LCDCPDIS1	LCDCPDIS0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-14. LCDBCPCTL Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved. Always reads as 0.
7	LCDCPDIS7	RW	0h	Reserved
6	LCDCPDIS6	RW	0h	Reserved
5	LCDCPDIS5	RW	0h	Reserved
4	LCDCPDIS4	RW	0h	Reserved
3	LCDCPDIS3	RW	0h	Reserved
2	LCDCPDIS2	RW	0h	LCD charge pump disable during ADC12 conversion 0b = LCD charge pump not automatically disabled during conversion. 1b = LCD charge pump automatically disabled during conversion.
1	LCDCPDIS1	RW	0h	Reserved
0	LCDCPDIS0	RW	0h	Reserved

1.3.11 LCDBIV Register

LCD_B Interrupt Vector Register

Figure 1-22. LCDBIV Register

15	14	13	12	11	10	9	8
LCDBIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
LCDBIVx							
r0	r0	r0	r0	r0	r0	r0	r0

Table 1-15. LCDBIV Register Description

Bit	Field	Type	Reset	Description
15-0	LCDBIVx	R	0h	LCD_B interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: No capacitor connected; Interrupt Flag: LCDNOCAPIFG; Interrupt Priority: Highest 04h = Interrupt Source: Blink, segments off; Interrupt Flag: LCDBLKOFFIFG 06h = Interrupt Source: Blink, segments on; Interrupt Flag: LCDBLKONIFG 08h = Interrupt Source: Frame interrupt; Interrupt Flag: LCDFRMIFG; Interrupt Priority: Lowest

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