LCD_C Controller

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The most current version of the full user's guide is available from http://www.ti.com/lit/pdf/slau208.

The LCD_C controller drives static and 2-mux to 8-mux LCDs. This chapter describes the LCD_C controller. The differences between LCD_B and LCD_C are listed in Table 1-1.

Topic **Page**

1.1 LCD_C Introduction

The LCD_C controller directly drives LCD displays by automatically creating the ac segment and common voltage signals. The LCD_C controller can support static and 2-mux to 8-mux LCD glasses.

The LCD_C controller features are:

- Display memory
- Automatic signal generation
- Configurable frame frequency
- Blinking of individual segments with separate blinking memory for static, and 2- to 4-mux LCDs
- Blinking of complete display for 5- to 8-mux LCDs
- Regulated charge pump up to 3.44 V (typical)
- Contrast control by software
- Support for the following types of LCDs
  - Static
  - 2-mux, 1/2 bias or 1/3 bias
  - 3-mux, 1/2 bias or 1/3 bias
  - 4-mux, 1/2 bias or 1/3 bias
  - 5-mux, 1/3 bias
  - 6-mux, 1/3 bias
  - 7-mux, 1/3 bias
  - 8-mux, 1/3 bias

The differences between LCD_B and LCD_C are listed in Table 1-1.

Table 1-1. Differences Between LCD_B and LCD_C

Feature	LCD_B	LCD_C
Supported types of LCDs	Static, 2-, 3-, 4-mux	Static, 2-, 3-, 4-, 5-, 6-, 7, 8-mux
Maximum VLCDx settings	001111b	001111b
Maximum LCD voltage ($V_{LCD,typ}$)	3.44 V	3.44 V
Supported biasing schemes for 5-mux to 8-mux	5- to 8-mux not supported	1/3 biasing

Figure 1-1 shows the LCD controller block diagram.

NOTE: Maximum LCD Segment Control

The maximum number of segment lines and memory registers available differs with device. See the device-specific data sheet for available segment pins and the maximum number of segments supported.

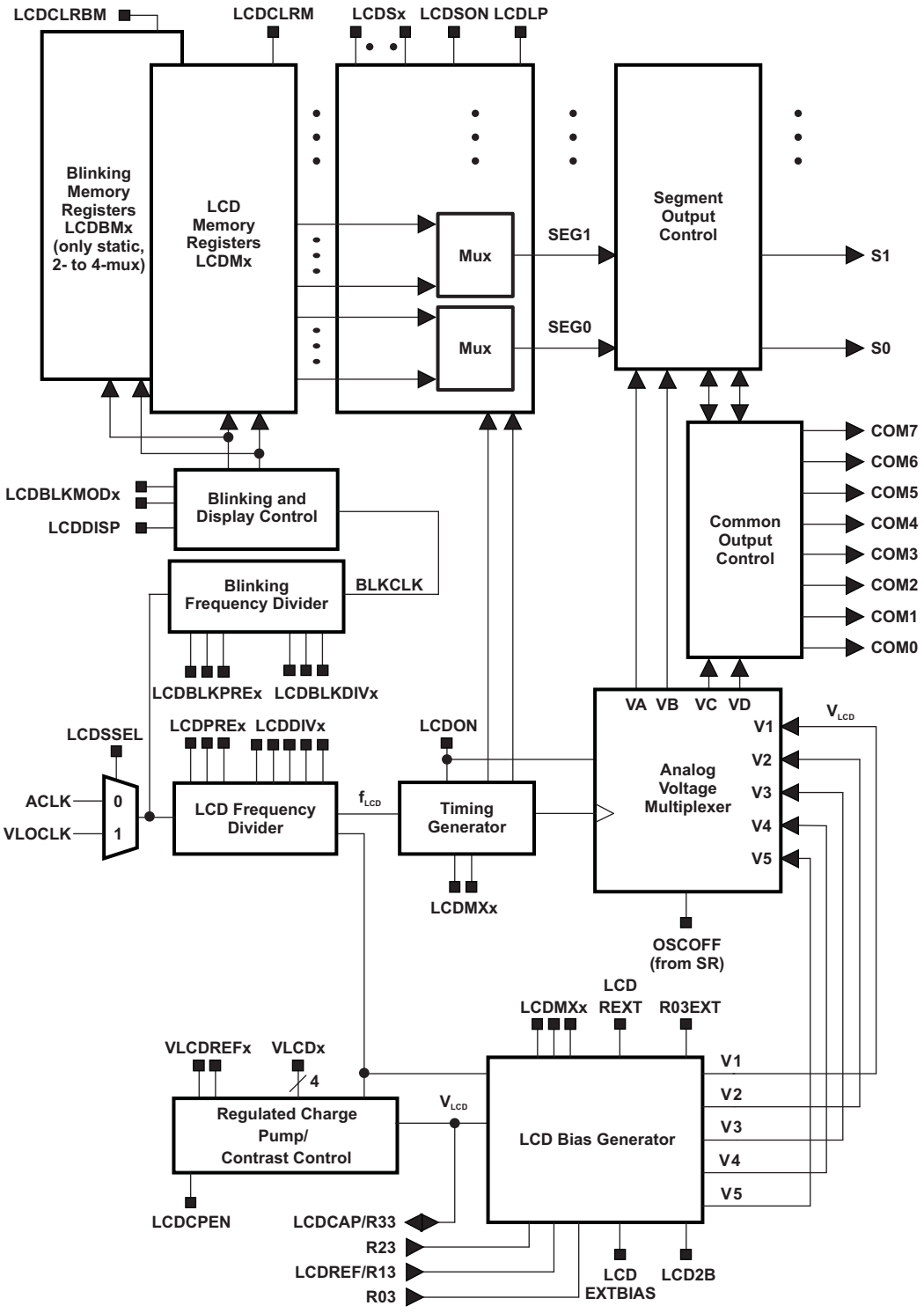

Figure 1-1. LCD Controller Block Diagram

1.2 LCD_C Operation

The LCD controller is configured with user software. The setup and operation of the LCD controller is discussed in the following sections.

1.2.1 LCD Memory

The LCD memory organization differs slightly depending on the mode.

Each memory bit corresponds to one LCD segment or is not used, depending on the mode. To turn on an LCD segment, its corresponding memory bit is set.

The memory can also be accessed word-wise using the even addresses starting at LCDM1, LCDM3, ...

Setting the bit LCDCLRM clears all LCD memory registers at the next frame boundary. It is reset automatically after the registers are cleared.

1.2.1.1 Static and 2-Mux to 4-Mux Mode

For static and 2-mux to 4-mux modes, one byte of the LCD memory contains the information for two segment lines. Figure 1-2 shows an example LCD memory map for these modes with 160 segments.

Associated Common Pins	3	2	1	0	3	2	1	0		
Register	7							0	n	Associated Segment Pins
LCDM20	--	--	--	--	--	--	--	--	38	39, 38
LCDM19	--	--	--	--	--	--	--	--	36	37, 36
LCDM18	--	--	--	--	--	--	--	--	34	35, 34
LCDM17	--	--	--	--	--	--	--	--	32	33, 32
LCDM16	--	--	--	--	--	--	--	--	30	31, 30
LCDM15	--	--	--	--	--	--	--	--	28	29, 28
LCDM14	--	--	--	--	--	--	--	--	26	27, 26
LCDM13	--	--	--	--	--	--	--	--	24	25, 24
LCDM12	--	--	--	--	--	--	--	--	22	23, 22
LCDM11	--	--	--	--	--	--	--	--	20	21, 20
LCDM10	--	--	--	--	--	--	--	--	18	19, 18
LCDM9	--	--	--	--	--	--	--	--	16	17, 16
LCDM8	--	--	--	--	--	--	--	--	14	15, 14
LCDM7	--	--	--	--	--	--	--	--	12	13, 12
LCDM6	--	--	--	--	--	--	--	--	10	1, 10
LCDM5	--	--	--	--	--	--	--	--	8	9, 8
LCDM4	--	--	--	--	--	--	--	--	6	7, 6
LCDM3	--	--	--	--	--	--	--	--	4	5, 4
LCDM2	--	--	--	--	--	--	--	--	2	3, 2
LCDM1	--	--	--	--	--	--	--	--	0	1, 0
	Sn+1				Sn					

Figure 1-2. LCD Memory for Static and 2-Mux to 4-Mux Mode - Example for 160 Segments

1.2.1.2 5-Mux to 8-Mux Mode

For 5-mux to 8-mux modes, one byte of the LCD memory contains the information for one segment line. Figure 1-3 shows an example LCD memory map for these modes with 160 segments.

Associated Common Pins	7	6	5	4	3	2	1	0		Associated Segment Pins
Register	7							0	n	
LCDM20	--	--	--	--	--	--	--	--	19	19
LCDM19	--	--	--	--	--	--	--	--	18	18
LCDM18	--	--	--	--	--	--	--	--	17	17
LCDM17	--	--	--	--	--	--	--	--	16	16
LCDM16	--	--	--	--	--	--	--	--	15	15
LCDM15	--	--	--	--	--	--	--	--	14	14
LCDM14	--	--	--	--	--	--	--	--	13	13
LCDM13	--	--	--	--	--	--	--	--	12	12
LCDM12	--	--	--	--	--	--	--	--	11	11
LCDM11	--	--	--	--	--	--	--	--	10	10
LCDM10	--	--	--	--	--	--	--	--	9	9
LCDM9	--	--	--	--	--	--	--	--	8	8
LCDM8	--	--	--	--	--	--	--	--	7	7
LCDM7	--	--	--	--	--	--	--	--	6	6
LCDM6	--	--	--	--	--	--	--	--	5	5
LCDM5	--	--	--	--	--	--	--	--	4	4
LCDM4	--	--	--	--	--	--	--	--	3	3
LCDM3	--	--	--	--	--	--	--	--	2	2
LCDM2	--	--	--	--	--	--	--	--	1	1
LCDM1	--	--	--	--	--	--	--	--	0	0
	Sn									

Figure 1-3. LCD Memory for 5-Mux to 8-Mux Mode - Example for 160 Segments

1.2.2 LCD Timing Generation

The LCD_C controller uses the f_{LCD} signal from the integrated clock divider to generate the timing for common and segment lines. With the LCDSSEL bit, ACLK with a frequency between 30 kHz and 40 kHz or VLOCLK can be selected as clock source into the divider. The f_{LCD} frequency is selected with the LCDPREx and LCDDIVx bits. The resulting f_{LCD} frequency is calculated by:

$$f_{LCD} = \frac{f_{ACLK/VLOCLK}}{(LCDDIVx + 1) \times 2^{LCDPRE}}$$

The proper f_{LCD} frequency depends on the LCD's requirement for framing frequency and the LCD multiplex rate. It is calculated by:

$f_{LCD} = 2 \times mux \times f_{Frame}$

For example, to calculate f_{LCD} for a 3-mux LCD with a frame frequency of 30 Hz to 100 Hz:

f_{Frame} (from LCD data sheet) = 30 Hz to 100 Hz

$f_{LCD} = 2 \times 3 \times f_{Frame}$

$f_{LCD}(min) = 180$ Hz

$f_{LCD}(max) = 600$ Hz

With $f_{ACLK/VLOCLK}$ = 32768 Hz, LCDPREx = 011, and LCDDIVx = 10101:

$f_{LCD} = 32768 \text{ Hz} / ((21+1) \times 2^3) = 32768 \text{ Hz} / 176 = 186 \text{ Hz}$

With LCDPREx = 001 and LCDDIVx = 11011:

f_{LCD} = 32768 Hz / ((27+1) × 2^1) = 32768 Hz / 56 = 585 Hz

The lowest frequency has the lowest current consumption. The highest frequency has the least flicker.

1.2.3 Blanking the LCD

The LCD controller allows blanking the complete LCD. The LCDSON bit is combined with a logical AND with each segment's memory bit. When LCDSON = 1, each segment is on or off according to its bit value. When LCDSON = 0, each LCD segment is off.

1.2.4 LCD Blinking

The LCD controller also supports blinking. In static and 2-mux to 4-mux mode, the blinking mode LCDBLKMODx = 01 allows blinking of individual segments; with LCDBLKMODx = 10 all segments are blinking; and with LCDBLKMODx = 00 blinking is disabled. In 5-mux mode and above, only blinking mode LCDBLKMODx = 10 that allows blinking of all segments is available; if another mode is selected, blinking is disabled.

1.2.4.1 Blinking Memory

In static and 2-mux to 4-mux mode, a separate blinking memory is implemented to select the blinking segments. To enable individual segments for blinking, the corresponding bit in the blinking memory LCDBMx registers must be set. The memory uses the same structure as the LCD memory (see Figure 1-2). Each memory bit corresponds to one LCD segment or is not used, depending on the multiplexing mode LCDMXx. To enable blinking for a LCD segment, its corresponding memory bit is set.

The blinking memory can also be accessed word-wise using the even addresses starting at LCDBM1, LCDBM3, ...

Setting the bit LCDCLRBM clears all blinking memory registers at the next frame boundary. It is automatically reset after the registers are cleared.

1.2.4.2 Blinking Frequency

The blinking frequency f_{BLINK} is selected with the LCDBLKPREx and LCDBLKDIVx bits. The same clock is used as selected for the LCD frequency f_{LCD}. The resulting f_{BLINK} frequency is calculated by:

$$f_{Blink} = \frac{f_{ACLK/VLO}}{(LCDBLKDIVx + 1) \times 2^{9+LCDBLKPREx}}$$

The divider generating the blinking frequency f_{BLINK} is reset when LCDBLKMODx = 00. After a blinking mode LCDBLKMODx = 01 or 10 is selected, the enabled segments or all segments go blank at the next frame boundary and stay off for half of a BLKCLK period. Then they go active at the next frame boundary and stay on for another half BLKCLK period before they go blank again at a frame boundary.

NOTE: Blinking Frequency Restrictions

The blinking frequency must be smaller than the frame frequency f_{Frame}.

The blinking frequency should only be changed when LCDBLKMODx = 00.

1.2.4.3 Dual Display Memory

In static and 2-mux to 4-mux mode, the blinking memory can also be used as a secondary display memory when no blinking mode LCDBLKMODx = 01 or 10 is selected. The memory to be displayed can be selected either manually using the LCDDISP bit or automatically with LCDBLKMODx = 11.

With LCDDISP = 0, the LCD memory is selected, and with LCDDISP = 1 the blinking memory is selected as display memory. Switching between the memories is synchronized to the frame boundaries.

With LCDBLKMODx = 11 the LCD controller switches automatically between the memories using the divider to generate the blinking frequency. After LCDBLKMODx = 11 is selected, the memory to be displayed for the first half a BLKCLK period is the LCD memory. In the second half, the blinking memory is used as display memory. Switching between the memories is synchronized to the frame boundaries.

1.2.5 LCD Voltage And Bias Generation

The LCD_C module allows selectable sources for the peak output waveform voltage, V1, as well as the fractional LCD biasing voltages V2 to V5. V_{LCD} may be sourced from V_{CC}, an internal charge pump, or externally.

All internal voltage generation is disabled if the selected clock source (ACLK or VLOCLK) is turned off (OSCOFF = 1) or the LCD_C module is disabled (LCDON = 0).

1.2.5.1 LCD Voltage Selection

V_{LCD} is sourced from V_{CC} when VLCDEXT = 0, VLCDx = 0, and VREFx = 0. V_{LCD} is sourced from the internal charge pump when VLCDEXT = 0, VLCDCPEN = 1, and VLCDx > 0. The charge pump is always sourced from DV_{CC}. The VLCDx bits provide a software selectable LCD voltage from 2.6 V to 3.44 V (typical) independent of DV_{CC}. See the device-specific data sheet for specifications.

When the internal charge pump is used, a 4.7-µF or larger capacitor must be connected between the LCDCAP pin and ground. If no capacitor is connected and the charge pump is enabled, the LCDNOCAPIFG interrupt flag is set, and the charge pump is disabled to prevent damage to the device.

To reduce system noise the charge pump can be temporarily disabled. It is disabled when LCDCPEN = 0 and re-enabled when LCDCPEN is changed back to 1. If the charge pump is temporarily disabled the voltage stored on the external capacitor is used for the LCD voltages until the charge pump is re-enabled.

Some devices can also automatically disable the charge pump during certain periods of time (for example during an ADC conversion). To enable this feature set the corresponding LCDCPDISx bits in the LCDBCPCTL register. For details see the device-specific data sheet (if the feature is not listed in the data sheet it is not supported by the respective device).

NOTE: Capacitor Required For Internal Charge Pump

A 4.7-µF or larger capacitor must be connected from the LCDCAP pin to ground when the internal charge pump is enabled. If no capacitor is connected, the LCDNOCAPIFG interrupt flag is set and the charge pump is disabled.

The internal charge pump may use an external reference voltage when VLCDREFx = 01 (and LCDREXT = 0 and LCDEXTBIAS = 0). In this case, the charge pump voltage is set to a multiply of the external reference voltage according to the VLCDx bits setting.

When VLCDEXT = 1, V_{LCD} is sourced externally from the LCDCAP, pin and the internal charge pump is disabled.

1.2.5.2 LCD Bias Generation

The fractional LCD biasing voltages, V2 to V5 can be generated internally or externally, independent of the source for V_{LCD}.

The bias generation block diagram for LCD_C static and 2-mux to 8-mux modes is shown in Figure 1-4.

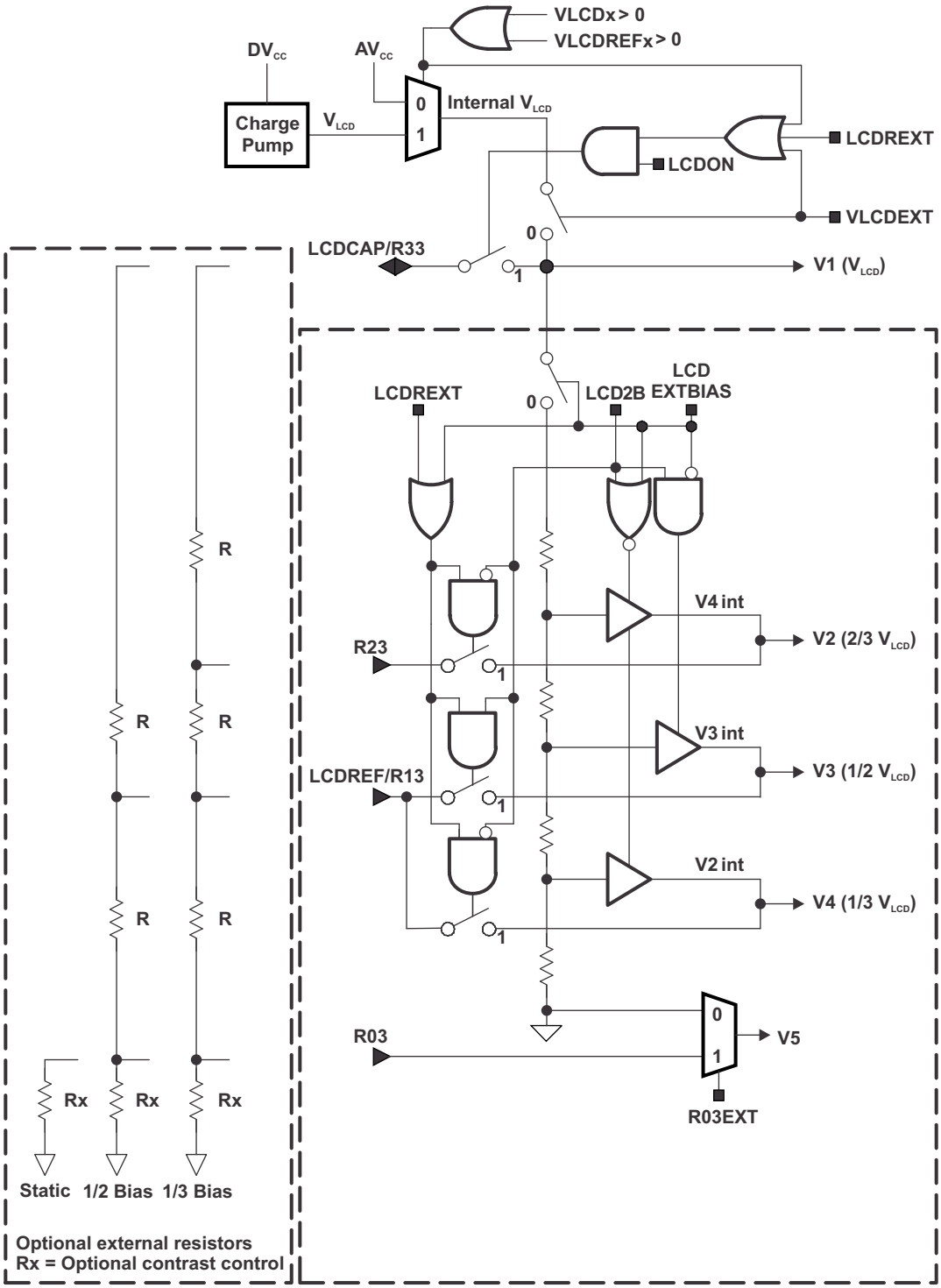

Figure 1-4. Bias Generation

The internally generated bias voltages V2 to V4 are switched to external pins with LCDREXT = 1.

To source the bias voltages V2 to V4 externally, LCDEXTBIAS is set. This also disables the internal bias generation. Typically, an equally weighted resistor divider is used with resistors ranging from a few kΩ to 1 MΩ, depending on the size of the display. When using an external resistor divider, the V_{LCD} voltage may be sourced from the internal charge pump when VLCDEXT = 0 taking the maximum charge pump load current into account. V5 can also be sourced externally when R03EXT = 1. In static mode and all mux modes using 1/2 biasing or 1/3 biasing, when R03EXT = 1 V5 can control the contrast of the connected display by changing the voltage at the low end of the external resistor divider Rx as shown in the left part of Figure 1-4.

When using an external resistor divider, R33 may serve as a switched V_{LCD} output when VLCDEXT = 0. This allows the power to the resistor ladder to be turned off, which eliminates current consumption when the LCD is not used. When VLCDEXT = 1, R33 serves as a V_{LCD} input.

The bias generator supports 1/2 biasing when LCD2B = 1 and 1/3 biasing when LCD2B = 0. In static mode, the internal divider is disabled.

Table 1-2. Bias Voltages and external Pins

Mode	Bias Configuration	LCD2B	Voltage Level	Pin	Condition
Static	Static	X	V1 ("1")	R33	if LCDREXT = 1 or LCDEXTBIAS = 1
			V5 ("0")	R03	if R03EXT = 1
2-mux, 3-mux, 4-mux	1/2	1	V1 ("1")	R33	if LCDREXT = 1 or LCDEXTBIAS = 1
			V3 ("1/2")	R13	if LCDREXT = 1 or LCDEXTBIAS = 1
			V5 ("0")	R03	if R03EXT = 1
2-mux, 3-mux, 4-mux	1/3	0	V1 ("1")	R33	if LCDREXT = 1 or LCDEXTBIAS = 1
			V2 ("2/3")	R23	if LCDREXT = 1 or LCDEXTBIAS = 1
			V4 ("1/3")	R13	if LCDREXT = 1 or LCDEXTBIAS = 1
			V5 ("0")	R03	if R03EXT = 1
5-mux to 8-mux	1/3	0	V1 ("1")	R33	if LCDREXT = 1 or LCDEXTBIAS = 1
			V2 ("2/3")	R23	if LCDREXT = 1 or LCDEXTBIAS = 1
			V4 ("1/3")	R13	if LCDREXT = 1 or LCDEXTBIAS = 1
			V5 ("0")	R03	if R03EXT = 1

1.2.5.3 LCD Contrast Control

The peak voltage of the output waveforms together with the selected mode and biasing determine the contrast and the contrast ratio of the LCD. The LCD contrast can be controlled in software by adjusting the LCD voltage generated by the integrated charge pump using the VLCDx settings.

The contrast ratio depends on the used LCD display and the selected biasing scheme. Table 1-3 shows the biasing configurations that apply to the different modes together with the RMS voltages for the segments turned on ($V_{RMS,ON}$) and turned off ($V_{RMS,OFF}$) as functions of V_{LCD}. It also shows the resulting contrast ratios between the on and off states.

Table 1-3. LCD Voltage and Biasing Characteristics

Mode	Bias Config	LCDMx	LCD2B	COM Lines	Voltage Levels	$V_{RMS,OFF}/ V_{LCD}$	$V_{RMS,ON}/ V_{LCD}$	Contrast Ratio $V_{RMS,ON}/ V_{RMS,OFF}$
Static	Static	0000	X	1	V1, V5	0	1	1/0
2-mux	1/2 (1)	0001	1	2	V1, V3, V5	0.354	0.791	2.236
	1/3	0001	0	2	V1, V2, V4, V5	0.333	0.745	2.236
3-mux	1/2	0010	1	3	V1, V3, V5	0.408	0.707	1.732
	1/3 (1)	0010	0	3	V1, V2, V4, V5	0.333	0.638	1.915
4-mux	1/2	0011	1	4	V1, V3, V5	0.433	0.661	1.528
	1/3 (1)	0011	0	4	V1, V2, V4, V5	0.333	0.577	1.732
5-mux	1/3 (1)	0100	0	5	V1, V2, V4, V5	0.333	0.537	1.612
6-mux	1/3 (1)	0101	0	6	V1, V2, V4, V5	0.333	0.509	1.528
7-mux	1/3(1)	0110	0	7	V1, V2, V4, V5	0.333	0.488	1.464
8-mux	1/3(1)	0111	0	8	V1, V2, V4, V5	0.333	0.471	1.414

(1) Recommended setting to achieve best contrast

A typical approach to determine the required V_{LCD} is by equating $V_{RMS,OFF}$ with a LCD threshold voltage provided by the LCD manufacturer, for example when the LCD exhibits approximately 10% contrast ($V_{th,10\%}$): $V_{RMS,OFF} = V_{th,10\%}$. Using the values for $V_{RMS,OFF}/V_{LCD}$ provided in the table results in $V_{LCD} = V_{th,10\%}/(V_{RMS,OFF}/V_{LCD})$. In the static mode, a suitable choice is V_{LCD} greater than or equal to three times $V_{th,10\%}$.

In 3-mux and 4-mux mode, a 1/3 biasing is typically used, but a 1/2 biasing scheme is also possible. The 1/2 bias reduces the contrast ratio, but the advantage is a reduction of the required full-scale LCD voltage V_{LCD}.

1.2.6 LCD Outputs

Some LCD segment, common, and Rxx functions are multiplexed with digital I/O functions. These pins can function either as digital I/O or as LCD functions.

The LCD segment functions, when multiplexed with digital I/O, are selected using the LCDSx bits in the LCDCPCTLx registers. The LCDSx bits select the LCD function for each segment line. When LCDSx = 0, a multiplexed pin is set to digital I/O function. When LCDSx = 1, a multiplexed pin is selected as LCD function.

The pin functions for COMx and Rxx, when multiplexed with digital I/O, are selected as described in the port schematic section of the device-specific data sheet. An some devices the COM1 to COM7 pins are shared with segment lines, refer to the device-specific data sheet. If these pins are required as COM pins due to the selected LCD multiplexing mode, the COM functionality takes precedence over the segment function that can be selected for those pins with the LCDSx bits as for all other segment pins.

See the port schematic section of the device-specific data sheet for details on controlling the pin functionality.

NOTE: LCDSx Bits Do Not Affect Dedicated LCD Segment Pins

The LCDSx bits only affect pins with multiplexed LCD segment functions and digital I/O functions. Dedicated LCD segment pins are not affected by the LCDSx bits.

1.2.7 LCD Interrupts

The LCD_C module has four interrupt sources available, each with independent enables and flags.

The four interrupt flags, namely LCDFRMIFG, LCDBLKOFFIFG, LCDBLKONIFG, and LCDNOCAPIFG, are prioritized and combined to source a single interrupt vector. The interrupt vector register LCDCIV is used to determine which flag requested an interrupt.

The highest priority enabled interrupt generates a number in the LCDCIV register (see register description). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled LCD interrupts do not affect the LCDCIV value.

Any read access of the LCDCIV register automatically resets the highest pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt. A write access to the LCDCIV register automatically resets all pending interrupt flags. In addition, all flags can be cleared by software.

The LCDNOCAPIFG indicates that no capacitor is present at the LCDCAP pin when the charge pump is enabled. Setting the LCDNOCAPIE bit enables the interrupt.

The LCDBLKONIFG is set at the BLKCLK edge synchronized to the frame boundaries that turns on the segments when blinking is enabled with LCDBLKMODx = 01 or 10. It is also set at the BLKCLK edge synchronized to the frame boundaries that selects the blinking memory as display memory when LCDBLKMODx = 11. It is automatically cleared when a LCD or blinking memory register is written. Setting the LCDBLKONIE bit enables the interrupt.

The LCDBLKOFFIFG is set at the BLKCLK edge synchronized to the frame boundaries that blanks the segments when blinking is enabled with LCDBLKMODx = 01 or 10. It is also set at the BLKCLK edge synchronized to the frame boundaries that selects the LCD memory as display memory when LCDBLKMODx = 11. It is automatically cleared when a LCD or blinking memory register is written. Setting the LCDBLKOFFIE bit enables the interrupt.

The LCDFRMIFG is set at a frame boundary. It is automatically cleared when a LCD or blinking memory register is written. Setting the LCDFRMIFGIE bit enables the interrupt.

1.2.7.1 LCDCIV Software Example

The following software example shows the recommended use of LCDCIV and the handling overhead. The LCDCIV value is added to the PC to automatically jump to the appropriate routine.

The numbers at the right margin show the necessary CPU cycles for each instruction. The software overhead for different interrupt sources includes interrupt latency and return-from-interrupt cycles, but not the task handling itself.

```
; Interrupt handler for LCD_B interrupt flags.
LCDB_HND             ; Interrupt latency          6
   ADD &LCDBIV,PC    ; Add offset to Jump table   3
   RETI              ; Vector 0: No interrupt     5
   JMP LCDNOCAP_HND  ; Vector 2: LCDNOCAPIFG      2
   JMP LCDBLKON_HND  ; Vector 4: LCDBLKONIFG      2
   JMP LCDBLKOFF_HND ; Vector 6: LCDBLKOFFIFG     2
LCDFRM_HND           ; Vector 8: LCDFRMIFG
   ...    ; Task starts here
   RETI                                          5
LCDNOCAP_HND ; Vector 2: LCDNOCAPIFG
   ... ; Task starts here
   RETI                                          5
LCDBLKON_HND ; Vector 4: LCDBLKONIFG
   ... ; Task starts here
   RETI ; Back to main program                   5
LCDBLKOFF_HND ; Vector 6: LCDBLKOFFIFG
   ... ; Task starts here
   RETI ; Back to main program                   5
```

1.2.8 Static Mode

In static mode, each MSP430 segment pin drives one LCD segment, and one common line (COM0) is used. Figure 1-5 shows some example static waveforms.

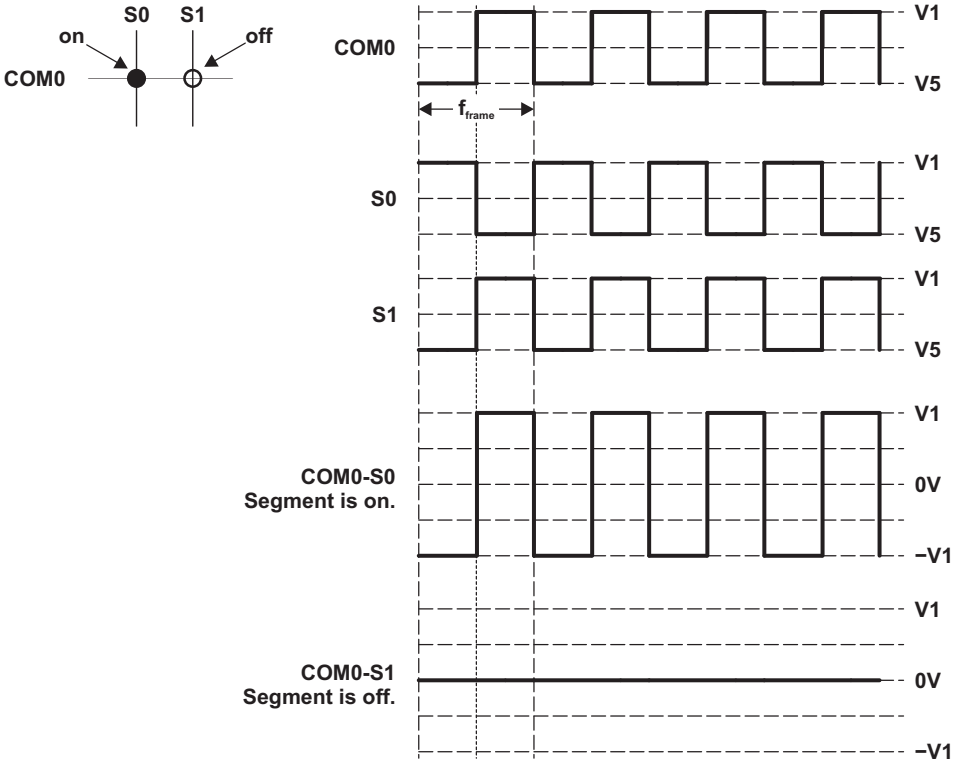

Figure 1-5. Example Static Waveforms

1.2.9 2-Mux Mode

In 2-mux mode, each MSP430 segment pin drives two LCD segments, and two common lines (COM0 and COM1) are used. Figure 1-6 shows some example 2-mux 1/2-bias waveforms.

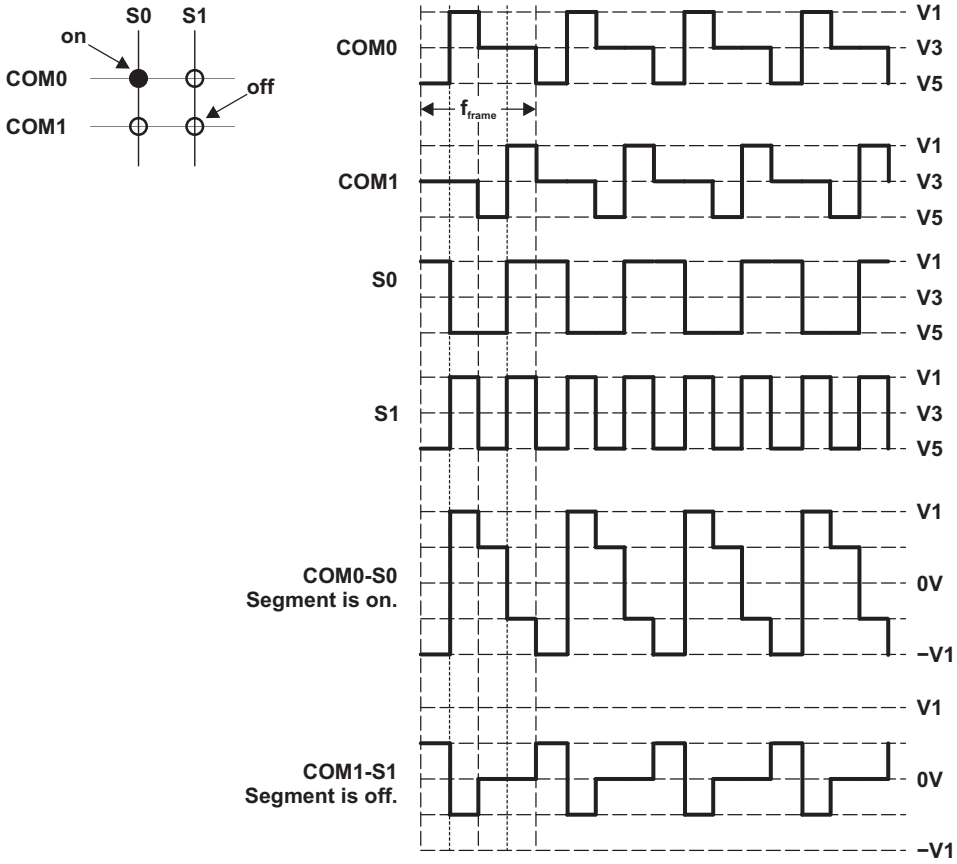

Figure 1-6. Example 2-Mux Waveforms

1.2.10 3-Mux Mode

In 3-mux mode, each MSP430 segment pin drives three LCD segments, and three common lines (COM0, COM1, and COM2) are used. Figure 1-7 shows some example 3-mux 1/3-bias waveforms.

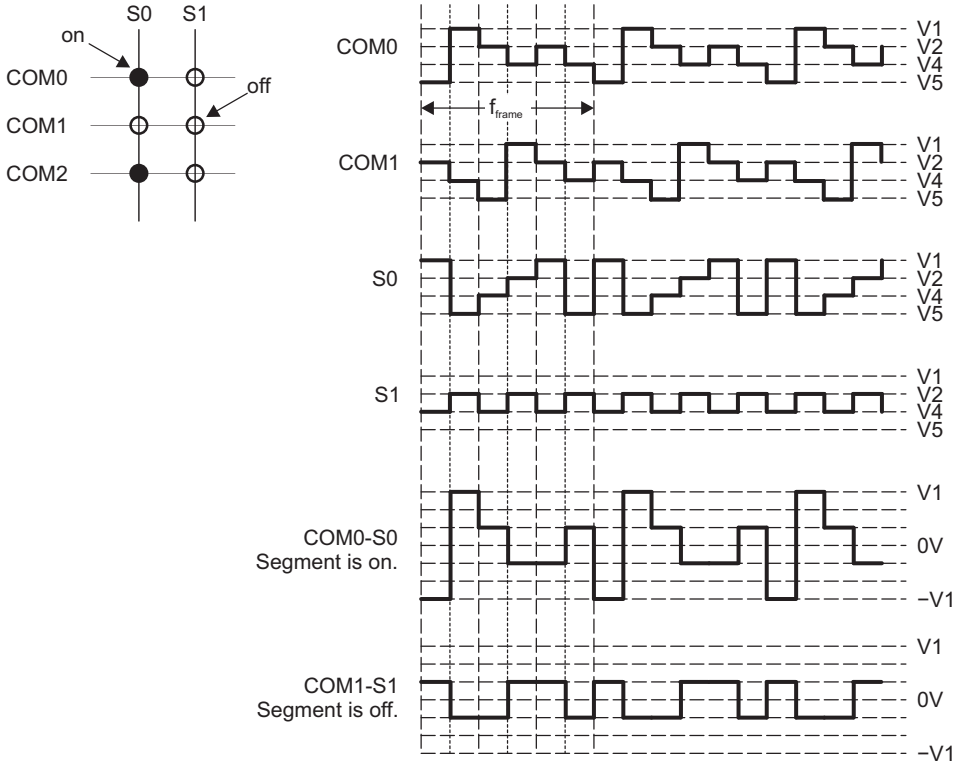

Figure 1-7. Example 3-Mux Waveforms

1.2.11 4-Mux Mode

In 4-mux mode, each MSP430 segment pin drives four LCD segments and four common lines (COM0, COM1, COM2, and COM3) are used. Figure 1-8 shows some example 4-mux 1/3-bias waveforms.

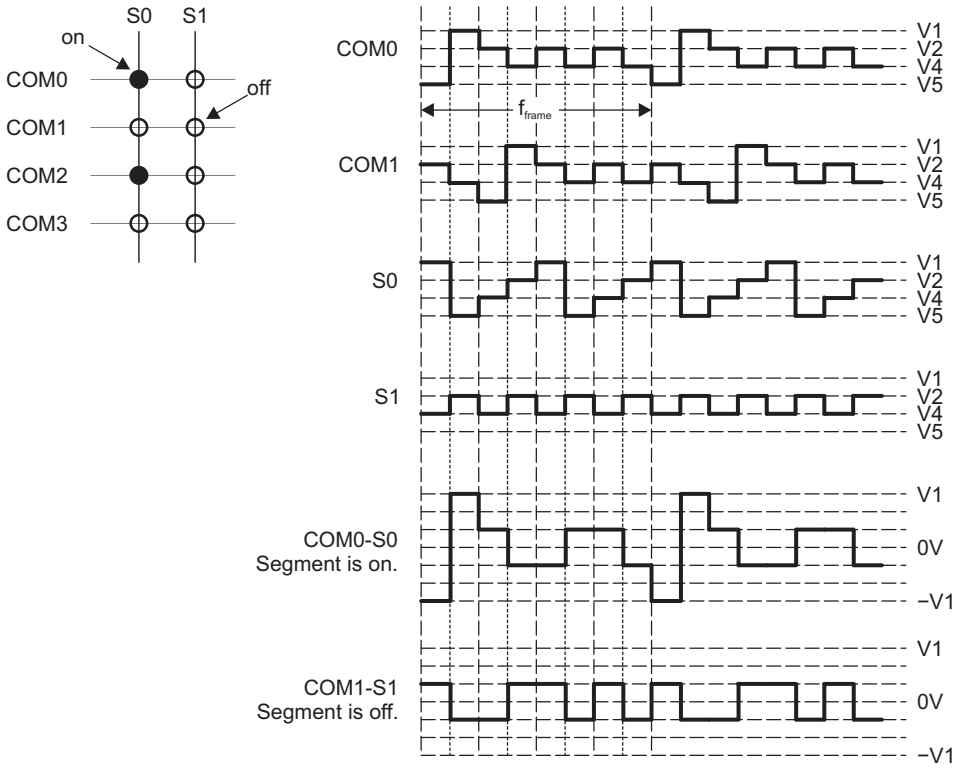

Figure 1-8. Example 4-Mux Waveforms

1.2.12 6-Mux Mode

In 6-mux mode, each MSP430 segment pin drives six LCD segments, and six common lines (COM0, COM1, COM2, COM3, COM4, and COM5) are used. Figure 1-9 shows some example 6-mux 1/3-bias waveforms.

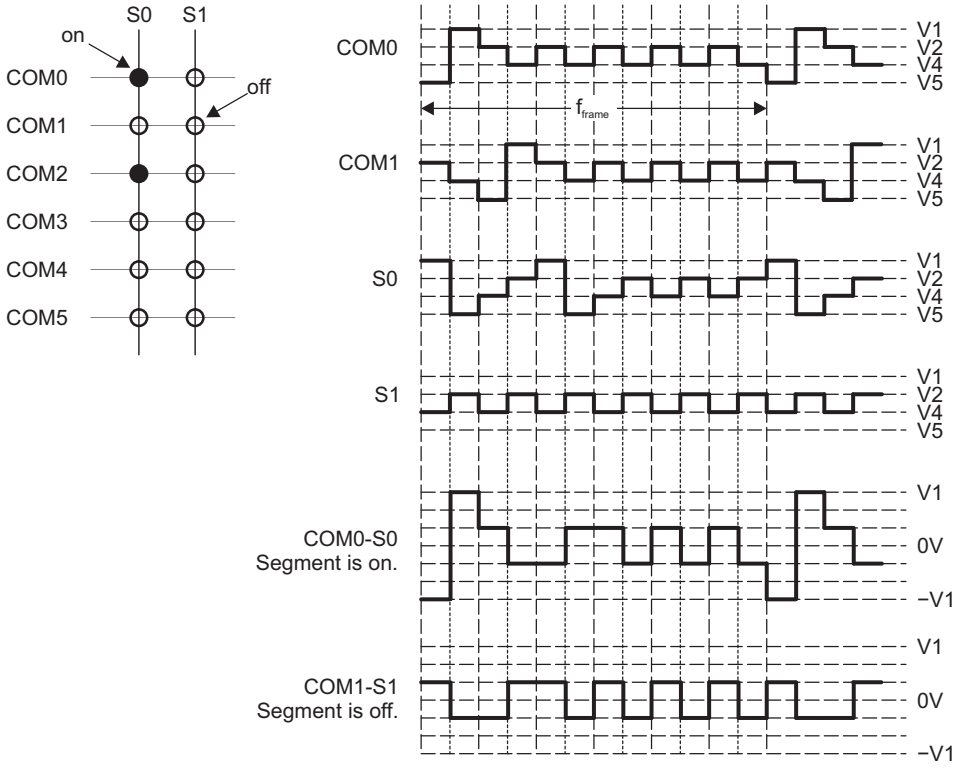

Figure 1-9. Example 6-Mux Waveforms

1.2.13 8-Mux Mode

In 8-mux mode, each MSP430 segment pin drives eight LCD segments, and eight common lines (COM0 through COM7) are used. Figure 1-10 shows some example 8-mux 1/3-bias waveforms.

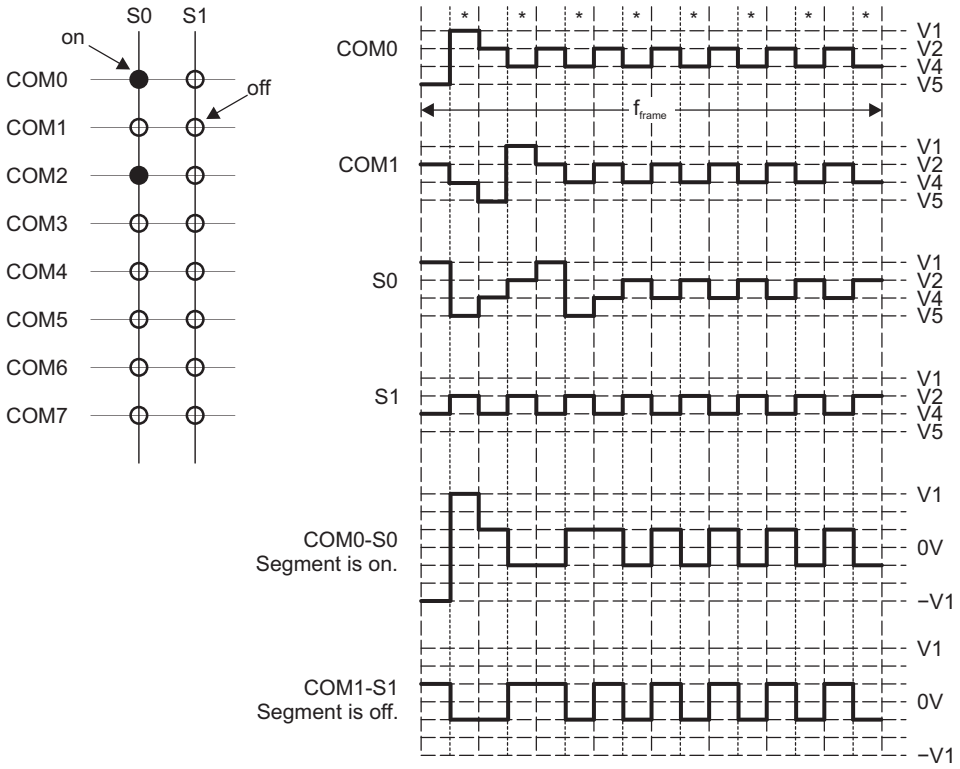

Figure 1-10. Example 8-Mux, 1/3 Bias Waveforms (LCDLP = 0)

Figure 1-11 shows some example 8-mux 1/3-bias waveforms with LCDLP = 1. With LCDLP = 1, the voltage sequence compared to the non-low power waveform is reshuffled; that is, all of the timeslots marked with "*" in Figure 1-10 are grouped together. The same principle applies to all mux modes.

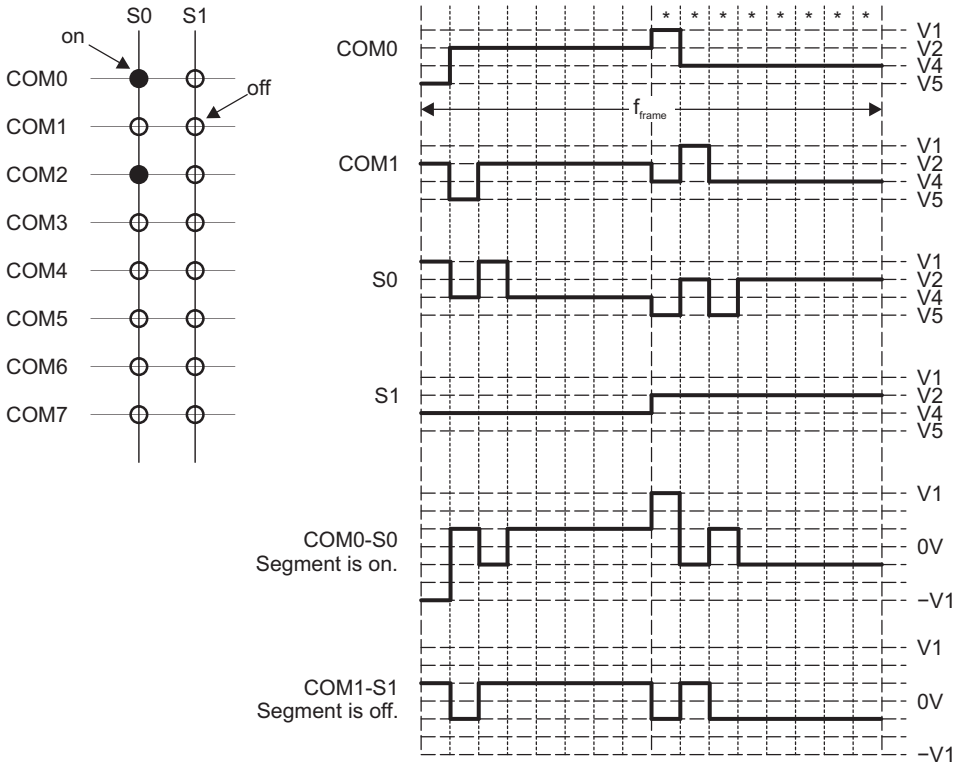

Figure 1-11. Example 8-Mux, 1/3 Bias Low-Power Waveforms (LCDLP = 1)

1.3 LCD_C Registers

The LCD_C registers are listed in Table 1-4 to Table 1-7. The LCD memory and blinking memory registers can also be accessed as word.

The number of available memory registers on a given device depends on the number of available segment pins; see the device-specific data sheet.

Table 1-4. LCD_C Control Registers

Offset	Acronym	Register Name	Type	Reset	Section
000h	LCDCCTL0	LCD_C control 0	Read/write	0000h	Section 1.3.1
002h	LCDCCTL1	LCD_C control 1	Read/write	0000h	Section 1.3.2
004h	LCDCBLKCTL	LCD_C blinking control	Read/write	0000h	Section 1.3.3
006h	LCDCMEMCTL	LCD_C memory control	Read/write	0000h	Section 1.3.4
008h	LCDCVCTL	LCD_C voltage control	Read/write	0000h	Section 1.3.5
00Ah	LCDCPCTL0	LCD_C port control 0	Read/write	0000h	Section 1.3.6
00Ch	LCDCPCTL1	LCD_C port control 1	Read/write	0000h	Section 1.3.7
00Eh	LCDCPCTL2	LCD_C port control 2 (≥256 segments)	Read/write	0000h	Section 1.3.8
010h	LCDCPCTL3	LCD_C port control 3 (384 segments)	Read/write	0000h	Section 1.3.9
012h	LCDCCPCTL	LCD_C charge pump control	Read/write	0000h	Section 1.3.10
014h		Reserved			
016h		Reserved			
018h		Reserved			
01Ah		Reserved			
01Ch		Reserved			
01Eh	LCDCIV	LCD_C interrupt vector	Read/write	0000h	Section 1.3.11

Table 1-5. LCD_C Memory Registers for Static and 2-Mux to 4-Mux Modes(1)(2)

Offset	Acronym	Register Name	Type	Reset
020h	LCDM1	LCD memory 1 (S1/S0)	Read/write	Unchanged
021h	LCDM2	LCD memory 2 (S3/S2)	Read/write	Unchanged
022h	LCDM3	LCD memory 3 (S5/S4)	Read/write	Unchanged
023h	LCDM4	LCD memory 4 (S7/S6)	Read/write	Unchanged
024h	LCDM5	LCD memory 5 (S9/S8)	Read/write	Unchanged
025h	LCDM6	LCD memory 6 (S11/S10)	Read/write	Unchanged
026h	LCDM7	LCD memory 7 (S13/S12)	Read/write	Unchanged
027h	LCDM8	LCD memory 8 (S15/S14)	Read/write	Unchanged
028h	LCDM9	LCD memory 9 (S17/S16)	Read/write	Unchanged
029h	LCDM10	LCD memory 10 (S19/S18)	Read/write	Unchanged
02Ah	LCDM11	LCD memory 11 (S21/S20)	Read/write	Unchanged
02Bh	LCDM12	LCD memory 12 (S23/S22)	Read/write	Unchanged
02Ch	LCDM13	LCD memory 13 (S25/S24)	Read/write	Unchanged
02Dh	LCDM14	LCD memory 14 (S27/S26)	Read/write	Unchanged
02Eh	LCDM15	LCD memory 15 (S29/S28)	Read/write	Unchanged
02Fh	LCDM16	LCD memory 16 (S31/S30)	Read/write	Unchanged
030h	LCDM17	LCD memory 17 (S33/S32)	Read/write	Unchanged
031h	LCDM18	LCD memory 18 (S35/S34)	Read/write	Unchanged
032h	LCDM19	LCD memory 19 (S37/S36)	Read/write	Unchanged
033h	LCDM20	LCD memory 20 (S39/S38)	Read/write	Unchanged
034h	LCDM21	LCD memory 21 (S41/S40)	Read/write	Unchanged
035h	LCDM22	LCD memory 22 (S43/S42)	Read/write	Unchanged
036h	LCDM23	LCD memory 23 (S45/S44)	Read/write	Unchanged
037h	LCDM24	LCD memory 24 (S47/S46)	Read/write	Unchanged
038h	LCDM25	LCD memory 25 (S49/S48)	Read/write	Unchanged
039h	LCDM26	LCD memory 26 (S51/S50)	Read/write	Unchanged
03Ah	LCDM27	LCD memory 27 (S53/S52)	Read/write	Unchanged
03Bh	LCDM28	LCD memory 28 (S54)	Read/write	Unchanged
03Ch		Reserved		
03Dh		Reserved		
03Eh		Reserved		
03Fh		Reserved		

(1) The LCD memory registers can also be accessed as word.

(2) The number of available memory registers on a given device depends on the number of available segment pins; see the device-specific data sheet.

Table 1-6. LCD Blinking Memory Registers for Static and 2-Mux to 4-Mux Modes(1)(2)

Offset	Acronym	Register Name	Type	Reset
040h	LCDBM1	LCD blinking memory 1	Read/write	Unchanged
041h	LCDBM2	LCD blinking memory 2	Read/write	Unchanged
042h	LCDBM3	LCD blinking memory 3	Read/write	Unchanged
043h	LCDBM4	LCD blinking memory 4	Read/write	Unchanged
044h	LCDBM5	LCD blinking memory 5	Read/write	Unchanged
045h	LCDBM6	LCD blinking memory 6	Read/write	Unchanged
046h	LCDBM7	LCD blinking memory 7	Read/write	Unchanged
047h	LCDBM8	LCD blinking memory 8	Read/write	Unchanged
048h	LCDBM9	LCD blinking memory 9	Read/write	Unchanged
049h	LCDBM10	LCD blinking memory 10	Read/write	Unchanged
04Ah	LCDBM11	LCD blinking memory 11	Read/write	Unchanged
04Bh	LCDBM12	LCD blinking memory 12	Read/write	Unchanged
04Ch	LCDBM13	LCD blinking memory 13	Read/write	Unchanged
04Dh	LCDBM14	LCD blinking memory 14	Read/write	Unchanged
04Eh	LCDBM15	LCD blinking memory 15	Read/write	Unchanged
04Fh	LCDBM16	LCD blinking memory 16	Read/write	Unchanged
050h	LCDBM17	LCD blinking memory 17	Read/write	Unchanged
051h	LCDBM18	LCD blinking memory 18	Read/write	Unchanged
052h	LCDBM19	LCD blinking memory 19	Read/write	Unchanged
053h	LCDBM20	LCD blinking memory 20	Read/write	Unchanged
054h	LCDBM21	LCD blinking memory 21	Read/write	Unchanged
055h	LCDBM22	LCD blinking memory 22	Read/write	Unchanged
056h	LCDBM23	LCD blinking memory 23	Read/write	Unchanged
057h	LCDBM24	LCD blinking memory 24	Read/write	Unchanged
058h	LCDBM25	LCD blinking memory 25	Read/write	Unchanged
059h	LCDBM26	LCD blinking memory 26	Read/write	Unchanged
05Ah	LCDBM27	LCD blinking memory 27	Read/write	Unchanged
05Bh	LCDBM28	LCD blinking memory 28	Read/write	Unchanged
05Ch		Reserved		
05Dh		Reserved		
05Eh		Reserved		
05Fh		Reserved		

(1) The LCD blinking memory registers can also be accessed as word.

(2) The number of available memory registers on a given device depends on the number of available segment pins; see the device-specific data sheet.

Table 1-7. LCD Memory Registers for 5-Mux to 8-Mux(1)(2)

Offset	Acronym	Register Name	Type	Reset
020h	LCDM1	LCD memory 1 (S0)	Read/write	Unchanged
021h	LCDM2	LCD memory 2 (S1)	Read/write	Unchanged
022h	LCDM3	LCD memory 3 (S2)	Read/write	Unchanged
023h	LCDM4	LCD memory 4 (S3)	Read/write	Unchanged
024h	LCDM5	LCD memory 5 (S4)	Read/write	Unchanged
025h	LCDM6	LCD memory 6 (S5)	Read/write	Unchanged
026h	LCDM7	LCD memory 7 (S6)	Read/write	Unchanged
027h	LCDM8	LCD memory 8 (S7)	Read/write	Unchanged
028h	LCDM9	LCD memory 9 (S8)	Read/write	Unchanged
029h	LCDM10	LCD memory 10 (S9)	Read/write	Unchanged
02Ah	LCDM11	LCD memory 11 (S10)	Read/write	Unchanged
02Bh	LCDM12	LCD memory 12 (S11)	Read/write	Unchanged
02Ch	LCDM13	LCD memory 13 (S12)	Read/write	Unchanged
02Dh	LCDM14	LCD memory 14 (S13)	Read/write	Unchanged
02Eh	LCDM15	LCD memory 15 (S14)	Read/write	Unchanged
02Fh	LCDM16	LCD memory 16 (S15)	Read/write	Unchanged
030h	LCDM17	LCD memory 17 (S16)	Read/write	Unchanged
031h	LCDM18	LCD memory 18 (S17)	Read/write	Unchanged
032h	LCDM19	LCD memory 19 (S18)	Read/write	Unchanged
033h	LCDM20	LCD memory 20 (S19)	Read/write	Unchanged
034h	LCDM21	LCD memory 21 (S20)	Read/write	Unchanged
035h	LCDM22	LCD memory 22 (S21)	Read/write	Unchanged
036h	LCDM23	LCD memory 23 (S22)	Read/write	Unchanged
037h	LCDM24	LCD memory 24 (S23)	Read/write	Unchanged
038h	LCDM25	LCD memory 25 (S24)	Read/write	Unchanged
039h	LCDM26	LCD memory 26 (S25)	Read/write	Unchanged
03Ah	LCDM27	LCD memory 27 (S26)	Read/write	Unchanged
03Bh	LCDM28	LCD memory 28 (S27)	Read/write	Unchanged
03Ch	LCDM29	LCD memory 29 (S28)	Read/write	Unchanged
03Dh	LCDM30	LCD memory 30 (S29)	Read/write	Unchanged
03Eh	LCDM31	LCD memory 31 (S30)	Read/write	Unchanged
03Fh	LCDM32	LCD memory 32 (S31)	Read/write	Unchanged
040h	LCDM33	LCD memory 33 (S32)	Read/write	Unchanged
041h	LCDM34	LCD memory 34 (S33)	Read/write	Unchanged
042h	LCDM35	LCD memory 35 (S34)	Read/write	Unchanged
043h	LCDM36	LCD memory 36 (S35)	Read/write	Unchanged
044h	LCDM37	LCD memory 37 (S36)	Read/write	Unchanged
045h	LCDM38	LCD memory 38 (S37)	Read/write	Unchanged
046h	LCDM39	LCD memory 39 (S38)	Read/write	Unchanged
047h	LCDM40	LCD memory 40 (S39)	Read/write	Unchanged
048h	LCDM41	LCD memory 41 (S40)	Read/write	Unchanged
049h	LCDM42	LCD memory 42 (S41)	Read/write	Unchanged
04Ah	LCDM43	LCD memory 43 (S42)	Read/write	Unchanged
04Bh	LCDM44	LCD memory 44 (S43)	Read/write	Unchanged
04Ch	LCDM45	LCD memory 45 (S44)	Read/write	Unchanged

(1) The LCD memory registers can also be accessed as word.

(2) The number of available memory registers on a given device depends on the number of available segment pins; see the device-specific data sheet.

Table 1-7. LCD Memory Registers for 5-Mux to 8-Mux[1][2] (continued)

Offset	Acronym	Register Name	Type	Reset
04Dh	LCDM46	LCD memory 46 (S45)	Read/write	Unchanged
04Eh	LCDM47	LCD memory 47 (S46)	Read/write	Unchanged
04Fh	LCDM48	LCD memory 48 (S47)	Read/write	Unchanged
050h	LCDM49	LCD memory 49 (S48)	Read/write	Unchanged
051h	LCDM50	LCD memory 50 (S49)	Read/write	Unchanged
052h	LCDM51	LCD memory 51 (S50)	Read/write	Unchanged
053h	LCDM52	LCD memory 52 (S51)	Read/write	Unchanged
054h		Reserved		
055h		Reserved		
056h		Reserved		
057h		Reserved		
058h		Reserved		
059h		Reserved		
05Ah		Reserved		
05Bh		Reserved		
05Ch		Reserved		
05Dh		Reserved		
05Eh		Reserved		
05Fh		Reserved		

1.3.1 LCDCCTL0 Register

LCD_C Control Register 0

NOTE: Settings for LCDDIVx, LCDPREx, LCDSSEL, LCDLP and LCDMXx should be changed only while LCDON = 0.

Figure 1-12. LCDCCTL0 Register

15	14	13	12	11	10	9	8
LCDDIVx					LCDPREx		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDSSEL	Reserved	LCDMXx			LCDSON	LCDLP	LCDON
rw-0	r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-8. LCDCCTL0 Register Description

Bit	Field	Type	Reset	Description
15-11	LCDDIVx	RW	0h	LCD frequency divider. Together with LCDPREx the LCD frequency f_{LCD} is calculated as $f_{LCD} = f_{ACLK/VLO} / ((LCDDIVx + 1) \times 2^{LCDPREx})$. 00000b = Divide by 1 00001b = Divide by 2 ⋮ 11110b = Divide by 31 11111b = Divide by 32
10-8	LCDPREx	RW	0h	LCD frequency pre-scaler. Together with LCDDIVx the LCD frequency f_{LCD} is calculated as $f_{LCD} = f_{ACLK/VLO} / ((LCDDIVx + 1) \times 2^{LCDPREx})$. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 4 011b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Reserved (defaults to divide by 32) 111b = Reserved (defaults to divide by 32)
7	LCDSSEL	RW	0h	Clock source select for LCD and blinking frequency 0b = ACLK (30 kHz to 40 kHz) 1b = VLOCLK
6	Reserved	R	0h	Reserved
5-3	LCDMXx	RW	0h	LCD mux rate. These bits select the LCD mode. 000b = Static 001b = 2-mux 010b = 3-mux 011b = 4-mux 100b = 5-mux 101b = 6-mux 110b = 7-mux 111b = 8-mux
2	LCDSON	RW	0h	LCD segments on. This bit supports flashing LCD applications by turning off all segment lines, while leaving the LCD timing generator and R33 enabled. 0b = All LCD segments are off 1b = All LCD segments are enabled and on or off according to their corresponding memory location
1	LCDLP	RW	0h	LCD low-power waveform 0b = Standard LCD waveforms on segment and common lines selected 1b = Low-power LCD waveforms on segment and common lines selected

Table 1-8. LCDCCTL0 Register Description (continued)

Bit	Field	Type	Reset	Description
0	LCDON	RW	0h	LCD on. This bit turns the LCD_C module on or off. 0b = LCD_C module off 1b = LCD_C module on

1.3.2 LCDCCTL1 Register

LCD_C Control Register 1

Figure 1-13. LCDCCTL1 Register

15	14	13	12	11	10	9	8
Reserved				LCDNOCAPIE	LCDBLKONIE	LCDBLKOFFIE	LCDFRMIE
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved				LCDNOCAPIFG	LCDBLKONIFG	LCDBLKOFFIFG	LCDFRMIFG
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0

Table 1-9. LCDCCTL1 Register Description

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0h	Reserved
11	LCDNOCAPIE	RW	0h	No capacitance connected interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
10	LCDBLKONIE	RW	0h	LCD blinking interrupt enable, segments switched on 0b = Interrupt disabled 1b = Interrupt enabled
9	LCDBLKOFFIE	RW	0h	LCD blinking interrupt enable, segments switched off 0b = Interrupt disabled 1b = Interrupt enabled
8	LCDFRMIE	RW	0h	LCD frame interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
7-4	Reserved	R	0h	Reserved
3	LCDNOCAPIFG	RW	0h	No capacitance connected interrupt flag. Set when charge pump is enabled but no capacitance is connected to LCDCAP pin. 0b = No interrupt pending 1b = Interrupt pending
2	LCDBLKONIFG	RW	0h	LCD blinking interrupt flag, segments switched on. Automatically cleared when data is written into a memory register. 0b = No interrupt pending 1b = Interrupt pending
1	LCDBLKOFFIFG	RW	0h	LCD blinking interrupt flag, segments switched off. Automatically cleared when data is written into a memory register. 0b = No interrupt pending 1b = Interrupt pending
0	LCDFRMIFG	RW	0h	LCD frame interrupt flag. Automatically cleared when data is written into a memory register. 0b = No interrupt pending 1b = Interrupt pending

1.3.3 LCDCBLKCTL Register

LCD_C Blink Control Register

NOTE: Settings for LCDBLKDIVx and LCDBLKPREx should only be changed while LCDBLKMODx = 00.

Figure 1-14. LCDCBLKCTL Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
LCDBLKDIVx			LCDBLKPREx			LCDBLKMODx	
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-10. LCDCBLKCTL Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved
7-5	LCDBLKDIVx	RW	0h	Clock divider for blinking frequency. Together with LCDBLKPREx, the blinking frequency f_{BLINK} is calculated as $f_{BLINK} = f_{ACLK/VLO} / ((LCDBLKDIVx + 1) \times 2^{9+LCDBLKPREx})$. NOTE: Should only be changed while LCDBLKMODx = 00. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8
4-2	LCDBLKPREx	RW	0h	Clock pre-scaler for blinking frequency. Together with LCDBLKDIVx, the blinking frequency f_{BLINK} is calculated as $f_{BLINK} = f_{ACLK/VLO} / ((LCDBLKDIVx + 1) \times 2^{9+LCDBLKPREx})$. NOTE: Should only be changed while LCDBLKMODx = 00. 000b = Divide by 512 001b = Divide by 1024 010b = Divide by 2048 011b = Divide by 4096 100b = Divide by 8162 101b = Divide by 16384 110b = Divide by 32768 111b = Divide by 65536
1-0	LCDBLKMODx	RW	0h	Blinking mode 00b = Blinking disabled 01b = Blinking of individual segments as enabled in blinking memory register LCDBMx. In mux mode >5 blinking is disabled. 10b = Blinking of all segments 11b = Switching between display contents as stored in LCDMx and LCDBMx memory registers. In mux mode >5 blinking is disabled.

1.3.4 LCDCMEMCTL Register

LCD_C Memory Control Register

Figure 1-15. LCDCMEMCTL Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved					LCDCLRBM	LCDCLRM	LCDDISP
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0

Table 1-11. LCDCMEMCTL Register Description

Bit	Field	Type	Reset	Description
15-3	Reserved	R	0h	Reserved
2	LCDCLRBM	RW	0h	Clear LCD blinking memory Clears all blinking memory registers LCDBMx. The bit is automatically reset when the blinking memory is cleared. Setting this bit has in 5-mux mode and above has no effect. It's immediately reset again. 0b = Contents of blinking memory registers LCDBMx remain unchanged 1b = Clear content of all blinking memory registers LCDBMx
1	LCDCLRM	RW	0h	Clear LCD memory Clears all LCD memory registers LCDMx. The bit is automatically reset when the LCD memory is cleared. 0b = Contents of LCD memory registers LCDMx remain unchanged 1b = Clear content of all LCD memory registers LCDMx
0	LCDDISP	RW	0h	Select LCD memory registers for display The bit is cleared in LCDBLKMODx = 01 and LCDBLKMODx = 10 or if a mux mode ≥5 is selected and cannot be changed by software. When LCDBLKMODx = 11, this bit reflects the currently displayed memory but cannot be changed by software. When returning to LCDBLKMODx = 00 the bit is cleared. 0b = Display content of LCD memory registers LCDMx 1b = Display content of LCD blinking memory registers LCDBMx

1.3.5 LCDCVCTL Register

LCD_C Voltage Control Register

NOTE: Settings for LCDREXT, R03EXT, LCDEXTBIAS, VLCDEXT, VLCDREFx, and LCD2B should be changed only while LCDON = 0.

Figure 1-16. LCDCVCTL Register

15	14	13	12	11	10	9	8
Reserved			VLCDx				Reserved
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	r0
7	6	5	4	3	2	1	0
LCDREXT	R03EXT	LCDEXTBIAS	VLCDEXT	LCDCPEN	VLCDREFx		LCD2B
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-12. LCDCVCTL Register Description

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0h	Reserved
12-9	VLCDx	RW	0h	Charge pump voltage select. LCDCPEN must be 1 for the charge pump to be enabled. VCC is used for V_{LCD} when VLCDx = 0000 and VLCDREFx = 00 and VLCDEXT = 0. 0000b = Charge pump disabled 0001b = If VLCDREFx = 00 or 10: V_{LCD} = 2.60 V; If VLCDREFx = 01 or 11: $V_{LCD} = 2.17 \times V_{REF}$ 0010b to 1110b = If VLCDREFx = 00 or 10: $V_{LCD} = 2.60\ V + (VLCDx - 1) \times 0.06\ V$; If VLCDREFx = 01 or 11: $V_{LCD} = 2.17 \times V_{REF} + (VLCDx - 1) \times 0.05 \times V_{REF}$ 1111b = If VLCDREFx = 00 or 10: $V_{LCD} = 2.60\ V + (15 - 1) \times 0.06\ V = 3.44\ V$; If VLCDREFx = 01 or 11: $V_{LCD} = 2.17 \times V_{REF} + (15 - 1) \times 0.05 \times V_{REF} = 2.87 \times V_{REF}$
8	Reserved	R	0h	Reserved
7	LCDREXT	RW	0h	V2 to V4 voltage on external Rx3 pins. This bit selects the external connections for voltages V2 to V4 with internal bias generation (LCDEXTBIAS = 0). The bit is don't care if external biasing is selected (LCDEXTBIAS = 1). NOTE: Should be changed only while LCDON = 0. 0b = Internally generated V2 to V4 are not switched to pins (LCDEXTBIAS = 0) 1b = Internally generated V2 to V4 are switched to pins (LCDEXTBIAS = 0)
6	R03EXT	RW	0h	V5 voltage select. This bit selects the external connection for the lowest LCD voltage. R03EXT is ignored if there is no R03 pin available. NOTE: Should be changed only while LCDON = 0. 0b = V5 is VSS 1b = V5 is sourced from the R03 pin
5	LCDEXTBIAS	RW	0h	V2 to V4 voltage select. This bit selects the generation for voltages V2 to V4. NOTE: Should be changed only while LCDON = 0. 0b = V2 to V4 are generated internally 1b = V2 to V4 are sourced externally and the internal bias generator is switched off
4	VLCDEXT	RW	0h	V_{LCD} source select NOTE: Should be changed only while LCDON = 0. 0b = V_{LCD} is generated internally 1b = V_{LCD} is sourced externally

Table 1-12. LCDCVCTL Register Description (continued)

Bit	Field	Type	Reset	Description
3	LCDCPEN	RW	0h	Charge pump enable 0b = Charge pump disabled 1b = Charge pump enabled when V_{LCD} is generated internally (VLCDEXT = 0) and VLCDx > 0 or VLCDREFx > 0
2-1	VLCDREFx	RW	0h	Charge pump reference select. If LCDEXTBIAS = 1 or LCDREXT = 1, settings 01, 10, and 11 are not supported; the internal reference voltage is used instead. NOTE: Should be changed only while LCDON = 0. 00b = Internal reference voltage 01b = External reference voltage 10b = Internal reference voltage switched to external pin LCDREF/R13 11b = Reserved (defaults to external reference voltage)
0	LCD2B	RW	0h	Bias select. LCD2B is ignored in static mode or mux modes ≥5. NOTE: Should be changed only while LCDON = 0. 0b = 1/3 bias 1b = 1/2 bias

1.3.6 LCDCPCTL0 Register

LCD_C Port Control Register 0

NOTE: Settings for LCDSx should be changed only while LCDON = 0.

Figure 1-17. LCDCPCTL0 Register

15	14	13	12	11	10	9	8
LCDS15	LCDS14	LCDS13	LCDS12	LCDS11	LCDS10	LCDS9	LCDS8
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDS7	LCDS6	LCDS5	LCDS4	LCDS3	LCDS2	LCDS1	LCDS0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-13. LCDCPCTL0 Register Description

Bit	Field	Type	Reset	Description
15-0	LCDSx	RW	0h	LCD segment line x enable. This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. NOTE: Settings for LCDSx should be changed only while LCDON = 0. 0b = Multiplexed pins are port functions 1b = Pins are LCD functions

1.3.7 LCDCPCTL1 Register

LCD_C Port Control Register 1

NOTE: Settings for LCDSx should be changed only while LCDON = 0.

Figure 1-18. LCDCPCTL1 Register

15	14	13	12	11	10	9	8
LCDS31	LCDS30	LCDS29	LCDS28	LCDS27	LCDS26	LCDS25	LCDS24
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDS23	LCDS22	LCDS21	LCDS20	LCDS19	LCDS18	LCDS17	LCDS16
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-14. LCDCPCTL1 Register Description

Bit	Field	Type	Reset	Description
15-0	LCDSx	RW	0h	LCD segment line x enable. On devices supporting a maximum of 192 segments LCDS31 is reserved, if COM7 to COM1 are shared with segments. If COM7 to COM1 are not shared with segments LCDS24 to LCDS31 are reserved. This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. NOTE: Settings for LCDSx should be changed only while LCDON = 0. 0b = Multiplexed pins are port functions 1b = Pins are LCD functions

1.3.8 LCDCPCTL2 Register

LCD_C Port Control Register 2 (≥ 256 Segments)

NOTE: Settings for LCDSx should be changed only while LCDON = 0.

Figure 1-19. LCDCPCTL2 Register

15	14	13	12	11	10	9	8
LCDS47	LCDS46	LCDS45	LCDS44	LCDS43	LCDS42	LCDS41	LCDS40
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
LCDS39	LCDS38	LCDS37	LCDS36	LCDS35	LCDS34	LCDS33	LCDS32
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-15. LCDCPCTL2 Register Description

Bit	Field	Type	Reset	Description
15-0	LCDSx	RW	0h	LCD segment line x enable. On devices supporting a maximum of 256 segments LCDS39 to LCDS47 are reserved, if COM7 to COM1 are shared with segments. If COM7 to COM1 are not shared with segments the complete register LCDCPCTL2 is not available. On devices supporting a maximum of 320 segments, LCDS47 is reserved if COM7 to COM1 are shared with segments. If COM7 to COM1 are not shared with segments, LCDS40 to LCDS47 are reserved. This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. NOTE: Settings for LCDSx should be changed only while LCDON = 0. 0b = Multiplexed pins are port functions 1b = Pins are LCD functions

1.3.9 LCDCPCTL3 Register

LCD_C Port Control Register 2 (384 Segments, COMs Shared With Segments)

NOTE: Settings for LCDSx should be changed only while LCDON = 0.

Figure 1-20. LCDCPCTL3 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved		LCDS53	LCDS52	LCDS51	LCDS50	LCDS49	LCDS48
r0	r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-16. LCDCPCTL3 Register Description

Bit	Field	Type	Reset	Description
15-6	Reserved	R	0h	Reserved
5-0	LCDSx	RW	0h	LCD segment line x enable. This bit affects only pins with multiplexed functions. Dedicated LCD pins are always LCD function. NOTE: Settings for LCDSx should be changed only while LCDON = 0. 0b = Multiplexed pins are port functions 1b = Pins are LCD functions

1.3.10 LCDCCPCTL Register

LCD_C Charge Pump Control Register

Figure 1-21. LCDCCPCTL Register

15	14	13	12	11	10	9	8
LCDCPCLKSYNC	Reserved						
rw-0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
LCDCPDISx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-17. LCDCCPCTL Register Description

Bit	Field	Type	Reset	Description
15	LCDCPCLKSYNC	RW	0h	LCD charge pump clock synchronization (device specific). The charge pump clock is synchronized to a device specific clock (device-specific) when the respective clock source is enabled and does not indicate a fault with its fault signal - if available. 0b = Synchronization disabled 1b = Synchronization enabled
14-8	Reserved	R	0h	Reserved
7-0	LCDCPDISx	RW	0h	LCD charge pump disable (number of implemented bits and connected function is device-specific) 0b = Connected function cannot disable charge pump 1b = Connected function can disable charge pump

1.3.11 LCDCIV Register

LCD_C Interrupt Vector Register

Figure 1-22. LCDCIV Register

15	14	13	12	11	10	9	8
LCDCIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
LCDCIVx							
r0	r0	r0	r0	r0	r0	r0	r0

Table 1-18. LCDCIV Register Description

Bit	Field	Type	Reset	Description
15-0	LCDCIVx	R	0h	LCD_C interrupt vector value 00h = No interrupt pending 02h = Interrupt Source: No capacitor connected; Interrupt Flag: LCDNOCAPIFG; Interrupt Priority: Highest 04h = Interrupt Source: Blink, segments off; Interrupt Flag: LCDBLKOFFIFG 06h = Interrupt Source: Blink, segments on; Interrupt Flag: LCDBLKONIFG 08h = Interrupt Source: Frame interrupt; Interrupt Flag: LCDFRMIFG; Interrupt Priority: Lowest

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