Chapter 1
SLAU422F–August 2012–Revised March 2018

Auxiliary Supply System (AUX)

The auxiliary supply system (AUX) allows the device to operate from alternate supplies (also called auxiliary supplies) if the primary supply (DVCC and AVCC) fails. The AUX includes simple charging circuitry to charge capacitors connected to the auxiliary supplies. This chapter describes the AUX.

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The latest version of the full user's guide can be downloaded from http://www.ti.com/lit/pdf/slau208.

Topic **Page**

1.1 Auxiliary Supply System Introduction

The auxiliary supply system features include:

- Automatic or manual switching from the primary supply to an auxiliary supply while maintaining full functionality.
- One or two auxiliary supplies (AUXVCC1 and AUXVCC2), depending on the specific device.
- Automatic threshold-based monitoring of primary and auxiliary supplies.
- At start-up, automatically chooses between the primary supply (DVCC/AVCC) and AUXVCC1, based on which one is higher voltage.
- A separate auxiliary supply (AUXVCC3) can power a backup subsystem [(1)].
- Simple charger for capacitors on AUXVCC2 and AUXVCC3.

NOTE: Unused auxiliary supplies

Any unused auxiliary supply inputs (AUXVCC1 or AUXVCC2) must be connected to DVSS.

If AUXVCC1 or AUXVCC2 are unused, they should be disabled by setting AUXxMD = 1 and AUXxOK = 0 in software, too.

If AUXVCC3 is not powered by a dedicated supply, it can either be connected to DVCC externally or powered by enabling the AUXVCC3 charger. If powered by the charger, the recommended capacitor should be connected externally. If AUXVCC3 is not powered or connected to DVSS, the backup subsystem (including, for example, the 32-kHz crystal oscillator) is not functional.

(1) The backup subsystem usually contains a real-time clock (RTC) module with a 32-kHz crystal oscillator, backup RAM, and optionally (device-specific) up to two digital I/O pins.

1.2 Auxiliary Supply Operation

The AUX module allows the device to switch between the primary supply (DVCC and AVCC) and up to two auxiliary supplies (AUXVCC1 and AUXVCC2) while maintaining full device functionality. When using an auxiliary supply, both AVCC and DVCC are switched to the same auxiliary supply.

Switching can be controlled automatically through hardware or manually through software. In the hardware-controlled mode, switching is triggered by the high-side supply voltage monitor (SVM), which must be enabled and configured as described in Section 1.2.4. In the software-controlled mode, switching is triggered by changing values in AUX module registers, as described in Section 1.2.3.

Figure 1-1 shows an overview of the auxiliary supply switches.

The digital core of the device is supplied through the Power Management Module (PMM) by the internal digital system voltage V_{DSYS}. In the PMM chapter of this user's guide, that supply is assumed to be DVCC; however, on devices with the AUX module, AUX switches V_{DSYS} among the DVCC, AUXVCC1, and AUXVCC2 inputs. V_{DSYS} is also output on the VDSYS pin, which must be connected to an external capacitor as specified in the device-specific data sheet.

The analog modules of the device are supplied by the internal analog system voltage V_{ASYS}. The AUX module switches V_{ASYS} among the AVCC, AUXVCC1, and AUXVCC2 inputs. V_{ASYS} is also output on the VASYS pin, which must be connected to an external capacitor as specified in the device-specific data sheet.

The switches for the digital and the analog system voltages are controlled by the same signals and always connect to the same voltage (primary voltage DVCC/AVCC, first auxiliary voltage AUXVCC1, or second auxiliary voltage AUXVCC2).

Auxiliary voltage AUXVCC3 supplies V_{BAK} to the backup subsystem, which usually contains a real-time clock (RTC) module with a 32-kHz crystal oscillator, some backup RAM, and optionally (device-specific) up to two digital I/O pins.

NOTE: Disabled SVS_H restricts access to backup subsystem

If the SVS_H is disabled, access to and control of modules located in the subsystem powered by AUXVCC3 is restricted:

- Changes to the LF crystal oscillator setting in the clock system do not take effect.
- The RTC, if enabled, together with the 32-kHz crystal oscillator continue to operate but the time and date information cannot be accessed.
- The data stored in the backup RAM (if available) is retained but cannot be accessed.

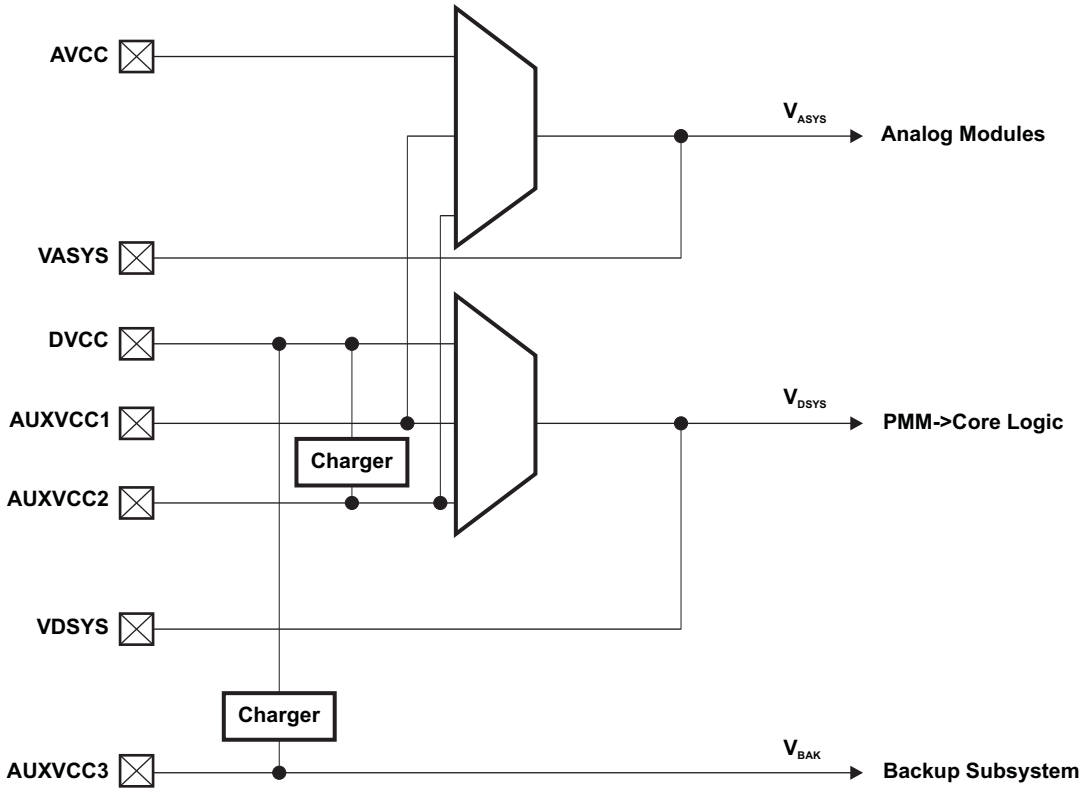


Figure 1-1. Auxiliary Supply Switch Overview

1.2.1 Start-up

The device starts whenever a supply is connected to DVCC or AUXVCC1. If both supplies are connected, AUX uses whichever voltage is higher to supply the digital and analog system voltages, V_{DSYS} and V_{ASYS}. If the supplies (DVCC/AVCC and AUXVCC1) differ by less than 100 mV, the selected supply can be either DVCC/AVCC or AUXVCC1. The supply with the higher voltage is selected only if the difference is greater than 100 mV.

After start-up from any condition that causes a BOR event (including connection of power or wake from LPMx.5), the AUX module is automatically locked. To configure the behavior of the auxiliary supply system, write AUXKEY = 0xA5 in the AUXCTL0 register to enable access to the AUXCTL1 and AUXCTL2 registers (see Section 1.2.2). After configuration is completed, the AUX module switches between the input supplies as defined during configuration.

NOTE: The AUXKEY field can be written only when LOCKAUX bit is clear. AUXKEY and LOCKAUX can be updated in the same CPU instruction.

If the LOCKAUX bit remains set, the device continues to be supplied by DVCC or AUXVCC1 (whichever was selected at start-up).

Section 1.2.7 describes additional considerations for setting the power supply before entering LPMx.5.

NOTE: Highest supply voltage

To ensure reliable operation, the selected supply voltage (by default, the highest voltage in the system) must always supply at least 0.5 µA to critical circuitry.

NOTE: DVCC and AUXVCC1 at start-up

Under normal operating conditions, TI recommends supplying DVCC by a voltage at least 100 mV higher than AUXVCC1. This ensures a reliable start-up from DVCC and avoids an unwanted start-up from AUXVCC1.

1.2.2 Switching Control

During normal operation (that is, when the LOCKAUX bit is cleared) switching to another supply is triggered either by software or by hardware (specifically, by the high-side SVM). Section 1.2.3 describes the configuration and control of the AUX for software-controlled switching. Section 1.2.4 describes configuration and control of the AUX for hardware-controlled switching. Section 1.2.13 includes examples of how to configure hardware-controlled mode based on different usage scenarios.

1.2.3 Software-Controlled Switching

To enable or disable a supply using software-controlled switching:

1. To enable software control of a supply, set AUXxMD = 1 (AUX0MD for DVCC, AUX1MD for AUXVCC1, and AUX2MD for AUXVCC2).
2. To select the supply to use, set AUXxOK = 1 (AUX0OK for DVCC, AUX1OK for AUXVCC1, and AUX2OK for AUXVCC2).

   When AUXxOK is set, the AUX module immediately switches to the specified supply.

   If AUXxOK = 1 for more than one supply, AUX uses the one with the highest priority. The default priority is DVCC, then AUXVCC1, then AUXVCC2. To make AUXVCC2 priority higher than AUXVCC1, set AUX2PRIO = 1.
3. To disable a supply, clear AUXxOK = 0. If the current supply is software-controlled (AUXxMD = 1) and AUXxOK is changed from 1 to 0, the next available supply (considering the priority defined by AUX2PRIO) is used to source the system voltages.

When a switch from one supply to another occurs, interrupts are generated as described in Section 1.2.11.

The software control can be used to permanently disable a supply or, for example, to qualify the quality of the supplies by measuring the actual supply voltage with an ADC (see Section 1.2.9) instead of using the auxiliary supply monitor (see Section 1.2.6).

When using software-controlled mode for all supplies, the SVS and SVM in the PMM are not required. They may be enabled, and they will operate as described in the PMM chapter, but they do not interact with the AUX during software-controlled mode.

1.2.4 Hardware-Controlled Switching

To enable hardware-controlled switching, clear AUXxMD = 0 (AUX0MD for DVCC, AUX1MD for AUXVCC1, and AUX2MD for AUXVCC2). A supply can be disabled and excluded from the automatic switching system by setting the corresponding AUXxMD = 1 and AUXxOK = 0. For example, to disable AUXVCC2, set AUX2MD = 1 and AUX2OK = 0.

During hardware-controlled switching, the SVM in the PMM must be enabled and configured. The SVS can also be enabled and operates as described in the PMM chapter, but it does not interact with the AUX module.

The high-side SVM of the PMM monitors V_{DSYS}, which is output from the AUX module. If V_{DSYS} falls below the voltage set by the SVSMHRRVL bits, the SVM notifies AUX to switch to the next valid supply. AUX switches to the next valid supply immediately after receiving the trigger from the SVM. When a switch occurs, interrupts are generated as described in Section 1.2.11.

NOTE: Voltage dip on V_{DSYS}

Because the SVM does not signal AUX to change the supply until the voltage on V_{DSYS} falls to the SVM monitoring level (set in the SVSMHRRL bits), there is a dip in V_{DSYS} from the nominal operating level. This change in voltage must be considered when selecting system frequency and core voltage (see Section 1.2.5).

AUX determines which supplies are valid based on the threshold voltage set in the AUXxLVL bits. The validity of a supply is reported by the corresponding AUXxOK bit. When AUXxMD = 0, the AUXxOK bit is controlled by hardware and cannot be written by software. AUXxOK = 1 indicates a valid or "good" supply voltage, and AUXxOK = 0 indicates an invalid or "bad" supply voltage. See Section 1.2.6 for details on the monitoring of the auxiliary supplies.

NOTE: Interactions among SVM_H, V_{CORE}, and AUX

Because of the relationship between supply voltage, core voltage, and maximum system frequency, see Section 1.2.5 for considerations when setting the AUXxLVL and SVM_H levels.

In particular, note that AUX0LVL must be higher than the SVM_H level.

The selection of the next valid supply depends on the state of the AUXxOK and AUX2PRIO bits when the trigger occurs as shown in Table 1-1. If no valid supply is available to switch to (that is, all other AUXxOK bits are 0) no switching takes place, and the device eventually goes into reset if the current supply continues to fall. To avoid rapid switching back and forth between supplies, any further switching is prevented during a "recovery time" of several hundred microseconds as specified in the device-specific data sheetafter each switch-over.

Table 1-1. Next Supply Voltage Selection

Current Supply	Next Supply[1]	DVCC OK? (AUX0OK)	AUXVCC1 OK? (AUX1OK)	AUXVCC2 OK? (AUX2OK)	AUXVCC1/ AUXVCC2 Priority (AUX2PRIO)
DVCC/AVCC	AUXVCC1	don't care	1	don't care	0
		don't care	1	0	1
	AUXVCC2	don't care	0	1	don't care
		don't care	1	1	1
AUXVCC1	DVCC	1	don't care	don't care	don't care
	AUXVCC2	0	don't care	1	don't care
AUXVCC2	DVCC	1	don't care	don't care	don't care
	AUXVCC1	0	1	don't care	don't care

(1) If there is no valid supply available to switch to, no switching takes place.

NOTE: Special case for switching to DVCC/AVCC

If the device is supplied by AUXVCC1 or AUXVCC2, and the AUX0OK bit transitions from 0 to 1 (either by hardware or by software), AUX switches to the DVCC/AVCC supply without any signal from the SVM.

AUX does not automatically switch from AUX2VCC to AUX1VCC when AUX1OK transitions from 0 to 1, unless the SVM signals that a switch is necessary.

1.2.5 Interactions Among f_{SYS}, V_{CORE}, V_{DSYS}, SVM_H, and AUXxLVL

The interactions that must be considered when setting the threshold levels in the SVM and AUX are:

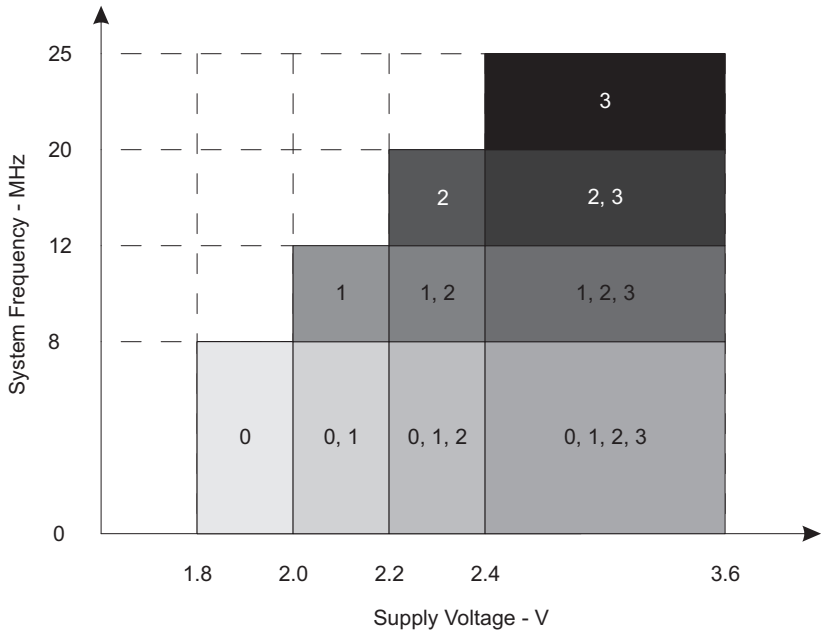
- Minimum V_{CORE} required to support the selected system frequency (f_{SYS})
- Valid SVM_H to support the selected V_{CORE}
- Minimum V_{DSYS} and minimum AUXxLVL required to support the selected V_{CORE}

The interactions among f_{SYS}, DVCC (V_{DSYS} for devices with AUX), V_{CORE}, and SVM_H are described in detail in the PMM chapter. This section adds considerations for the valid AUXxLVL values.

NOTE: Maximum system frequency

The following discussion describes all system frequencies supported in this family. However, the maximum system frequency varies by device; therefore, see the device-specific data sheet to determine this value.

Figure 1-2 shows typical requirements for supply voltage and V_{CORE} compared to the system frequency (see the device-specific data sheet for the values required for each device). As shown here, there is a minimum V_{CORE} (set by PMMCOREV[1:0]) and a minimum supply voltage (V_{DSYS}) for each system frequency. For details on the recommended settings for PMMCOREV[1:0] and supply voltage, see .



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1-2. System Frequency vs Supply Voltage

After selecting the system frequency and PMMCOREV[1:0] values, the SVM threshold must be selected. Figure 1-3 shows the valid values for SVM_H (SVSMHRRL[2:0]) based on the selected V_{CORE} (PMMCOREV[1:0]). This information is also included in .

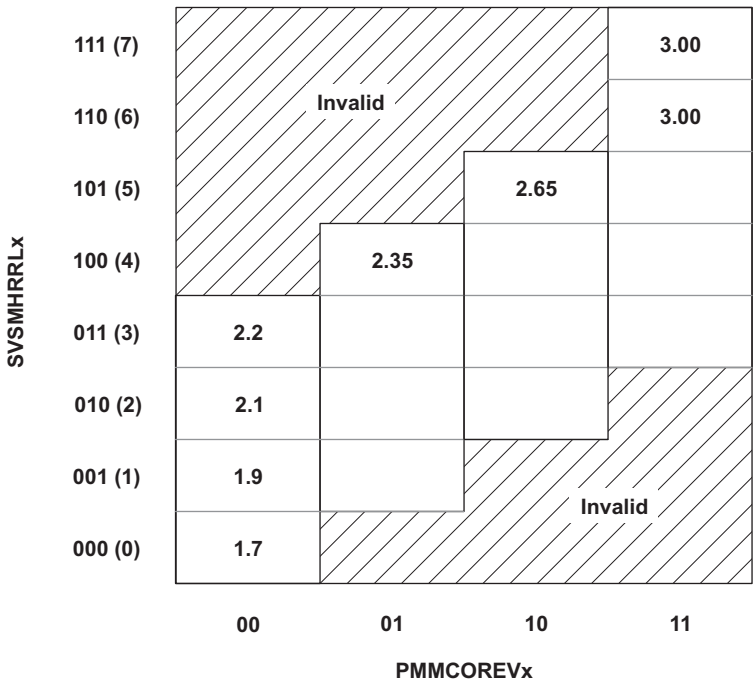


Figure 1-3. Available SVM_H Settings vs V_{CORE} Settings

Based on the preceding selections, the auxiliary supply threshold levels must be set. These thresholds are the minimum supply voltage that are available from each auxiliary supply. Figure 1-4 shows the valid AUXxLVL settings compared to the selected SVM setting. The level setting for DVCC/AVCC AUX0LVL must be chosen at least one step above the SVSMHRRLx level to avoid any unwanted switching between DVCC/AVCC and AUXVCC1 or AUXVCC2.

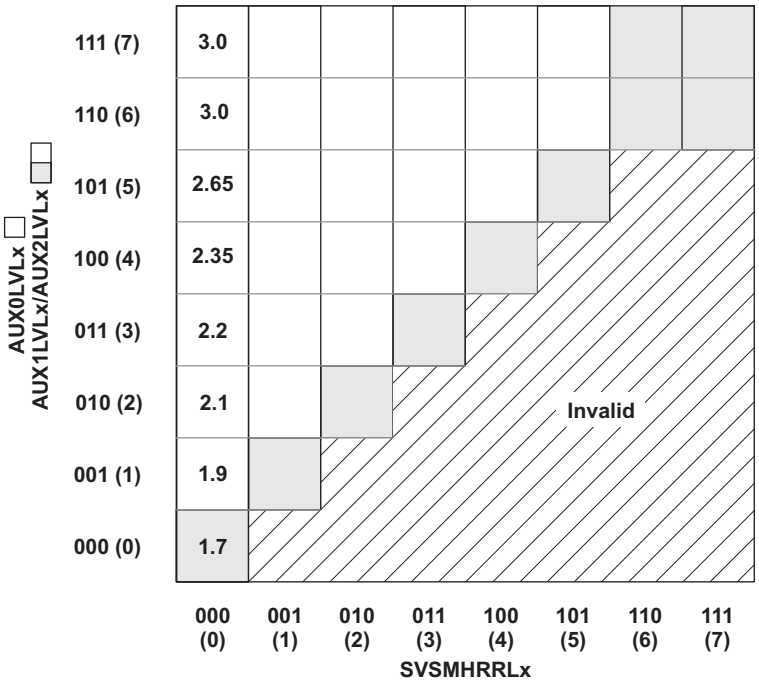


Figure 1-4. Available AUXxLVL Settings vs SVM_H Settings

Table 1-2 combines the information from the preceding figures and discussions.

Table 1-2. Minimum Voltage Thresholds for Selected f_{SYS}

f_{SYS} (max) (MHz)	Minimum PMMCOREV[1:0]	Minimum SVSMHRRL[2:0] (Sets SVM_H Level)	Minimum V_{DSYS}	Minimum AUX0LVL	Minimum AUX1LVL, AUX2LVL
8	00	000	1.8 V	001	000
12	01	001	2.0 V	010	001
20	10	010	2.2 V	011	010
25	11	011	2.4 V	100	011

1.2.6 Auxiliary Supply Monitor

Supplies that are not currently in use and that are not software controlled (AUXxMD = 0) are monitored using a low-power comparator. For example, if DVCC supplies the device and the AUXxMD bits are 0 for both AUXVCC1 and AUXVCC2, then AUXVCC1 and AUXVCC2 are monitored. As another example, if AUXVCC1 supplies the device and AUX2MD = 1, only DVCC is monitored. If all unselected supplies are controlled by software (AUXxMD = 1), then the automatic monitoring is disabled. The level the supply voltages are compared against is programmable with the AUXxLVL bits. If a supply drops below the selected threshold level, the corresponding AUXxDRPIFG is set. Figure 1-5 shows a principle block diagram of the monitoring circuitry.

If two supplies are monitored, this happens in a time-division multiplexing scheme clocked by the VLO. During one VLO clock period, one supply is compared against its AUXxLVL threshold; during the next VLO clock period, the other supply is compared against its threshold. This means the AUXxOK bits of these supplies are updated approximately every 300 µs (worst case) with VLO clock frequency of approximately 6 kHz. If only one supply is monitored, the output of the comparator is sampled using the VLO clock, so that an update of the corresponding AUXxOK bit occurs approximately every 150 µs (worst case).

Each monitoring cycle uses some charge from the monitored supply. The discharge of the monitored supplies can be reduced by decreasing the monitoring rate by changing the AUXMRx bits. By default (with AUXMRx = 00b) the supplies are monitored continuously as described above. By setting AUXMRx = 01b, the supplies are monitored every 32 VLO clock cycles; by setting AUXMRx = 10b, the supplies are monitored every 1024 VLO clock cycles. The AUXMONIFG bit signals the completion of each monitoring cycle.

If an unused supply is changed from software to hardware control (AUXxMD is changed from 1 to 0) a new monitoring cycle is started with the next VLO clock cycle. Switching of the supplies does not affect the timing of the monitoring cycles, it only changes which supplies are monitored.

The auxiliary supply monitor is enabled after clearing the LOCKAUX bit unless all unused supplies are controlled by software. The monitored supplies are considered "not okay" until the first monitoring cycle completes.

NOTE: Switching and monitoring

Switching is independent from the update interval of the AUXxOK bits. Switching is triggered either by the high-side SVM or by software and takes place immediate after the trigger occurs, taking the current AUXxOK states into account to select the next supply. Only a change of AUX0OK from 0 to 1 indicating the DVCC changed from a "not okay" to an "okay" state triggers a switch back to DVCC.

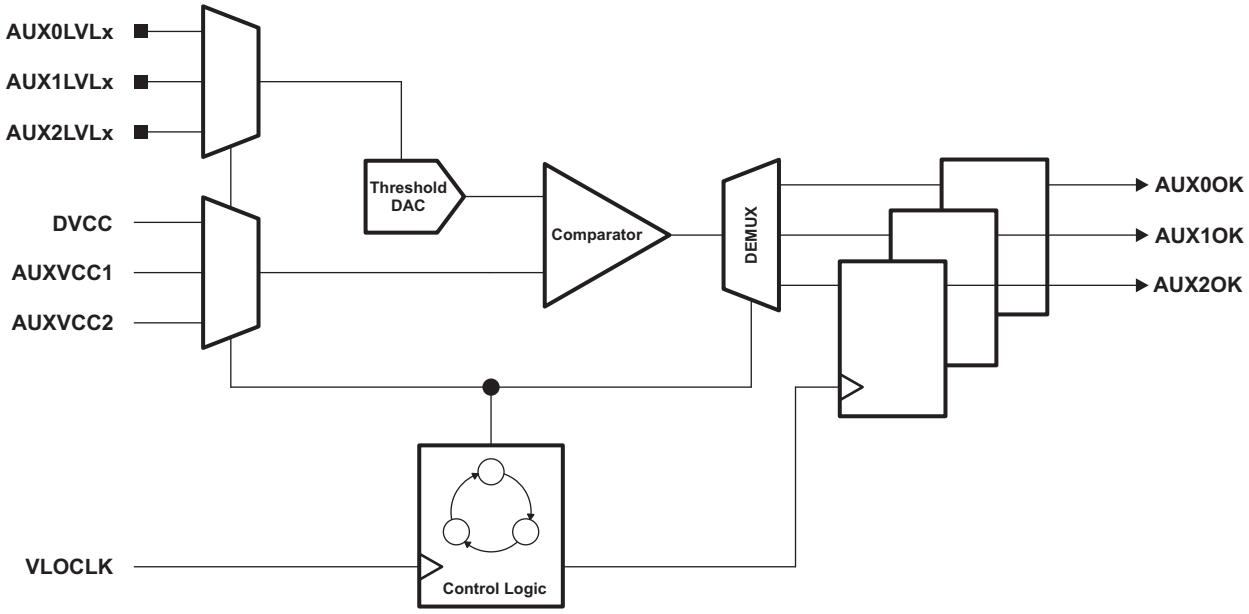


Figure 1-5. Auxiliary Supply Monitor Block Diagram

1.2.7 LPMx.5 and Auxiliary Supply Operation

During LPMx.5, the device is powered by whichever input supply was active when entering the low-power mode. To force the device to use a specific supply during LPMx.5, activate that supply before entering LPMx.5. Table 1-3 lists the supply selection during LPMx.5 based on the disabled supplies. The automatic threshold-based supply monitoring scheme is always disabled during LPMx.5.

Table 1-3. Supply Selection During LPMx.5

Supply During LPMx.5	DVCC/AVCC Status[1]	AUXVCC1 Status[2]
DVCC/AVCC or AUXVCC1 (whichever is higher[3])	Not disabled	Not disabled
DVCC/AVCC	Not disabled	Disabled
AUXVCC1	Disabled	Not disabled
AUXVCC2	Disabled	Disabled

(1) DVCC/AVCC is disabled if AUX0MD = 1 and AUX0OK = 0; otherwise it is enabled.
(2) AUXVCC1 is disabled if AUX1MD = 1 and AUX1OK = 0; otherwise it is enabled.
(3) If the supplies (DVCC/AVCC and AUXVCC1) differ by less than 100 mV, the selected supply can be either DVCC/AVCC or AUXVCC1. The supply with the higher voltage is selected only if the difference is greater than 100 mV.

After wakeup from LPMx.5, the LOCKAUX bit is set. The LPMx.5 supply selection remains active until the LOCKAUX bit is cleared. When the LOCKAUX bit is cleared, the auxiliary supply system is controlled as defined by the control register settings that were configured before clearing the LOCKAUX bit. None of the AUX registers are retained during LPMx.5; thus, all registers must be reconfigured after wakeup from LPMx.5 and before releasing LOCKAUX.

The supplies monitored by hardware (AUXxMD = 0) are considered "not okay" until the status is updated for the first time by the auxiliary supply monitor. Only the supply that was used during LPMx.5 is considered "okay" unless it drops below the programmed SVM level. If this behavior is unwanted, the state can be set to "okay" by temporarily switching to software mode (AUXxMD = 1), setting the AUXxOK bit to 1, and then return to hardware mode (AUXxMD = 0). The last state defined in software mode is retained when switching back to hardware mode until the first update occurs by the auxiliary supply monitor.

The supplies controlled by software (AUXxMD = 1) are considered "not okay" or "okay" according to their AUXxOK setting. If the supply that was used during LPMx.5 is set to "not okay" (AUXxMD = 1 and AUXxOK = 0) the auxiliary supply system tries to switch to another ("okay") supply according to Table 1-1 as soon as LOCKAUX is cleared.

NOTE: DVCC and AUXVCC1 during LPMx.5

Under normal operating conditions, TI recommends supplying DVCC by a voltage at least 100 mV higher than AUXVCC1, if automatic switching between DVCC and AUXVCC1 is active (that is, if both supplies are not disabled when entering LPMx.5) (see Table 1-3). This ensures a reliable operation from DVCC and avoids a potentially unwanted operation from AUXVCC1.

1.2.8 Digital I/Os and Auxiliary Supplies

In most devices that implement the auxiliary supply system, the digital I/Os can be powered by the switched supplies. In this case, care must be taken that large currents sink to DVSS and are not sourced from the switched supplies, because of the voltage drop across the supply switches (see Figure 1-6).

CAUTION

Check connection of external loads at digital I/Os to avoid high voltage drops across switches. This might cause unwanted resets.

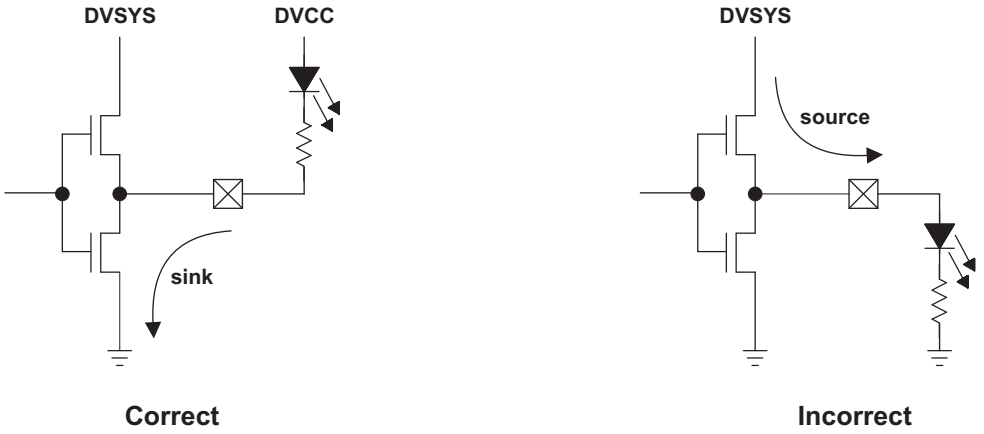


Figure 1-6. I/Os Powered by Auxiliary Supplies

1.2.9 Measuring the Supplies

The primary and all auxiliary supply voltages can be measured if the device provides an ADC. The supply to be measured is selected with the AUXADCSELx bit in the AUXADCCTL register. In addition, the resistive load applied to the selected supply during the sampling phase of the ADC can be selected with the AUXADCRx bits. This allows to perform a "health" check of the supplies even when not loaded by the application. The ADC supply voltage channel (usually channel 12 (0Ch)) must be selected and the auxiliary supply voltage measurement must be enabled with AUXADC = 1. The resistive divider is connected to the supplies only during the sampling phase of the ADC.

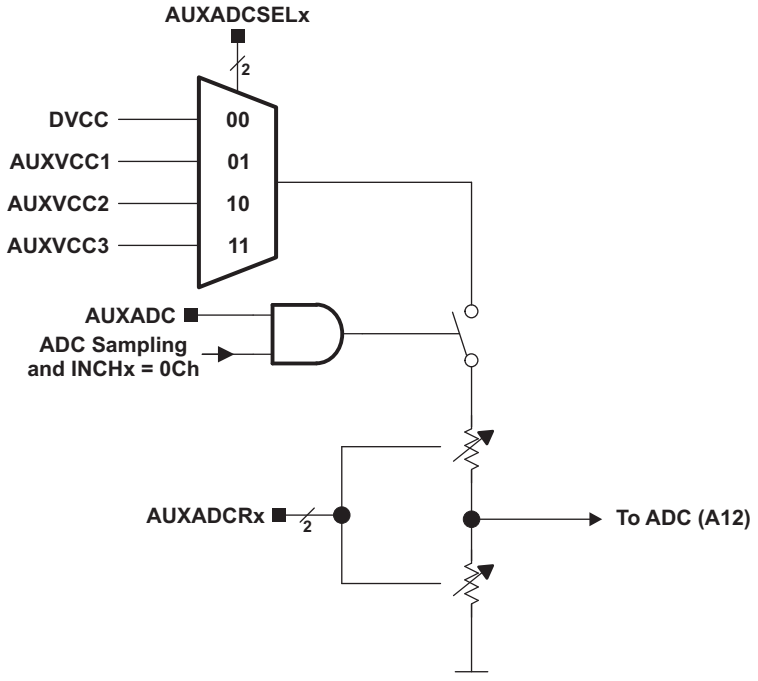


Figure 1-7. AUX Connection to ADC

1.2.10 Resistive Charger

Two simple resistive charging circuits are implemented to charge capacitors connected to AUXVCC2 and AUXVCC3. Figure 1-8 shows a simplified block diagram of the charger. The charger for AUXVCC2 or AUXVCC3 is enabled by writing the correct key (069h) into the upper byte of AUX2CHCTL or AUX3CHCTL, respectively, together with AUXCHVx = 01b, AUXCHEN = 1 and selecting a charging resistor with AUXCHCx ≠ 00b. Writing to the charger control register with an incorrect key disables the charger, and all control register bits are reset to 0.

Both chargers are disabled when DVCC is not selected as the supply source and AUXCHEN is reset by hardware.

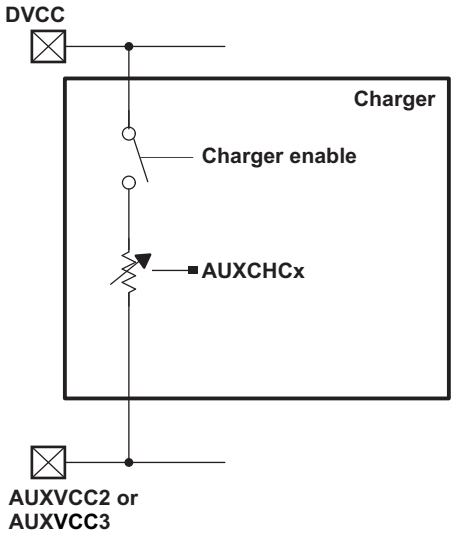


Figure 1-8. Charger Block Diagram

1.2.11 Auxiliary Supply Interrupts

The auxiliary supply system provides seven interrupt sources:

- AUXSWNMIFG: (non-)maskable supplies switched interrupt
- AUX0SWIFG: switched to DVCC interrupt
- AUX1SWIFG: switched to AUXVCC1 interrupt
- AUX2SWIFG: switched to AUXVCC2 interrupt
- AUX1DRPIFG: AUXVCC1 dropped below threshold interrupt
- AUX2DRPIFG: AUXVCC2 dropped below threshold interrupt
- AUXMONIFG: supply monitor interrupt

The AUXSWNMIFG is set after the system switched from one supply to another supply. A nonmaskable interrupt request is generated if the AUXSWNMIE bit is set; otherwise, if (only) the AUXSWGIE bit and additionally the GIE bit are set, a maskable interrupt request is generated.

The AUXxSWIFG bits are set if the auxiliary supply system switched to the corresponding supply (DVCC, AUXVCC1 or AUXVCC2). This information can be used in the interrupt service routine together with the interrupt vector generator AUXIV to reconfigure the device to the new supply situation. A (maskable) interrupt request is generated if the corresponding AUXxSWIE bit and the GIE bit are set.

The AUXxDRPIFG bits are set if the corresponding supplies AUXxOK state changes from 1 to 0 due to the supply voltage dropping below the selected threshold value AUXxLVL with the hardware monitor being enabled (AUXxMD = 0). A (maskable) interrupt request is generated if the corresponding AUXxDRPIE bit and the GIE bit are set.

The AUXMONIFG bit is set if a hardware monitoring cycle is completed and the supply AUXxOK states are updated accordingly. A (maskable) interrupt request is generated if the corresponding AUXMONIE bit and the GIE bit are set.

1.2.11.1 AUXIV, Interrupt Vector Generator

All (maskable) auxiliary supply system interrupt sources are prioritized and combined to source a single interrupt vector. AUXIV is used to determine which enabled interrupt source requested an interrupt. The highest priority interrupt request that is enabled generates a number in the AUXIV register (see register description). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled interrupts do not affect the AUXIV value.

Any read access of the AUXIV register automatically resets the highest pending interrupt flag. A write access to the AUXIV register automatically resets all pending interrupt flags. All interrupt flags can also be cleared by software.

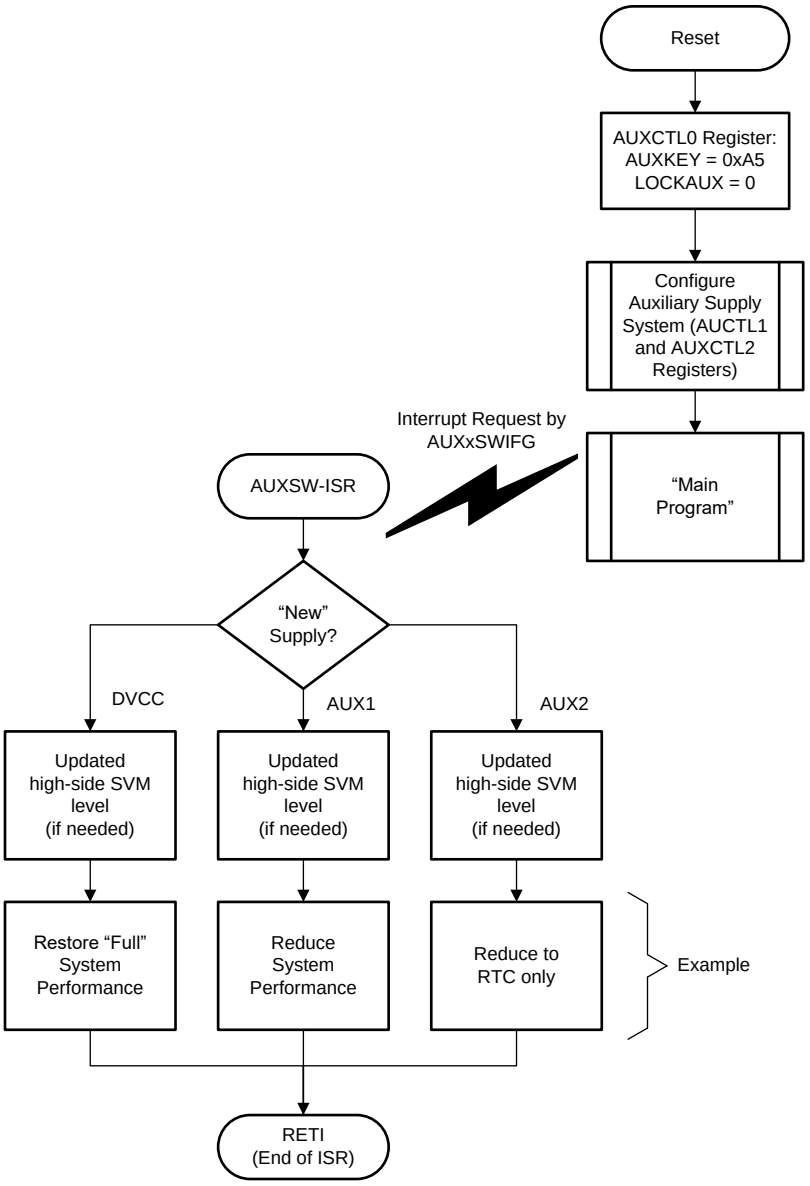
1.2.11.2 Auxiliary Supply Nonmaskable Interrupt

If AUXSWNMIFG is configured as a nonmaskable interrupt source (with AUXSWNMIE=1), it will source (together with interrupt flags from other modules) the user-NMI interrupt vector. In the user-NMI interrupt service routine, the SYSUNIV interrupt vector word register can be evaluated or added to the program counter to automatically enter the appropriate part of the user-NMI interrupt service routine. See the device-specific data sheet concerning the user-NMI interrupt vector sources and priorities.

If both AUXSWNMIE and AUXSWGIE are set, the nonmaskable interrupt service routine is called when AUXSWNMIFG is set because the user-NMI has a higher priority. In this case, both interrupt vector generators, the SYSUNIV and the AUXIV, indicate a pending AUXSWNMIFG.

1.2.12 Software Flow

Figure 1-9 shows a sample software flow chart for the use and control of the auxiliary supply system.



NOTE: Configuration of the auxiliary supply system is required after wakeup from LPMx.5. None of the AUX registers are retained during LPMx.5.

Figure 1-9. Software Flow Chart

1.2.13 Examples of AUX Operation

The following sections describe sample configurations of the AUX module. Some settings in these examples do not apply to all devices; see the device-specific data sheet.

1.2.13.1 Example 1

This example shows configuration for running at 25-MHz system frequency at a supply voltage of 3 V ±0.3 V, maintaining that frequency when switching to AUX1 or AUX2.

The maximum SVM_H level must be less than or equal to 2.7 V, so that switching occurs only when V_{DSYS} goes outside 3 V ±0.3 V. To switch back to DVCC/AVCC as soon as possible when it is within 3 V ±0.3 V, the maximum AUX0LVL must also be less than or equal to 2.7 V. Because AUX0LVL must be 1 higher than SVSMHRRL, set AUX0LVL = 4 and SVSMHRRL = 3.

To support 25-MHz operation, PMMCOREV must equal 3. With SVSMHRRL = 3, all core voltage settings are supported, so this is valid. Based on this core voltage setting, configure SVS levels (see for details).

To continue operation at 25-MHz without glitches even when using AUX1 and AUX2, the thresholds for these must be equal to or higher than SVSMHRRL. To minimize use of the auxiliary supplies, they should be set equal to SVSMHRRL. Therefore, set AUX1LVL and AUX2LVL = 3.

1.2.13.2 Example 2

This example shows configuration for running at a supply voltage of 3.3 V ±0.3 V and allowing for switching supplies without functional glitches.

The maximum SVM_H level must be less than or equal to 3 V, so that switching occurs only when V_{DSYS} goes outside 3.3 V ±0.3 V. To switch back to DVCC/AVCC as soon as possible when it is within 3.3 V ±0.3 V, the maximum AUX0LVL must also be less than or equal to 3 V. Because AUX0LVL must be 1 higher than SVSMHRRL, set = 6 and SVSMHRRL = 5.

With SVSMHRRL = 5, the core voltage setting (PMMCOREV) must be 2 or 3. Assuming the application requires a system frequency up to 20 MHz, set PMMCOREV = 2. Based on this core voltage setting, configure SVS levels (see for details).

To continue operation without glitches when switching to AUX1 and AUX2, the thresholds for these must be equal to or higher than SVSMHRRL. To minimize use of the auxiliary supplies, they should be set equal to SVSMHRRL. Therefore, set AUX1LVL = AUX2LVL = 5.

1.2.13.3 Example 3

This example shows configuration for running at a system frequency of 8 MHz an a nominal supply voltage of 3.3 V with settings designed to minimize power consumption.

To minimize power consumption at 8 MHz, set PMMCOREV = 0. With this core voltage, the recommended SVM_H setting is SVSMHRRL = 0. Because AUX0LVL must be at least 1 higher than SVSMHRRL, set AUX0LVL = 1.

To continue operation without glitches when switching to AUX1 and AUX2, the thresholds for these must be equal to or higher than SVSMHRRL. To minimize use of the auxiliary supplies, they should be set equal to SVSMHRRL. Therefore, set AUX1LVL and AUX2LVL = 0.

1.2.13.4 Example 4

This example shows configuration for running at a system frequency of 25 MHz when operating on a supply voltage of 3 V ±0.3 V from DVCC, and then changing the system frequency to 12 MHz when supplied from AUX1 and to 8 MHz when supplied from AUX2.

The maximum SVM_H level must be less than or equal to 2.7 V, so that switching occurs only when V_{DSYS} goes outside 3 V ±0.3 V. To switch back to DVCC/AVCC as soon as possible when it is within 3 V ±0.3 V, the maximum AUX0LVL must also be less than or equal to 2.7 V. Because AUX0LVL must be 1 higher than SVSMHRRL, set = 4 and SVSMHRRL = 3.

To support 25-MHz operation, PMMCOREV must equal 3. With SVSMHRRL = 3, all core voltage settings are supported, so this is valid. Based on this core voltage setting, configure SVS levels (see for details).

When switching back to AUX0 (DVCC/AVCC) after having failed over to AUX1 or AUX2, these same settings must be restored.

Given that the system frequency should be changed to 12 MHz when running from AUX1, settings must be changed when switching to AUX1.

When switching from AUX0 (DVCC/AVCC) to AUX1:

1. Decrease system frequency to 12 MHz

2. Decrease core voltage level by setting PMMCOREV = 1 (also change SVS settings)
3. Decrease the SVM level by setting SVSMHRRL = 1
4. Set AUX1LVL and AUX2LVL to 1

When switching from AUX2 to AUX1:

1. Increase AUX1LVL and AUX2LVL to 1
2. Increase the SVM level by setting SVSMHRRL = 1
3. Increase core voltage level by setting PMMCOREV = 1 (also change SVS settings)
4. Increase system frequency to 12 MHz

Given that the system frequency should be changed to 8 MHz when running from AUX2, settings must be changed when switching to AUX2.

1. Decrease system frequency to 8 MHz
2. Decrease core voltage level by setting PMMCOREV = 0 (also change SVS settings)
3. Decrease the SVM level by setting SVSMHRRL = 0
4. Set AUX1LVL and AUX2LVL to 0

1.3 AUX Registers

The registers to control the auxiliary supplies are listed in Table 1-4. The base address for the registers can be found in the device-specific data sheet. The address offsets are given in Table 1-4.

The access key, AUXKEY, defined in the AUXCTL0 register controls access to the AUXCTLx registers. Once the correct key is written, the write access is enabled. The write access is disabled by writing a wrong key in byte mode to the AUXCTL0 upper byte. Word accesses to AUXCTL0 with a wrong key also disables the write access. A write access to a AUXCTLx register other than AUXCTL0 while write access is not enabled is ignored.

NOTE: Bit Naming Convention

The bits and bit fields in the AUXCTL0 to AUXCTL2 registers are named according to what supplies they refer to: AUX0... refers to DVCC, AUX1... refers to AUXVCC1, and AUX2... refers to AUXVCC2. In any description, the occurence of a bit name like AUXx... refers to all the bit names AUX0..., AUX1..., and AUX2....

Table 1-4. Auxiliary Supply Registers

Offset	Acronym	Register Name	Type	Reset	Section
00h	AUXCTL0	Auxiliary Supply Control 0 register(1)	Read/write	9601h	Section 1.3.1
02h	AUXCTL1	Auxiliary Supply Control 1 register(1)	Read/write	0000h	Section 1.3.2
04h	AUXCTL2	Auxiliary Supply Control 2 register(1)	Read/write	0000h	Section 1.3.3
06h to 10h		Reserved			
12h	AUX2CHCTL	AUX2 Charger Control	Read/write	5A00h	Section 1.3.4
14h	AUX3CHCTL	AUX3 Charger Control	Read/write	5A00h	Section 1.3.5
16h	AUXADCCTL	AUX ADC Control	Read/write	0000h	Section 1.3.6
18h		Reserved			
1Ah	AUXIFG	AUX Interrupt Flag	Read/write	0000h	Section 1.3.7
1Ch	AUXIE	AUX Interrupt Enable	Read/write	0000h	Section 1.3.8
1Eh	AUXIV	AUX Interrupt Vector Word	Read/write	0000h	Section 1.3.9

(1) Access protected by key AUXKEY in AUXCTL0.

1.3.1 AUXCTL0 Register

Auxiliary Supply Control 0 Register

Figure 1-10. AUXCTL0 Register

15	14	13	12	11	10	9	8
AUXKEY							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved				AUX2SW	AUX1SW	AUX0SW	LOCKAUX
r0	r0	r0	r0	r-(0)	r-(0)	r-(0)	r/w0-[1]

Table 1-5. AUXCTL0 Register Description

Bit	Field	Type	Reset	Description
15-8	AUXKEY	RW	96h	AUX access key. Always reads as 096h. To enable write access to AUXCTLx registers, write AUXKEY = 0A5h. The AUXKEY field can be written only when LOCKAUX bit is clear. AUXKEY and LOCKAUX can be updated in the same CPU instruction.
7-4	Reserved	R	0h	Reserved. Always reads as 0.
3	AUX2SW	R	0h	AUXVCC2 switch state 0b = AUXVCC2 switch open 1b = AUXVCC2 switch closed
2	AUX1SW	R	0h	AUXVCC1 switch state 0b = AUXVCC1 switch open 1b = AUXVCC1 switch closed
1	AUX0SW	R	0h	DVCC switch state 0b = DVCC switch open 1b = DVCC switch closed
0	LOCKAUX	RW	1h	Lock auxiliary supply system. Can only be written as 0. LOCKAUX is always set to 1 by hardware after the core was powered down either due to a complete power cycle of the main suppies (DVCC, AUXVCC1, or AUXVCC2) or due to LPMx.5 operation. 0b = Auxiliary supply system not locked 1b = Auxiliary supply system is locked and operating from DVCC or AUXVCC1

1.3.2 AUXCTL1 Register

Auxiliary Supply Control 1 Register

Figure 1-11. AUXCTL1 Register

15	14	13	12	11	10	9	8
Reserved					AUX2MD	AUX1MD	AUX0MD
r0	r0	r0	r0	r0	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
Reserved				AUX2PRIO	AUX2OK	AUX1OK	AUX0OK
r0	r0	r0	r0	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 1-6. AUXCTL1 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10	AUX2MD	RW	0h	AUXVCC2 auxiliary supply mode 0b = Hardware controlled 1b = Software controlled
9	AUX1MD	RW	0h	AUXVCC1 auxiliary supply mode 0b = Hardware controlled 1b = Software controlled
8	AUX0MD	RW	0h	DVCC auxiliary supply mode 0b = Hardware controlled 1b = Software controlled
7-4	Reserved	R	0h	Reserved. Always reads as 0.
3	AUX2PRIO	RW	0h	Auxiliary supply AUXVCC2 priority. Defines order of switching between AUXVCC1 and AUXVCC2. 0b = AUXVCC2 has lower priority than AUXVCC1 1b = AUXVCC2 has higher priority than AUXVCC1
2	AUX2OK	RW	0h	AUXVCC2 okay flag. Read-only if AUX2MD = 0 and indicates the status monitored by the hardware based on the selected level AUX2LVLx. If AUX2MD = 1 the bit must be controlled by software to indicate the status of the supply. It is not modified by hardware in this case. 0b = Supply not okay, below AUX2LVLx if AUX2MD = 0 1b = Supply okay, above AUX2LVLx if AUX2MD = 0
1	AUX1OK	RW	0h	AUXVCC1 okay flag. Read-only if AUX1MD = 0 and indicates the status monitored by the hardware based on the selected level AUX1LVLx. If AUX1MD = 1 the bit must be controlled by software to indicate the status of the supply. It is not modified by hardware in this case. 0b = Supply not okay, below AUX1LVLx if AUX1MD = 0 1b = Supply okay, above AUX1LVLx if AUX1MD = 0
0	AUX0OK	RW	0h	DVCC okay flag. Read-only if AUX0MD = 0 and indicates the status monitored by the hardware based on the selected level AUX0LVLx. If AUX0MD = 1 the bit must be controlled by software to indicate the status of the supply. It is not modified by hardware in this case. 0b = Supply not okay, below AUX0LVLx if AUX0MD = 0 1b = Supply okay, above AUX0LVLx if AUX0MD = 0

1.3.3 AUXCTL2 Register

Auxiliary Supply Control 2 Register

Figure 1-12. AUXCTL2 Register

15	14	13	12	11	10	9	8
Reserved		AUXMRx		Reserved	AUX2LVLx		
r0	r0	rw-(0)	rw-(0)	r0	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
Reserved	AUX1LVLx			Reserved	AUX0LVLx		
r0	rw-(0)	rw-(0)	rw-(0)	r0	rw-(0)	rw-(0)	rw-(0)

Table 1-7. AUXCTL2 Register Description

Bit	Field	Type	Reset	Description
15-14	Reserved	R	0h	Reserved. Always reads as 0.
13-12	AUXMRx	RW	0h	Auxiliary supply monitoring rate 00b = Continous monitoring 01b = Monitoring every 32 VLO clock cycles (≈5ms) 10b = Monitoring every 1024 VLO clock cycles (≈150ms) 11b = Reserved
11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	AUX2LVLx	RW	0h	AUXVCC2 auxiliary supply threshold level. The levels are specified in the device-specific data sheet. 000b = ≈1.74 V 001b = ≈1.94 V 010b = ≈2.14 V 011b = ≈2.26 V 100b = ≈2.40 V 101b = ≈2.70 V 110b = ≈3.00 V 111b = ≈3.00 V
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	AUX1LVLx	RW	0h	AUXVCC1 auxiliary supply threshold level. The levels are specified in the device-specific data sheet. 000b = ≈1.74 V 001b = ≈1.94 V 010b = ≈2.14 V 011b = ≈2.26 V 100b = ≈2.40 V 101b = ≈2.70 V 110b = ≈3.00 V 111b = ≈3.00 V
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	AUX0LVLx	RW	0h	DVCC auxiliary supply threshold level. The levels are specified in the device-specific data sheet. 000b = ≈1.74 V 001b = ≈1.94 V 010b = ≈2.14 V 011b = ≈2.26 V 100b = ≈2.40 V 101b = ≈2.70 V 110b = ≈3.00 V 111b = ≈3.00 V

1.3.4 AUX2CHCTL Register

AUX Charger Control Register for AUX2

Figure 1-13. AUX2CHCTL Register

15	14	13	12	11	10	9	8
AUXCHKEYx							
rw-0	rw-1	rw-0	rw-1	rw-1	rw-0	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved		AUXCHVx		Reserved	AUXCHCx		AUXCHEN
r0	r0	rw-0	rw-0	r0	rw-0	rw-0	rw-0

Table 1-8. AUX2CHCTL Register Description

Bit	Field	Type	Reset	Description
15-8	AUXCHKEYx	RW	5Ah	Charger access key. Always read as 05Ah. Must be written as 069h together with low byte; writing any other value disables the charger and all control register bits are reset to 0.
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	AUXCHVx	RW	0h	Charger end voltage 00b = Charger disabled 01b = VCC 10b = Reserved 11b = Reserved
3	Reserved	R	0h	Reserved. Always reads as 0.
2-1	AUXCHCx	RW	0h	Charger charge current 00b = Charger disabled 01b = Charge current defined by a maximum 5-kΩ resistor 10b = Charge current defined by a maximum 10-kΩ resistor 11b = Charge current defined by a maximum 20-kΩ resistor
0	AUXCHEN	RW	0h	Charger enable 0b = Charger disabled 1b = Charger enabled

1.3.5 AUX3CHCTL Register

AUX Charger Control Register for AUX3

Figure 1-14. AUX3CHCTL Register

15	14	13	12	11	10	9	8
AUXCHKEYx							
rw-0	rw-1	rw-0	rw-1	rw-1	rw-0	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved		AUXCHVx		Reserved	AUXCHCx		AUXCHEN
r0	r0	rw-0	rw-0	r0	rw-0	rw-0	rw-0

Table 1-9. AUX3CHCTL Register Description

Bit	Field	Type	Reset	Description
15-8	AUXCHKEYx	RW	5Ah	Charger access key. Always read as 05Ah. Must be written as 069h together with low byte; writing any other value disables the charger and all control register bits are reset to 0.
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	AUXCHVx	RW	0h	Charger end voltage 00b = Charger disabled 01b = VCC 10b = Reserved 11b = Reserved
3	Reserved	R	0h	Reserved. Always reads as 0.
2-1	AUXCHCx	RW	0h	Charger charge current 00b = Charger disabled 01b = Charge current defined by a maximum 5-kΩ resistor 10b = Charge current defined by a maximum 10-kΩ resistor 11b = Charge current defined by a maximum 20-kΩ resistor
0	AUXCHEN	RW	0h	Charger enable 0b = Charger disabled 1b = Charger enabled

1.3.6 AUXADCCTL Register

Auxiliary Supply ADC Control Register

Figure 1-15. AUXADCCTL Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved		AUXADCRx		Reserved	AUXADCSELx		AUXADC
r0	r0	rw-0	rw-0	r0	rw-0	rw-0	rw-0

Table 1-10. AUXADCCTL Register Description

Bit	Field	Type	Reset	Description
15-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	AUXADCRx	RW	0h	Load resistance ($R_{(tot)}$ = 3R) during sampling of selected supply. Also see the device-specific data sheet. 00b = $R_{(tot)}$ ≈ 15 kΩ – I = U/R = 3.6 V / 15 kΩ = 240 µA; I = 1.8 V / 16 kΩ = 120 µA 01b = $R_{(tot)}$ ≈ 1.5 kΩ – I = 2.4 mA at 3.6 V; I = 1.2 mA at 1.8 V 10b = $R_{(tot)}$ ≈ 0.5 kΩ – I = 7.2 mA at 3.6 V; I = 3.6 mA at 1.8 V 11b = Reserved
3	Reserved	R	0h	Reserved. Always reads as 0.
2-1	AUXADCSELx	RW	0h	Select supply to be measured with ADC. 00b = DVCC 01b = AUXVCC1 10b = AUXVCC2 11b = AUXVCC3
0	AUXADC	RW	0h	Auxiliary supplies to ADC 0b = Auxiliary supply measurement disabled 1b = Auxiliary supply measurement enabled

1.3.7 AUXIFG Register

Auxiliary Supply Interrupt Flag Register

Figure 1-16. AUXIFG Register

15	14	13	12	11	10	9	8
Reserved							AUXSWNMIFG
r0	r0	r0	r0	r0	r0	r0	rw-(0)
7	6	5	4	3	2	1	0
AUXMONIFG	AUX2DRPIFG	AUX1DRPIFG	Reserved	Reserved	AUX2SWIFG	AUX1SWIFG	AUX0SWIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	r0	rw-(0)	rw-(0)	rw-(0)

Table 1-11. AUXIFG Register Description

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0h	Reserved. Always reads as 0.
8	AUXSWNMIFG	RW	0h	Supplies switched (non-)maskable interrupt flag. Set if a switch from any supply to any other supply happened. Sources an NMI if AUXSWNMIE is set, otherwise sources a maskable interrupt if AUXSWGIE and GIE is set. 0b = No interrupt pending 1b = Interrupt pending
7	AUXMONIFG	RW	0h	Supply monitor interrupt flag. Set after completion of a hardware monitoring cycle. 0b = No interrupt pending 1b = Interrupt pending
6	AUX2DRPIFG	RW	0h	AUXVCC2 dropped below its threshold interrupt flag. 0b = No interrupt pending 1b = Interrupt pending
5	AUX1DRPIFG	RW	0h	AUXVCC1 dropped below its threshold interrupt flag. 0b = No interrupt pending 1b = Interrupt pending
4	Reserved	RW	0h	Reserved. Always write as 0.
3	Reserved	R	0h	Reserved. Always reads as 0.
2	AUX2SWIFG	RW	0h	Switched to AUXVCC2 interrupt flag. 0b = No interrupt pending 1b = Interrupt pending
1	AUX1SWIFG	RW	0h	Switched to AUXVCC1 interrupt flag. 0b = No interrupt pending 1b = Interrupt pending
0	AUX0SWIFG	RW	0h	Switched to DVCC interrupt flag. 0b = No interrupt pending 1b = Interrupt pending

1.3.8 AUXIE Register

Auxiliary Supply Interrupt Enable Register

Figure 1-17. AUXIE Register

15	14	13	12	11	10	9	8
Reserved							AUXSWNMIE
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
AUXMONIE	AUX2DRPIE	AUX1DRPIE	Reserved	AUXSWGIE	AUX2SWIE	AUX1SWIE	AUX0SWIE
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-12. AUXIE Register Description

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0h	Reserved. Always reads as 0.
8	AUXSWNMIE	R	0h	Supplies switched non-maskable interrupt enable. 0b = Non-maskable interrupt disabled 1b = Non-maskable interrupt enabled
7	AUXMONIE	RW	0h	Supply monitor interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
6	AUX2DRPIE	RW	0h	AUXVCC2 dropped below its threshold interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
5	AUX1DRPIE	RW	0h	AUXVCC1 dropped below its threshold interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
4	Reserved	RW	0h	Reserved. Always write as 0.
3	AUXSWGIE	RW	0h	Global supply switched interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
2	AUX2SWIE	RW	0h	Switched to AUXVCC2 interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
1	AUX1SWIE	RW	0h	Switched to AUXVCC1 interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled
0	AUX0SWIE	RW	0h	Switched to DVCC interrupt enable. 0b = Interrupt disabled 1b = Interrupt enabled

1.3.9 AUXIV Register

Auxiliary Supply Interrupt Vector Register

Figure 1-18. AUXIV Register

15	14	13	12	11	10	9	8
AUXIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
AUXIVx							
r0	r0	r-(0)	r-(0)	r-(0)	r-(0)	r-(0)	r0

Table 1-13. AUXIV Register Description

Bit	Field	Type	Reset	Description
15-0	AUXIVx	R	0h	Auxiliary Supply Interrupt vector value. It generates a value that can be used as address offset for fast interrupt service routine handling. Writing to this register clears all pending interrupt flags. 00h = No interrupt pending 02h = Interrupt Source: Global (non-)maskable supply switched interrupt flag; Interrupt Flag: AUXSWNMIFG; Interrupt Priority: Highest 04h = Interrupt Source: Switched to DVCC interrupt flag; Interrupt Flag: AUX0SWIFG 06h = Interrupt Source: Switched to AUXVCC1 interrupt flag; Interrupt Flag: AUX1SWIFG 08h = Interrupt Source: Switched to AUXVCC2 interrupt flag; Interrupt Flag: AUX2SWIFG 0Ah = Interrupt Source: Reserved; Interrupt Flag: - 0Ch = Interrupt Source: AUXVCC1 below threshold interrupt flag; Interrupt Flag: AUX1DRPIFG 0Eh = Interrupt Source: AUXVCC2 below threshold interrupt flag; Interrupt Flag: AUX2DRPIFG 10h = Interrupt Source: Supply monitor interrupt flag; Interrupt Flag: AUXMONIFG; Interrupt Priority: Lowest

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