SD24_B

The SD24_B is a multiple-input multiple-converter sigma-delta analog-to-digital conversion module. This chapter describes the operation of the SD24_B module.

Topic **Page**

1.1 SD24_B Introduction

The SD24_B module consists of up to eight independent sigma-delta analog-to-digital converters. The converters are based on second-order oversampling sigma-delta modulators and digital decimation filters. The decimation filters are comb filters with selectable oversampling ratios of up to 1024. Additional filtering can be done in software.

Features of the SD24_B include:

- Second-order sigma-delta architecture
- Up to eight independent simultaneously-sampling ADCs (the number of converters is device dependent, see the device-specific data sheet).

Figure 1-1 shows an overview block diagram of the SD24_B module. Figure 1-2 shows the block diagram of the voltage reference and clock generation circuitry. The reference voltage generation is located in the shared reference module (see the device-specific data sheet). Figure 1-3 shows the converter-specific block diagram.

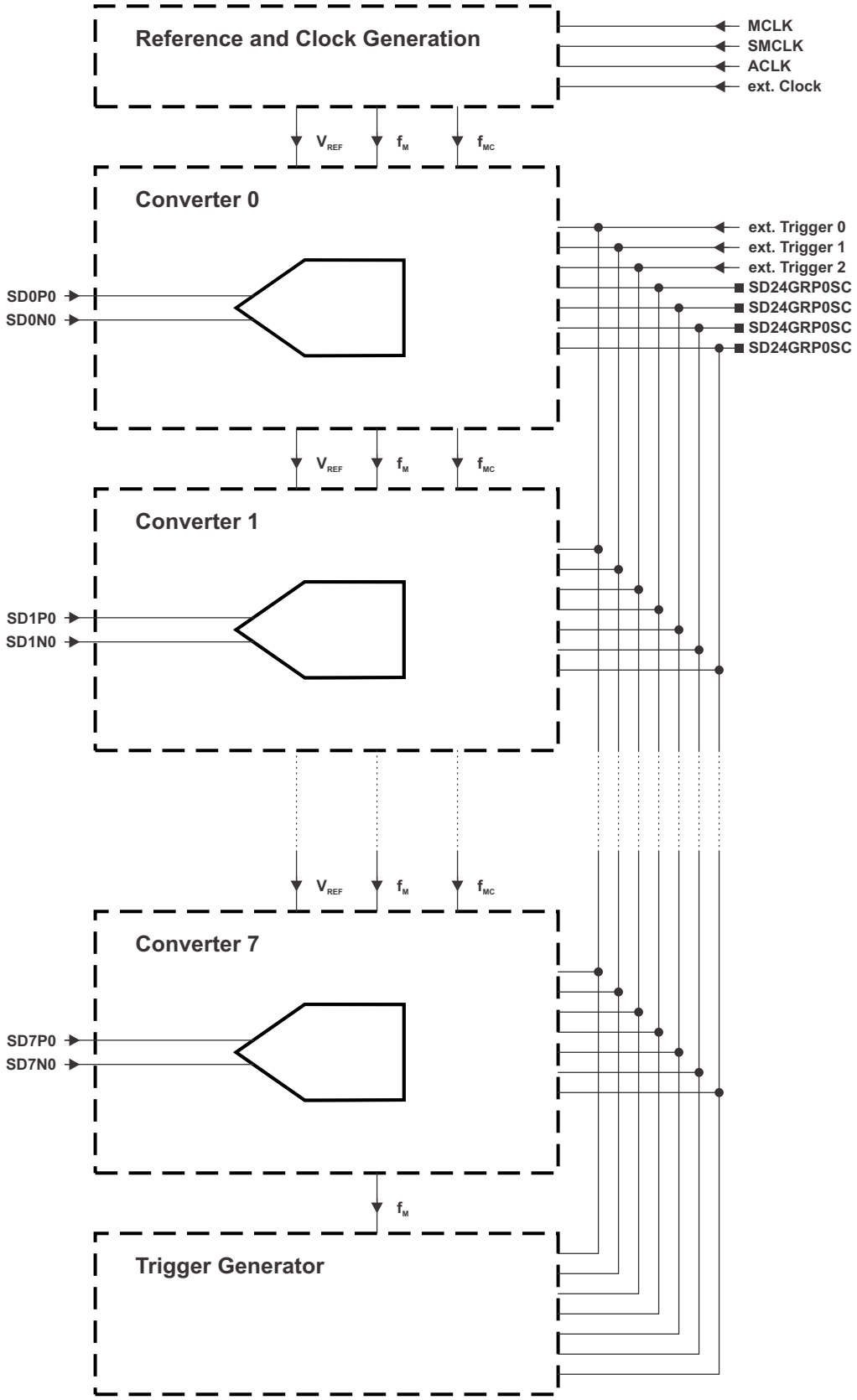

Figure 1-1. SD24_B Overview Block Diagram

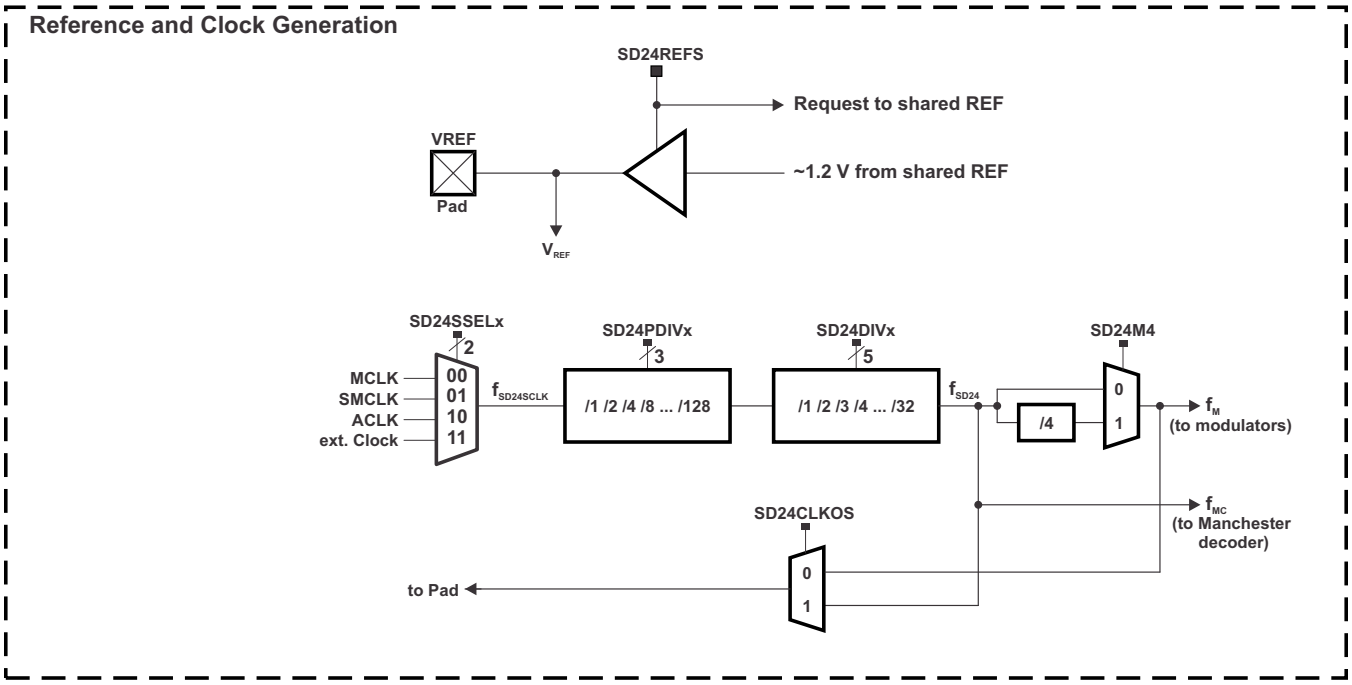

Figure 1-2. SD24_B Reference and Clock Generation Block Diagram

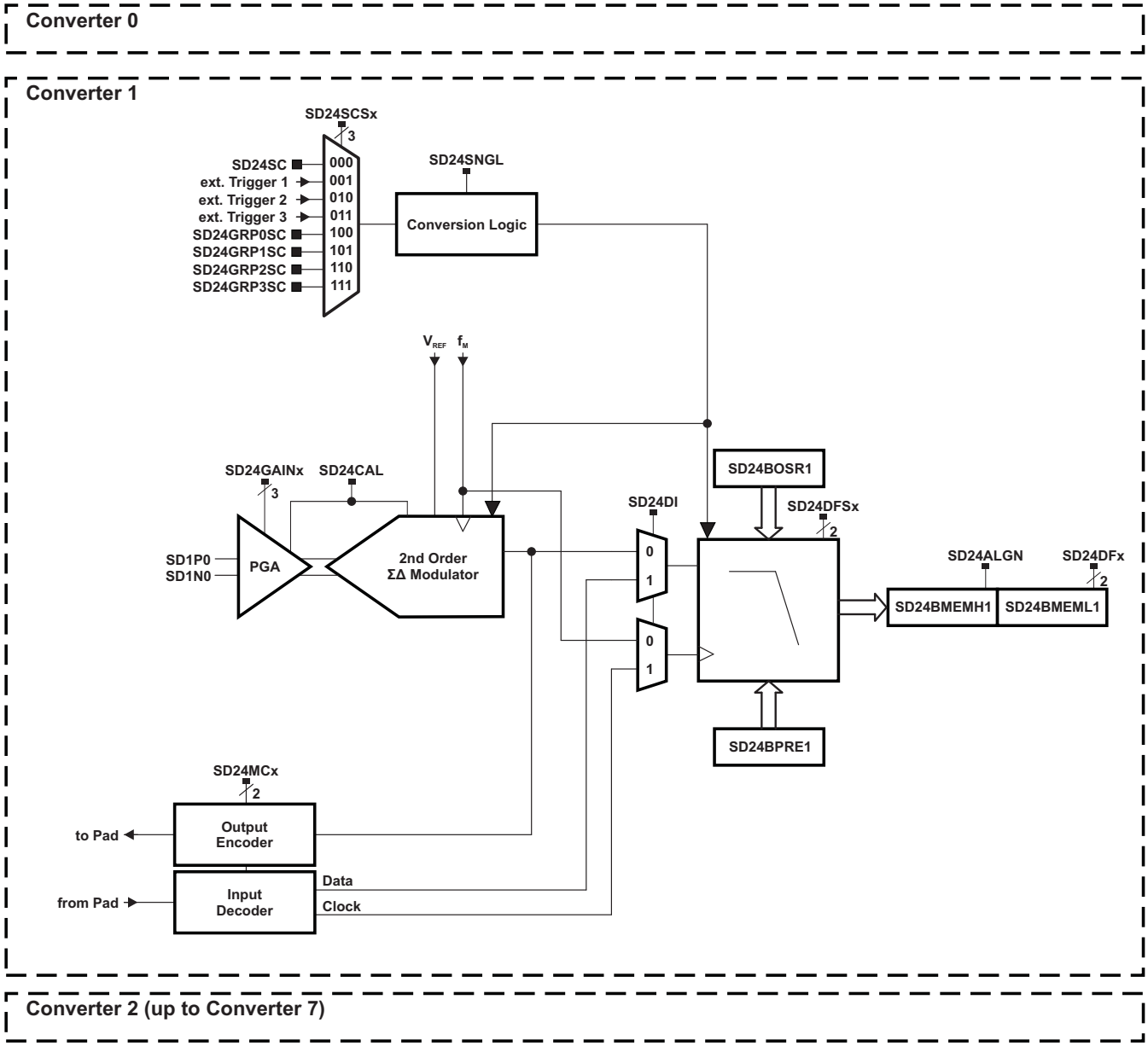

Figure 1-3. SD24_B Converter Block Diagram

1.2 SD24_B Operation

The SD24_B module is configured with user software. The setup and operation of the SD24_B is described in the following sections.

1.2.1 Principle of Operation

A sigma-delta analog-to-digital converter basically consists of two parts: the analog part (called the modulator) and the digital part (called the decimation filter). The modulator of the SD24_B provides a bitstream of zeros and ones to the digital decimation filter. The digital filter averages the bitstream from the modulator over a given number of bits (specified by the oversampling rate) and provides samples at a reduced rate for further processing to the CPU.

Averaging can be used to increase the signal-to-noise performance of a conversion (see Figure 1-4 a and b). With a conventional ADC, each factor-of-4 oversampling can improve the SNR by approximately 6 dB or 1 bit. To achieve a 16-bit resolution out of a simple 1-bit ADC would require an impractical oversampling rate of 4^{15} = 1 073 741 824. To overcome this limitation, the sigma-delta modulator implements a technique called noise-shaping—due to an implemented feedback loop and integrators, the quantization noise is pushed to higher frequencies and, thus, much lower oversampling rates are sufficient to achieve high resolutions (see Figure 1-4 c).

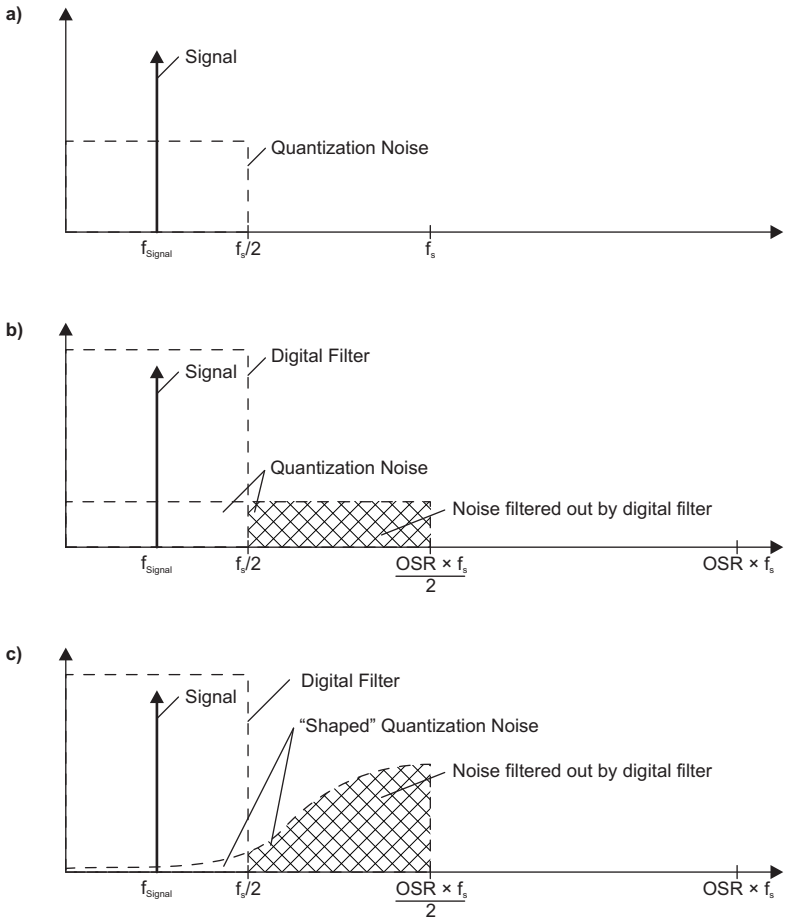

Figure 1-4. Sigma-Delta Principle

1.2.2 ADC Core

The analog-to-digital conversion is performed by a 1-bit second-order sigma-delta modulator. A single-bit comparator within the modulator quantizes the input signal with the modulator frequency f_M. The resulting 1-bit data stream is averaged by the digital filter for the conversion result.

1.2.3 Voltage Reference

The SD24_B module can use an external reference voltage (SD24REFS = 0) or an internal reference (SD24REFS = 1).

The internal SD24_B reference provides one fixed voltage of approximately 1.2 V. It requests and uses the bandgap voltage provided by the shared reference (REF) module as its reference voltage. The internal reference voltage is used by all SD24_B converters when requested with SD24REFS = 1. When using the internal reference, connect an external 100-nF capacitor connected from VREF to AVSS to reduce noise. See the device-specific data sheet for the parameters of the internal reference.

An external voltage reference must be applied to the VREF input when SD24REFS = 0. See the device-specific data sheet for the supported voltage range.

1.2.4 Modulator Clock

The modulator clock is generated globally for all modulators so that all modulators convert synchronously.

NOTE: Using an FLL-Based Clock

When an FLL-based clock with enabled clock modulation (DISMOD = 0 in UCSCTL1) is selected to clock the sigma-delta modulator, the clock that is provided to the modulator must be DCOCLK divided at least by 2. The division can be done in the FLL itself by selecting DCOCLKDIV instead of DCOCLK as the clock source and setting the FLLD bits to a nonzero value, by using the clock system clock dividers DIVM, DIVS, or DIVA corresponding to the sigma-delta input clock MCLK, SMCLK, or ACLK, respectively, or by using the clock divider build into the sigma-delta module.

1.2.5 Auto Power-Down

The SD24_B is designed for low-power applications. When a SD24_B converter is not actively converting, it is automatically disabled; it is automatically re-enabled when a conversion is started. When a converter is disabled, it consumes no current.

1.2.6 Analog Inputs

1.2.6.1 Analog Input Range and PGA

The full-scale input voltage range for each analog input pair is dependent on the gain setting of each converter. See the device-specific data sheet for full-scale input specifications.

1.2.6.2 Analog Input Setup

The analog input of each converter is configured using the SD24BINCTLx register. These settings can be independently configured for each SD24_B converter.

The gain for each PGA is selected by the SD24GAINx bits. A total of eight gain settings are available.

During conversion, any modification of the SD24BINCTLx register becomes effective with the next decimation step of the digital filter. After these bits are modified, the next three conversions may be invalid due to the settling time of the digital filter. This can be handled automatically with the SD24INTDLYx bits. When SD24INTDLYx = 00b, conversion interrupt requests do not begin until the fourth conversion after a start condition.

An external RC anti-aliasing filter is recommended for the SD24_B to prevent aliasing of the input signal. The cutoff frequency should be less than 10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements.

With SD24CAL = 1, the offset of the converter can be measured and calibrated in software afterwards.

1.2.6.3 Analog Input Characteristics

The SD24_B uses a switched-capacitor input stage that appears as an impedance to external circuitry (see Figure 1-5).

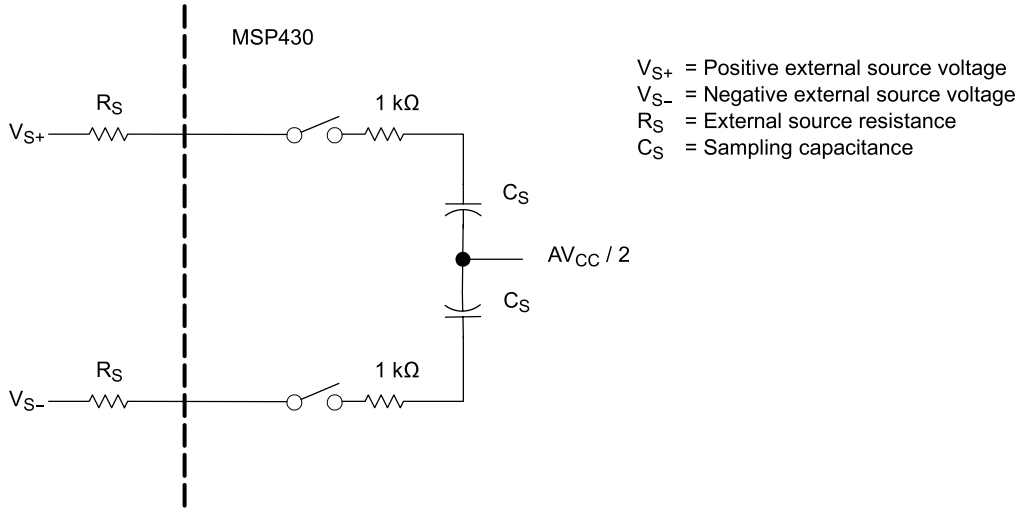

Figure 1-5. Analog Input Equivalent Circuit

The maximum modulator frequency f_M may be calculated from the minimum settling time $t_{Settling}$ of the sampling circuit.

$$t_{Settling} \geq (R_S + 1k\Omega) \times C_S \times \ln\left(\frac{GAIN \times 2^{17} \times V_{Ax}}{V_{REF}}\right) \quad (1)$$

Where

$$f_M = \left(\frac{1}{2 \times t_{settling}}\right) \text{ and } V_{Ax} = \max\left(\left|\frac{AV_{CC}}{2} - V_{S+}\right|, \left|\frac{AV_{CC}}{2} - V_{S-}\right|\right) \quad (2)$$

The sampling capacitor C_S varies with the gain setting. See the device-specific data sheet for parameters.

1.2.7 Digital Filter

The digital filter processes the 1-bit data stream from the modulator.

1.2.7.1 SINC^3 Filter

Figure 1-6 shows the structure of a SINC^3 filter.

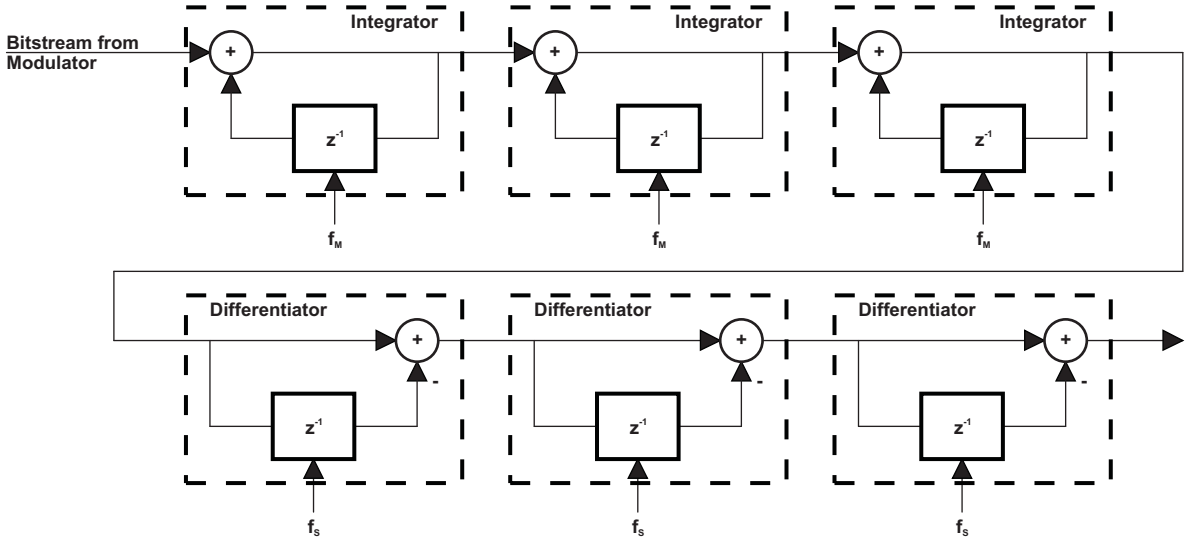

Figure 1-6. SINC^3 Filter Structure

The transfer function is described in the z-domain by:

$$H(z) = \left(\frac{1}{OSR} \times \frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{3}$$

The transfer function is described in the frequency domain by:

$$H(f) = \left(\frac{\text{sinc}\left(OSR\pi \frac{f}{f_M} \right)}{\text{sinc}\left(\pi \frac{f}{f_M} \right)} \right)^3 = \left(\frac{1}{OSR} \times \frac{\sin\left(OSR \times \pi \times \frac{f}{f_M} \right)}{\sin\left(\pi \times \frac{f}{f_M} \right)} \right)^3 \tag{4}$$

where the oversampling rate, OSR, is the ratio of the modulator frequency f_M to the sample frequency f_S. Figure 1-7 shows the filter's frequency response for an OSR of 32. The first filter notch is always at $f_S = f_M/OSR$. The notch's frequency can be adjusted by changing the modulator's frequency, f_M, using SD24SSELx, SD24PDIVx, and SD24DIVx or by adjusting the oversampling rate using the SD24BOSRx registers.

The digital filter for each enabled ADC converter completes the decimation of the digital bitstream and outputs new conversion results to the corresponding SD24BMEMx register at the sample frequency f_S.

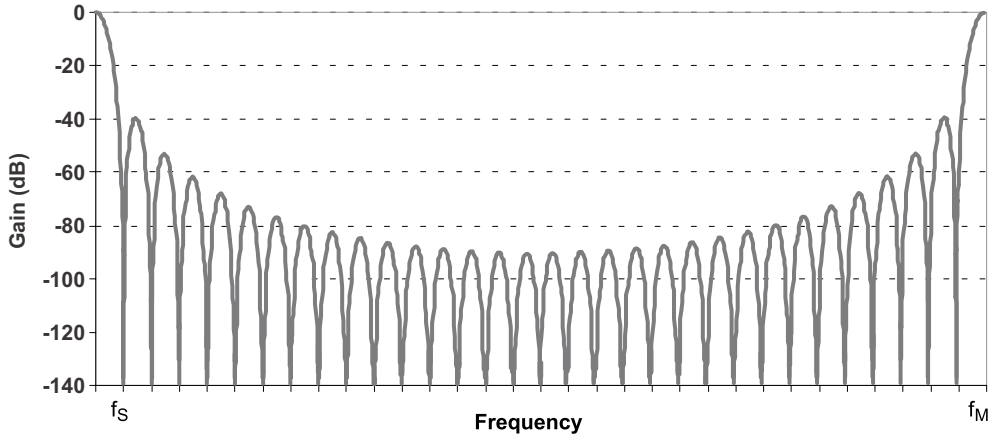

Figure 1-7. Comb Filter's Frequency Response With OSR = 32

Figure 1-8 shows the digital filter step response and conversion points. For step changes at the input after start of conversion, a settling time must be allowed before a valid conversion result is available. The SD24INTDLYx bits can provide sufficient filter settling time for a full-scale change at the ADC input. If the step occurs synchronously to the decimation of the digital filter, the valid data is available on the third conversion. An asynchronous step requires one additional conversion before valid data is available.

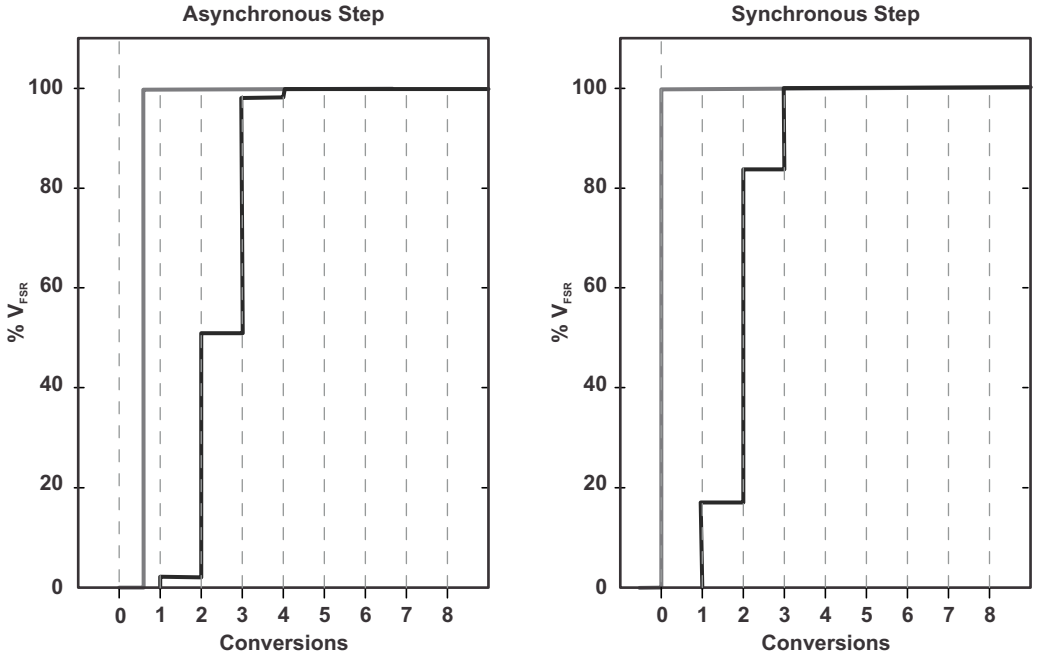

Figure 1-8. Digital Filter Step Response and Conversion Points Digital Filter Output

1.2.7.2 Cascade of Integrators

With each start of conversion or after change of the SD24INCTLx register for a given converter, the digital filter of this converter is reset. This allows the integrators implemented into the SINC filter to be used as a "Cascade of Integrators" by setting the interrupt delay to SD24INTDLYx = 11b and starting a new conversion (for example by writing SD24INCTLx) after each decimation step.

The full-scale value output by the "Cascade of Integrators" is given by FS = 1/6 × (OSR^3 + 3×OSR^2 + 2×OSR). In offset binary mode, the full-scale range is from 0 to FS. In twos-complement mode, the full-scale range is from -FS to +FS.

1.2.7.3 Digital Filter Output

The full-scale value output by the $SINC^3$ digital filter is dependent on the oversampling ratio OSR and is given by FS = 2^(3×$\log_2$(OSR)). In offset binary mode, the full-scale range is from 0 to FS. In twos-complement mode, the full-scale range is from -FS to +FS.

For example, the maximum OSR of 1024 results in a full-scale value of 1073741824 or 4000 000h; that is, a value that can be represented by 31 bits. All 31 bits can be accessed using the SD24BMEMHx and SD24BMEMLx registers. Depending on the selected data format and alignment, the representation within the SD24BMEMx registers differs.

In offset binary mode (SD24DFx = 00b), the bitstream coming from the modulator is interpreted as a stream of ones (1) and zeros (0). In twos-complement mode (SD24DFx = 01b), the bitstream is interpreted as ones (1) and minus ones (-1). In offset binary mode (SD24DFx = 00b) the output values range from 0 to FS. In twos-complement mode (SD24DFx = 01b), the output values range from -FS to +FS.

If right alignment is selected with SD24ALGN = 0, the digital filter's output value is directly mapped to the SD24_B conversion result registers SD24BMEMHx and SD24BMEMLx with the LSB of the filter's output being mapped to the LSB of SD24BMEMLx.

If left alignment is selected with SD24ALGN = 1, the mapping of the filter's output value to the conversion registers is dependent on the selected oversampling rate. In left aligned offset binary mode, the 32-bit value is left-shifted according to Table 1-1. In left aligned twos-complement mode, the 32-bit twos complement of the digital filter's output is left-shifted according to Table 1-2.

Table 1-3 gives an example for an oversampling rate of 256.

Table 1-1. Offset Binary Left Aligned Mapping

OSR Range	SD24BOSRx Register	Filter Output Left Shifted by	Filter's LSB Mapped to
1 to 32	0000h to 001Fh	17 bits	Bit 1of SD24BMEMHx
33 to 64	0020h to 003Fh	14 bits	Bit 14 of SD24BMEMLx
65 to 128	0040h to 007Fh	11 bits	Bit 11 of SD24BMEMLx
129 to 256	0080h to 00FFh	8 bits	Bit 8 of SD24BMEMLx
257 to 512	0100h to 01FFh	5 bits	Bit 5 of SD24BMEMLx
513 to 1024	0200h to 03FFh	2 bits	Bit 2 of SD24BMEMLx

Table 1-2. Twos-Complement Left Aligned Mapping

OSR Range	SD24BOSRx Register	Filter Output Left Shifted by	Filter's LSB Mapped to
1 to 32	0000h to 001Fh	16 bits	Bit 16 of SD24BMEMLx
33 to 64	0020h to 003Fh	13 bits	Bit 13 of SD24BMEMLx
65 to 128	0040h to 007Fh	10 bits	Bit 10 of SD24BMEMLx
129 to 256	0080h to 00FFh	7 bits	Bit 7 of SD24BMEMLx
257 to 512	0100h to 01FFh	4 bits	Bit 4 of SD24BMEMLx
513 to 1024	0200h to 03FFh	1 bit	Bit 1 of SD24BMEMLx

Table 1-3. Data Format Example for OSR = 256

SD24DFx	SD24ALGN	Format	Analog Input	Filter Output (hex)	SD24BMEMHx SD24BMEMLx (hex)
00b	0	Bipolar offset binary, right aligned	$+V_{FSR}$	0FF FFFF	00FF FFFF
			0 V	080 0000	0080 0000
			$-V_{FSR}$	000 0000	0000 0000
00b	1	Bipolar offset binary, left aligned	$+V_{FSR}$	0FF FFFF	FFFF FF00
			0 V	080 0000	8000 0000
			$-V_{FSR}$	000 0000	0000 0000
01b	0	Bipolar twos complement, right aligned	$+V_{FSR}$	00FF FFFF	00FF FFFF
			0 V	0000 0000	0000 0000
			$-V_{FSR}$	FF00 0000	FF00 0000
01b	1	Bipolar twos complement, left aligned	$+V_{FSR}$	00FF FFFF	7FFF FF80
			0 V	0000 0000	0000 0000
			$-V_{FSR}$	FF00 0000	8000 0000

1.2.8 Bitstream Input and Output

The bitstream of each modulator can be fed to pins. The SD24MCx selects the encoding of the output bitstream.

The SD24_B module also allows to feed in a modulator bitstream into the digital filter with SD24DI = 1. Setting SD24DI = 1 for a converter disables the associated modulator. The incoming bitstream can be either synchronous to the modulator frequency f_M or it can be a Manchester decoded bitstream. The format is selected with the SD24MCx bits. The Manchester decoder requires a zero-to-one or a one-to-zero transition in the incoming bitstream to be able to synchronize correctly to it. Up to the first transition, the decoded data can be incorrect.

Figure 1-9 shows the block diagram of the output encoder and the input decoder.

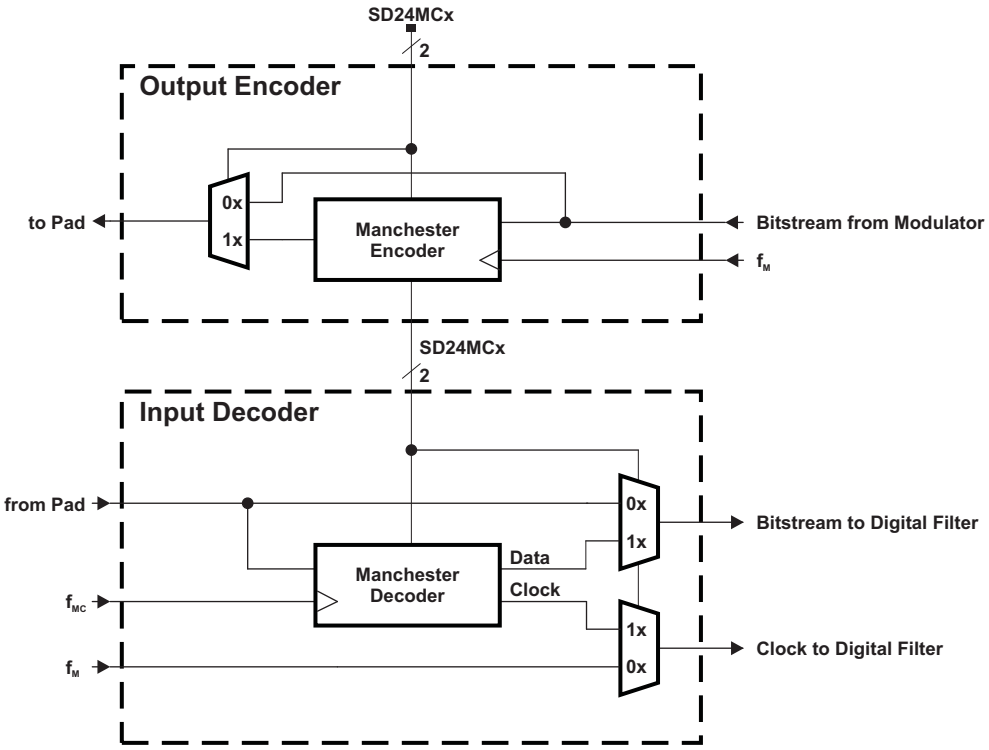

Figure 1-9. SD24_B Output Encoder and Input Decoder Block Diagram

1.2.9 Conversion Modes

Each SD24_B converter can be configured for two modes of operation, single conversion and continuous conversion, as listed in Table 1-4. The SD24SNGL bit selects the converter's conversion mode.

Table 1-4. Conversion Mode Summary

SD24SNGL	Mode	Operation
1	Single conversion	The converter converts once, until the corresponding IFG is set.
0	Continuous conversion	The converter converts continuously.

In addition, the converters can be grouped together by selecting a common start-of-conversion trigger using the SD24SCSx bits. There are up to four software start-of-conversion triggers and three external (for example a timer output) start-of-conversion triggers available.

1.2.9.1 Single Converter, Single Conversion

Setting the SD24SC bit of a converter initiates one conversion on that converter when SD24SNGL = 1 and SD24SCSx = 00b; that is, the converter is not grouped with any other converters. The SD24SC bit is automatically cleared after conversion completion; that is, when the converter's interrupt flag is set. Clearing SD24SC before the conversion is completed immediately stops conversion of the selected converter, the converter is powered down, and the corresponding digital filter is turned off.

Figure 1-10 shows examples of single conversions with different SD24INTDLYx and SD24PREx settings.

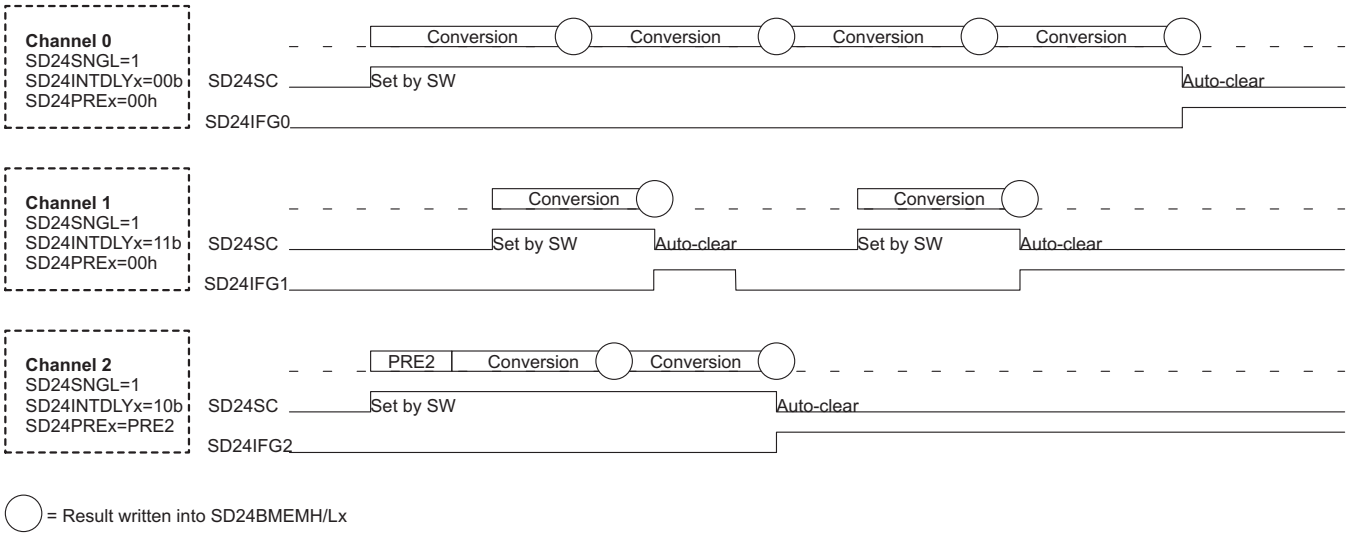

Figure 1-10. Single Conversion Examples

1.2.9.2 Single Converter, Continuous Conversion

When SD24SNGL = 0, continuous conversion mode is selected. A converter configured with SD24SCSx = 00b begins converting when SD24SC is set and continues until the SD24SC bit is cleared by software. Clearing SD24SC immediately stops conversion of the selected converter, the converter is powered down, and the corresponding digital filter is turned off.

1.2.9.3 Group of Converters

SD24_B converters can be grouped together with a common start-of-conversion trigger by setting SD24SCSx to a nonzero value. All converters with the same SD24SCS settings form a group, and the conversion is started by the selected group for all attached converters synchronously. The conversion can be started either by software by setting the respective SD24GRPxSC bit (see Figure 1-11) or by a rising edge on an external trigger signal like a timer output (see Figure 1-12). The connected trigger sources are device dependent–see the device-specific data sheet for details.

When SD24SNGL = 1 for a converter in a group, single conversion mode is selected. A single conversion of this converter occurs synchronously when the group trigger starts conversion.

The start of conversion is also reflected in each converter's SD24SC bit. By clearing the SD24SC bit of one converter in a group, the conversion of this converter is immediately stopped. Setting the SD24SC bit of an individual converter in a group immediately starts conversion for this converter independent of the group's start of conversion trigger.

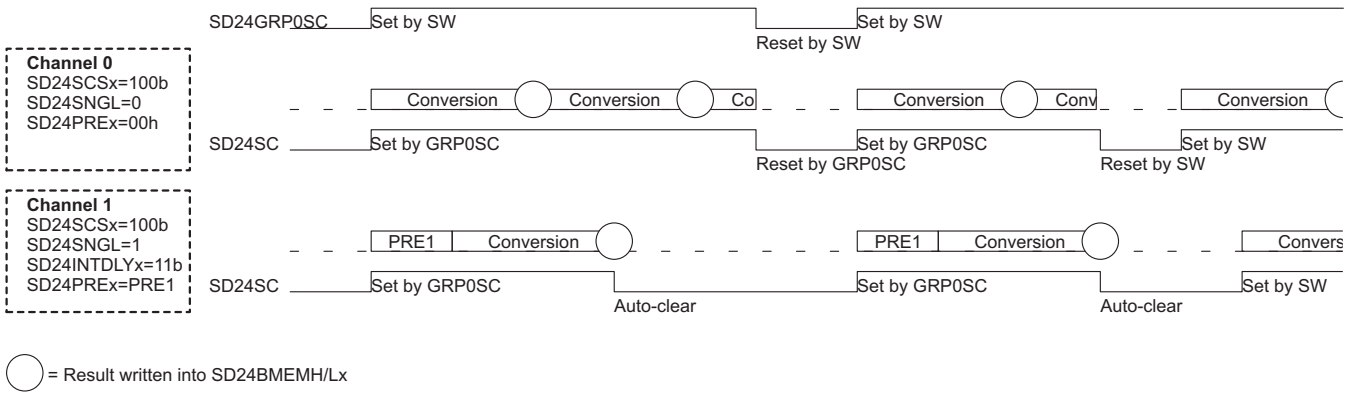

Figure 1-11. Grouped Operation - Internal Start-of-Conversion Trigger

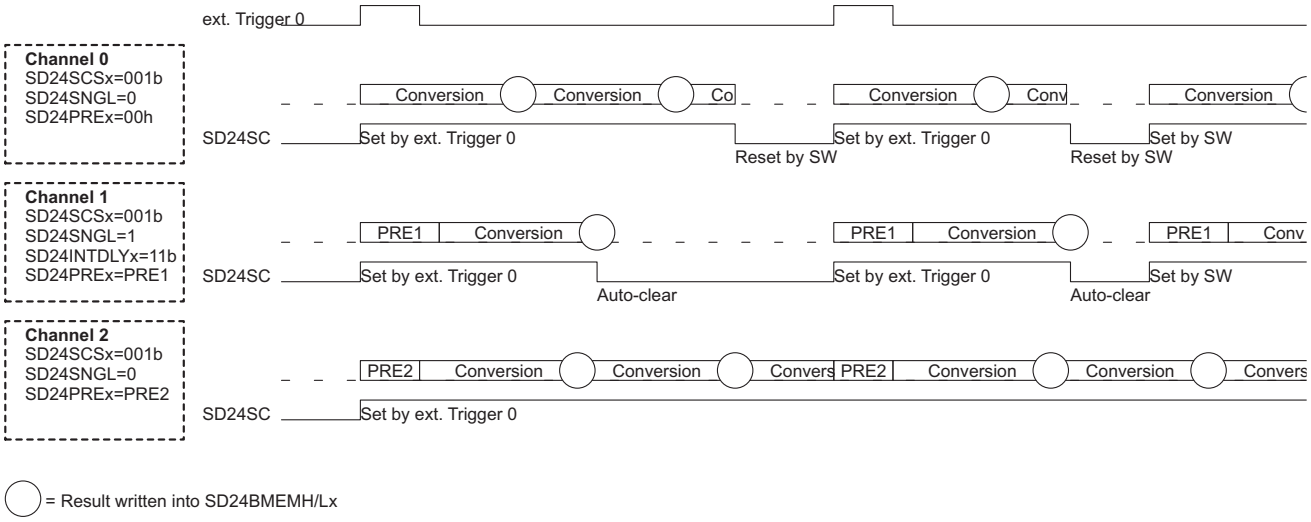

Figure 1-12. Grouped Operation - External Start-of-Conversion Trigger

1.2.10 Conversion Operation Using Preload

When multiple converters are grouped, the SD24BPREx registers can be used to delay the conversion time frame for each converter. Using SD24BPREx, the decimation time of the digital filter is increased one time by the specified number of f_M clock cycles. The value can range from 0 (no increase) to the value of SD24BOSRx (oversampling rate minus 1). Figure 1-13 shows an example using SD24BPREx.

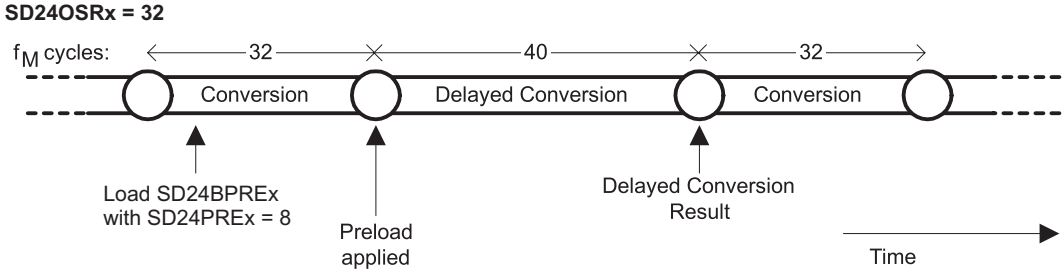

Figure 1-13. Conversion Delay Using Preload - Example

The SD24BPREx delay is applied at the beginning of the next conversion cycle after it is written; that is, the specified number of delay cycles is applied to the conversion cycle following the write to SD24BPREx. Further conversions are not delayed. After modifying SD24BPREx, the next write to SD24BPREx should not occur until the current conversion cycle is completed and the written value is applied. For example, the preload value can be modified after the corresponding SD24IFGx is set. At start of conversion, the first conversion is delayed by the latest value written into SD24BPREx. If no delay at start of conversion is desired, a previously written nonzero value must be changed to zero before starting the conversion.

The accuracy of the result for the delayed conversion cycle using SD24BPREx is dependent on the length of the delay and the frequency of the analog signal being sampled. For example, when measuring a DC signal, SD24BPREx delay has no effect on the conversion result regardless of the duration. The user must determine when the delayed conversion result is useful in an application.

Figure 1-14 shows the operation of grouped converters 0 and 1. The preload register of converter 1 is loaded with zero, which results in immediate conversion, while the conversion cycle of converter 0 is delayed by setting SD24BPRE0 = 8. The first converter 0 conversion uses SD24BPREx = 8, shifting all subsequent conversions by 8 f_M clock cycles.

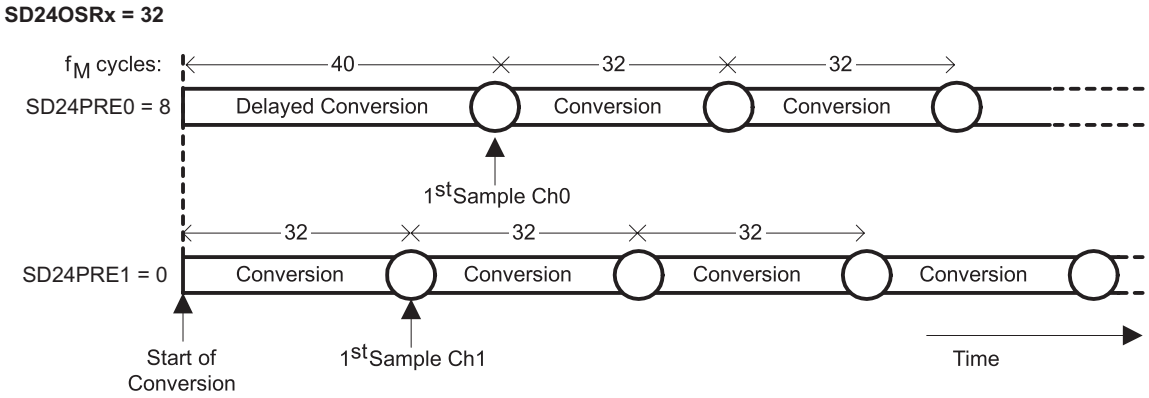

Figure 1-14. Start of Conversion Using Preload - Example

1.2.11 Grounding and Noise Considerations

As with any high-resolution ADC, appropriate printed circuit board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. Therefore, solid decoupling on both the digital and analog supply is required (best with two capacitors, one 10 µF and one 100 nF, per supply).

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommended to achieve high accuracy.

If the internal reference is used, the reference voltage should be buffered externally by connecting a small (approximately 100 nF) capacitor to VREF to reduce the noise on the reference.

1.2.12 Trigger Generator

The SD24_B module provides a trigger generator that allows synchronization of external modules (for example other ADCs) with the SD24_B. Configuration of the trigger generator (see the block diagram in Figure 1-15) is similar to a converter (although it does not provide the analog part and thus all associated digital logic). It can be started the same as a converter, and the trigger pulse and the setting of the interrupt flag is generated as it would be generated by a converter with the same OSR and preload settings. This means that the trigger generator mimics the timing of a converter. If the trigger generator is configured the same as the converters and is started together with the converters, it can trigger external modules synchronous with the conversion (that is, decimation) of the SD24_B converters.

NOTE: Only the MSP430F674xx(1)(A), MSP430F676xx(1)(A), and MSP430F677x(1)(A) devices support the trigger generator.

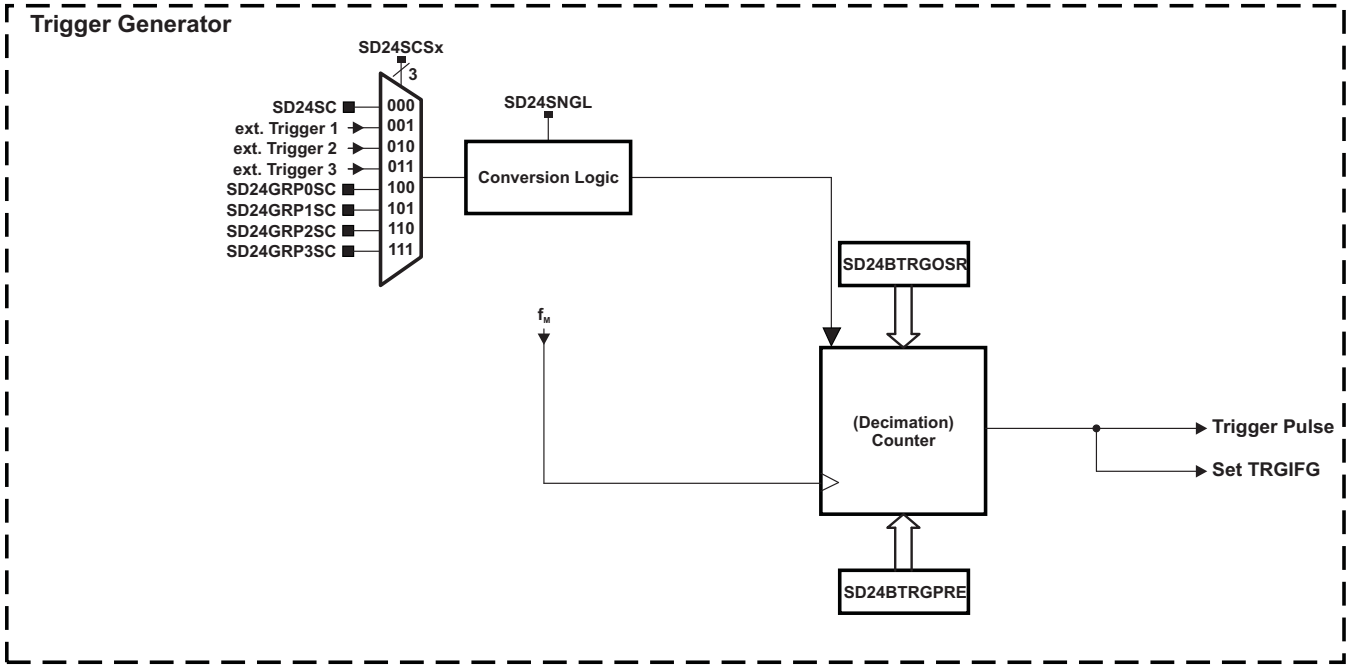

Figure 1-15. SD24_B Trigger Generator Block Diagram

1.2.13 SD24_B Interrupts

The SD24_B has these interrupt sources for each ADC converter:

- SD24IFGx : conversion ready interrupt
- SD24OVIFGx : conversion memory overflow
- SD24TRGIFG: trigger generator interrupt

The SD24IFGx bits are set when their corresponding SD24BMEMHx and SD24BMEMLx memory registers are written with a conversion result. An interrupt request is generated if the corresponding SD24IEx bit and the GIE bit are set. Whether or not an SD24_B overflow condition sets a SD24OVIFG depends on the SD24OV32 setting: If SD24OV32 = 0, the overflow occurs when a conversion result is written to a SD24BMEMHx and SD24BMEMLx register pair before one of the registers was read. If SD24OV32 = 1, the overflow occurs when a new conversion result is written before the complete 32-bit of the previous conversion result was read.

1.2.13.1 SD24BIV, Interrupt Vector Generator

All SD24_B interrupt sources are prioritized and combined to source a single interrupt vector. SD24BIV is used to determine which enabled SD24_B interrupt source requested an interrupt. The highest priority SD24_B interrupt request that is enabled generates a number in the SD24BIV register (see register description). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled SD24_B interrupts do not affect the SD24BIV value.

Any read access of the SD24BIV register has no effect on the SD24OVIFG or SD24IFG flags. The SD24IFG flags are reset by reading the associated SD24BMEMx register or by clearing the flags in software. SD24OVIFG bits can only be reset with software. The SD24TRGIFG is reset by reading SD24BIV or by clearing the flag in software. A write access to SD24BIV clears all interrupt flags.

If another interrupt is pending after servicing of an interrupt, another interrupt is generated. For example, if a SD24OVIFGx and one or more SD24IFGx interrupts are pending when the interrupt service routine accesses the SD24BIV register, the SD24OVIFGx interrupt condition is serviced first and the corresponding flags must be cleared in software. After the RETI instruction of the interrupt service routine is executed, the highest priority SD24IFGx pending generates another interrupt request.

1.2.13.2 Interrupt Delay Operation

The SD24INTDLYx bits control the timing for the first interrupt service request for the corresponding converter. This feature delays the interrupt request for a completed conversion by up to four conversion cycles allowing the digital filter to settle prior to generating an interrupt request. The delay is applied each time the conversion is started or when the SD24BINCTLx register is modified. SD24INTDLYx disables overflow interrupt generation for the converter for the selected number of delay cycles. Interrupt requests for the delayed conversions are not generated during the delay.

1.2.14 Using SD24_B With DMA

Devices with an integrated DMA controller can automatically move data from any SD24BMEMHx and SD24BMEMLx register to another location. DMA transfers are done without CPU intervention and independent of any low-power modes.

The SD24DMAx bits in SD24BCTL1 register select the converter that triggers a DMA transfer. The transfer is triggered by the respective SD24IFGx flag. If the respective interrupt enable bit SD24IEx is set, the selected SD24IFGx flag does not trigger a transfer. Any SD24IFGx is automatically cleared when the DMA controller accesses the corresponding SD24BMEMHx and SD24BMEMLx registers.

1.3 SD24_B Registers

The SD24_B registers are listed in Table 1-5. The available converter registers are device-specific depending on the number of implemented converters.

The base address of the SD24_B module can be found in the device-specific data sheet. The address offset of each SD24_B register is given in Table 1-5.

Table 1-5. SD24_B Registers

Offset	Acronym	Register Name	Type	Reset	Section
00h	SD24BCTL0	SD24_B Control 0 Register	Read/write	0000h	Section 1.3.1
02h	SD24BCTL1	SD24_B Control 1 Register	Read/write	0800h	Section 1.3.2
04h	SD24BTRGCTL	SD24_B Trigger Control Register	Read/write	0000h	Section 1.3.3
06h	SD24BTRGOSR	SD24_B Trigger OSR Control Register	Read/write	00FFh	Section 1.3.10
08h	SD24BTRGPRE	SD24_B Trigger Preload Register	Read/write	0000h	Section 1.3.12
0Ah	SD24BIFG	SD24_B Interrupt Flag Register	Read/write	0000h	Section 1.3.4
0Ch	SD24BIE	SD24_B Interrupt Enable Register	Read/write	0000h	Section 1.3.5
0Eh	SD24BIV	SD24_B Interrupt Vector Register	Read/write	0000h	Section 1.3.6
10h	SD24BCCTL0	SD24_B Converter 0 Control Register	Read/write	0000h	Section 1.3.7
12h	SD24BINCTL0	SD24_B Converter 0 Input Control Register	Read/write	0000h	Section 1.3.8
14h	SD24BOSR0	SD24_B Converter 0 OSR Control Register	Read/write	00FFh	Section 1.3.9
16h	SD24BPRE0	SD24_B Converter 0 Preload Register	Read/write	0000h	Section 1.3.11
18h	SD24BCCTL1	SD24_B Converter 1 Control Register	Read/write	0000h	Section 1.3.7
1Ah	SD24BINCTL1	SD24_B Converter 1 Input Control Register	Read/write	0000h	Section 1.3.8
1Ch	SD24BOSR1	SD24_B Converter 1 OSR Control Register	Read/write	00FFh	Section 1.3.9
1Eh	SD24BPRE1	SD24_B Converter 1 Preload Register	Read/write	0000h	Section 1.3.11
20h	SD24BCCTL2	SD24_B Converter 2 Control Register	Read/write	0000h	Section 1.3.7
22h	SD24BINCTL2	SD24_B Converter 2 Input Control Register	Read/write	0000h	Section 1.3.8
24h	SD24BOSR2	SD24_B Converter 2 OSR Control Register	Read/write	00FFh	Section 1.3.9
26h	SD24BPRE2	SD24_B Converter 2 Preload Register	Read/write	0000h	Section 1.3.11
28h	SD24BCCTL3	SD24_B Converter 3 Control Register	Read/write	0000h	Section 1.3.7
2Ah	SD24BINCTL3	SD24_B Converter 3 Input Control Register	Read/write	0000h	Section 1.3.8
2Ch	SD24BOSR3	SD24_B Converter 3 OSR Control Register	Read/write	00FFh	Section 1.3.9
2Eh	SD24BPRE3	SD24_B Converter 3 Preload Register	Read/write	0000h	Section 1.3.11
30h	SD24BCCTL4	SD24_B Converter 4 Control Register	Read/write	0000h	Section 1.3.7
32h	SD24BINCTL4	SD24_B Converter 4 Input Control Register	Read/write	0000h	Section 1.3.8
34h	SD24BOSR4	SD24_B Converter 4 OSR Control Register	Read/write	00FFh	Section 1.3.9
36h	SD24BPRE4	SD24_B Converter 4 Preload Register	Read/write	0000h	Section 1.3.11
38h	SD24BCCTL5	SD24_B Converter 5 Control Register	Read/write	0000h	Section 1.3.7
3Ah	SD24BINCTL5	SD24_B Converter 5 Input Control Register	Read/write	0000h	Section 1.3.8
3Ch	SD24BOSR5	SD24_B Converter 5 OSR Control Register	Read/write	00FFh	Section 1.3.9
3Eh	SD24BPRE5	SD24_B Converter 5 Preload Register	Read/write	0000h	Section 1.3.11
40h	SD24BCCTL6	SD24_B Converter 6 Control Register	Read/write	0000h	Section 1.3.7
42h	SD24BINCTL6	SD24_B Converter 6 Input Control Register	Read/write	0000h	Section 1.3.8
44h	SD24BOSR6	SD24_B Converter 6 OSR Control Register	Read/write	00FFh	Section 1.3.9
46h	SD24BPRE6	SD24_B Converter 6 Preload Register	Read/write	0000h	Section 1.3.11
48h	SD24BCCTL7	SD24_B Converter 7 Control Register	Read/write	0000h	Section 1.3.7
4Ah	SD24BINCTL7	SD24_B Converter 7 Input Control Register	Read/write	0000h	Section 1.3.8
4Ch	SD24BOSR7	SD24_B Converter 7 OSR Control Register	Read/write	00FFh	Section 1.3.9
4Eh	SD24BPRE7	SD24_B Converter 7 Preload Register	Read/write	0000h	Section 1.3.11
50h	SD24BMEML0	SD24_B Converter 0 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13

Table 1-5. SD24_B Registers (continued)

Offset	Acronym	Register Name	Type	Reset	Section
52h	SD24BMEMH0	SD24_B Converter 0 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
54h	SD24BMEML1	SD24_B Converter 1 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
56h	SD24BMEMH1	SD24_B Converter 1 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
58h	SD24BMEML2	SD24_B Converter 2 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
5Ah	SD24BMEMH2	SD24_B Converter 2 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
5Ch	SD24BMEML3	SD24_B Converter 3 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
5Eh	SD24BMEMH3	SD24_B Converter 3 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
60h	SD24BMEML4	SD24_B Converter 4 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
62h	SD24BMEMH4	SD24_B Converter 4 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
64h	SD24BMEML5	SD24_B Converter 5 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
66h	SD24BMEMH5	SD24_B Converter 5 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
68h	SD24BMEML6	SD24_B Converter 6 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
6Ah	SD24BMEMH6	SD24_B Converter 6 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14
6Ch	SD24BMEML7	SD24_B Converter 7 Conversion Memory Low Word Register	Read/write	0000h	Section 1.3.13
6Eh	SD24BMEMH7	SD24_B Converter 7 Conversion Memory High Word Register	Read/write	0000h	Section 1.3.14

1.3.1 SD24BCTL0 Register

SD24_B Control Register 0

Figure 1-16. SD24BCTL0 Register

15	14	13	12	11	10	9	8
SD24DIVx					SD24PDIVx		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24CLKOS	SD24M4	SD24SSELx		Reserved	SD24REFS	SD24OV32	Reserved
rw-0	rw-0	rw-0	rw-0	r0	rw-0	rw-0	r0

Table 1-6. SD24BCTL0 Register Description

Bit	Field	Type	Reset	Description
15-11	SD24DIVx	RW	0h	SD24_B frequency divider. Together with SD24PDIVx, the SD24_B frequency f_{SD24} is calculated as $f_{SD24} = f_{SD24SCLK} / [(SD24DIVx + 1) \times 2^{SD24PDIVx}]$. 0000b = Divide by 1 0001b = Divide by 2 ⋮ 11110b = Divide by 31 11111b = Divide by 32
10-8	SD24PDIVx	RW	0h	SD24_B frequency prescaler. Together with SD24DIVx, the SD24_B frequency f_{SD24} is calculated as $f_{SD24} = f_{SD24SCLK} / [(SD24DIVx + 1) \times 2^{SD24PDIVx}]$. 000b = Divide by 1 001b = Divide by 2 010b = Divide by 4 011b = Divide by 8 100b = Divide by 16 101b = Divide by 32 110b = Divide by 64 111b = Divide by 128
7	SD24CLKOS	RW	0h	Clock output select 0b = Modulator clock, f_M 1b = Manchester decoder clock, f_{MC}. Depending on SD24M4, the Manchester decoder clock is equal to the modulator clock or four times the modulator clock.
6	SD24M4	RW	0h	Modulator clock to Manchester decoder clock ratio 0b = Modulator clock equals Manchester decoder clock, $f_M = f_{MC} = f_{SD24}$ 1b = Modulator clock is 1/4 of the Manchester decoder clock, $f_M = f_{MC}/4 = f_{SD24}/4$, $f_{MC} = f_{SD24}$
5-4	SD24SSEL	RW	0h	SD24_B clock source select 00b = MCLK 01b = SMCLK 10b = ACLK 11b = External SD24_B clock (SD24CLK)
3	Reserved	R	0h	Reserved. Always reads as 0.
2	SD24REFS	RW	0h	Reference select 0b = External reference selected. Internal reference voltage buffer disabled. 1b = Internal reference from shared REF selected. This requests the reference voltage from the shared REF and buffers it internally to the SD24_B.
1	SD24OV32	RW	0h	SD24_B overflow control 0b = Overflow on 16-bit (1 word) only; that is, only one of the SD24BMEMLx and SD24BMEMHx registers must be read to prevent the overflow interrupt flag being set. 1b = Overflow on 32-bit (2 words); that is, both SD24BMEMx and SD24BMEMHx registers must be read to prevent the overflow interrupt flag being set.
0	Reserved	R	0h	Reserved. Always reads as 0.

1.3.2 SD24BCTL1 Register

SD24_B Control Register 1

Figure 1-17. SD24BCTL1 Register

15	14	13	12	11	10	9	8
Reserved				SD24DMAx			
r0	r0	r0	r0	rw-1	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved				SD24GRP3SC	SD24GRP2SC	SD24GRP1SC	SD24GRP0SC
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0

Table 1-7. SD24BCTL1 Register Description

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0h	Reserved. Always reads as 0.
11-8	SD24DMAx	RW	8h	DMA trigger select. Selects the converter that should trigger a DMA transfer. 0000b = SD24IFG0 triggers DMA (if SD24IE0 = 0) 0001b = SD24IFG1 triggers DMA (if SD24IE1 = 0) 0010b = SD24IFG2 triggers DMA (if SD24IE2 = 0) 0011b = SD24IFG3 triggers DMA (if SD24IE3 = 0) 0100b = SD24IFG4 triggers DMA (if SD24IE4 = 0) 0101b = SD24IFG5 triggers DMA (if SD24IE5 = 0) 0110b = SD24IFG6 triggers DMA (if SD24IE6 = 0) 0111b = SD24IFG7 triggers DMA (if SD24IE7 = 0) 1000b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1001b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1010b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1011b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1100b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1101b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1110b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0) 1111b = SD24TRGIFG triggers DMA (if SD24TRGIE = 0)
7-4	Reserved	R	0h	Reserved. Always reads as 0.
3	SD24GRP3SC	RW	0h	SD24_B Group 3 start of conversion. Software controlled start of conversion for all converters belonging to group 3. 0b = No conversion start 1b = Start conversion for group 3
2	SD24GRP2SC	RW	0h	SD24_B Group 2 start of conversion. Software controlled start of conversion for all converters belonging to group 2. 0b = No conversion start 1b = Start conversion for group 2
1	SD24GRP1SC	RW	0h	SD24_B Group 1 start of conversion. Software controlled start of conversion for all converters belonging to group 1. 0b = No conversion start 1b = Start conversion for group 1
0	SD24GRP0SC	RW	0h	SD24_B Group 0 start of conversion. Software controlled start of conversion for all converters belonging to group 0. 0b = No conversion start 1b = Start conversion for group 0

1.3.3 SD24BTRGCTL Register

SD24_B Trigger Control Register
Note: Only the MSP430F674xx(1)(A), MSP430F676xx(1)(A), and MSP430F677x(1)(A) devices support the trigger generator.

Figure 1-18. SD24BTRGCTL Register

15	14	13	12	11	10	9	8
Reserved				SD24TRGIE	SD24TRGIFG	Reserved	SD24SNGL
r0	r0	r0	r0	rw-0	rw-0	r0	rw-0
7	6	5	4	3	2	1	0
Reserved				SD24SCSx			SD24SC
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0

Table 1-8. SD24BTRGCTL Register Description

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0h	Reserved. Always reads as 0.
11	SD24TRGIE	RW	0h	SD24_B trigger interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
10	SD24TRGIFG	RW	0h	SD24_B trigger interrupt flag 0b = No interrupt pending 1b = Interrupt pending
9	Reserved	R	0h	Reserved. Always reads as 0.
8	SD24SNGL	RW	0h	Single trigger mode select 0b = Continuous triggers generated (like a converter in continuous conversion mode). 1b = Single trigger generated (like a converter in single conversion mode).
7-4	Reserved	R	0h	Reserved. Always reads as 0.
3-1	SD24SCSx	RW	0h	Start of conversion or trigger generation select 000b = SD24SC bit 001b = External trigger 1 (see the device-specific data sheet) 010b = External trigger 2 (see the device-specific data sheet) 011b = External trigger 3 (see the device-specific data sheet) 100b = Group 0 - Start of conversion defined by SD24GRP0SC bits in register SD24BCTL1 101b = Group 1 - Start of conversion defined by SD24GRP1SC bits in register SD24BCTL1 110b = Group 2 - Start of conversion defined by SD24GRP2SC bits in register SD24BCT1L 111b = Group 3 - Start of conversion defined by SD24GRP3SC bits in register SD24BCTL1
0	SD24SC	RW	0h	Start of conversion or trigger generation. Software controlled start of conversion if SD24SCS = 00b. Manual stop of conversion (independent of SD24SCS setting). If a conversion is ongoing (triggered by any source selected through SD24SCS) this is indicated by SD24SC = 1. 0b = No conversion start or stop conversion 1b = Start conversion or trigger generation

1.3.4 SD24BIFG Register

SD24_B Interrupt Flag Register

Figure 1-19. SD24BIFG Register

15	14	13	12	11	10	9	8
SD24OVIFG7	SD24OVIFG6	SD24OVIFG5	SD24OVIFG4	SD24OVIFG3	SD24OVIFG2	SD24OVIFG1	SD24OVIFG0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24IFG7	SD24IFG6	SD24IFG5	SD24IFG4	SD24IFG3	SD24IFG2	SD24IFG1	SD24IFG0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-9. SD24BIFG Register Description

Bit	Field	Type	Reset	Description
15	SD24OVIFG7	RW	0h	SD24_B converter 7 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML7 or SD24BMEMH7 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML7 or SD24BMEMH7 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
14	SD24OVIFG6	RW	0h	SD24_B converter 6 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML6 or SD24BMEMH6 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML6 or SD24BMEMH6 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
13	SD24OVIFG5	RW	0h	SD24_B converter 5 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML5 or SD24BMEMH5 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML5 or SD24BMEMH5 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
12	SD24OVIFG4	RW	0h	SD24_B converter 4 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML4 or SD24BMEMH4 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML4 or SD24BMEMH4 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
11	SD24OVIFG3	RW	0h	SD24_B converter 3 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML3 or SD24BMEMH3 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML3 or SD24BMEMH3 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending

Table 1-9. SD24BIFG Register Description (continued)

Bit	Field	Type	Reset	Description
10	SD24OVIFG2	RW	0h	SD24_B converter 2 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML2 or SD24BMEMH2 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML2 or SD24BMEMH2 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
9	SD24OVIFG1	RW	0h	SD24_B converter 1 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML1 or SD24BMEMH1 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML1 or SD24BMEMH1 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
8	SD24OVIFG0	RW	0h	SD24_B converter 0 overflow interrupt flag. These bits are set depending on the SD24OV32 bit settings: When none of the corresponding conversion registers SD24BMEML0 or SD24BMEMH0 are read before new values are loaded (SD24OV32 = 0). When only one of the corresponding conversion registers SD24BMEML0 or SD24BMEMH0 is read before new values are loaded (SD24OV32 = 1). 0b = No interrupt pending 1b = Interrupt pending
7	SD24IFG7	RW	0h	SD24_B converter 7 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML7 and SD24BMEMH7 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML7 or SD24BMEMH7 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending
6	SD24IFG6	RW	0h	SD24_B converter 6 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML6 and SD24BMEMH6 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML6 or SD24BMEMH6 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending
5	SD24IFG5	RW	0h	SD24_B converter 5 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML5 and SD24BMEMH5 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML5 or SD24BMEMH5 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending
4	SD24IFG4	RW	0h	SD24_B converter 4 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML4 and SD24BMEMH4 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML4 or SD24BMEMH4 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending
3	SD24IFG3	RW	0h	SD24_B converter 3 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML3 and SD24BMEMH3 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML3 or SD24BMEMH3 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending

Table 1-9. SD24BIFG Register Description (continued)

Bit	Field	Type	Reset	Description
2	SD24IFG2	RW	0h	SD24_B converter 2 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML2 and SD24BMEMH2 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML2 or SD24BMEMH2 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending
1	SD24IFG1	RW	0h	SD24_B converter 1 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML1 and SD24BMEMH1 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML1 or SD24BMEMH1 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending
0	SD24IFG0	RW	0h	SD24_B converter 0 interrupt flag. These bits are set when the corresponding conversion registers SD24BMEML0 and SD24BMEMH0 are loaded with a new conversion result. The bits are reset by reading one of the SD24BMEML0 or SD24BMEMH0 registers, or may be reset by software. 0b = No interrupt pending 1b = Interrupt pending

1.3.5 SD24BIE Register

SD24_B Interrupt Enable Register

Figure 1-20. SD24BIE Register

15	14	13	12	11	10	9	8
SD24OVIE7	SD24OVIE6	SD24OVIE5	SD24OVIE4	SD24OVIE3	SD24OVIE2	SD24OVIE1	SD24OVIE0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24IE7	SD24IE6	SD24IE5	SD24IE4	SD24IE3	SD24IE2	SD24IE1	SD24IE0
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-10. SD24BIE Register Description

Bit	Field	Type	Reset	Description
15	SD24OVIE7	RW	0h	SD24_B converter 7 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
14	SD24OVIE6	RW	0h	SD24_B converter 6 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
13	SD24OVIE5	RW	0h	SD24_B converter 5 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
12	SD24OVIE4	RW	0h	SD24_B converter 4 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
11	SD24OVIE3	RW	0h	SD24_B converter 3 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
10	SD24OVIE2	RW	0h	SD24_B converter 2 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
9	SD24OVIE1	RW	0h	SD24_B converter 1 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
8	SD24OVIE0	RW	0h	SD24_B converter 0 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
7	SD24IE7	RW	0h	SD24_B converter 7 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
6	SD24IE6	RW	0h	SD24_B converter 6 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
5	SD24IE5	RW	0h	SD24_B converter 5 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
4	SD24IE4	RW	0h	SD24_B converter 4 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
3	SD24IE3	RW	0h	SD24_B converter 3 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

Table 1-10. SD24BIE Register Description (continued)

Bit	Field	Type	Reset	Description
2	SD24IE2	RW	0h	SD24_B converter 2 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
1	SD24IE1	RW	0h	SD24_B converter 1 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	SD24IE0	RW	0h	SD24_B converter 0 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

1.3.6 SD24BIV Register

SD24_B Interrupt Vector Register

Figure 1-21. SD24BIV Register

15	14	13	12	11	10	9	8
SD24BIVx							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
SD24BIVx							
r0	r0	r0	r-0	r-0	r-0	r-0	r0

Table 1-11. SD24BIV Register Description

Bit	Field	Type	Reset	Description
15-0	SD24BIVx	R	0h	SD24_B Interrupt vector value. It generates an value that can be used as address offset for fast interrupt service routine handling. Writing to this register clears all pending interrupt flags. When an overflow occurs (02h), the software must check all SD24OVIFGx flags to determine which converter caused the overflow. 00h = No Interrupt pending 02h = Interrupt Source: SD24_B memory overflow; Interrupt Flag: SD24OVIFGx; Interrupt Priority: Highest 04h = Interrupt Source: SD24_B trigger interrupt flag; Interrupt Flag: SD24TRGIFG 06h = Interrupt Source: SD24_B converter 0 memory interrupt flag; Interrupt Flag: SD24IFG0 08h = Interrupt Source: SD24_B converter 1 memory interrupt flag; Interrupt Flag: SD24IFG1 0Ah = Interrupt Source: SD24_B converter 2 memory interrupt flag; Interrupt Flag: SD24IFG2 0Ch = Interrupt Source: SD24_B converter 3 memory interrupt flag; Interrupt Flag: SD24IFG3 0Eh = Interrupt Source: SD24_B converter 4 memory interrupt flag; Interrupt Flag: SD24IFG4 10h = Interrupt Source: SD24_B converter 5 memory interrupt flag; Interrupt Flag: SD24IFG5 12h = Interrupt Source: SD24_B converter 6 memory interrupt flag; Interrupt Flag: SD24IFG6 14h = Interrupt Source: SD24_B converter 7 memory interrupt flag; Interrupt Flag: SD24IFG7; Interrupt Priority: Lowest

1.3.7 SD24BCCTLx Register

SD24_B Converter x Control Register

Figure 1-22. SD24BCCTLx Register

15	14	13	12	11	10	9	8
Reserved	SD24MCx		SD24DI	SD24DFSx		SD24CAL	SD24SNGL
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	SD24ALGN	SD24DFx		SD24SCSx			SD24SC
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-12. SD24BCCTLx Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14-16	SD24MCx	RW	0h	Manchester Coding of bitstream. 00b = Bitstream synchronous to f_M. Output data changes with falling clock edge, input data is captured with rising clock edge. 01b = Bitstream synchronous to f_M. Output data changes with rising clock edge, input data is captured with falling clock edge. 10b = Output bitstream Manchester encoded. Input bitstream Manchester decoded with oversampling of the input signal. A logic 1 is represented by a high-low transition, a logic 0 is represented by a low-high transition. 11b = Output bitstream Manchester encoded. Input bitstream Manchester decoded with oversampling of the input signal. A logic 1 is represented by a low-high transition, a logic 0 is represented by a high-low transition.
12	SD24DI	RW	0h	Digital bitstream input 0b = Bitstream from modulator fed into digital filter 1b = External bitstream fed into digital filter. Modulator is off.
11-10	SD24DFSx	RW	0h	Digital filter select 00b = SINC3 filter 01b = Reserved (defaults to 00, SINC) 10b = Reserved (defaults to 00, SINC) 11b = Reserved (defaults to 00, SINC)
9	SD24CAL	RW	0h	Calibration 0b = Calibration disabled. 1b = Calibration enabled. With a single conversion the offset of the modulator and PGA can be measured.
8	SD24SNGL	RW	0h	Single conversion mode select 0b = Continuous conversion mode 1b = Single conversion mode
7	Reserved	R	0h	Reserved. Always reads as 0.
6	SD24ALGN	RW	0h	Data alignment 0b = Right-aligned. LSB of filter output is bit 0. 1b = Left-aligned. MSB of filter output (depending on OSR) is bit 31.
5-4	SD24DFx	RW	0h	Data format 00b = Offset binary 01b = Twos complement 10b = Reserved (defaults to 00, offset binary) 11b = Reserved (defaults to 01, twos complement)

Table 1-12. SD24BCCTLx Register Description (continued)

Bit	Field	Type	Reset	Description
3-1	SD24SCSx	RW	0h	Start of conversion select 000b = SD24SC bit 001b = External trigger 1. See the device-specific data sheet. 010b = External trigger 2. See the device-specific data sheet. 011b = External trigger 3. See the device-specific data sheet. 100b = Group 0 - Start of conversion defined by SD24GRP0SC bits in register SD24BCTL1. 101b = Group 1 - Start of conversion defined by SD24GRP1SC bits in register SD24BCTL1. 110b = Group 2 - Start of conversion defined by SD24GRP2SC bits in register SD24BCT1L. 111b = Group 3 - Start of conversion defined by SD24GRP3SC bits in register SD24BCTL1.
0	SD24SC	RW	0h	Start of conversion. Software controlled start of conversion if SD24SCS = 00b. Manual stop of conversion (independent of SD24SCS setting). If a conversion is ongoing (triggered by any source selected through SD24SCS) this is indicated by SD24SC = 1. When starting the conversion (also by setting SD24SC) this bit will only read 1 when the start of conversion was synchronization to the modulator clock and the actual conversion started. 0b = No conversion start (that is, conversion stopped) 1b = Conversion ongoing

1.3.8 SD24BINCTLx Register

SD24_B Converter x Input Control Register

Figure 1-23. SD24BINCTLx Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
SD24INTDLYx		SD24GAINx			Reserved		
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-13. SD24BINCTLx Register Description

Bit	Field	Type	Reset	Description
15-8	Reserved	R	0h	Reserved. Always reads as 0.
7-6	SD24INTDLYx	RW	0h	Interrupt delay generation after conversion start. These bits select the delay for the first interrupt after conversion start. 00b = Fourth sample causes interrupt 01b = Third sample causes interrupt 10b = Second sample causes interrupt 11b = First sample causes interrupt
5-3	SD24GAINx	RW	0h	Gain 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
2-0	Reserved	RW	0h	Reserved

1.3.9 SD24BOSRx Register

SD24_B Converter x Oscillator Control Register

Figure 1-24. SD24BOSRx Register

15	14	13	12	11	10	9	8
Reserved						SD24OSRx	
r0	r0	r0	r0	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24OSRx							
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

Table 1-14. SD24BOSRx Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0h	Reserved. Always reads as 0.
9-0	SD24OSRx	RW	0h	Oversampling rate. The oversampling rate is defined as OSRx + 1. Valid oversampling rates are 1 to 1024. Default is 256.

1.3.10 SD24BTRGOSR Register

SD24_B Trigger Oversampling Control Register
Note: Only the MSP430F674xx(1)(A), MSP430F676xx(1)(A), and MSP430F677x(1)(A) devices support the trigger generator.

Figure 1-25. SD24BTRGOSR Register

15	14	13	12	11	10	9	8
Reserved						SD24OSRx	
r0	r0	r0	r0	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24OSRx							
rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1	rw-1

Table 1-15. SD24BTRGOSR Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0h	Reserved. Always reads as 0.
9-0	SD24OSRx	RW	0h	Oversampling rate. The oversampling rate is defined as OSRx + 1. Valid oversampling rates are 1 to 1024. Default is 256.

1.3.11 SD24BPREx Register

SD24_B Converter x Preload Register

Figure 1-26. SD24BPREx Register

15	14	13	12	11	10	9	8
Reserved						SD24PREx	
r0	r0	r0	r0	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24PREx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-16. SD24BPREx Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0h	Reserved. Always reads as 0.
9-0	SD24BPREx	RW	0h	Digital filter preload value

1.3.12 SD24BTRGPRE Register

SD24_B Trigger Preload Register
Note: Only the MSP430F674xx(1)(A), MSP430F676xx(1)(A), and MSP430F677x(1)(A) devices support the trigger generator.

Figure 1-27. SD24BTRGPRE Register

15	14	13	12	11	10	9	8
Reserved						SD24PREx	
r0	r0	r0	r0	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
SD24PREx							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-17. SD24BTRGPRE Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0h	Reserved. Always reads as 0.
9-0	SD24BPREx	RW	0h	Digital filter preload value

1.3.13 SD24BMEMLx Register

SD24_B Converter x Conversion Memory Low Word Register

Figure 1-28. SD24BMEMLx Register

15	14	13	12	11	10	9	8
Conversion Results - Low Word							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Conversion Results - Low Word							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

Table 1-18. SD24BMEMLx Register Description

Bit	Field	Type	Reset	Description
15-0	Conversion Results - Low Word	R	0h	Conversion results. Actual format depends on selected data format, and oversampling rate.

1.3.14 SD24BMEMHx Register

SD24_B Converter x Conversion Memory High Word Register

Figure 1-29. SD24BMEMHx Register

15	14	13	12	11	10	9	8
Conversion Results - High Word							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Conversion Results - High Word							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

Table 1-19. SD24BMEMHx Register Description

Bit	Field	Type	Reset	Description
15-0	Conversion Results - High Word	R	0h	Conversion results. Actual format depends on selected data format, and oversampling rate.

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