CSD85301Q2 20V Dual N-Channel NexFET™ Power MOSFETs

1 Features

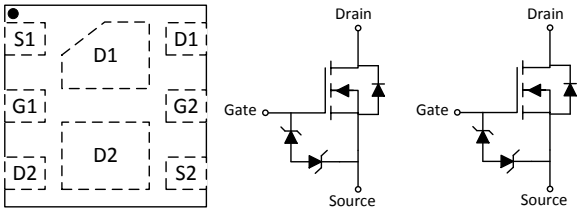
- Low on-resistance
- Dual independent MOSFETs
- Space saving SON 2mm × 2mm plastic package
- Optimized for 5V gate driver
- Avalanche rated
- Pb and halogen free
- RoHS compliant

2 Applications

- Point-of-load synchronous buck converter for applications in networking, telecom, and computing systems
- Adaptor or USB input protection for notebook PCs and tablets
- Battery protection

3 Description

The CSD85301Q2 is a 20V, 23mΩ N-Channel device with dual independent MOSFETs in a SON 2mm x 2mm plastic package. The two FETs were designed to be used in a half bridge configuration for synchronous buck and other power supply applications. Additionally, this part can be used for adaptor, USB input protection and battery charging applications. The dual FETs feature low drain to source on-resistance that minimizes losses and offers low component count for space constrained applications.



Top View and Circuit Image

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	20		V
Q_g	Gate Charge Total (4.5V)	4.2		nC
Q_{gd}	Gate Charge Gate to Drain	1.0		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 1.8V	65	mΩ
		V_{GS} = 2.5V	33	mΩ
		V_{GS} = 3.8V	25	mΩ
		V_{GS} = 4.5V	23	mΩ
$V_{GS(th)}$	Threshold Voltage	0.9		V

Ordering Information

Device(1)	Media	Qty	Package	Ship
CSD85301Q2	7-Inch Reel	3000	SON 2mm x 2mm Plastic Package	Tape and Reel
CSD85301Q2T	7-Inch Reel	250		

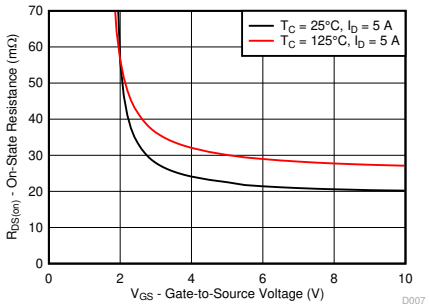
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

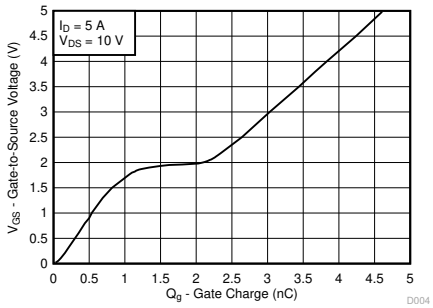
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current (Package limited)	5.0	A
I_{DM}	Pulsed Drain Current(1)	26	A
P_D	Power Dissipation(2)	2.3	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 8.7A, L = 0.1mH, R_G = 25Ω	3.8	mJ

(1) Max $R_{\theta JA}$ = 185 °C/W, pulse duration ≤100µs, duty cycle ≤1%.

(2) Typical $R_{\theta JA}$ = 55 °C/W on a 1 inch², 2oz. Cu pad on a 0.06 inch thick FR4 PCB.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

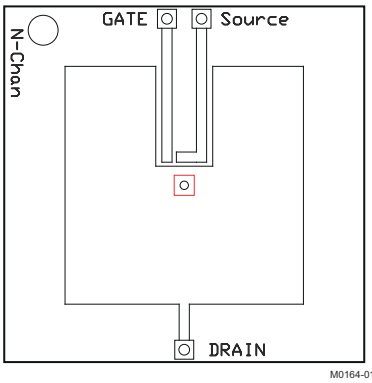
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0V, I_D = 250µA	20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0V, V_{DS} = 16V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0V, V_{GS} = 10V			10	µA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6	0.9	1.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 1.8V, I_D = 0.5A		65	99	mΩ
		V_{GS} = 2.5V, I_D = 5A		33	39	mΩ
		V_{GS} = 3.8V, I_D = 5A		25	29	mΩ
		V_{GS} = 4.5V, I_D = 5A		23	27	mΩ
g_{fs}	Transconductance	V_{DS} = 2V, I_D = 5A		20		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		361	469	pF
C_{oss}	Output Capacitance			68	89	pF
C_{rss}	Reverse Transfer Capacitance			48	62	pF
R_G	Series Gate Resistance			7.3		Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 10V, I_D = 5A		4.2	5.4	nC
Q_{gd}	Gate Charge Gate-to-Drain			1.0		nC
Q_{gs}	Gate Charge Gate-to-Source			1.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.5		nC
Q_{oss}	Output Charge	V_{DS} = 10V, V_{GS} = 0V		1.3		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 10V, V_{GS} = 5V, I_{DS} = 5A, R_G = 0Ω		6		ns
t_r	Rise Time			26		ns
$t_{d(off)}$	Turn Off Delay Time			14		ns
t_f	Fall Time			15		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 5A, V_{GS} = 0V		0.8	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 10V, I_F = 5A, di/dt = 300A/µs		7.2		nC
t_{rr}	Reverse Recovery Time			14		ns

4.2 Thermal Information

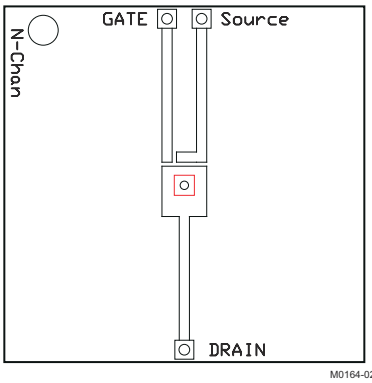
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)			70	°C/W
	Junction-to-Ambient Thermal Resistance(2)			185	

(1) Device mounted on FR4 material with 1 $inch^2$ (6.45cm^2), 2oz. (0.071mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.



Max $R_{\theta JA}$ = 70 when mounted on 1 inch^2 (6.45cm^2) of 2oz. (0.071mm thick) Cu.



Max $R_{\theta JA}$ = 185 when mounted on minimum pad area of 2oz. (0.071mm thick) Cu.

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

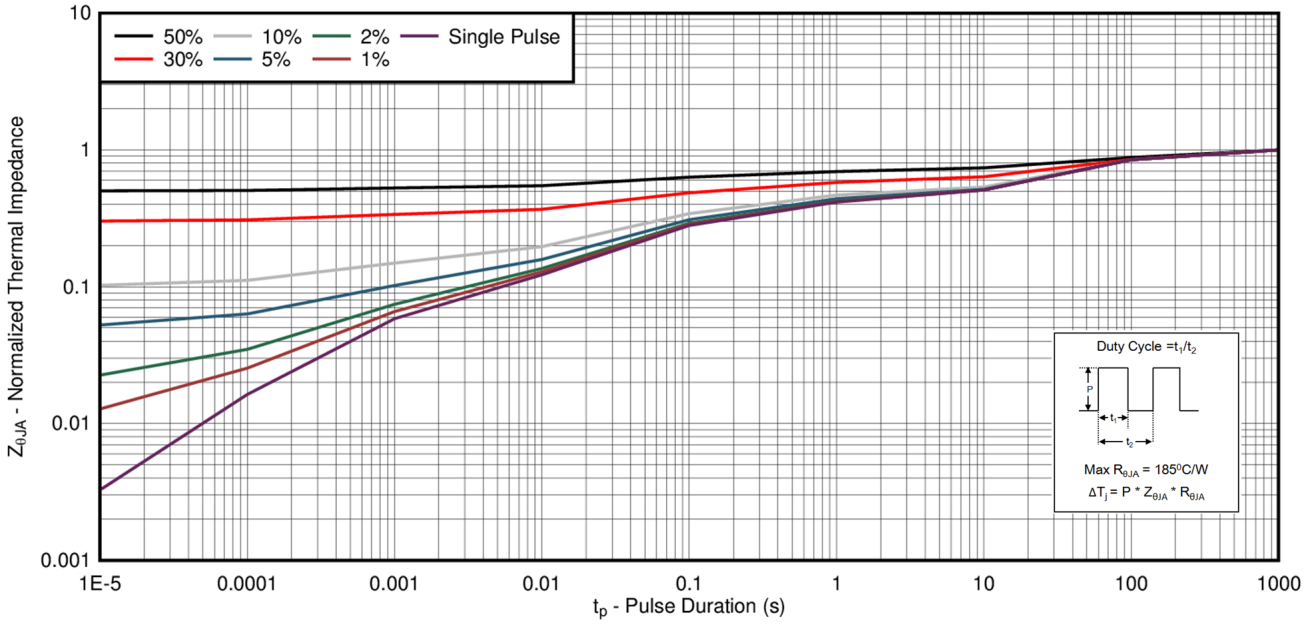


Figure 4-1. Transient Thermal Impedance

4.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

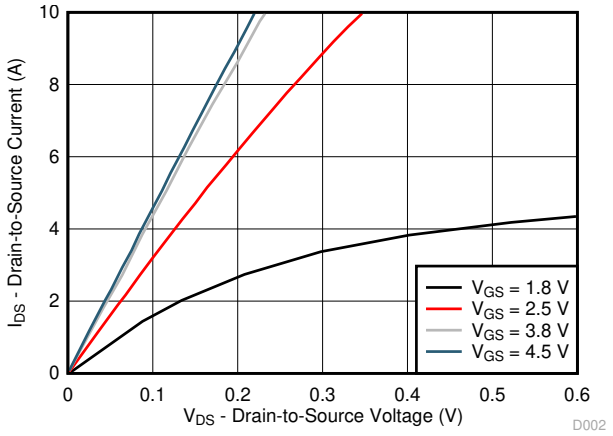
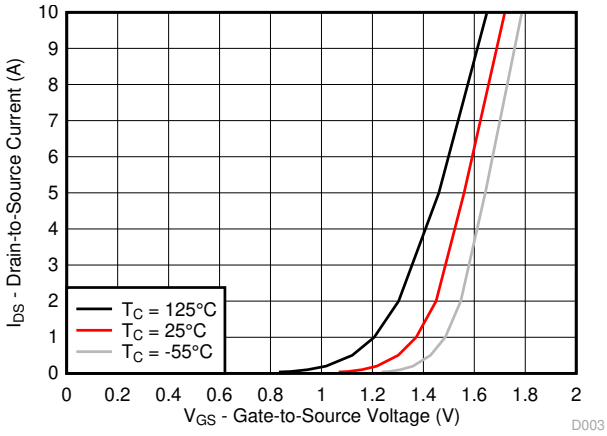
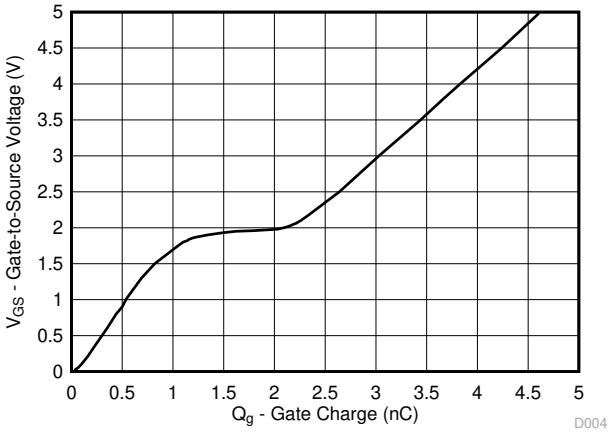


Figure 4-2. Saturation Characteristics



V_{DS} = 5V

Figure 4-3. Transfer Characteristics



I_D = 5A V_{DS} = 10V

Figure 4-4. Gate Charge

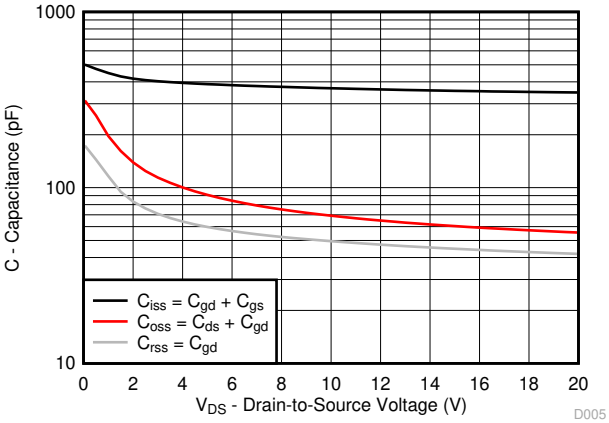
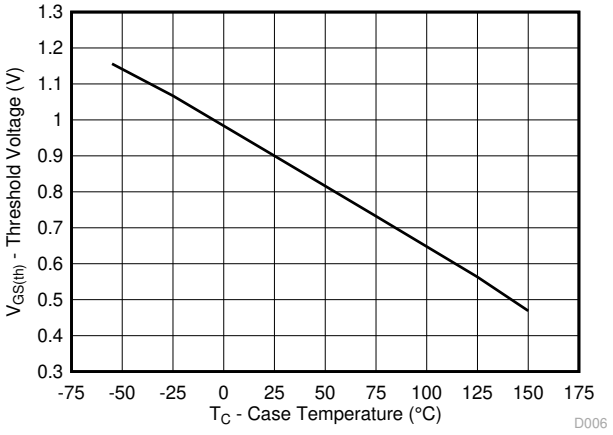


Figure 4-5. Capacitance



I_D = 5A

Figure 4-6. Threshold Voltage vs Temperature

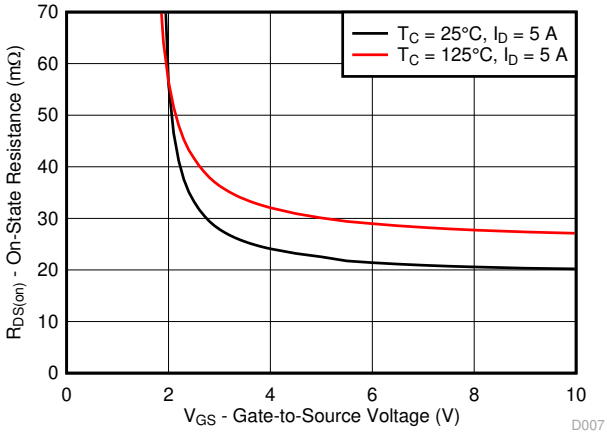
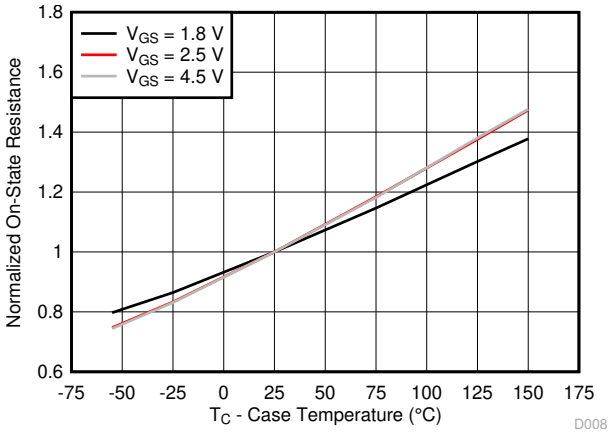


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

4.3 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)



I_D = 5A

Figure 4-8. Normalized On-State Resistance vs Temperature

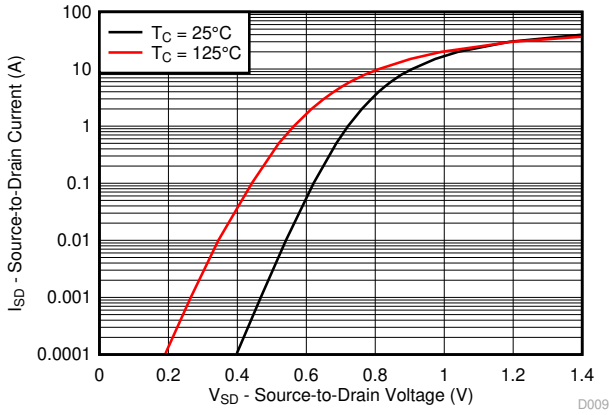
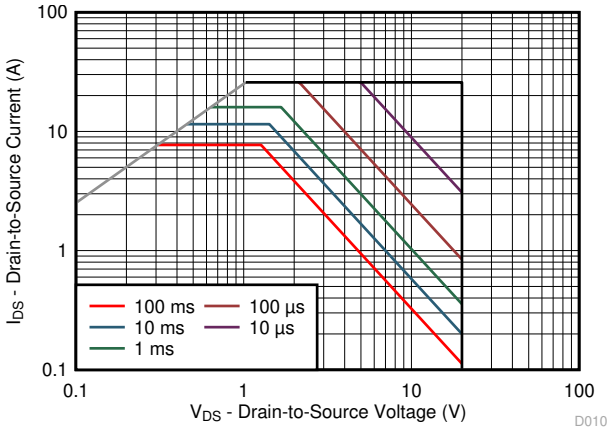


Figure 4-9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JA}$ = 185°C/W

Figure 4-10. Maximum Safe Operating Area

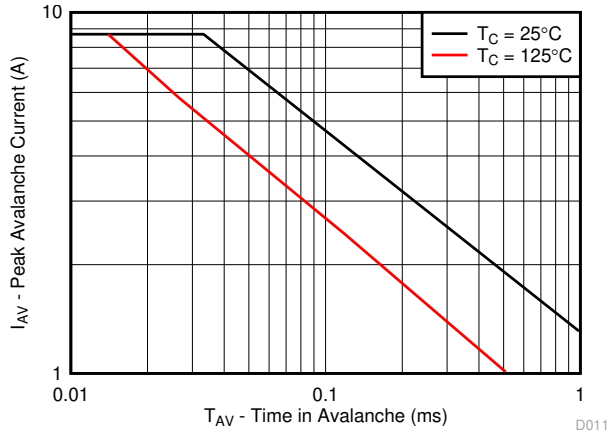


Figure 4-11. Single Pulse Unclamped Inductive Switching

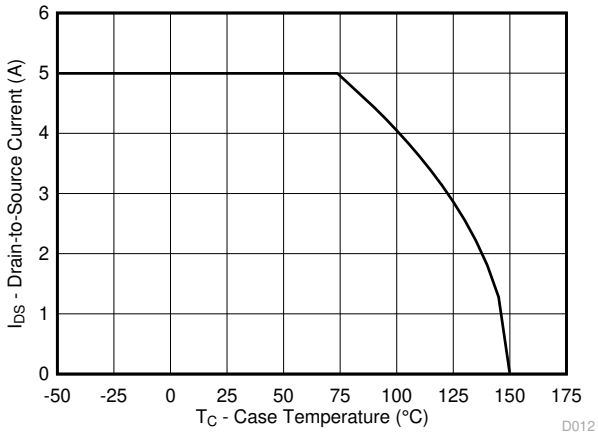


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.3 Trademarks

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

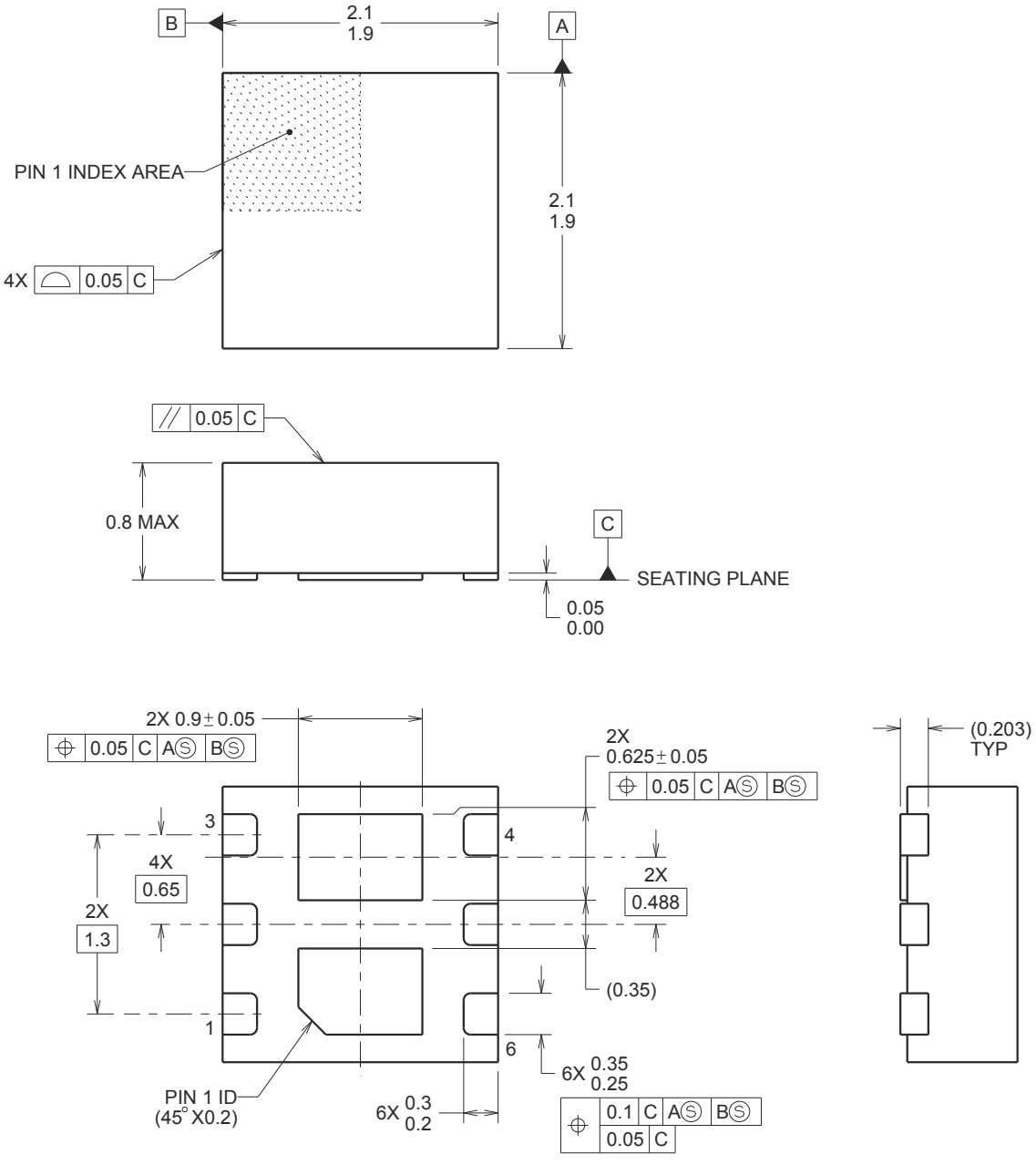
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2014) to Revision A (May 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

7 Mechanical, Packaging, and Orderable Information

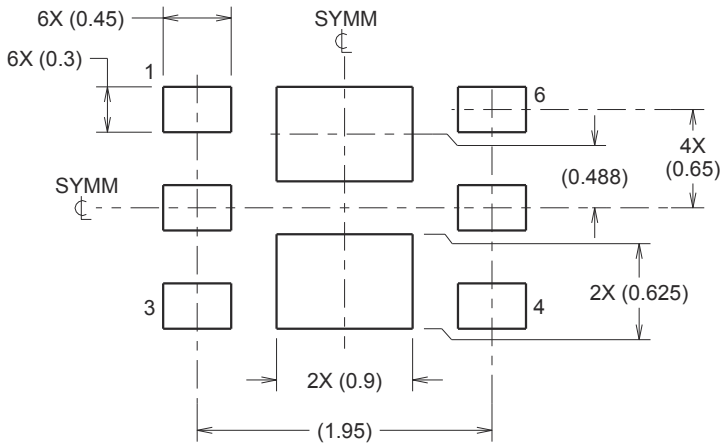
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions



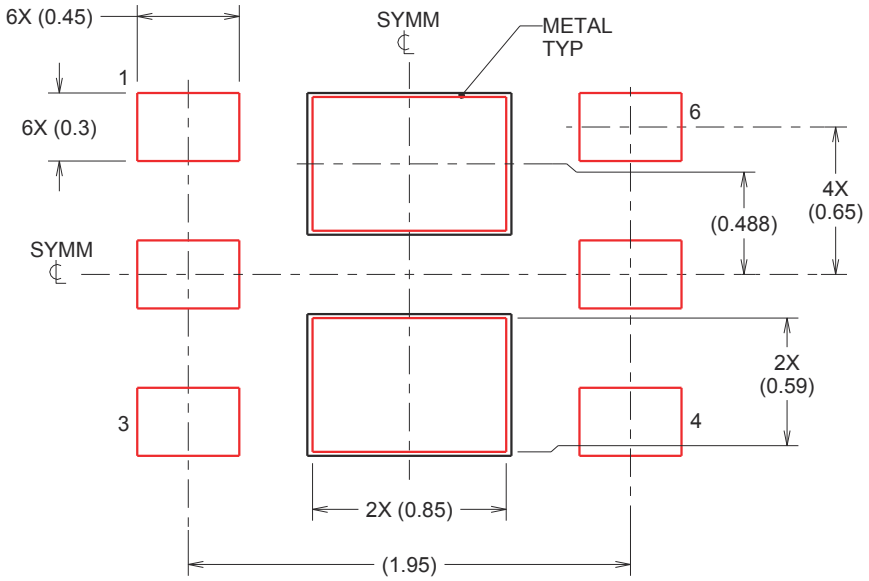
All dimensions are in mm, unless otherwise stated.

7.2 PCB Land Pattern



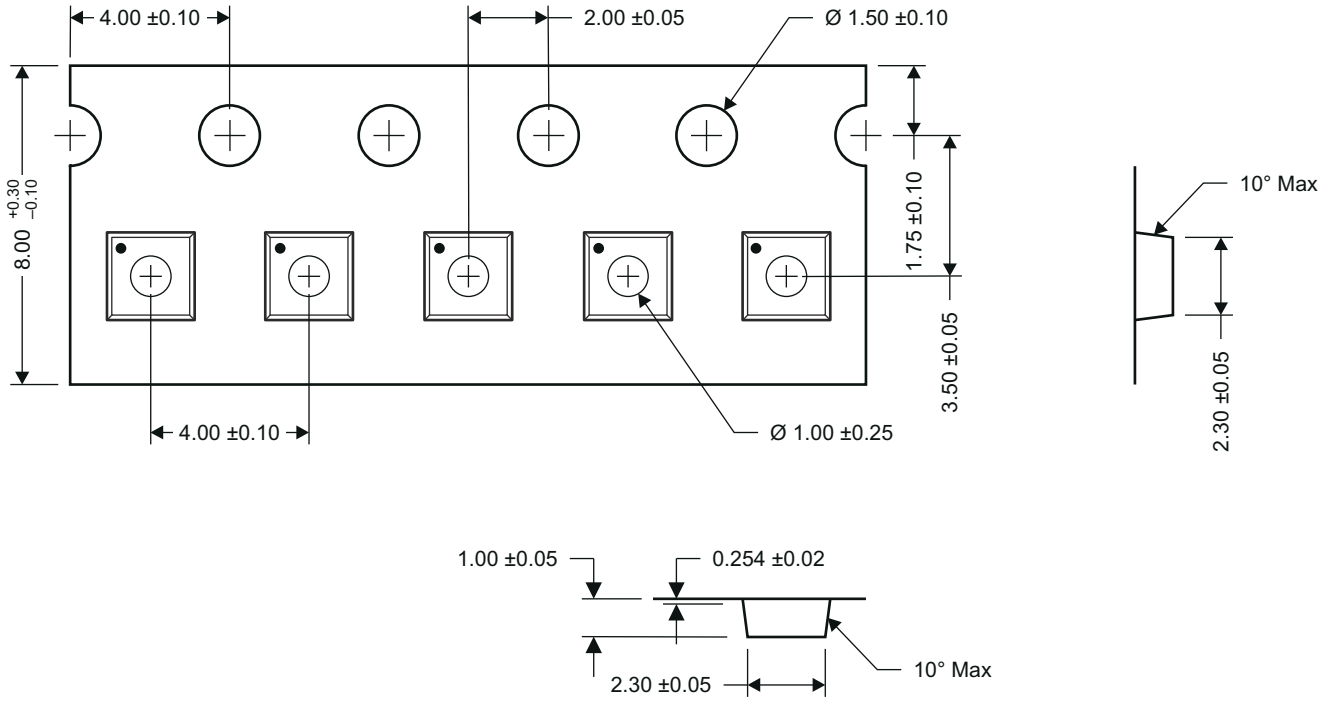
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise stated.

7.4 Q2 Tape and Reel Information



1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^9 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD85301Q2	ACTIVE	WSON	DLV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531	Samples
CSD85301Q2T	ACTIVE	WSON	DLV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	8531	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

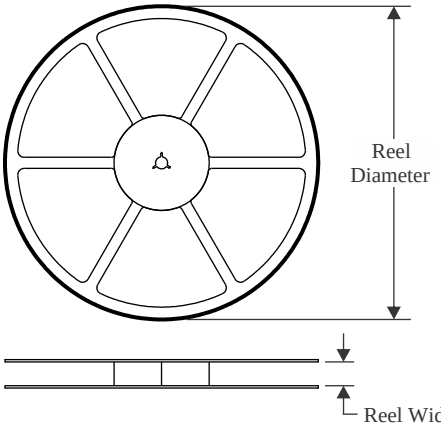
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

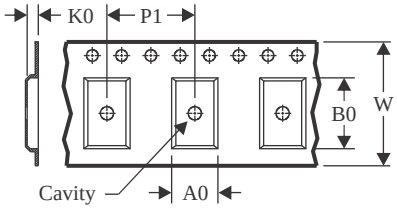
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

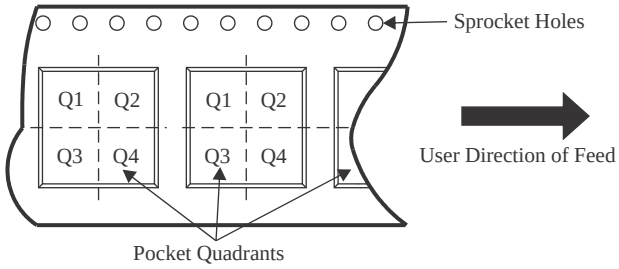


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

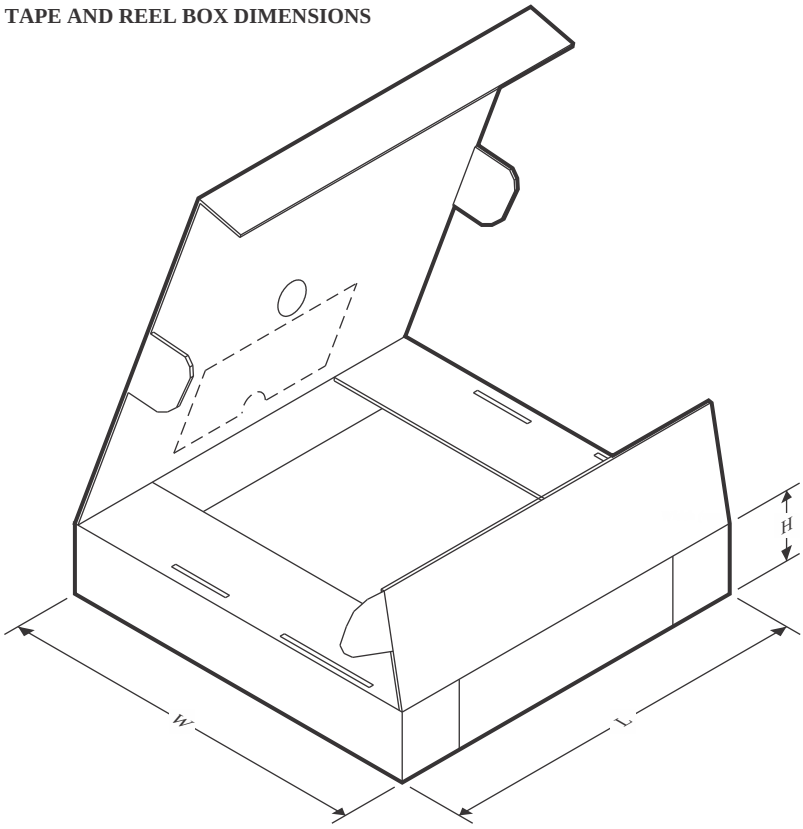
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD85301Q2	WSON	DLV	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD85301Q2T	WSON	DLV	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD85301Q2	WSON	DLV	6	3000	189.0	185.0	36.0
CSD85301Q2T	WSON	DLV	6	250	189.0	185.0	36.0

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