Power Supply Design Seminar

Tips, tricks and advanced applications of linear regulators

Author

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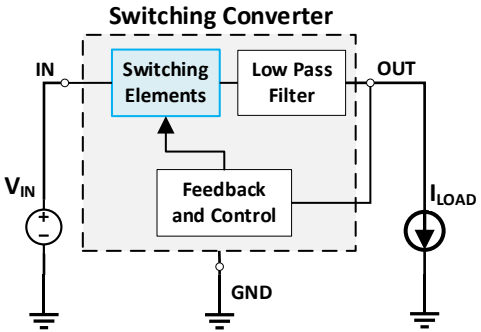
Agenda

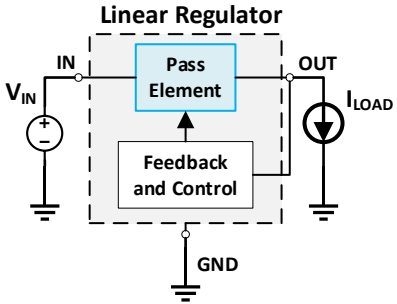
- Linear regulator (LDO) overview
- LDO tips and tricks:
  - Noise
  - Power-supply rejection ratio (PSRR)
  - Thermal performance
  - Transient performance near dropout
- Advanced LDO applications:
  - Parallel LDOs using ballast resistors
  - Constant current regulation
  - Multiple-input single-output (MISO) LDOs

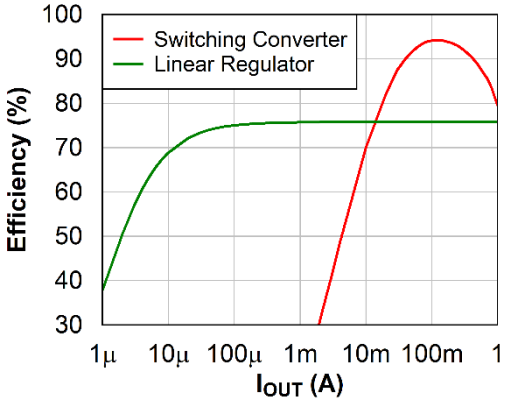
LDOs vs. switching converters

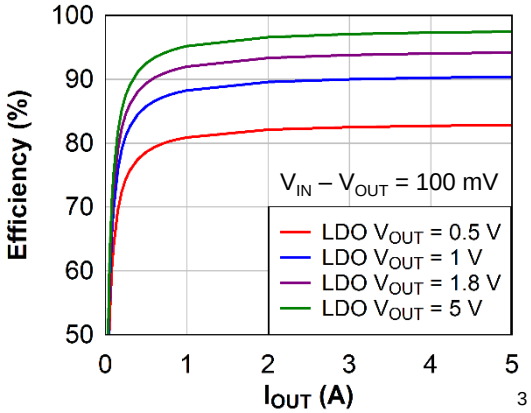
- Power converter types:
  - Switching converters: switches are either on or turned off
  - LDO: pass element is always on
- LDO
  - Pros: cheap, simple, quiet
  - Cons: efficiency, temperature

$$\text{Efficiency } (\eta) = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (I_{OUT} + I_Q)}$$

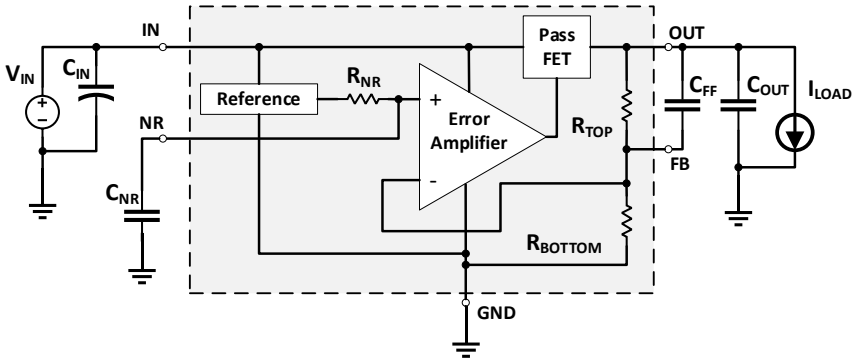








What is the structure of an LDO?

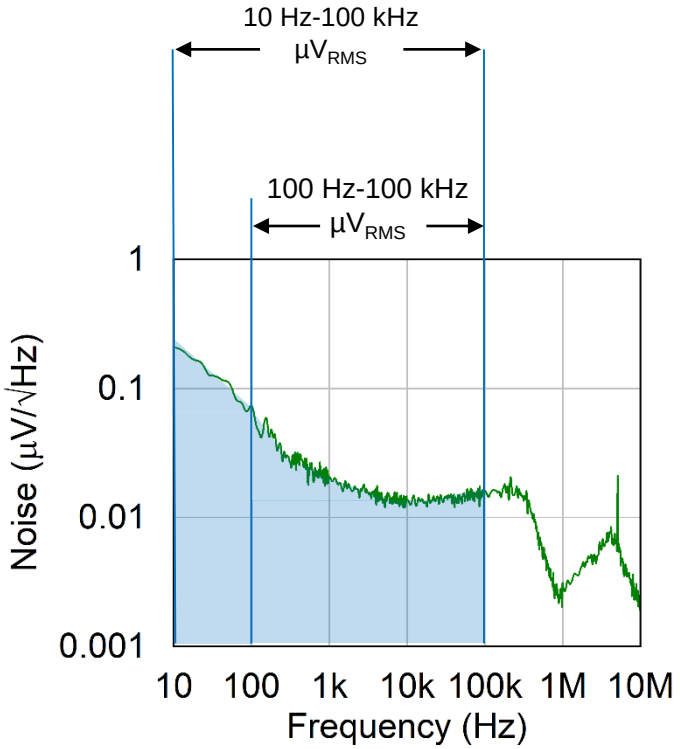


Key LDO characteristics:

- Dropout voltage (V_{DO})
- Power dissipation (P_D) and relationship to temperature rise of the LDO
- Noise
  - **Intrinsic noise** (e_n) is dominated by the noise of the internal reference and error amplifier
  - **PSRR** measures how much noise from the input couples into the output through the LDO
- Quiescent current (I_Q)
- Stability
- Turnon time

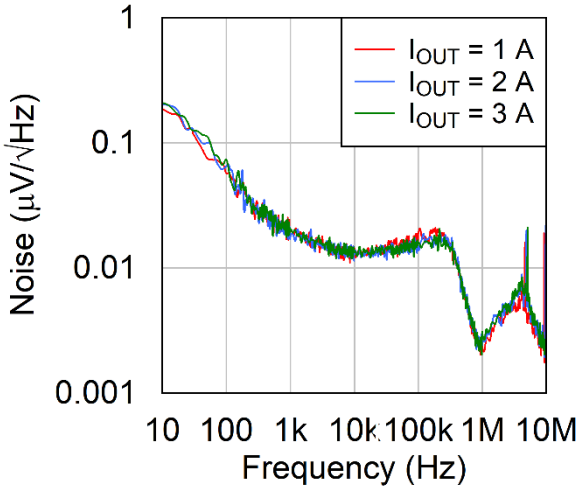
Noise fundamentals

- LDO noise measurements:
  - Noise spectral density (μV/√Hz)
  - Total (integrated) output noise (μV_{RMS})
    - An industry standard to compare different LDOs against one another
- Integrated output noise is typically measured from 10 Hz to 100 kHz
  - 100 Hz to 100 kHz was also sometimes used in the past
  - For accurate noise comparison, be sure the measurements are using the same frequency range

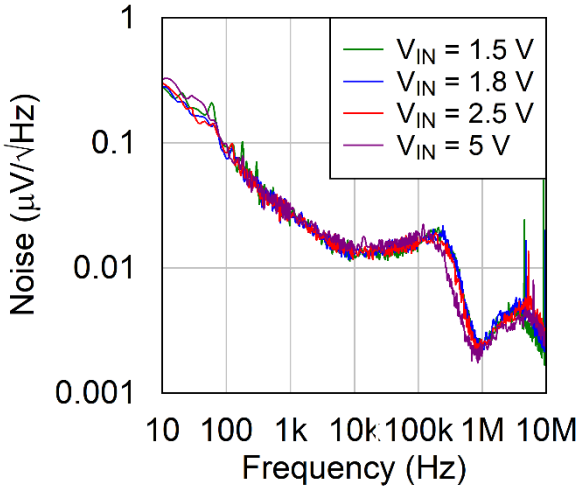


What conditions do not affect intrinsic noise

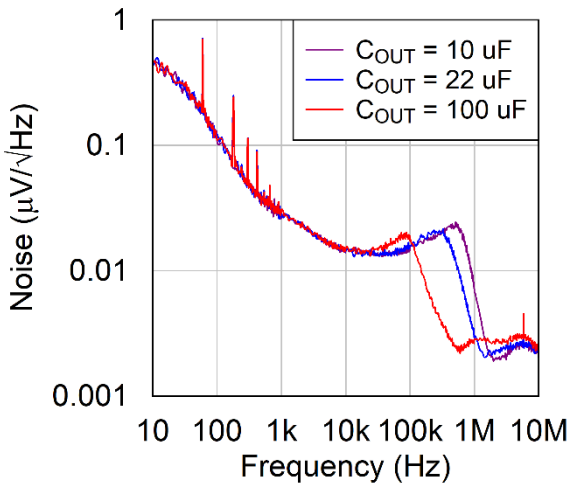
Output current (ΔI_{OUT})*



Input voltage (ΔV_{IN})



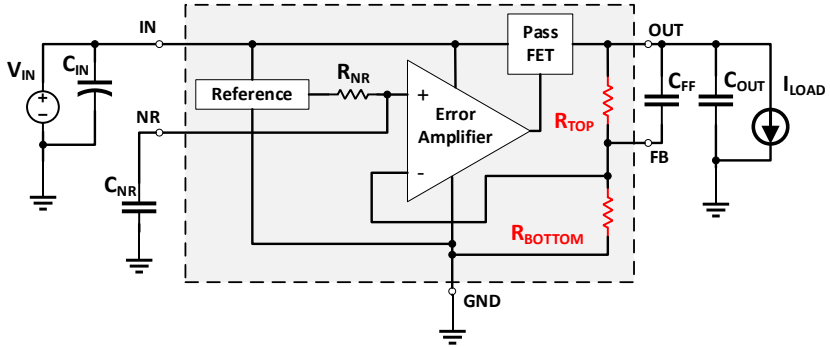
Output capacitance** (ΔC_{OUT})

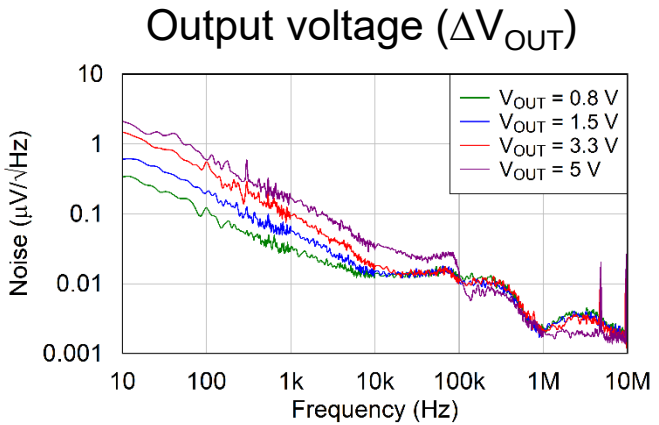


*For ultra-low-I_Q devices, I_{LOAD} may affect noise

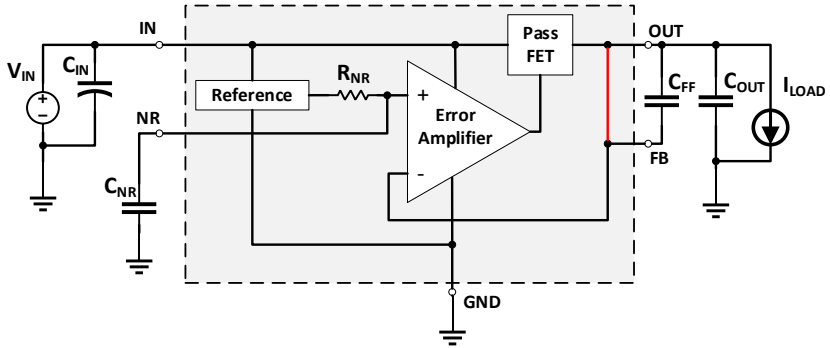
**Very high values of C_{OUT} may affect noise

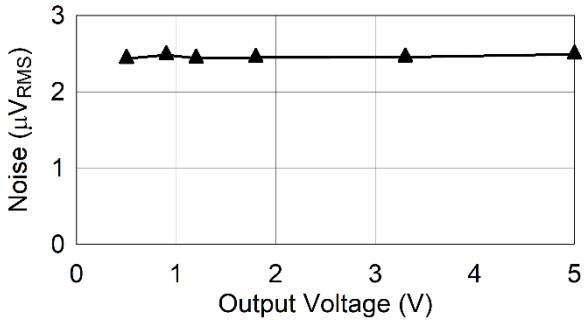
What conditions affect intrinsic noise



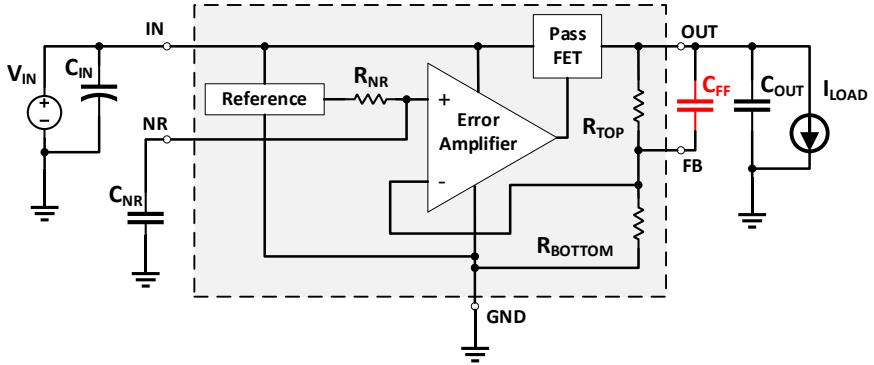


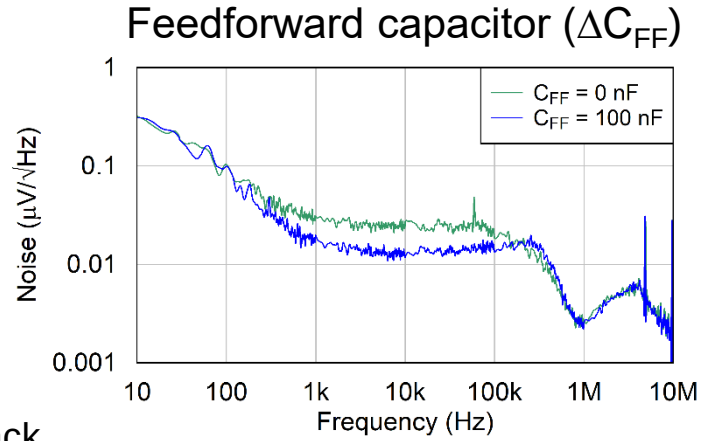
V_{OUT} has no effect when placing an LDO in unity gain feedback



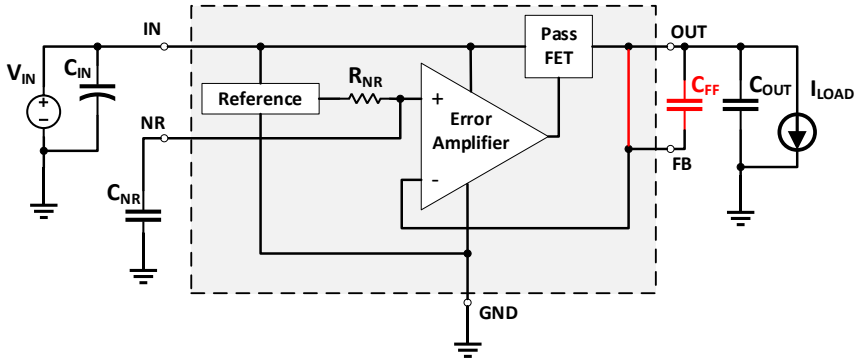


What conditions affect intrinsic noise



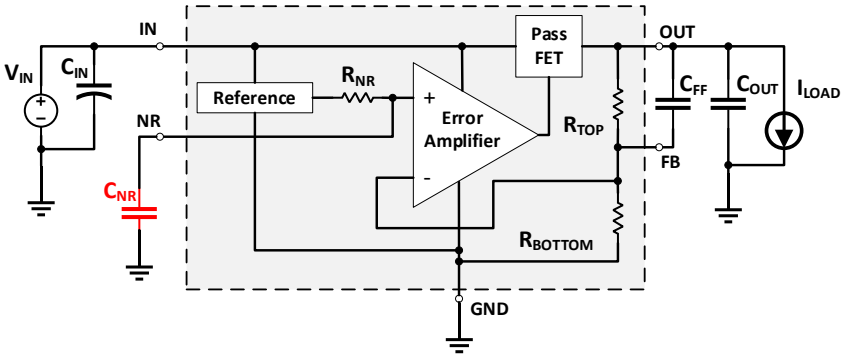


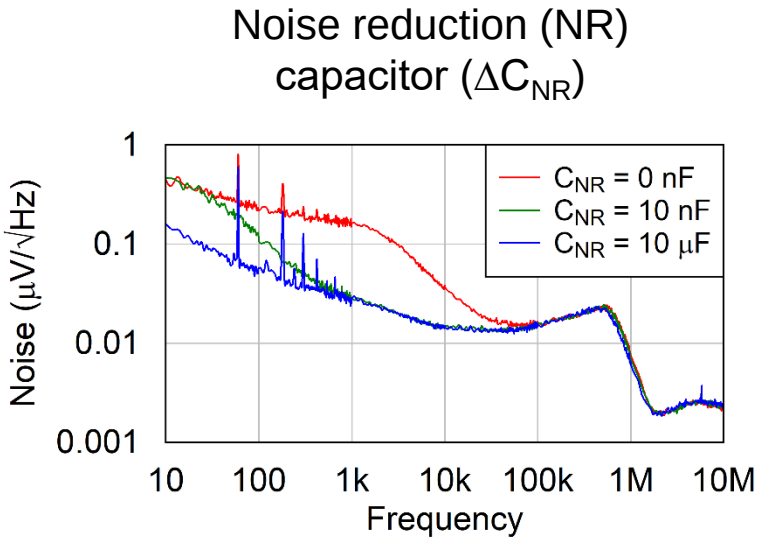
C_{FF} has no effect when placing an LDO in unity gain feedback



- C_{FF} creates a short across R_{TOP} in the mid-band frequency
- The error amplifier operates closer to unity gain feedback within the mid-band frequency range

What conditions affect intrinsic noise





- The NR capacitor and internal NR resistor form a low-pass filter
- This low-pass filter removes noise from the reference voltage before the error amplifier

PSRR

PSRR represents the ability of the LDO to filter input-voltage changes

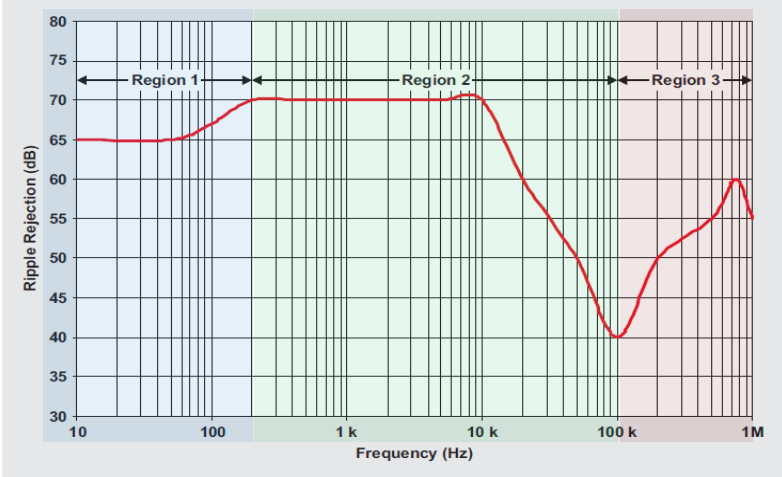
$$\text{PSRR} = 20 \times \log\left(\frac{V_{IN(AC)}}{V_{OUT(AC)}}\right)$$

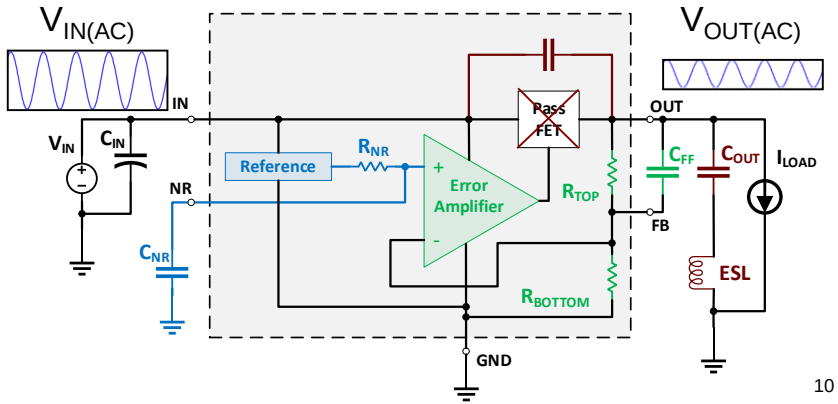
Region 1: PSRR of the reference and the resistor-capacitor filter

Region 2: Open-loop gain of the error amplifier

Region 3: Parasitic capacitance of the field-effect transistor and the output capacitor and associated parasitic (capacitive divider)

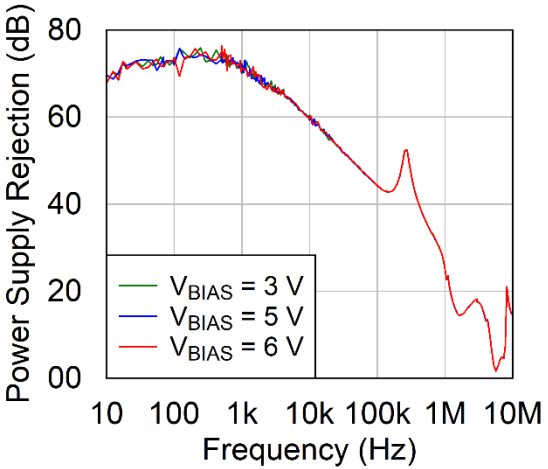
- The smaller the parasitic capacitor, the less the V_{IN} AC-couples to V_{OUT}
- The larger the C_{OUT}, the more noise shunted to GND
- Associated equivalent series inductance (ESL) can also impact PSRR performance





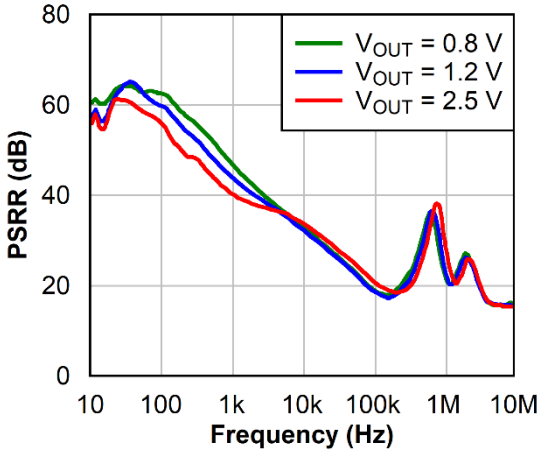
What conditions do not affect PSRR

Bias voltage (V_{BIAS})



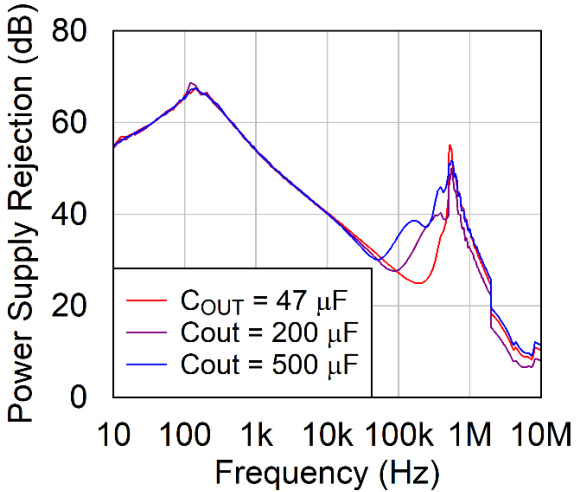
No impact if V_{BIAS} is above the minimum value

Output voltage (V_{OUT})



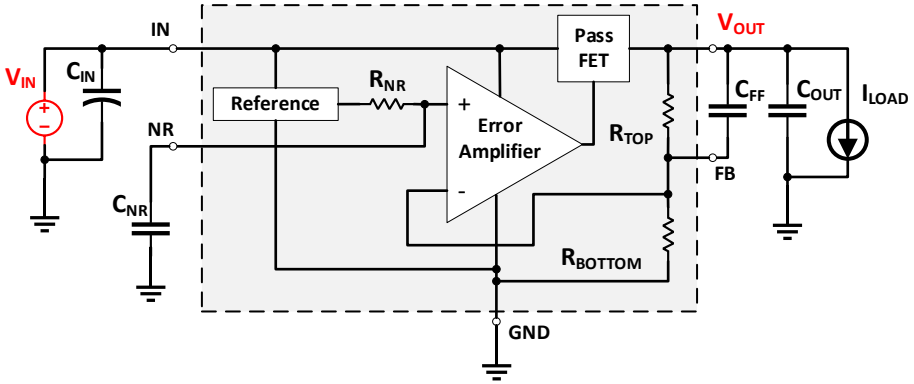
Small impact at low frequency

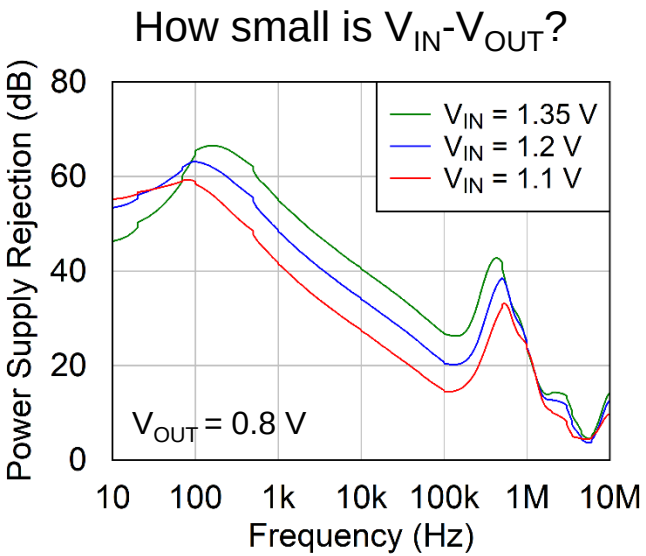
Output capacitance (ΔC_{OUT})



Small impact at high frequency

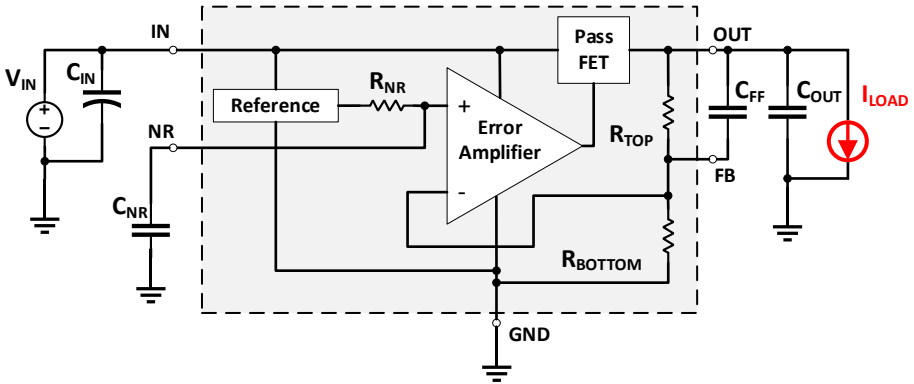
What conditions affect PSRR

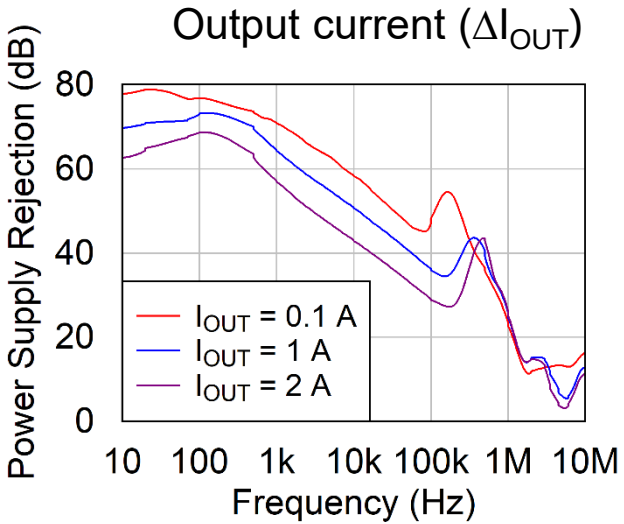




- When the pass field-effect transistor (FET) is in the saturation region, you can maintain the necessary gain (large V_{DS})
- When the pass FET enters the linear region, you cannot maintain the necessary gain (small V_{DS})

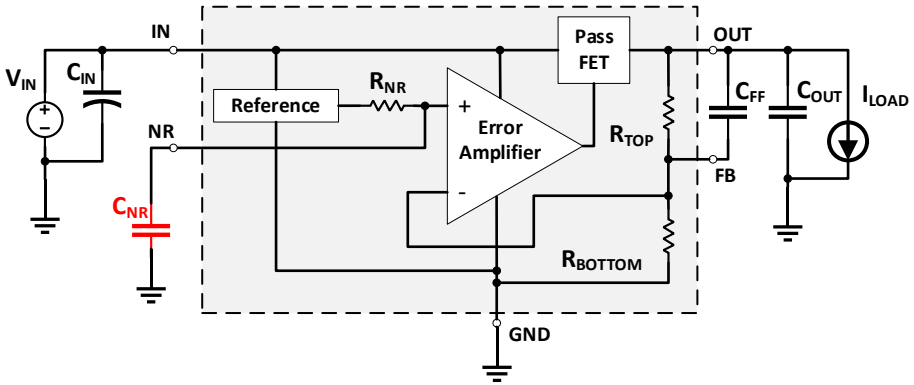
What conditions affect PSRR



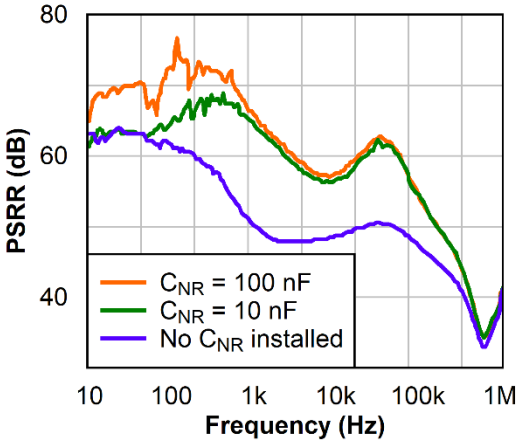


- As the load increases, at some point the pass FET will enter the metal-oxide semiconductor triode region and the gain of the pass FET will be degraded for the same V_{DS}

What conditions affect PSRR

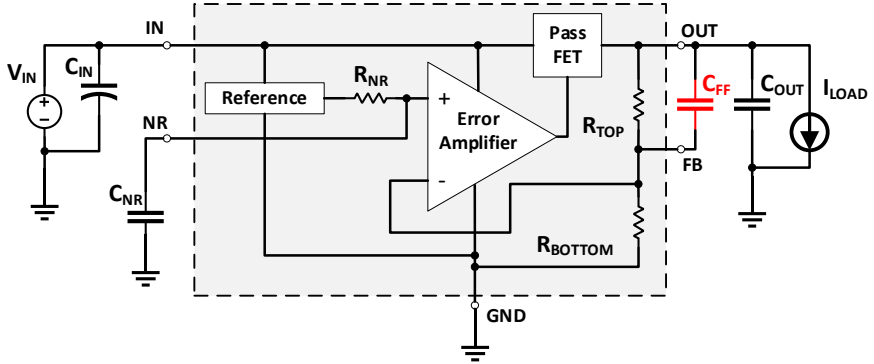


NR capacitor (ΔC_{NR})

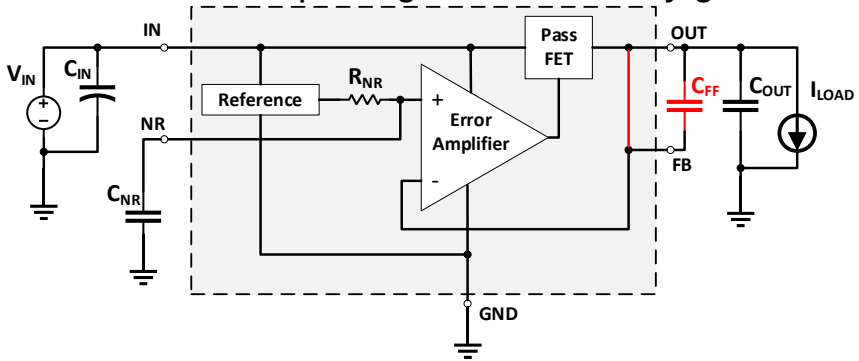


- The PSRR of V_{REF} itself affects the PSRR of the LDO
- Adding a low-pass filter increases the PSRR of V_{REF}

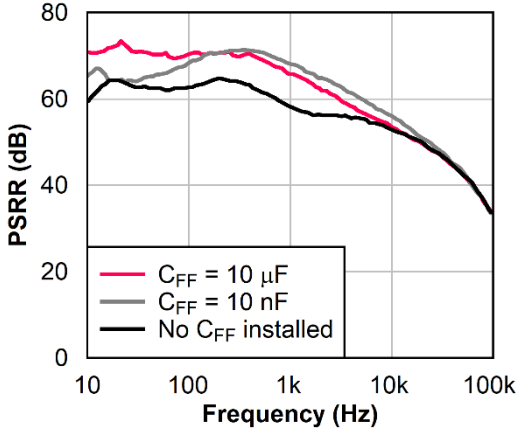
What conditions affect PSRR



C_{FF} has no effect when placing an LDO in unity gain feedback



Feedforward capacitor (ΔC_{FF})



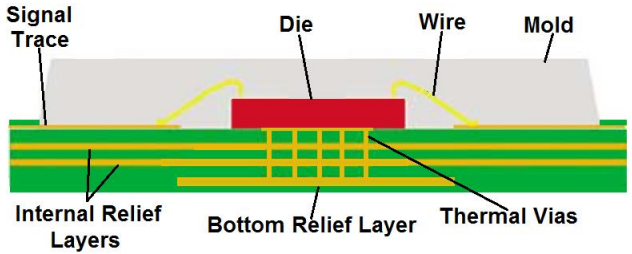
- At higher frequencies, feedback and V_{OUT} are effectively shorted by C_{FF}, which prevents the gain of the error amplifier from increasing the reference noise

JEDEC thermal metrics

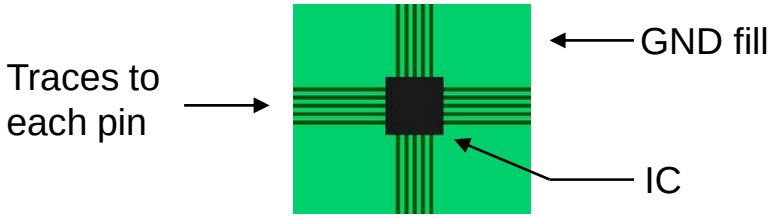
- TI LDO thermal metrics are modeled using the Joint Electron Device Engineering Council (JEDEC) high-K board in order to easily compare devices
- The most common thermal characteristic is the junction-to-ambient (θ_{JA}) thermal resistance
- θ_{JA} is a measure of the thermal performance of an integrated circuit (IC) mounted on a printed circuit board (PCB)

JEDEC high-k board

Side view



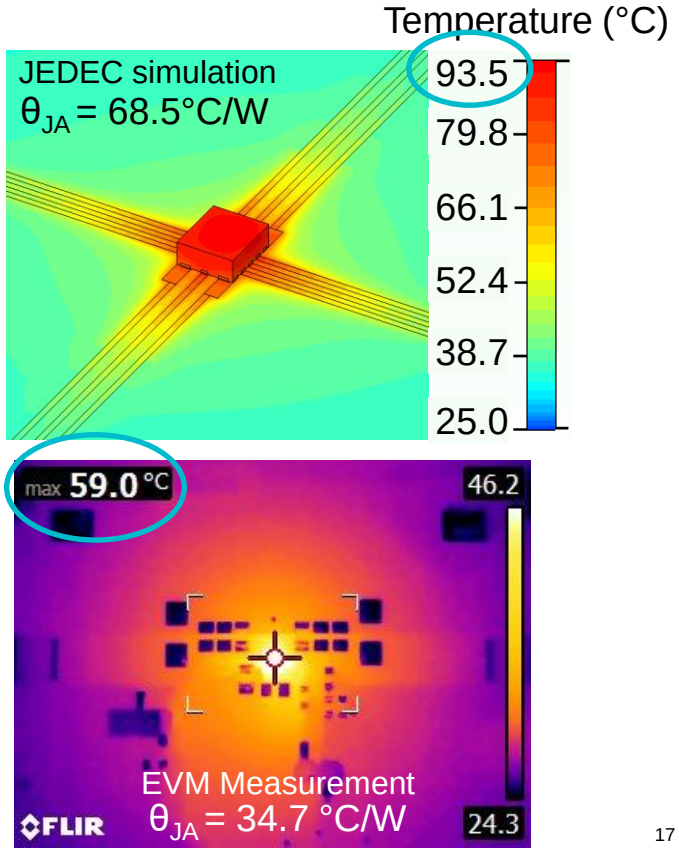
Top view



θ_{JA}: Understanding usage and limitations

- It is possible to reduce the θ_{JA} **25% to 50%** through good layout practices
- Good layout practices:
  - Maximize the number of thermal vias within the thermal pad to transfer heat away from the LDO
  - Maximize the PCB copper around the device

$$P_D = (V_{IN} - V_{OUT}) \times (I_{OUT} + I_Q)$$
$$P_D \cong (V_{IN} - V_{OUT}) \times I_{OUT}$$
$$T_J = T_A + (\theta_{JA} \times P_D)$$

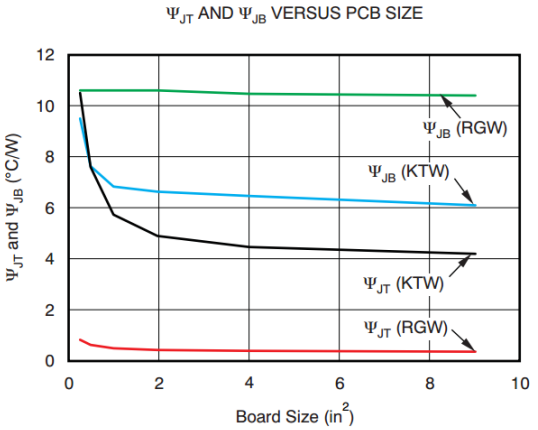


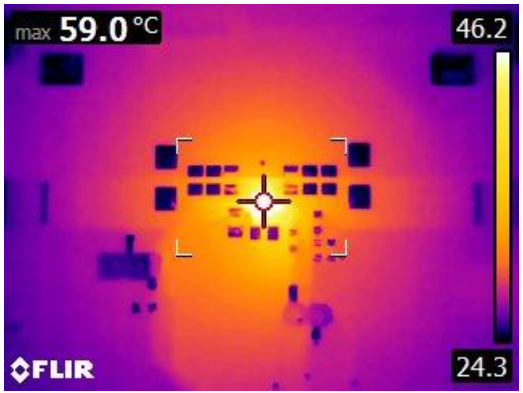
Using Ψ_{JB} and Ψ_{JT} in-application

- JEDEC has defined Ψ_{JB} and Ψ_{JT} thermal metrics to provide a more accurate way to estimate the junction temperature from the **measured case temperature** (T_C) on a PCB

$$T_J = T_C + \Psi_{JT} \times P_D$$

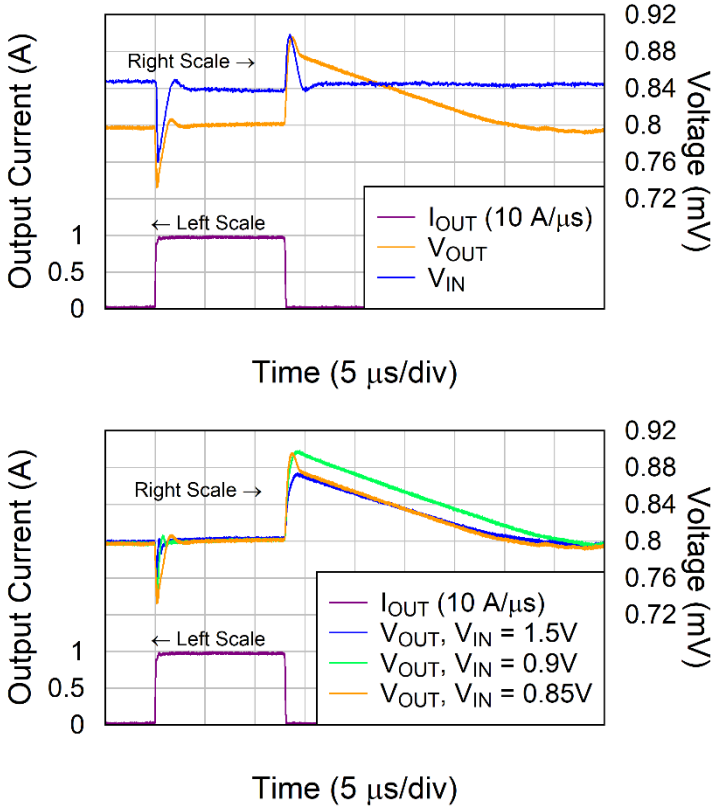
$$T_J = 59°C + 4.5\ {}^{°C}/_{W} \times 1\ W = 63.5°C$$





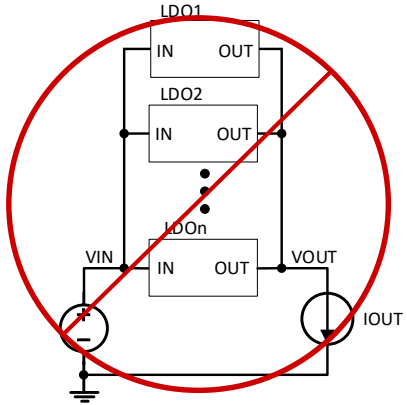
Transient performance near dropout

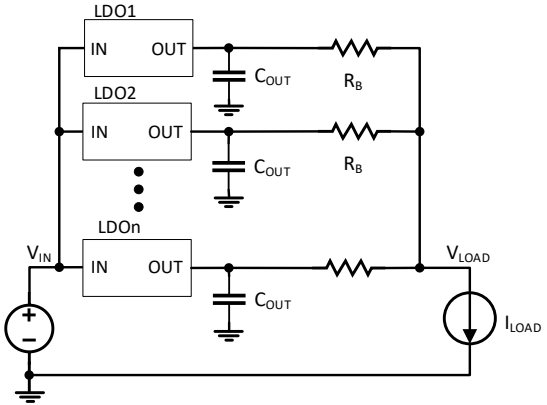
- Transient performance is typically characterized with more headroom voltage than the dropout specification
- An LDO enters dropout when it can no longer regulate the output voltage
  - Dropout is a DC specification
- The dropout of the TPS7A14 is typically 45 mV at 1 A (25°C)



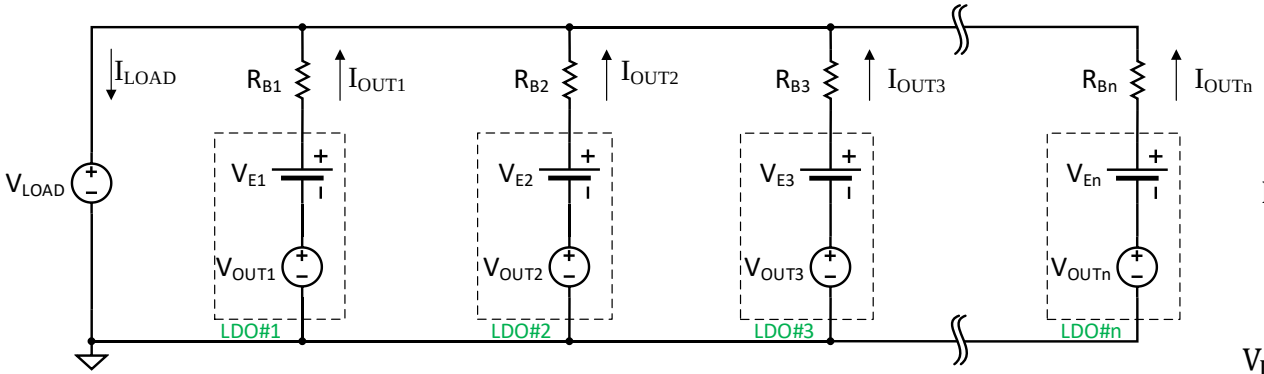
Parallel LDOs

- Benefits:
  - Increased load current
  - Reduced noise (√n)
  - Improved PSRR for a given load current
  - Improved thermal spreading
  - Reduced headroom requirement (dropout)
  - Reduced volume over other converters: C_{OUT} typically drives the maximum system height
- You must use a ballast resistor to connect each LDO's output together
  - Direct V_{OUT} connection: Small differences in V_{OUT} will result in one LDO turning on and trying to carry the load while the rest are turned off





Parallel LDOs: Fundamental equations and analysis



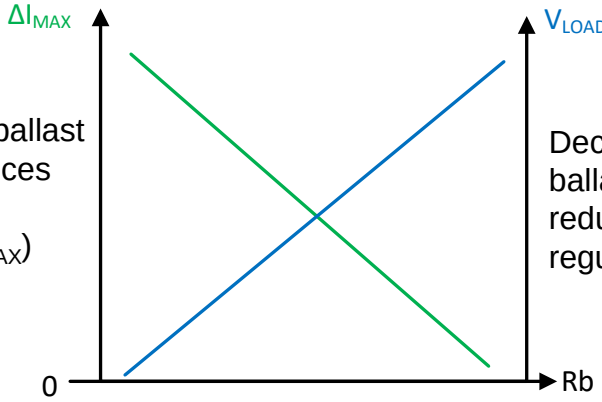
$$R_B = \frac{\max\limits_{1<x<n} V_{En} - \min\limits_{1<x<n} V_{En}}{\Delta I_{MAX}}$$

Maximum current imbalance between LDOs

$$I_{LOAD} = \sum_{n=1}^{n} \frac{V_{OUTn} - V_{LOAD} + V_{En}}{R_{Bn}}$$

$$V_{LOAD} = \frac{\sum_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{Bn}} - I_{LOAD}}{\sum_{n=1}^{n} \frac{1}{R_{Bn}}}$$

$$I_{OUTn} = \frac{V_{OUTn} - V_{LOAD}}{R_{Bn}} + \frac{V_{En}}{R_{Bn}}$$



Increasing the ballast resistance reduces the current imbalance (ΔI_{MAX}) between LDOs

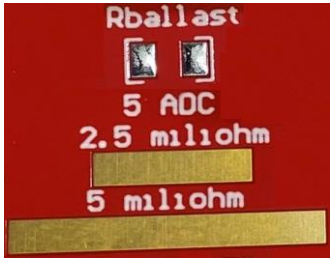
Decreasing the ballast resistance reduces the load regulation V_{LOAD_REG}

If $R_{B1} = \ldots = R_{Bn}$ and $V_{OUT1} = \ldots = V_{OUTn}$:

$$I_{OUTn} = \frac{I_{LOAD} - \left(\sum_{n=1}^{n} \frac{V_{En}}{R_B}\right)}{n} + \frac{V_{En}}{R_B}$$

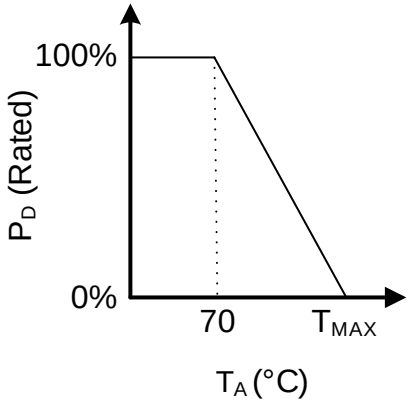
Ballast resistor design

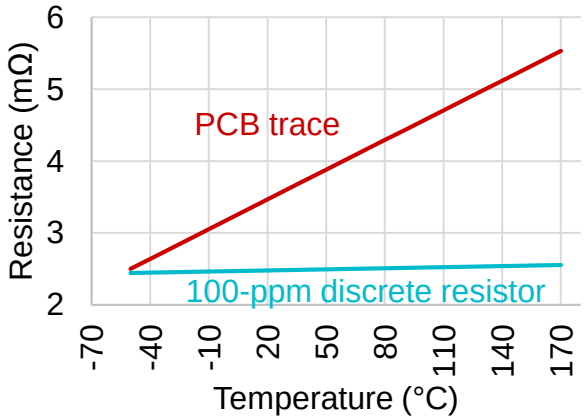
- Option 1: PCB trace
  - Avoid microstrip analysis; use Institute of Printed Circuits (IPC) 2221
  - Include temperature rise of the PCB trace and T_G of the PCB dielectric in the analysis
  - Pros: Low production costs, high temperature, will not go out of stock or become obsolete
- Option 2: discrete resistor
  - Typically 0603- or 0805-sized
  - Review the data-sheet power derating curve
  - Pros: Low tolerance, low parasitics, smallest footprint



1206-sized resistor

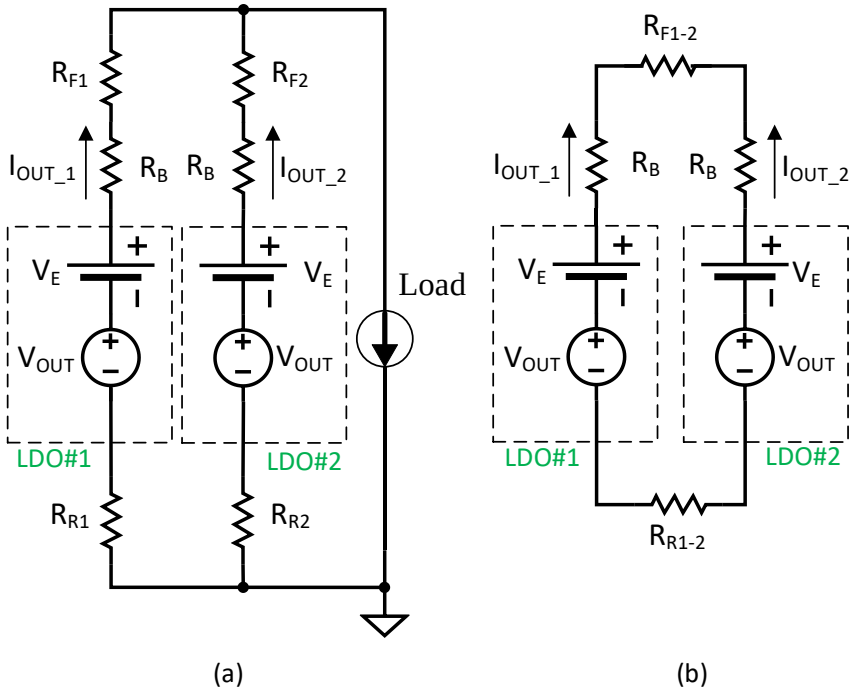
PCB resistors





Effects of PCB impedance

- Ideally, the PCB resistance is significantly less than the ballast resistance
  - PCB copper has a wide tolerance
- The PCB resistance (forward and return) is in series with the ballast resistance
- When R_B < 50 mΩ, the PCB resistance can meaningfully change the design
  - Conduct a post-route analysis to simulate the PCB resistance at hot temperatures
- You must assess two paths



Parallel LDO calculator

Step 1: Select the LDO using the drop-down box

Step 2: The data-sheet parameters are automatically entered

Step 3: Enter the system requirements

Not included: Abs Max voltage assessment or DC setpoint analysis
This calculator assumes the same LDO IC, ballast resistor, and output voltage is used for all LDO's in parallel

TPS7A57

LDO Specifications

Parameter	Value	Units	Optional User Entry	Units
V_E, high	2	mVdc		mVdc
V_E, low	-2	mVdc		mVdc
Thermal Impedance T_{JA}	21.9	°C / W		°C / W

Parallel LDO System Requirements

Parameter	Value	Units		
T_A	85	°C		°C
Maximum T_J per LDO	125	°C		°C
V_{IN}	1.25	Vdc		Vdc
V_{OUT}	0.75	Vdc		Vdc
Allowable load regulation	0.02	Vdc		Vdc
System Noise Requirement (10 Hz - 100 kHz)	2.45	µVrms		µVrms
Total System Load:	8.48	A		A

Minimum Ballast Resistance needed	0.8	mΩ		
Optimum Ballast Resistance	5.608043	mΩ		
Ballast Resistance Selected	5.608043	mΩ		mΩ

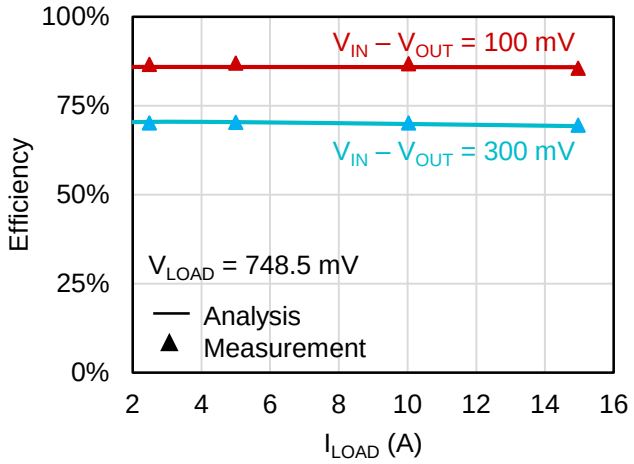
	N =
Minimum number of parallel LDO's required:	3

Step 4: Select the ballast resistor

Step 5: Use this many LDOs to meet the system requirements

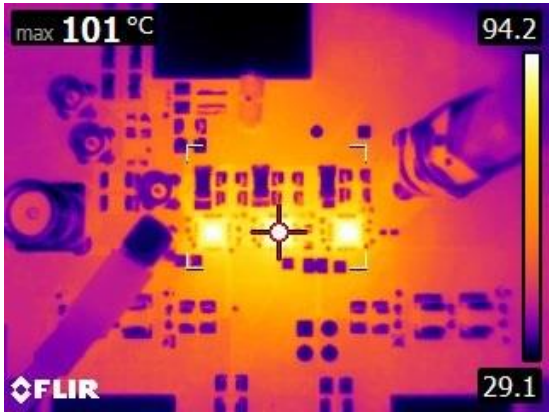
Parallel LDO calculator

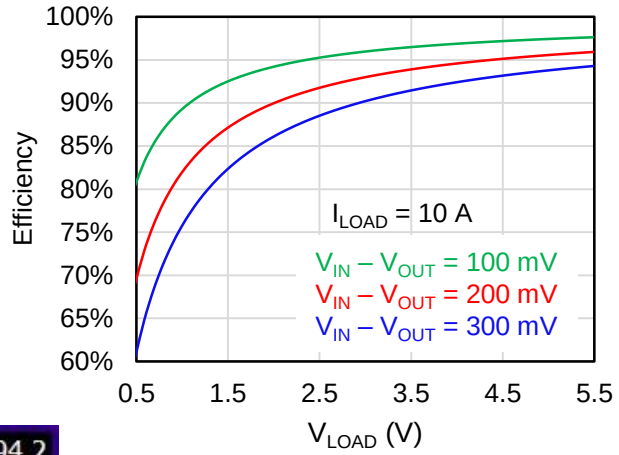
Three parallel TPS7A57 LDO analysis and test data



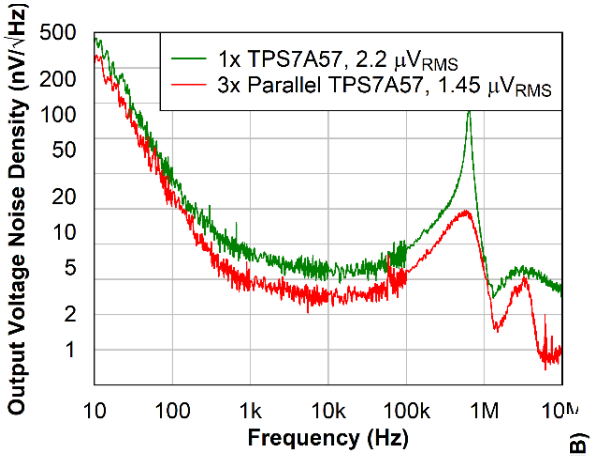
P_D = 6.75 W, 30 minutes

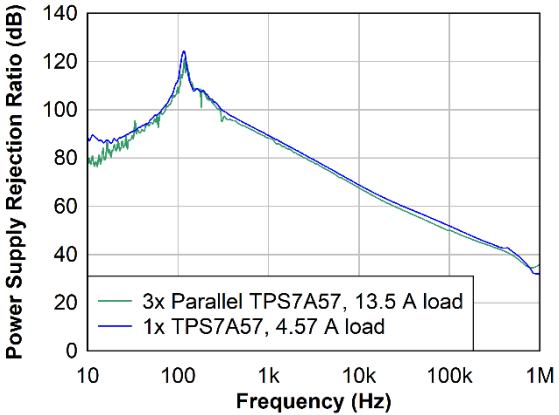
V_{IN} = 1.5 V, V_{LOAD} = 1 V, I_{LOAD} = 13.5 A

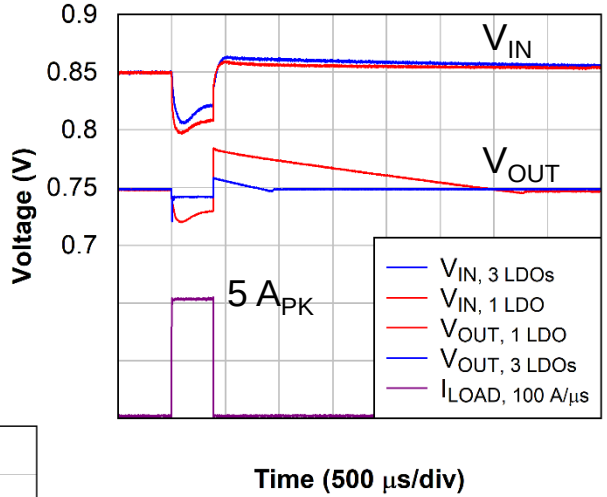




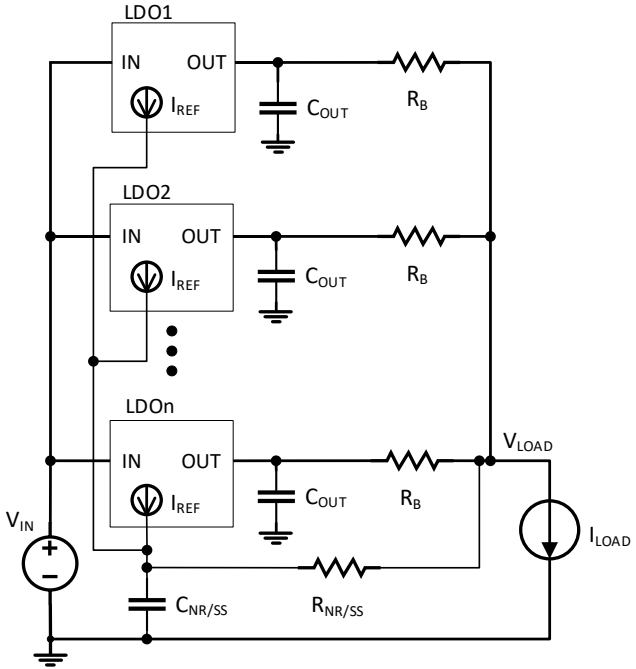
Three parallel TPS7A57 LDO analysis and test data



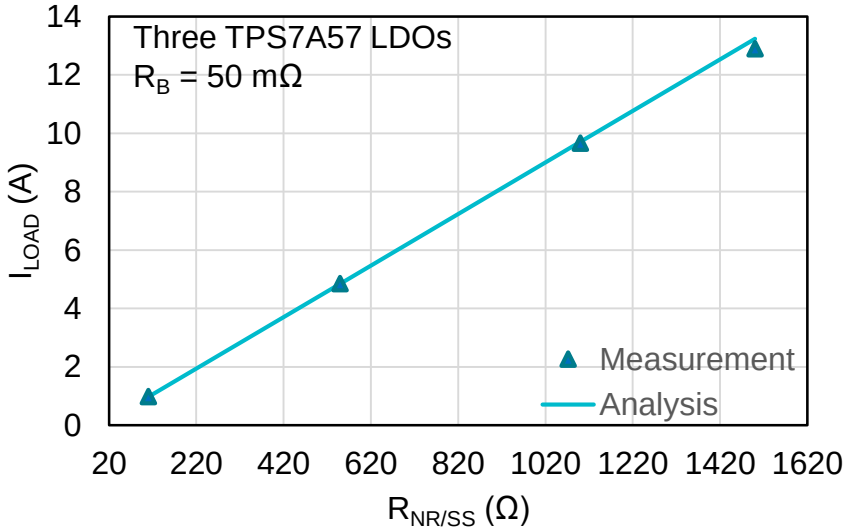




LDOs configured as constant-current sources



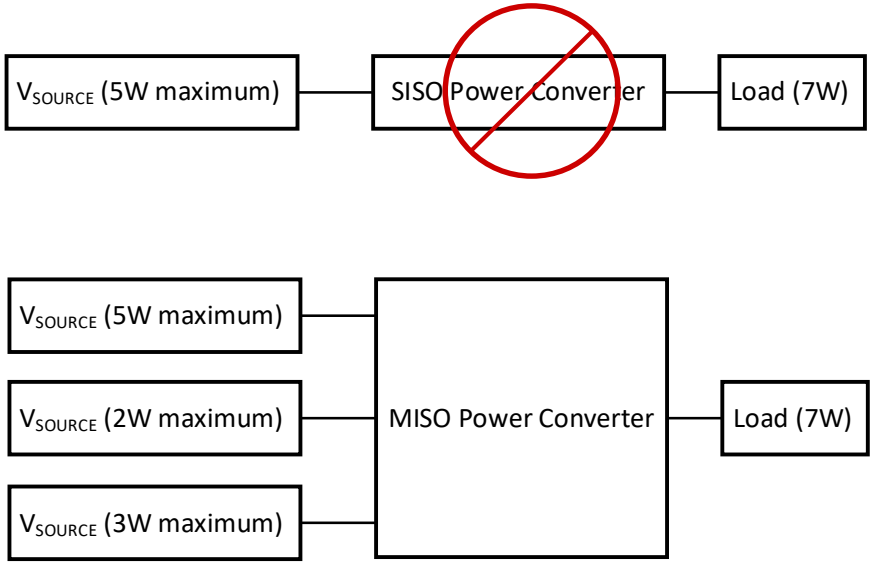
$$R_{NR/SS} = \frac{I_{OUT} R_B}{N \times I_{REF}} = \frac{I_{LOAD} R_B}{N^2 \times I_{REF}}$$



- Applications include noise-sensitive electronics typically driven by constant-current drivers (laser diodes, LEDs)

MISO power supply

- Modern complex systems have many power supplies, both on the input to the system and internally
- Sometimes the required power to a load is higher than the available power from a single input rail
- MISO power supplies can take multiple input supplies and merge power to provide a load on a single output



MISO parallel LDO design process

#1
Obtain:
- Maximum rail current
- Number of parallel LDOs required

#2
Set V_{LOAD} based on V_{OUTn} and the allowable load regulation

#3 Assume V_E for each rail

$V_{E,high}$:	↑ I_{OUTn}	↓ V_{LOAD}
$V_{E,low}$:	↓ I_{OUTn}	↑ V_{LOAD}
$V_{E,typical}$:	I_{OUTn}	V_{LOAD}

#4 Calculate R_{Bn} for each LDO

$$R_{Bn} = \frac{V_{OUTn} - V_{LOAD}}{I_{OUTn}} + \frac{V_{En}}{I_{OUTn}}$$

#5
Simulate in PSpice for TI

#6
Does the simulated I_{OUTn} and V_{LOAD} meet the system requirements?

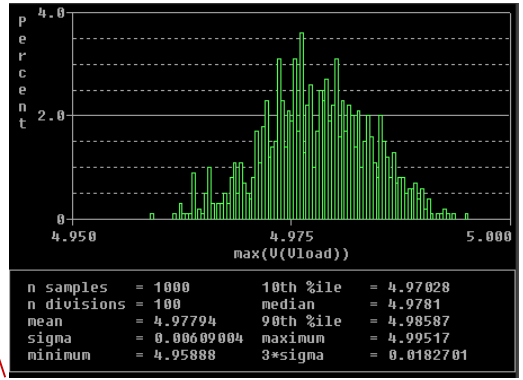
No

Yes

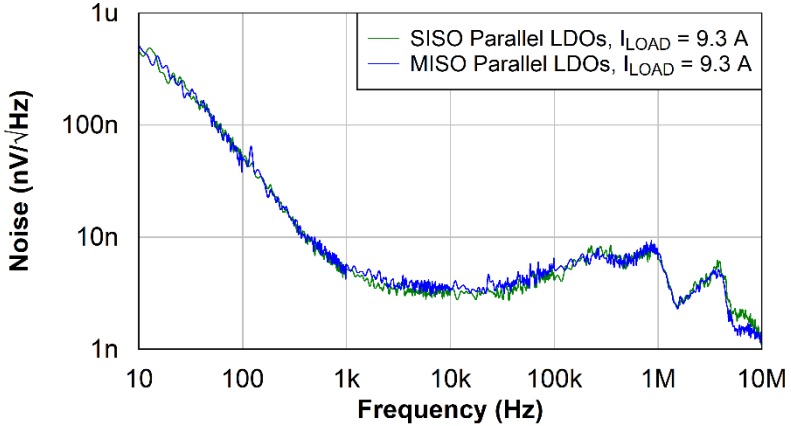
#7
Fabricate the design

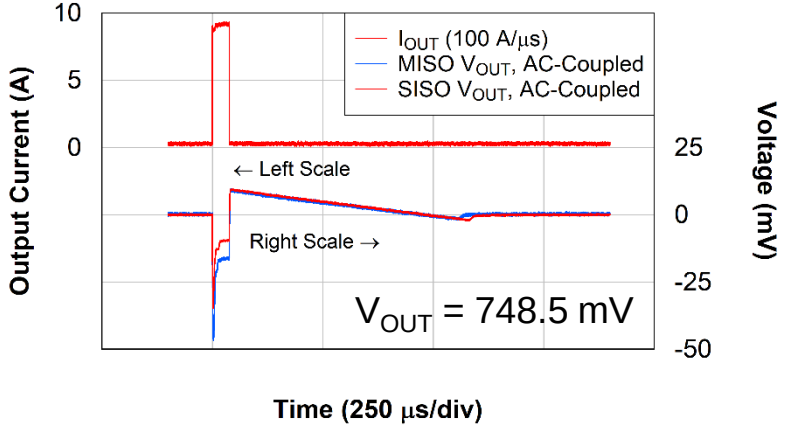
Sensitivity Component Filter = [*]

	Component	Parameter	Original	@Min	@Max	Rel ...	Linear
▶	Rb1	VALUE	22m	44m	0	-6.3830m	100
	Rb3	VALUE	5.5000m	0	11m	4.8780m	76
	Rb2	VALUE	11m	0	22m	2.2222m	34
	R24	VALUE	0.0020	0	4m	779.2208u	12
	R30	VALUE	0.0020	4m	0	-519.4805u	8
	R25	VALUE	0.0020	4m	0	-259.7403u	4
	R26	VALUE	5	0	10	0.9992f	< MIN >
	Rb11	VALUE	4m	4m	4m	0	0
	Rb21	VALUE	4m	4m	4m	0	0
	R27	VALUE	2.2000	2.2000	2.2000	0	0
	R31	VALUE	1	1	1	0	0



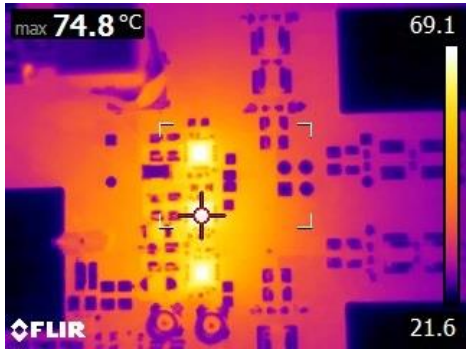
Parallel SISO LDOs vs. MISO LDOs



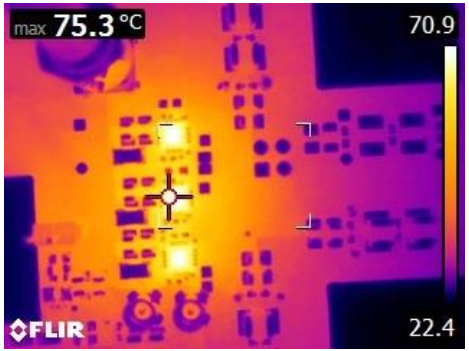


V_{LOAD} = 0.75 V
P_D each LDO = 1.55 W

V_{IN1} = 1.72 V, I_{OUT1} = 1.6 A
V_{IN2} = 1.25 V, I_{OUT2} = 3.1 A
V_{IN3} = 1.09 V, I_{OUT3} = 4.6 A



MISO LDO



Single-input single-output (SISO) LDO

V_{LOAD} = 0.75 V
P_D each LDO = 1.55 W

V_{IN1} = V_{IN2} = V_{IN3} = 1.25 V
I_{LOAD} = 9.3 A

Summary

- Covered the basic characteristics of LDO noise, PSRR, thermal performance and operation near dropout
  - Discussed what does and does not affect LDO noise and PSRR
- It is easy to configure LDOs to regulate current instead of voltage
- New resources allow you to quickly design with parallel LDOs using ballast resistors
  - Parallel LDOs can increase the load current, reduce system noise, improve PSRR, improve thermal performance and reduce the required headroom
- Connecting different input voltages to each parallel LDO input creates a MISO converter
  - Changing the ballast resistor adjusts the power sourced from each input supply

Resources

- "Accurately measuring efficiency of ultralow Iq devices"
- "Overcoming Low-Iq Challenges in Low-Power Applications“
- "Optimizing feedforward compensation in linear regulators“
- "Simplifying Stability Checks“
- "Avoid Start-up Overshoot of LDO"
- "LDOs Ease the Stress of Start-Up"
- "Soft-start circuits for LDO linear regulators"
- “LDO Basics”
- “How to Measure LDO Noise”
- “LDO PSRR Measurement Simplified”

Resources

- "Understanding power supply ripple rejection in linear regulators“
- “Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator”
- “An Empirical Analysis of the Impact of Board Layout on LDO Thermal Performance”
- “Measuring the Thermal Impedance of LDOs in Situ”
- "Switch-mode power converter compensation made easy“
- “Comprehensive Analysis and Universal Equations for Parallel LDOs Using Ballast Resistors”
- “Parallel LDO Architecture Design Using Ballast Resistors”
- "Parallel LDO calculator"

Resources

- “Scalable, High-Current, Low-Noise Parallel LDO Reference Design”
- “Semiconductor and IC Package Thermal Metrics”

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