UCD3138A64/UCD3138128 Programmer's Manual

SLUUB54B – April 2016

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- Added Interfaces for External EEPROM
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- How to migrate firmware programs from UCD3138 to UCD3138064

For the most up to date product specifications please consult the UCD3138A64 Device datasheet (Lit # SLUSBZ8) available at www.ti.com.

1 Introduction

The UCD3138A64 device is an 80-pin, 64kB product offering in TI's UCD3138 family of digital controllers for isolated power. It offers more RAM, higher pin count, a real-time clock, and enhancements to several peripherals, compared to the UCD3138064 devices which are available in 64-pin and 48-pin package options.The UCD3138128 is the same as the 'A64, except it offers twice the program flash – 128K bytes arranged in 4 independent 32K blocks.

This manual highlights the differences between the UCD3138064 and the UCD3138A64 devices. It describes the added features and changes to existing features. It also gives guidance on converting programs from the UCD3138 and the UCD3138064 to the UCD3138A64. The UCD3138 Programmer's Manuals (SLUU994, SLUU995, and SLUU996) and the UCD3138064 Enhancements Programmer's Manual (SLUUAD8) should be used for information on all elements that are common to these devices.

There are also sections on the describing the UCD3138128 enhancements, and how to convert programs to the '128.

Compared to the UCD3138064, the UCD3138A64 device is differentiated based on the following considerations:

- Faster checksum calculations in ROM for quick firmware startup
- 4K additional RAM for a total of 8K RAM
- Boot Flash based Dual Memory Image support for 'on-the-fly' firmware updates (vs ROM based support in UCD3138064)
- Instead of a PMBus and an I2C interface there are 2 enhanced PMBus/I2C interfaces
    - Each interface now supports master and slave, I2C and PMBus
    - Each interface has enhanced recovery from bus faults
    - Each interface supports automatic address acknowledge of a second address
- Real Time Clock for accurate time/date information.
- 4 additional General Purpose I/O lines
- 1 additional timer capture register
- Support for fixed sampling rates for LLC**
- Information on PCM (Peak Current Mode) pulse width for each cycle
    - This makes it much easier to measure average current on every cycle
- Enhanced Burst Mode and Fault Handling for PCM.
    - Increased fault count from 32 to 128 consecutive faults before shut down.
- QFP-80 package for UCD3138A64, instead of QFN-64 & QFN-48 in UCD3138064
- Capability to disable the RESET pin under firmware control
- Clock Trim registers that make it possible to adjust the clock speed more easily
- Unused bits removed from DPWM registers

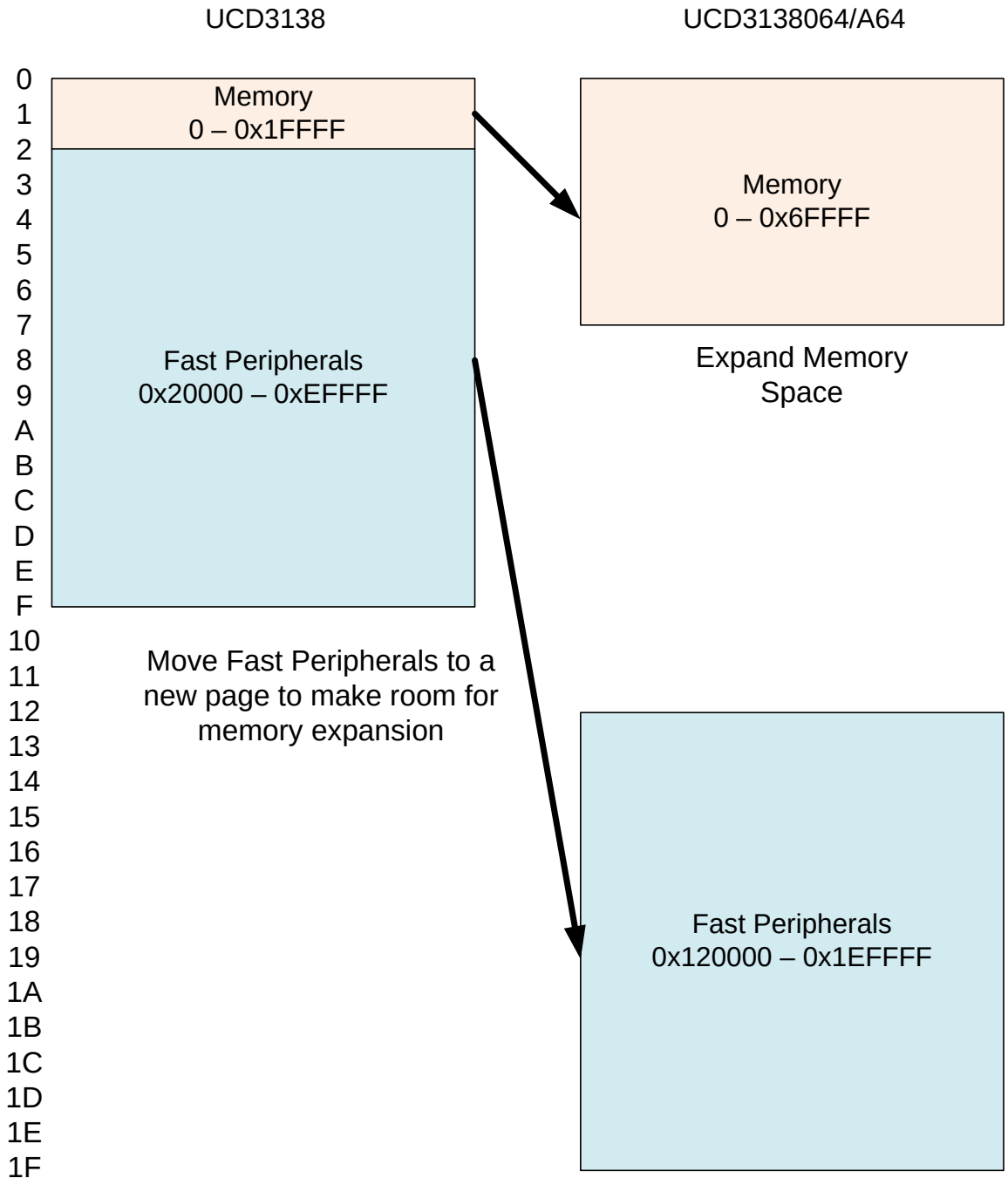
****NOTE**: Adding the fixed sample rate to LLC has lengthened the DPWM calculation time at the beginning of the period. It has increased from 72 nsec to 120 nsec. Moving DPWM edges in and out of this window could cause pulse extension and shoot through in some power supply topologies.

2 More Memory - Memory Map Changes for UCD3138A64

The larger 8K RAM requires changes to the addressing for the RAM and data FLASH.

2.1 *Memory Map Overview*

The memory map overview for the UCD3138A64 is the same as the overview of the UCD3138064. Compared with the UCD3138, the fast peripherals are moved up to make room for the larger FLASH.



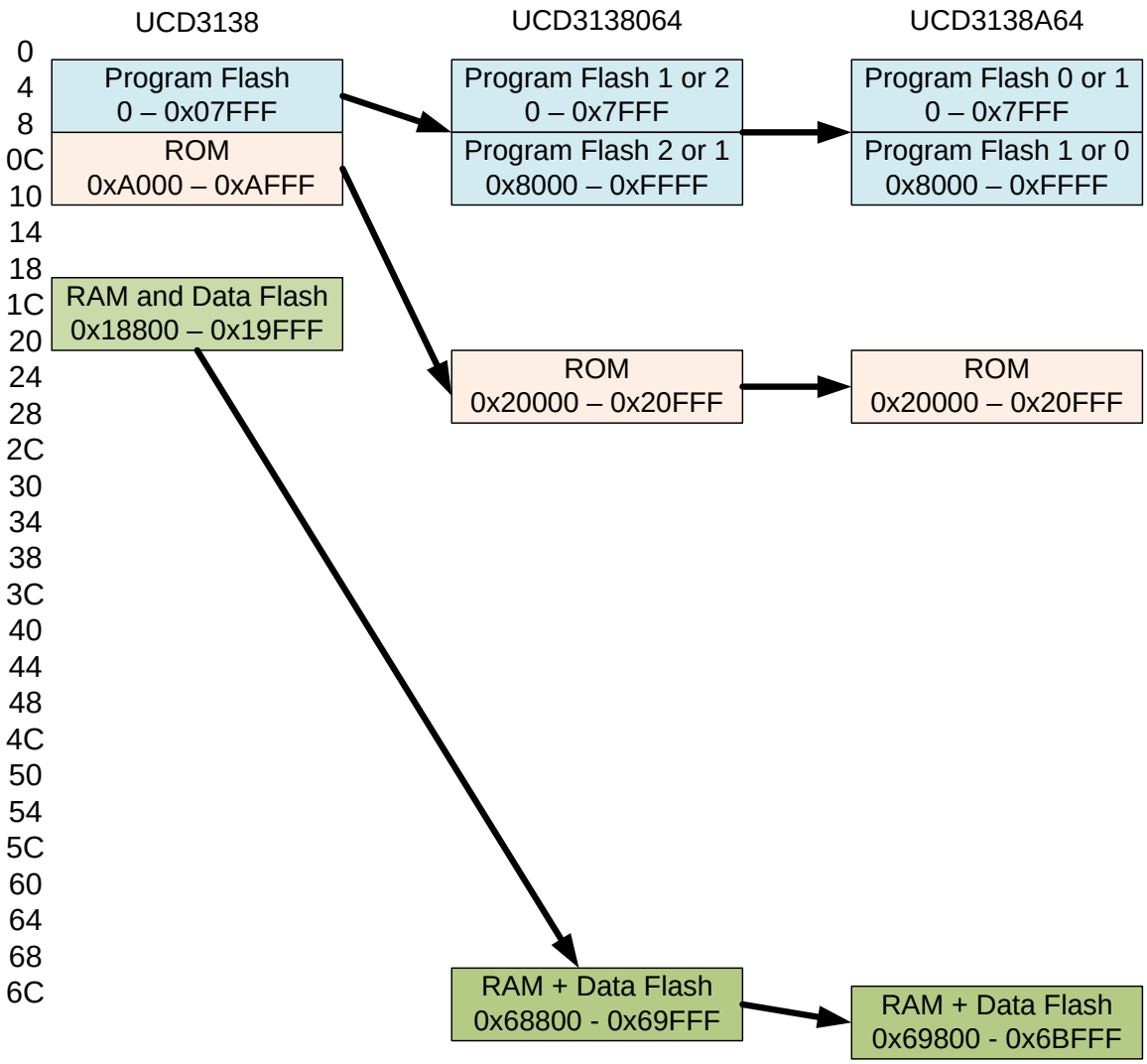
Overall Memory Map Changes

The fast peripherals are moved up by 0x100000 bytes. This makes it very simple to calculate their new addresses. The slow peripherals, those mapped to 0xFFF7EC00 and above, are not moved at all, so they are not shown on the figure. The RTC is added at 0xFFF7E400. The SPI interface was added in the UCD3138064 at 0xFFF7E600, and is still the same on the UCD3138A64.

Fast peripherals use the same address decode scheme as memories. They have address mapping registers and run at the processor clock speed. Slow peripherals are on a separate I/O bus with no address mapping registers. The I/O bus and the slow peripherals run at half the processor clock speed.

2.2 *Memory Map Details – Flash Mode*

There are some changes, however, in the details between the UCD3138064 and UCD3138A64. Here is a block diagram:



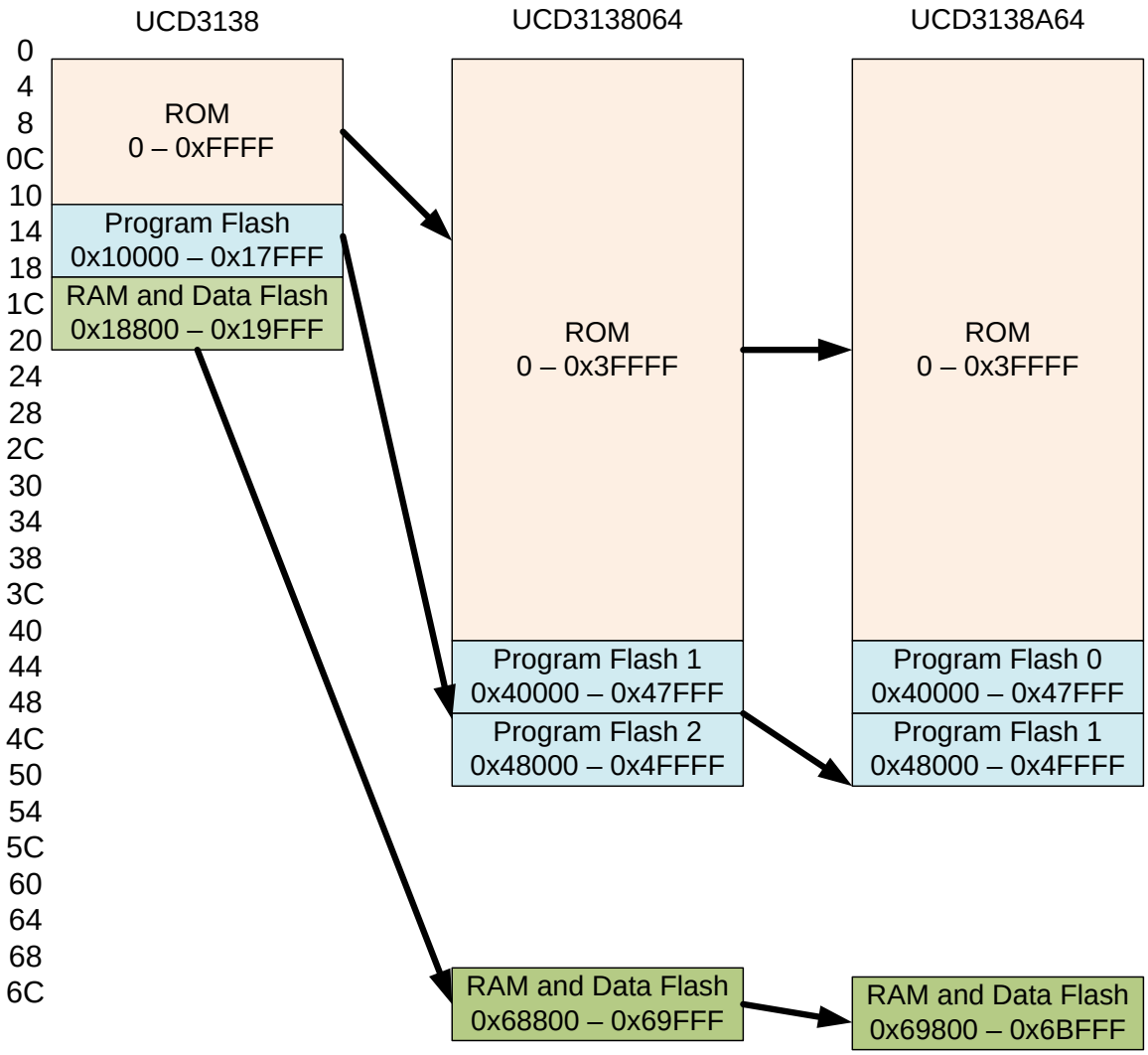
Detailed Memory Map Changes in FLASH Mode

The numbering system for the flash blocks is changed. For the UCD3138064, the blocks are referred to as 1 and 2. On the UCD3138A64, they are numbered from 0 to 1.

The RAM is now 8K. The memory addressing logic requires that an 8K block be on an 8K boundary. This means that the RAM is moved from 0x69000 to 0x6A000. The data FLASH is moved from 0x68800 to 0x69800. It is kept next to the data FLASH so that a single CPU register can be used with an offset to access both memory blocks at the same time.

2.3 *Memory Map Details – ROM Mode*

The changes between the UCD3138064 and UCD3138A64 in ROM mode are similar to the changes in flash mode – the flash block names are changed, and the data FLASH and RAM are moved further up in memory.



Memory Map changes to ROM, RAM, and FLASH in ROM mode

In the ARM core, the reset and interrupt vectors start at location 0 in memory. At power up reset, the ROM must be at location 0 to provide the vectors. In flash mode, the flash must be at location 0 to control the interrupt vectors. This is accomplished by changing the addresses of the ROM and FLASH. In ROM mode, the ROM must extend from location 0 to the location where it will be in FLASH mode. In the UCD3138064 and UCD3138A64, this address is 0x20000. The ROM reset vectors jump to this area. This way, when flash mode is entered, the ROM simply remaps itself to the higher address. The program is already executing there. Then it remaps the flash to location 0 and jumps the vector at 0. The ROM on the UCD3138064 is 8K. That same 8K image is repeated throughout the entire memory space from 0 to 0x3FFFF in ROM mode. The ROM in

the UCD3138A64 is also 8K, but 4K is reserved for built in self test. Because of this, the sine and exponent tables in the UCD3138 and UCD3138064 ROM are not provided in the ROM. The UCD3138A64 has plenty of flash for any sine or exponent tables desired.

2.4 *Register Changes for Program Flash Blocks*

Each Flash block has 3 registers associated with it:

- DecRegs.PFLASHCTRLx – page and mass erase and block busy status
- DecRegs.MFBAHRx – sets high bits of address for flash block – used for moving blocks
- DecRegs.MFBALRx – sets lower bits of address and block size – used for moving blocks

See the UCD3138 ARM and System manual for more information on these types of registers. The PFLASHCTRLx registers have different numbers depending on which device is being used. Here is a table of PFLASHCTRLx names across the 3 devices:

Block Number on A64	UCD3138	UCD3138064	UCD3138A64
0	PFLASHCTRL	PFLASHCTRL1	PFLASHCTRL0
1		PFLASHCTRL2	PFLASHCTRL1

Note that there is no block number for the single block in the UCD3138. On the UCD3138064, blocks are numbered 1 and 2, and on the UCD3138A64, blocks are numbered from 0 to 1.

The MFBAHR and MFBALR registers (Memory Fine Base Address High and Low) are numbered sequentially. Some of them are used for addressing the faster peripherals. This explains the numbers between the first flash block and subsequent flash blocks. Here is a table:

Block	MFBAHR	MFBALR
0	MFBAHR1	MFBALR1
1	MFBAHR17	MFBALR17

There is only one DecRegs.FLASHILOCK register. It must have a key written to it before each write or erase to a flash block. Different values must be written to it depending on which flash block is being modified.

#define PROGRAM_FLASH0_INTERLOCK_KEY 0x42DC157E
#define PROGRAM_FLASH1_INTERLOCK_KEY 0x6C97D0C5
#define DATA_FLASH_INTERLOCK_KEY 0x42DC157E

These codes are the same as the ones on the UCD3138064.

See Section 20.16, DEC – Address Manager of this document for information on the detailed memory and bit maps for these registers.

3 Changes to ROM Boot Program

The ROM changes the response to the version command and it also changes the handling of flash checksums when it powers up.

3.1 ROM Version

The UCD3138A64 will return a 0006 as the first half of the version, indicating the device. The first version of the ROM will return a 0001 as the second half of the version, indicating version 1 of the ROM. If other versions of the ROM are produced, the number will increment.

3.2 Flash Checksum Handling

The ROM program changes how it handles program startup. Instead of 2 possible checksum locations on the UCD3138, there are 4 on the UCD3138064, and 3 on the UCD3138A64. To speed up calculations on the UCD3138A64, the checksum changes from 4 to 8 bytes. Now it is a sum of the memory read as 32 bit words, rather than as 8 bit bytes. This makes the checksum calculation about 4 times faster. This means that the ROM can verify the checksum for 64 kbytes in about 5 msec while the UCD3138 takes 10 msec for 32 kbytes.

Here is the code for calculating the checksum:

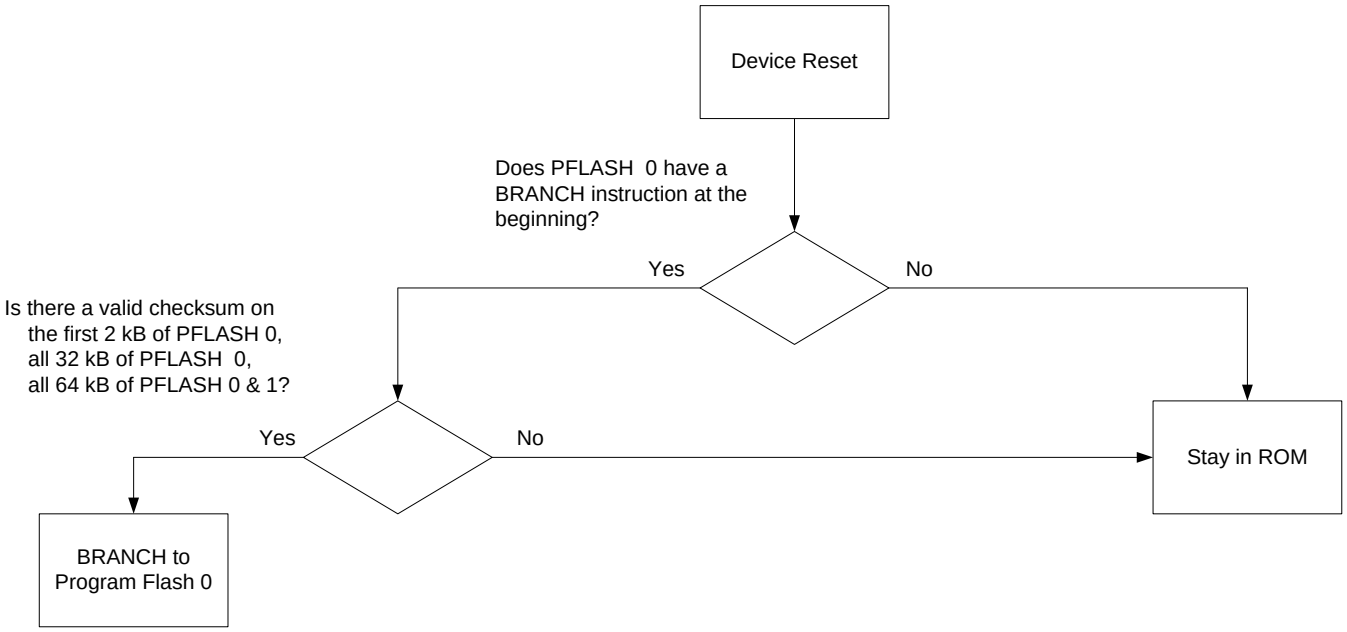
```
void calculate_checksum(register Uint32 *start_address, register Uint32 *end_address)
{
        register unsigned long long lcs = long_checksum;  //use local register variable for
speed.

        while(start_address < end_address)
        {
                lcs = lcs + *start_address ;
                lcs = lcs + (Uint32)*(start_address + 1) ;
                start_address = start_address + 2;
        }
        long_checksum = lcs;
}
```

Two words are added each time through the loop to improve the speed by reducing the loop overhead.

The checksums and their locations are:

0x7f8 – Boot block for Block 0
0x7ff8 – Overall checksum for Block 0
0xfff8 – Overall checksum for a 64K program combining Blocks 0 and 1

Here is a flowchart showing the order in which the ROM verifies the checksums:

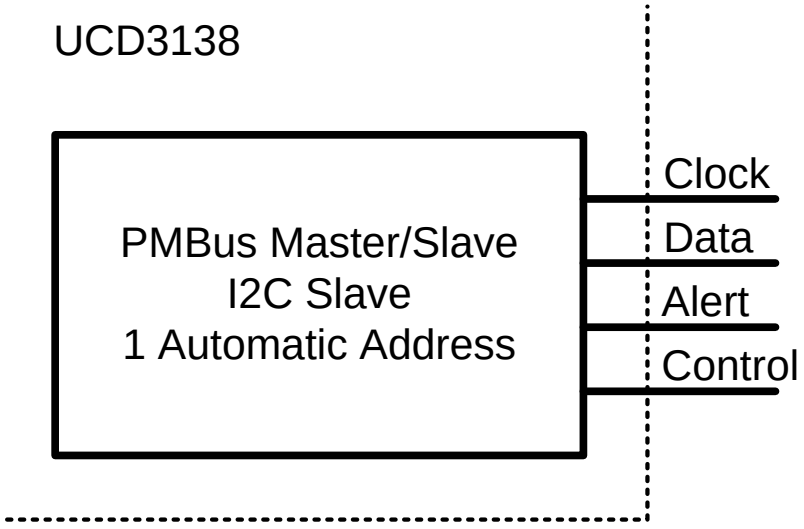


The branch instruction check prevents the checksum program from looking at an empty block of memory. Otherwise a block filled with zeroes would pass the checksum test.

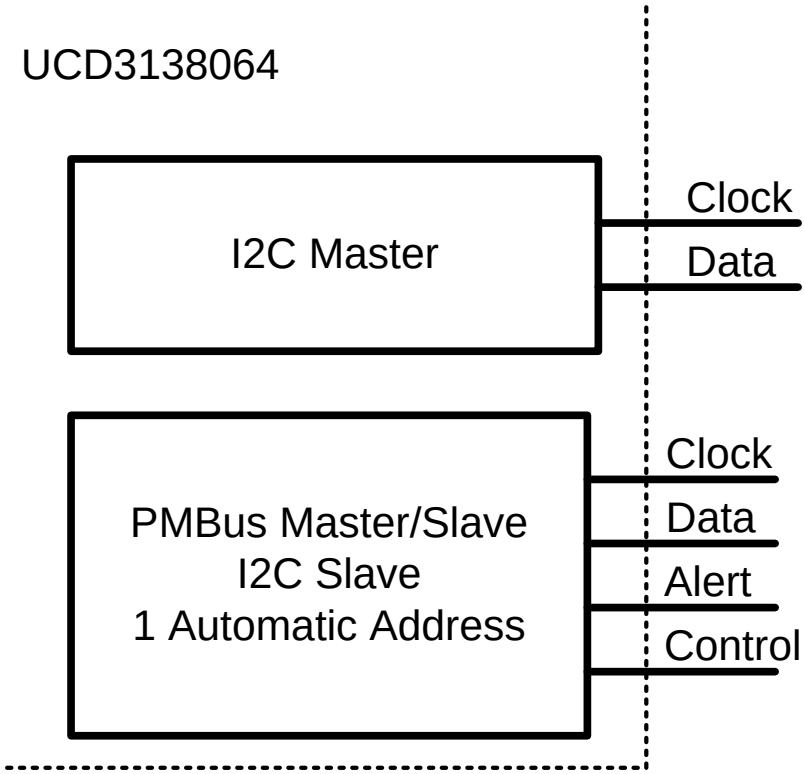
The UCD3138A64 doesn't have ROM support for putting 2 separate programs into flash, one in each flash block. This can still be done, however, using boot flash. Or the program in block 0 can be a fixed program, which checks the program in block 1 and jumps to it if appropriate.

4 Two Enhanced I2C/PMBus Interfaces

The UCD3138 has a single PMBus interface which supports master and slave modes for PMBus. It can also be used as an I2C slave.

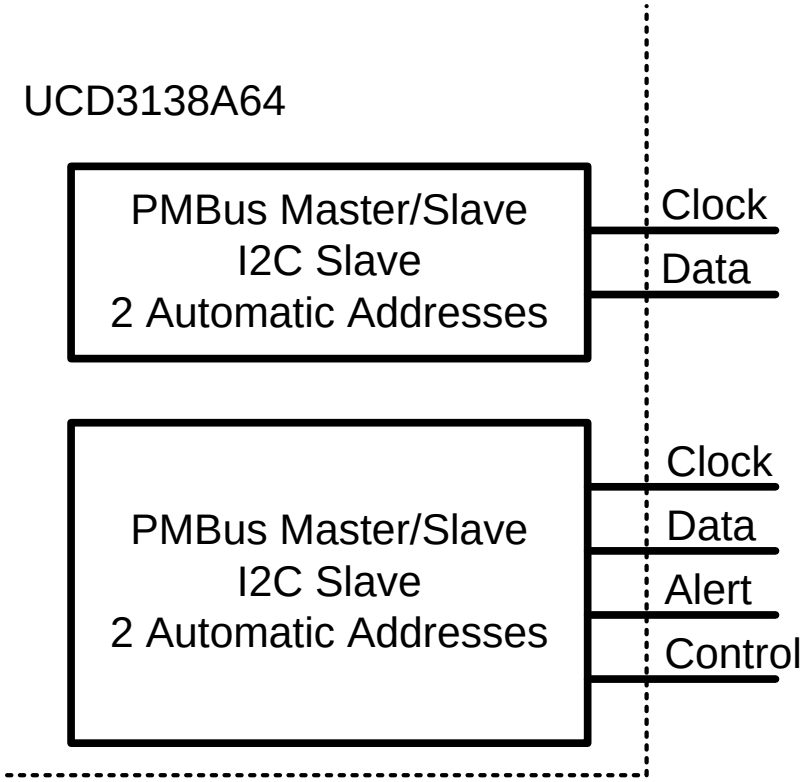


The UCD3138064 adds an I2C interface which can be used as a master for both I2C and PMBus. It does not support slave mode for either I2C or PMBus.



The UCD3138A64 has 2 essentially identical I2C/PMBus interfaces which support both master and slave modes. They also both support automatic acknowledgment of 2 addresses, making a total of 4 addresses in all. The previous devices only provided automatic acknowledgement of 1 address. The UCD3138A64 also provides enhanced fault handling for PMBus and I2C bus faults.

Only one of the interfaces supports the PMBus Alert and Control lines and IBIAS bits, but otherwise they are identical.



See the UCD3138 documentation for using the interfaces as PMBus slaves. The UCD3138064 manual describes how to use the I2C interface master mode with EEPROMS. Note that the I2C master mode is designed for use with EEPROMS. If other devices have unusual requirements for the placement of repeated start, they may not work.

4.1 *PMBus/I2C Register Names are Different on UCD3138064 and UCD3138A64*

On the UCD3138064, the I2C port registers are called I2CRegs, and the individual register names have I2C in the first 3 letters, like "I2CCTRL1". The PMBus registers are very similar, except they are called PMBusRegs, and have PMB in the first 3 letters, like PMBCTRL1. The fields within the registers are very similar.

In the UCD3138A64, the registers are called PMBusRegs and PMBus1Regs, and all the register names start with PMB. To convert an I2C code from the UCD3138064 to the UCD3138A64, change all the "I2C"s to "PMB"s, and select either PMBus or PMBus1 regs. The bits related to Alert, Control, and IBIAS are duplicated in both register sets, but they are only implemented fully in PMBus. In PMBus1, they will not provide correct results, because they are not connected to pins.

4.2 *Automatic Acknowledgement of 2 Slave Addresses*

The UCD3138A64 adds two additional bitfields to the PMBCTRL2 register, called SLAVE_ADDR_2_EN and SLAVE_ADDR_2. If SLAVE_ADDR_2_EN is set, the PMBus/I2C slave interface will acknowledge the address in SLAVE_ADDR_2 as well as the one in

SLAVE_ADDR. To determine which address was acknowledged, read from the PMBHSA (PMBus Hold Slave Address) Register.

4.3 *Alert and Control Support on PMBus*

Both PMBus ports use the same register definitions for convenience, but on PMBus1 the bits relating to Alert and Control pins should be left in their default states. There is only one set of Alert and Control pins, and they are connected to PMBus 0.

4.4 *Improved Clock High Timeout Handling*

Reading the CLK_HIGH_TIMEOUT bit was not recommended in the earlier devices. On the UCD3138A64, this bit in the PMBST register will go high if the clock stays high for more than 55 milliseconds in the middle of a message. There is an added bit in the PMBINTM register as well to enable an interrupt for clock high timeout. There is also a CLK_HI_DIS bit in PMBCTRL3 which disables clock high timeout.

4.5 *Improved Bit Counter Reset*

On the UCD3138A64, messages can be stopped in the middle of a byte and the PMBus will recover. Anything which resets the PMBus state machine now resets the bit counter as well. Events which reset the state machine include: Start, Stop, Clock High Timeout, Clock Low Timeout, and setting the RESET bit in PMBCTRL3.

4.6 *Change in Test Mode Address*

On the UCD3138A64, there is still a PMBus/I2C address which will start to put the chip into test mode. On the earlier devices, the address is 0x7f. On the UCD3138A64, the address has been changed to 0x7e. This way if the clock line is active but the data line is released, the device will not go into test mode.

5 External Clock Controlled Real-Time Clock

The UCD3138064 adds a Real-Time clock controlled by an external 10 MHz clock source. This provides a precise reference for time measurement. It can also be used to adjust UART and DPWM frequencies for better frequency control. Here are the major features of the real time clock:

- Counts seconds, minutes, hours and days
- Digital trim of external frequency from -500 to +250 ppm in 0.8 ppm steps.
- Provides interrupts at 1 second, 10 seconds, 30 seconds and 60 seconds.

5.1 *Trimming the External Frequency*

The RTC is configured to count seconds based on a 10 MHz clock input. Changing the value in the RTCPRESCALE register can compensate for small variations in the clock frequency. The RTCPRESCALE register has a default value of 0x2CF. It can be varied from 0 to 0x3ff. Each step in the register value will compensate for a 0.8 ppm variation in the clock frequency.

Inside the RTC, the 10 MHz clock is first divided by 8, giving a nominal 1.25 MHz. This number is divided by 1,250,000 to give the 1 second interval. The number in the prescale register is actually 1,250,000 – 1. In hex, this is 0x1312CF. The PRESCALE register permits modification of the least significant 10 bits of this number. The higher bits are fixed. This permits digital compensation for crystal manufacturing variations.

The range goes from 0x131000 (9,994,240 Hz) to 0x1313FF (10,002,424 Hz). This provides +240, -570 ppm coverage for crystal variation.

5.2 *RTC Calendar Data*

The RTC provides simplified calendar data (seconds, minutes, hours, days) in the RTCCOUNT register. There are 11 bits for days, so up to 5.5 years of on-time can be recorded. If date, month and year are required, this is simple to determine in firmware.

The calendar data can be written to using the RTCPRESET register and the PRESET_EN bit in the RTCCTRL register. Simply write the desired value to the RTCPRESET register and toggle the PRESET_EN register high and then low. This will copy the value from the RTCPRESET to the RTCCOUNT register.

5.3 *RTC Polling and Interrupts*

The RTC has two registers for polling and interrupts:

RTCINTEN – enables interrupts
RTCINTSTAT – Shows which interrupts are active

The RTC sets bits in the RTCINTSTAT registers every 1, 10, 30, and 60 seconds. These bits are set even if the corresponding bits in the RTCINTEN register are not set. The RTCINTSTAT bits are clear on read.

There is a bit in the RTCINTEN register for every bit in the RTCINTSTAT register. If the bit in RTCINTEN is set, it enables an interrupt for the corresponding bit in RTCINTSTAT.

6 Four Additional General Purpose I/O Pins

The UCD3138A64 adds 4 General Purpose I/O pins, GPIOA through GPIOD. They are configured in the FAULTDIR, FAULTIN, and similar registers. They can be inputs or outputs, and can trigger interrupts just like fault pins. However, they cannot be used as fault inputs to the DPWMs. There are no bits associated with the GIO pins in the various FAULTDET registers. So they are best used as simple general purpose I/O registers.

7 SPI Port Pins Move Around – JTAG_MUX_SEL Bit

The TAG_MUX_SEL bit in the MiscAnalogRegs.IOMUX register provides a way to disable JTAG to preserve code security. It has a side effect of moving the SPI bits to different pins. There is a way to provide both code security and keep the SPI on the same pins.

If JTAG is disabled, the SPI bits are moved to the JTAG pins. Depending on the state of the flash at chip reset, this bit can be either a zero or a one.

1. If flash memory has a valid checksum and ROM jumps directly to flash, the bit will be a 1, JTAG will be disabled, and the SPI function will appear on the JTAG pins

   TCK -> SPI_CLK
   TMS -> SPI_CS
   TDI -> SPI_MISO
   TDO -> SPI_MOSI

2. If flash memory does not have a valid checksum, the ROM will stay in ROM, and the bit will be a 0. JTAG will be enabled and the SPI function will appear on the SPI pins.

There is a way to keep the pinout the same for both cases and still preserve code security.

1. In the debug code, simply enable JTAG and use it for debugging
2. In the production code, use the GLBIO registers to map the JTAG pins as outputs before enabling JTAG. This way the SPI will stay on the SPI pins and the JTAG will be disabled.

8 One Additional Timer Capture Register

The UCD3138A64 adds a second timer capture register with its associated hardware This added register makes it much easier to measure pulse width (by setting one register to capture the rising edge and one to capture the falling edge). It makes it easier to measure the relationship of any edge to any other edge, or to measure two independent edges. This requires several changes to the timer registers:

- T24CAPDAT and T24CAPCTRL are duplicated and numbered 0 and 1.
- T24CAPIO gets additional bits to control TCAP1

9 Support for Fixed Sampling Rates for LLC

The UCD3138A64 has modified DPWM logic. With the earlier UCD31XX parts, LLC programs had to sample at the LLC switching frequency to avoid pulse extension. The UCD3138A64 permits sampling at a fixed rate, as high as 2 MHz, which permits consistent filter bandwidth across the load range. As a result of this change, however, the DPWM takes longer to calculate its edges for the current switching cycle. Moving edges into or out of this calculation window may result in pulse extension. This window is enlarged to 120 ns on the UCD3138A64.

For implementation details on fixed sample rates for LLC, please see the TI LLC Reference Program.

10 Information on Pulse Width in Peak Current Mode

The UCD3138A64 adds the DPWMCBCLOCATION register to the DPWM registers. In Peak Current mode, and in any other mode where the cycle-by-cycle (CBC) signal is used, this register will contain the DPWM period counter value at which the last CBC occurred. In Peak

Current mode, this will give the pulse width for the previous switching cycle. This counter value is in low resolution, meaning that each count represents 4 nsec.

This value can be used to place the sample trigger near the center of the FET on-time, making it possible to measure average current. See the EVM firmware for specific topologies for more information.

11 Improvements to Fault Handling and Burst Mode

The UCD3138A64 adds 3 enhancements to the UCD31xx fault handling:

- Fault counter goes from 5 bits to 7 bits
- Blanking can be extended to the CBC Fault by setting a bit.
- All DPWM lines are turned off by a fault, even if the Edge Generator is being used (PSFB topology, for example)
    - This also helps with hardware burst mode for PSFB because it uses the same shut-down mechanism as the fault does.

11.1 *Fault Counter Changes from 5 to 7 Bits*

The UCD31XX family has sophisticated fault handling logic. For a detailed description of this logic, see the UCD3138 Digital Power Peripherals Programmer's Manual.

There are several fault signals which latch off the DPWM when a fault occurs. To restart the DPWM, the DPWM must be disabled and reenabled. All of these fault signals have a count value in a register. For the fault to be triggered, x consecutive switching cycles have to have the fault signal occur, where x is the value in the count register plus 1. On the UCD3138 and UCD3138064, the maximum count value is 32. On the UCD3138A64, the maximum value is 128. See Section 20.8.15 DPWM Fault Control Register (DPWMFLTCTRL) for the specific bitfields involved.

11.2 *Blanking for the Cycle-by-Cycle Fault Added*

In addition to the faults described above, there is also one signal called CBC (Cycle By Cycle), which turns the DPWM off for the remainder of the switching cycle, but permits it to turn on again at the beginning of the next cycle. Unlike the faults, the CBC does not latch the DPWM off permanently. This signal is typically used for current limiting, but is also used for peak current mode.

The CBC signal can be blanked with 2 blanking periods set by the blank a and blank b registers in the DPWM.

There is also something called the CBC fault. The CBC fault uses the same CBC signal which is used for the CBC non-latching DPWM shutdown. The CBC fault, however, has a count register and will latch the DPWM off when the count is exceeded. This is useful for two stage current limiting. The non-latching CBC can be used for a short time, but if it happens for (for example) for 100 consecutive switching cycles, the CBC fault can be used to latch the DPWM off.

On the UCD3138 and UCD3138064, the blanking only works on the non-latching CBC logic. The latching CBC fault has no blanking. With the UCD3138A64, setting the new CBC_FAULT_MODE bit in the DPWMFLTCTRL register enables blanking for the CBC fault too. Leaving CBC_FAULT_MODE as the default zero value makes the UCD3138A64 function just like the other UCD31xx parts, with no blanking for the latched CBC fault.

11.3 *Improved Fault and Burst Mode with Edge Generator in Use*

On previous devices, the fault logic worked on the DPWM outputs before the edge generator logic. This meant that sometimes one of the 4 FET control lines for PSFB (Phase Switching Full Bridge) would not be turned off right away, and firmware would be required to turn it off. The same was true of the hardware burst or light load mode. When the burst was over, sometimes one of the lines would not be turned off automatically.

Now the fault logic has been extended past the edge generation logic, so that all 4 lines are turned off immediately by a fault or by burst mode. There are no register changes associated with this enhancement.

12 Eighty Pins Instead of 64

The UCD3138A64 is available in an 80 pin package instead of a 64 pin one. This makes it possible to have 4 more general purpose I/O pins. In addition, the second PMBus/I2C bus and the SPI bus are no longer multiplexed, but now have dedicated pins. This has caused significant changes to the IOMUX register. Consult the IOMUX register reference below and the pinout in the data sheet for more information.

Pins have been added so that the output of Timers 2 and 3 are available for PWM and general purpose I/O. There is also a second capture pin to go with the second capture register

All of this has caused changes in the global I/O registers. The Timer 2 and 3 pins have been added to global I/O, as has the capture 1 pin. What was the capture pin has been renamed to be capture 0.

To make room for capture 1, the PMBus clock pin has been removed from global I/O. The PMBus data pin has been replaced by the I2C data pin in all the global I/O registers.

13 Disabling the RESET Pin

On the UCD3138A64, it is possible to disable the $\overline{\text{RESET}}$ pin. This may be useful in very noisy systems. If the $\overline{\text{RESET}}$ pin is disabled, the only way to reset the UCD3138A64 with hardware is to remove power from the device. Of course software reset, or reenabling the reset pin is possible in firmware. Here is the code to disable the reset:

```
MiscAnalogRegs.CLKTRIM.bit.RESET_DISABLE = 1;
```

14 Adjusting the Clock Speed

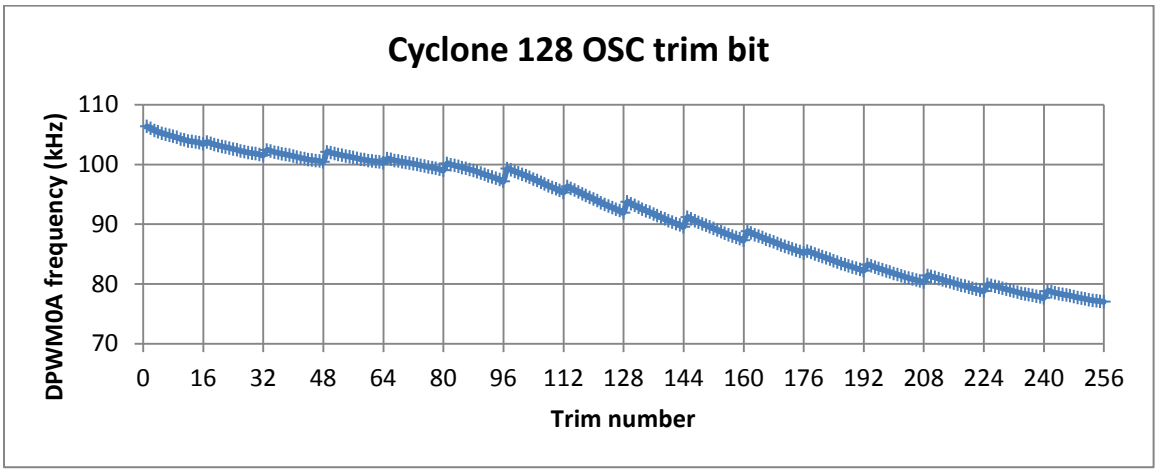
The UCD3138A64 is designed to make it possible to change the clock speed for the processor and the peripherals. The main clock is called the HFO (High Frequency Oscillator), and all other clocks except for the RTC are derived from the HFO.

There are two clock speed control bitfields, HFO_FINE_TRIM and HFO_COARSE_TRIM. Here is how to write to them:

```
MiscAnalogRegs.CLKTRIM.bit.HFO_COARSE_TRIM = x;
MiscAnalogRegs.CLKTRIM.bit.HFO_FINE_TRIM = y;
```

When each device is tested, the correct values for these registers are determined. The device will power up with the optimal values. By adjusting the trim registers and comparing the HFO clock to the RTC clock or some other precise reference, it is possible to make the clock more accurate over the temperature range.

The coarse and fine trim registers are monotonic as individual registers, but the same does not apply if the coarse and fine trim registers are used together. The range of the fine trim register is bigger than the size of a coarse trim register step. And the two registers will not necessarily align the same way on different devices. Any firmware which modifies the clock trim fields will have to take this into account. The graph below shows an example of clock speed variation. The vertical axis is DPWM frequency with a nominal value of 100 KHz. The horizontal axis is a number which combines fine and coarse trim into one. Every 16 steps, the fine trim goes from its minimum to its maximum value, and the coarse trim is incremented by 1. Since the fine trim overlaps more than 1 coarse trim step, there is a non-monotonicity in the combined numbers. Clock adjustment firmware needs to account for this variation.



15 No Write to HFO_LN_FILTER_EN

The clock filter logic has also been changed, so it is no longer necessary to put this statement into the program:

MiscAnalogRegs.CLKTRIM.bit.HFO_LN_FILTER_EN = 0;

The clock filter is handled as part of the trim process, and should not be modified by the customer.

16 Unused bits Removed from DPWM Registers

There are several bits and mode settings which were removed from the DPWM registers. These bits were removed because they were always set to the same values in all applications. All writes to them in initialization codes from older devices can be removed.

17 Sample and Hold Buffer Available on ADC even if Sample and Hold are Not Used

The ADC12 has a small capacitor which is charged at the beginning of every sample. This means that the output impedance of anything driving the ADC has to be relatively low to ensure ADC accuracy. The sample and hold feature requires a larger sample and hold capacitor to be

charged to retain the voltage until the next sampling cycle. This is done to provide simultaneous sampling for functions like power measurement.

This function works exactly the same on the UCD3138A64 as it does on the earlier models of the UCD31xx.

On the new devices, it is possible to use the buffer even if the sample and hold function is not being used. This makes it possible to use 1 of 3 ADC inputs for a voltage source with a higher impedance. To use this, there are several steps:

3. Select the ADC channel which will be buffered by writing to the BYPASS_EN bits in ADCCTRL.
   - 011 = Channel 2
   - 101 = Channel 1
   - 110 = Channel 0
4. Make sure that there are no SEQx_SH bits set
5. Set the ADC_SH_BUFFER_EN bit in ADCTSTCTRL

This should provide a buffer on the selected channel, but no sample and hold functionality.

18 DAC Dither on Sample Trigger

The UCD3138A64 devices add a new bit in the EADCDAC register called DAC_DITHER_ON_SAMPLE. This bit causes the EADC DAC to dither on the sample trigger. Normally the DAC dithers on the frame sync, so dither takes place only once every switching cycle. This means that the dither frequency will be 1/16th the switching frequency. If the sample trigger is set to oversample, the dither could move to 8, 4, or 2 times the switching frequency, providing faster dither.

19 Consolidation of PCM Control Registers

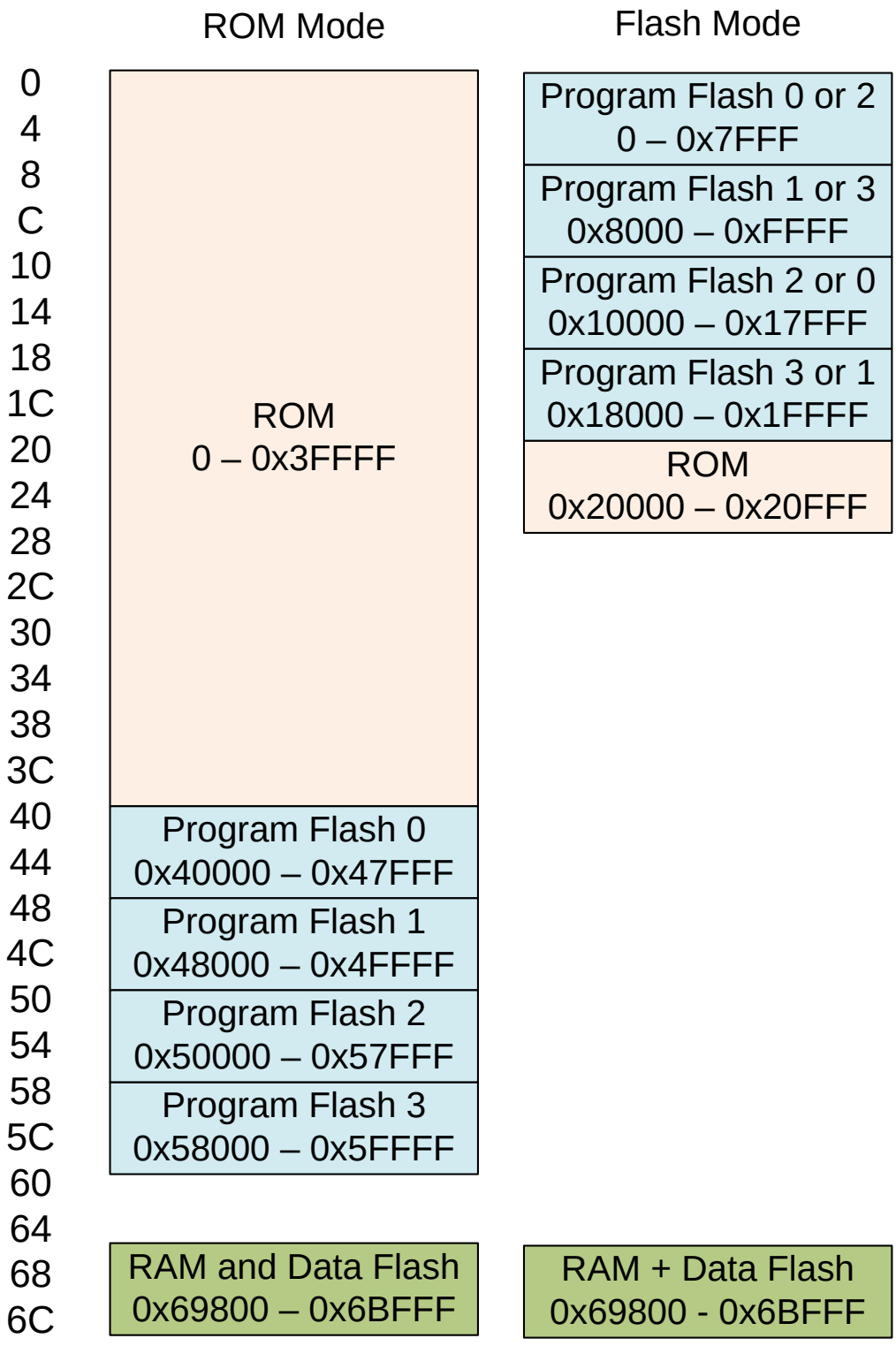
Earlier devices had a PCMCTRL register with only one bitfield in it – FILTER_SEL. The other peak current mode bitfields were in APCMCTRL. Now all the relevant bits are in APCMCTRL, and PCMCTRL has been removed.

20 Enhancements for UCD3138128

The UCD3138128 is very similar to the UCD3138A64. The only difference is the addition of 2 more 32K byte Flash blocks along with the extra registers and boot ROM support for the 2 more blocks. The additional blocks of boot flash are called Block 2 and Block 3.

20.1 *Added Flash Memory*

Blocks 2 and 3 are added after Blocks 0 and 1 in ROM mode. In Flash mode, either blocks 0 and 1 or blocks 2 and 3 can be placed starting at zero. The RAM and peripherals are all at the same addresses as they are on the A64. The Flash mapping options are shown below:



20.2 *Changes to ROM Boot Program*

The ROM changes the response to the version command, and it also changes the handling of flash checksums when it powers up.

20.2.1 ROM Version

The UCD3138128 will return a 0005 as the first half of the version, indicating the device. The first version of the ROM will return a 0001 as the second half of the version, indicating version 1 of the ROM. If other versions of the ROM are produced, the number will increment.

20.2.2 Flash Checksum Handling

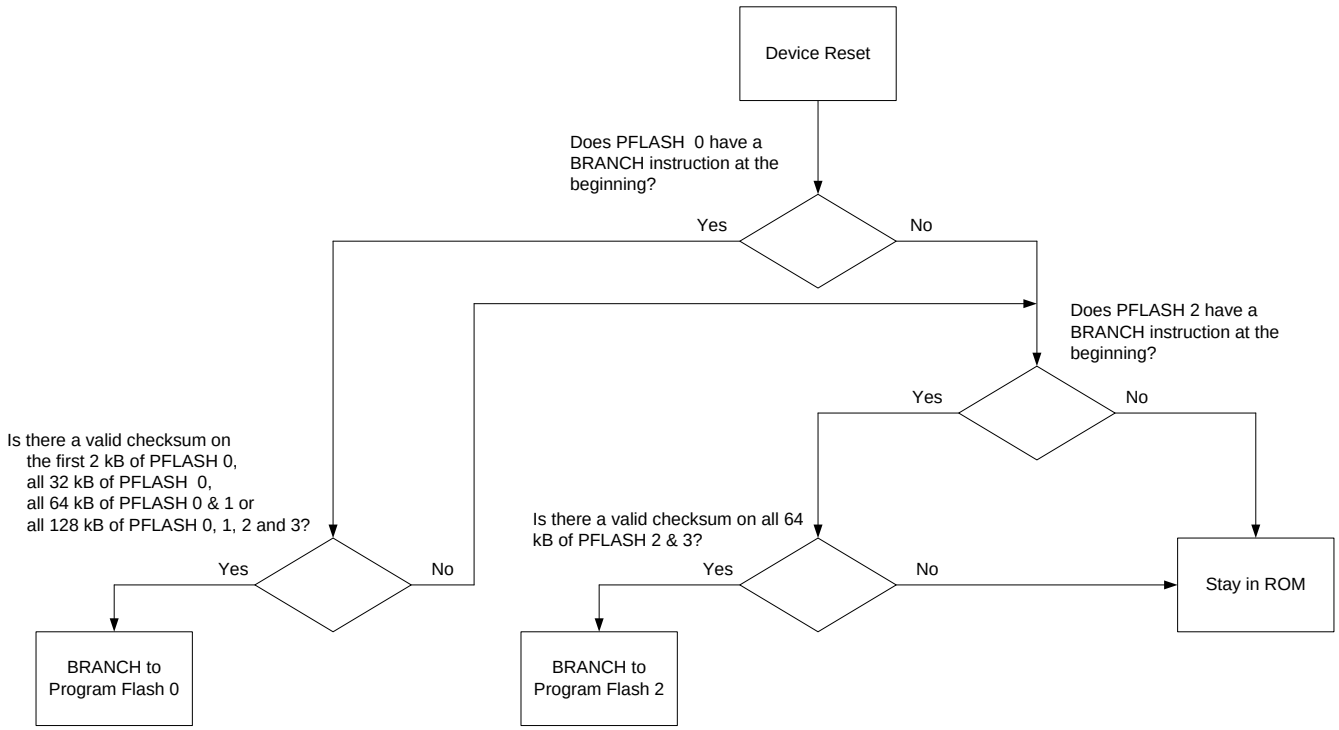
The UCD3138128 does checksums for the first 2K, 32K and 64K of program flash just like the 'A64. It adds checksums for the second 64K and for the full 128K. This provides Boot ROM support for 2 independent versions of the firmware in a single device.

The checksums and their locations are:

0x7f8 – Boot block for Block 0
0x7ff8 – Overall checksum for Block 1
0xfff8 – Overall checksum for a 64K program combining Blocks 1 and 2
0x1fff8 – Overall checksum for a 128K program. This is also used for a 64K program using blocks 2 and 3.

The locations above assume that Block 0 is mapped to location 0, Block 1 is at 0x8000, Block 2 is at 0x10000, and Block 3 is mapped to 0x18000.

Here is a flowchart showing the order in which the ROM verifies the checksums:



The branch instruction check prevents the checksum program from looking at an empty block of memory. Otherwise a block filled with zeroes would pass the checksum test.

When the flowchart says "Branch to Program Flash 0", this means that it puts block 0 at location 0, block 1 at 0x8000, block 2 at 0x10000, and block 3 at 0x18000 and branches to location 0. For ""Branch to Program Flash 2", it puts Block 2 at 0, block 3 at 0x8000, block 0 at 0x10000, and block 1 at 0x18000. It always branches to zero.

The UCD3138 has a PMBus command code 0xF0 which causes the program to execute. On the UCD3138128, the same command causes Blocks 0 and 1 to be placed starting at address 0 and starts execution. A 0xF7 command has been added which puts Blocks 2 and 3 starting at location 0 and starts executing there.

20.3 *Registers Added for '128*

The addition of Blocks 2 and 3 also requires the addition of more registers to control those blocks. Here is a list of the registers:

Register Name	Function	Flash Block Controlled
PFLASHCTRL_2	Program Flash Control Register 2	2
PFLASHCTRL_3	Program Flash Control Register 3	3
MFBAHR18	Memory Fine Base Address High Register 18	2
MFBALR18	Memory Fine Base Address Low Register 18	2
MFBAHR19	Memory Fine Base Address High Register 19	3
MFBALR19	Memory Fine Base Address Low Register 19	3

20.4 *Additional FLASH Keys*

There are additional flash keys for the two new blocks:

#define PROGRAM_FLASH2_INTERLOCK_KEY 0x184219b3
#define PROGRAM_FLASH3_INTERLOCK_KEY 0x5973ef21

These keys need to be written to the DecRegs.FLASHILOCK register before writing or erasing the respective flash blocks.

21 UCD3138A64 Memory Map

This section describes all the registers in the UCD3138A64 peripherals. Changes from the UCD3138064 are marked in green.

21.1 *Loop Mux Registers*

21.1.1 Front End Control 0 Mux Register (FECTRL0MUX)

Address 00120000

Bit Number	13:12	11
Bit Name	NL_SEL	DPWM3_FRAME_SYNC_EN
Access	R/W	R/W
Default	00	0

Bit Number	10	9
Bit Name	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN

Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	DPWM0_FRAME_SYNC_EN	DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bits 13-12: NL_SEL – Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting
- 0 = Filter 0 NL Results used
- 1 = Filter 1 NL Results used
- 2 = Filter 2 NL Results used (Default)

Bit 11: DPWM3_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control
- 0 = DPWM 3 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 3 Frame Sync routed to Front End Control

Bit 10: DPWM2_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control
- 0 = DPWM 2 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 2 Frame Sync routed to Front End Control

Bit 9: DPWM1_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control
- 0 = DPWM 1 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 1 Frame Sync routed to Front End Control

Bit 8: DPWM0_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control
- 0 = DPWM 0 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 0 Frame Sync routed to Front End Control

Bit 7: DPWM3_B_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control
- 0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default)
- 1 = DPWM 3 PWM-B trigger routed to Front End Control

Bit 6: DPWM2_B_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control
- 0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default)
- 1 = DPWM 2 PWM-B trigger routed to Front End Control

Bit 5: DPWM1_B_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control
- 0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default)

1 = DPWM 1 PWM-B trigger routed to Front End Control

Bit 4: DPWM0_B_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-B trigger routed to Front End Control

Bit 3: DPWM3_A_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control

0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-A trigger routed to Front End Control

Bit 2: DPWM2_A_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-A trigger routed to Front End Control

Bit 1: DPWM1_A_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-A trigger routed to Front End Control

Bit 0: DPWM0_A_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-A trigger routed to Front End Control

21.1.2 Front End Control 1 Mux Register (FECTRL1MUX)

Address 00120004

Bit Number	13:12	11
Bit Name	NL_SEL	DPWM3_FRAME_SYNC_EN
Access	R/W	R/W
Default	01	0

Bit Number	10	9
Bit Name	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	DPWM0_FRAME_SYNC_EN	DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bits 13-12: NL_SEL – Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting
- 0 = Filter 0 NL Results used
- 1 = Filter 1 NL Results used
- 2 = Filter 2 NL Results used (Default)

Bit 11: DPWM3_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control
- 0 = DPWM 3 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 3 Frame Sync routed to Front End Control

Bit 10: DPWM2_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control
- 0 = DPWM 2 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 2 Frame Sync routed to Front End Control

Bit 9: DPWM1_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control
- 0 = DPWM 1 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 1 Frame Sync routed to Front End Control

Bit 8: DPWM0_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control
- 0 = DPWM 0 Frame Sync not routed to Front End Control (Default)

1 = DPWM 0 Frame Sync routed to Front End Control

Bit 7: DPWM3_B_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control

0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-B trigger routed to Front End Control

Bit 6: DPWM2_B_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-B trigger routed to Front End Control

Bit 5: DPWM1_B_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-B trigger routed to Front End Control

Bit 4: DPWM0_B_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-B trigger routed to Front End Control

Bit 3: DPWM3_A_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control

0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-A trigger routed to Front End Control

Bit 2: DPWM2_A_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-A trigger routed to Front End Control

Bit 1: DPWM1_A_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-A trigger routed to Front End Control

Bit 0: DPWM0_A_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-A trigger routed to Front End Control

21.1.3 Front End Control 2 Mux Register (FECTRL2MUX)

Address 00120008

Bit Number	13:12	11
Bit Name	NL_SEL	DPWM3_FRAME_SYNC_EN
Access	R/W	R/W
Default	10	0

Bit Number	10	9
Bit Name	DPWM2_FRAME_SYNC_EN	DPWM1_FRAME_SYNC_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	DPWM0_FRAME_SYNC_EN	DPWM3_B_TRIG_EN	DPWM2_B_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	DPWM1_B_TRIG_EN	DPWM0_B_TRIG_EN	DPWM3_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	DPWM2_A_TRIG_EN	DPWM1_A_TRIG_EN	DPWM0_A_TRIG_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bits 13-12: NL_SEL – Configures source of Non-Linear (NL) comparison results used in Automatic Gain Shifting
- 0 = Filter 0 NL Results used
- 1 = Filter 1 NL Results used
- 2 = Filter 2 NL Results used (Default)

Bit 11: DPWM3_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 3 Frame Sync to Front End Control
- 0 = DPWM 3 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 3 Frame Sync routed to Front End Control

Bit 10: DPWM2_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 2 Frame Sync to Front End Control
- 0 = DPWM 2 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 2 Frame Sync routed to Front End Control

Bit 9: DPWM1_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 1 Frame Sync to Front End Control
- 0 = DPWM 1 Frame Sync not routed to Front End Control (Default)
- 1 = DPWM 1 Frame Sync routed to Front End Control

Bit 8: DPWM0_FRAME_SYNC_EN – Enables DPWM Trigger from DPWM 0 Frame Sync to Front End Control
- 0 = DPWM 0 Frame Sync not routed to Front End Control (Default)

1 = DPWM 0 Frame Sync routed to Front End Control

Bit 7: DPWM3_B_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-B to Front End Control

0 = DPWM 3 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-B trigger routed to Front End Control

Bit 6: DPWM2_B_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-B trigger routed to Front End Control

Bit 5: DPWM1_B_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-B trigger routed to Front End Control

Bit 4: DPWM0_B_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-B trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-B trigger routed to Front End Control

Bit 3: DPWM3_A_TRIG_EN – Enables DPWM Trigger from DPWM 3 PWM-A to Front End Control

0 = DPWM 3 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 3 PWM-A trigger routed to Front End Control

Bit 2: DPWM2_A_TRIG_EN – Enables DPWM Trigger from DPWM 2 PWM-B to Front End Control

0 = DPWM 2 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 2 PWM-A trigger routed to Front End Control

Bit 1: DPWM1_A_TRIG_EN – Enables DPWM Trigger from DPWM 1 PWM-B to Front End Control

0 = DPWM 1 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 1 PWM-A trigger routed to Front End Control

Bit 0: DPWM0_A_TRIG_EN – Enables DPWM Trigger from DPWM 0 PWM-B to Front End Control

0 = DPWM 0 PWM-A trigger not routed to Front End Control (Default)
1 = DPWM 0 PWM-A trigger routed to Front End Control

21.1.4 Sample Trigger Control Register (SAMPTRIGCTRL)

Address 0012000C

Bit Number	11	10	9
Bit Name	FE2_TRIG_DPWM3_EN	FE2_TRIG_DPWM2_EN	FE2_TRIG_DPWM1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	8	7	6
Bit Name	FE2_TRIG_DPWM0_EN	FE1_TRIG_DPWM3_EN	FE1_TRIG_DPWM2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	FE1_TRIG_DPWM1_EN	FE1_TRIG_DPWM0_EN	FE0_TRIG_DPWM3_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	FE0_TRIG_DPWM2_EN	FE0_TRIG_DPWM1_EN	FE0_TRIG_DPWM0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 11: FE2_TRIG_DPWM3_EN – Enables Sample Trigger from DPWM 3 to Front End Control 2
0 = DPWM 3 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 3 Sample Trigger routed to Front End Control 2
Bit 10: FE2_TRIG_DPWM2_EN – Enables Sample Trigger from DPWM 2 to Front End Control 2
0 = DPWM 2 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 2 Sample Trigger routed to Front End Control 2
Bit 9: FE2_TRIG_DPWM1_EN – Enables Sample Trigger from DPWM 1 to Front End Control 2
0 = DPWM 1 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 1 Sample Trigger routed to Front End Control 2
Bit 8: FE2_TRIG_DPWM0_EN – Enables Sample Trigger from DPWM 0 to Front End Control 2
0 = DPWM 0 Sample Trigger not routed to Front End Control 2 (Default)
1 = DPWM 0 Sample Trigger routed to Front End Control 2
Bit 7: FE1_TRIG_DPWM3_EN – Enables Sample Trigger from DPWM 3 to Front End Control 1
0 = DPWM 3 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 3 Sample Trigger routed to Front End Control 1
Bit 6: FE1_TRIG_DPWM2_EN – Enables Sample Trigger from DPWM 2 to Front End Control 1
0 = DPWM 2 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 2 Sample Trigger routed to Front End Control 1
Bit 5: FE1_TRIG_DPWM1_EN – Enables Sample Trigger from DPWM 1 to Front End Control 1

0 = DPWM 1 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 1 Sample Trigger routed to Front End Control 1

Bit 4: FE1_TRIG_DPWM0_EN – Enables Sample Trigger from DPWM 0 to Front End Control 1
0 = DPWM 0 Sample Trigger not routed to Front End Control 1 (Default)
1 = DPWM 0 Sample Trigger routed to Front End Control 1

Bit 3: FE0_TRIG_DPWM3_EN – Enables Sample Trigger from DPWM 3 to Front End Control 0
0 = DPWM 3 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 3 Sample Trigger routed to Front End Control 0

Bit 2: FE0_TRIG_DPWM2_EN – Enables Sample Trigger from DPWM 2 to Front End Control 0
0 = DPWM 2 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 2 Sample Trigger routed to Front End Control 0

Bit 1: FE0_TRIG_DPWM1_EN – Enables Sample Trigger from DPWM 1 to Front End Control 0
0 = DPWM 1 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 1 Sample Trigger routed to Front End Control 0

Bit 0: FE0_TRIG_DPWM0_EN – Enables Sample Trigger from DPWM 0 to Front End Control 0
0 = DPWM 0 Sample Trigger not routed to Front End Control 0 (Default)
1 = DPWM 0 Sample Trigger routed to Front End Control 0

21.1.5 External DAC Control Register (EXTDACCTRL)

Address 00120010

Bit Number	26:24	23:19	18:16	15:11	10:8
Bit Name	DAC2_SEL	RESERVED	DAC1_SEL	RESERVED	DAC0_SEL
Access	R/W	-	R/W	-	R/W
Default	000	0_0000	000	0_0000	000

Bit Number	7:3	2	1	0
Bit Name	RESERVED	EXT_DAC2_EN	EXT_DAC1_EN	EXT_DAC0_EN
Access	-	R/W	R/W	R/W
Default	0_0000	0	0	0

Bits 26-24: DAC2_SEL – Configures DAC 2 setpoint in External DAC Mode
0 = DAC 0 Setpoint Selected (Default)
1 = DAC 1 Setpoint Selected
3 = Output of Constant Power Module Selected
4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected

Bits 23-19: RESERVED – Unused bits

Bits 18-16: DAC1_SEL – Configures DAC 1 setpoint in External DAC Mode
0 = DAC 0 Setpoint Selected (Default)
2 = DAC 2 Setpoint Selected
3 = Output of Constant Power Module Selected
4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected

Bits 15-11: RESERVED – Unused bits

Bits 10-8: DAC0_SEL – Configures DAC 0 setpoint in External DAC Mode
1 = DAC 1 Setpoint Selected

2 = DAC 2 Setpoint Selected
3 = Output of Constant Power Module Selected
4 = Filter 0 Output Selected
5 = Filter 1 Output Selected
6 = Filter 2 Output Selected

Bits 7-3: RESERVED – Unused bits

Bit 2: EXT_DAC2_EN – External DAC 2 Mode Enable
0 = External DAC Mode disabled. DAC 2 setpoint driven from Front End Control Module (Default)
1 = External DAC Mode enabled, DAC 2 setpoint driven by DAC2_SEL configuration

Bit 1: EXT_DAC1_EN – External DAC 1 Mode Enable
0 = External DAC Mode disabled. DAC 1 setpoint driven from Front End Control Module (Default)
1 = External DAC Mode enabled, DAC 1 setpoint driven by DAC1_SEL configuration

Bit 0: EXT_DAC0_EN – External DAC 0 Mode Enable
0 = External DAC Mode disabled. DAC 0 setpoint driven from Front End Control Module (Default)
1 = External DAC Mode enabled, DAC 0 setpoint driven by DAC0_SEL configuration

21.1.6 Filter Mux Register (FILTERMUX)

Address 00120014

Bit Number	29:28	27:26	25:24
Bit Name	FILTER2_KCOMP_SEL	FILTER1_KCOMP_SEL	FILTER0_KCOMP_SEL
Access	R/W	R/W	R/W
Default	00	00	00

Bit Number	23:19	18	17	16
Bit Name	RESERVED	FILTER2_FFWD_SEL	FILTER1_FFWD_SEL	FILTER0_FFWD_SEL
Access	R/W	R/W	R/W	R/W
Default	0_0000	0	0	0

Bit Number	15:14	13:12	11:10	9:8
Bit Name	RESERVED	FILTER2_PER_SEL	FILTER1_PER_SEL	FILTER0_PER_SEL
Access	R/W	R/W	R/W	R/W
Default	00	00	00	00

Bit Number	7:6	5:4	3:2	1:0
Bit Name	RESERVED	FILTER2_FE_SEL	FILTER1_FE_SEL	FILTER0_FE_SEL
Access	-	R/W	R/W	R/W
Default	00	10	01	00

Bits 29-28: FILTER2_KCOMP_SEL – Selects KComp value routed to Filter 2 Module
0 = KComp 0 Value Selected (Default)
1 = KComp 1 Value Selected
2 = KComp 2 Value Selected
Bits 27-26: FILTER1_KCOMP_SEL – Selects KComp value routed to Filter 1 Module
0 = KComp 0 Value Selected (Default)
1 = KComp 1 Value Selected
2 = KComp 2 Value Selected
Bits 25-24: FILTER0_KCOMP_SEL – Selects KComp value routed to Filter 0 Module
0 = KComp 0 Value Selected (Default)
1 = KComp 1 Value Selected
2 = KComp 2 Value Selected
Bits 23-19: RESERVED – Unused bits
Bit 18: FILTER2_FFWD_SEL – Configures Feedforward value routed to Filter 2 Module
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
Bit 17: FILTER1_FFWD_SEL – Configures Feedforward value routed to Filter 1 Module
0 = Filter 0 Output Selected (Default)
1 = Filter 2 Output Selected
Bit 16: FILTER0_FFWD_SEL – Configures Feedforward value routed to Filter 0 Module
0 = Filter 1 Output Selected (Default)
1 = Filter 2 Output Selected
Bits 15-14: RESERVED – Unused bits
Bits 13-12: FILTER2_PER_SEL – Selects source of switching cycle period for Filter 2 Module
0 = DPWM 0 Switching Period (Default)
1 = DPWM 1 Switching Period
2 = DPWM 2 Switching Period

3 = DPWM 3 Switching Period

Bits 11-10: FILTER1_PER_SEL – Selects source of switching cycle period for Filter 1 Module

0 = DPWM 0 Switching Period (Default)
1 = DPWM 1 Switching Period
2 = DPWM 2 Switching Period
3 = DPWM 3 Switching Period

Bits 9-8: FILTER0_PER_SEL – Selects source of switching cycle period for Filter 0 Module

0 = DPWM 0 Switching Period (Default)
1 = DPWM 1 Switching Period
2 = DPWM 2 Switching Period
3 = DPWM 3 Switching Period

Bits 7-6: RESERVED – Unused bits

Bits 5-4: FILTER2_FE_SEL – Selects which Front End Module provides data for Filter 2 Module

0 = Front End Module 0 provides data to Filter
1 = Front End Module 1 provides data to Filter
2 = Front End Module 2 provides data to Filter (Default)

Bits 3-2: FILTER1_FE_SEL – Selects which Front End Module provides data for Filter 1 Module

0 = Front End Module 0 provides data to Filter
1 = Front End Module 1 provides data to Filter (Default)
2 = Front End Module 2 provides data to Filter

Bits 1-0: FILTER0_FE_SEL – Selects which Front End Module provides data for Filter 0 Module

0 = Front End Module 0 provides data to Filter (Default)
1 = Front End Module 1 provides data to Filter
2 = Front End Module 2 provides data to Filter

21.1.7 Filter KComp A Register (FILTERKCOMPA)

Address 00120018

Bit Number	29:16	15:14	13:0
Bit Name	KCOMP1	RESERVED	KCOMP0
Access	R/W	-	R/W
Default	00_0000_0000_0000	00	00_0000_0111_1101

Bits 29-16: KCOMP1 – 14-bit value used in filter output calculations replacing the DPWM switching period value
Bits 15-14: RESERVED – Unused bits
Bits 13-0: KCOMP0 – 14-bit value used in filter output calculations replacing the DPWM switching period value

21.1.8 Filter KComp B Register (FILTERKCOMPB)

Address 0012001C

Bit Number	13:0
Bit Name	KCOMP2
Access	R/W
Default	00_0000_0000_0000

Bits 13-0: KCOMP2 – 14-bit value used in filter output calculations replacing the DPWM switching period value

21.1.9 DPWM Mux Register (DPWMMUX)

Address 00120020

Bit Number	31:30	29:28
Bit Name	DPWM3_SYNC_FET_SEL	DPWM2_SYNC_FET_SEL
Access	R/W	R/W
Default	00	00

Bit Number	27:26	25:24
Bit Name	DPWM1_SYNC_FET_SEL	DPWM0_SYNC_FET_SEL
Access	R/W	R/W
Default	00	00

Bit Number	23:20	19:18	17:16
Bit Name	RESERVED	DPWM3_SYNC_SEL	DPWM2_SYNC_SEL
Access	-	R/W	R/W
Default	0000	00	00

Bit Number	15:14	13:12	11:9
Bit Name	DPWM1_SYNC_SEL	DPWM0_SYNC_SEL	DPWM3_FILTER_SEL
Access	R/W	R/W	R/W
Default	00	00	010

Bit Number	8:6	5:3	2:0
Bit Name	DPWM2_FILTER_SEL	DPWM1_FILTER_SEL	DPWM0_FILTER_SEL
Access	R/W	R/W	R/W
Default	010	001	000

Bits 31-30: DPWM3_SYNC_FET_SEL – Selects Ramp source for DPWM3 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected
Bits 29-28: DPWM2_SYNC_FET_SEL – Selects Ramp source for DPWM2 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected
Bits 27-26: DPWM1_SYNC_FET_SEL – Selects Ramp source for DPWM1 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected
Bits 25-24: DPWM0_SYNC_FET_SEL – Selects Ramp source for DPWM0 PWM-B SyncFET soft on/off
0 = Front End 0 Ramp output selected (Default)
1 = Front End 1 Ramp output selected
2 = Front End 2 Ramp output selected
Bits 23-20: RESERVED – Unused bits
Bits 19-18: DPWM3_SYNC_SEL – Selects Master Sync for DPWM 3 when DPWM 3 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 17-16: DPWM2_SYNC_SEL – Selects Master Sync for DPWM 2 when DPWM 2 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 15-14: DPWM1_SYNC_SEL – Selects Master Sync for DPWM 1 when DPWM 1 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 13-12: DPWM0_SYNC_SEL – Selects Master Sync for DPWM 0 when DPWM 0 configured in slave mode
0 = DPWM 0 Sync (Default)
1 = DPWM 1 Sync
2 = DPWM 2 Sync
3 = DPWM 3 Sync
Bits 11-9: DPWM3_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 3
0 = Filter 0 Output Selected (Default)

1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register

Bits 8-6: DPWM2_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 2

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register

Bits 5-3: DPWM1_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 1

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register

Bits 2-0: DPWM0_FILTER_SEL – Selects source of duty cycle/resonant period for DPWM Module 0

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Constant Power Module Selected
4 = DPWM_ON_TIME value from Light Load Control Register

21.1.10 Constant Power Control Register (CPCTRL)

Address 00120024

Bit Number	16	15	14	13
Bit Name	CPCC_INT_EN	DAC_COMP_EN	FW_DIVISOR_EN	LOWER_COMP_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	12	11:10	9:8	7:5
Bit Name	VLOOP_FREEZE_EN	VLOOP_SEL	CLOOP_SEL	THRESH_SEL
Access	R/W	R/W	R/W	R/W
Default	0	00	00	000

Bit Number	4:3	2:1	0
Bit Name	DIVISOR_SEL	CPCC_CONFIG	CPCC_EN
Access	R/W	R/W	R/W
Default	00	0	0

Bit 16: CPCC_INT_EN – Constant Power/Constant Current Interrupt Enable
0 = Interrupt disabled on mode switches (Default)
1 = Interrupt enabled on mode switches

Bit 15: DAC_COMP_EN – Enables comparison of DAC Setpoint and quotient of Max Power/Sense Current in Loop Switching Mode. Minimum of DAC setpoint and calculated quotient sets voltage loop setpoint in Constant Voltage and Constant Power modes
0 = Operating Mode controls Voltage Loop DAC Setpoint (Default)
1 = Minimum of DAC setpoint and calculated quotient used as Voltage Loop DAC Setpoint

Bit 14: FW_DIVISOR_EN – Enables Firmware value for divisor in Constant Power calculations
0 = Divisor selected by **DIVISOR_SEL** (Bits 7:6) (Default)
1 = Divisor driven by Firmware Current Register

Bit 13: LOWER_COMP_EN – Enables output of lowest duty from current or voltage loop when Constant Power/Constant Current module controls loop output
0 = Loop output controlled by mode selection, voltage loop selected in constant voltage and constant power mode, current loop selected in constant current mode (Default)
1 = Loop output controlled by lowest duty from voltage or current loops

Bit 12: VLOOP_FREEZE_EN – Enables freezing of Voltage Loop Integrator when current loop selected in Loop Switching configuration
0 = Freezing of Voltage Loop Integrator disabled (Default)
1 = Freezing of Voltage Loop Integrator enabled

Bits 11-10: VLOOP_SEL – Configures voltage loop for loop switching mode
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected

Bits 9-8: CLOOP_SEL – Configures current loop for loop switching mode
0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected

Bits 7-5: THRESH_SEL – Configures input threshold selected for use in Constant Power comparison

0 = Filter 0 Output Selected (Default)
1 = Filter 1 Output Selected
2 = Filter 2 Output Selected
3 = Front End 0 Absolute Value Data Selected
4 = Front End 1 Absolute Value Data Selected
5 = Front End 2 Absolute Value Data Selected

Bits 4-3: DIVISOR_SEL – Configures value used for divisor in Constant Power calculations

0 = Front End 0 Absolute Value Data Selected (Default)
1 = Front End 1 Absolute Value Data Selected
2 = Front End 2 Absolute Value Data Selected

Bit 2-1: CPCC_CONFIG – Controls Constant Power/Constant Current module configuration

0 = Average Current Mode (Default)
1 = Constant Power Module controls selection of voltage/current loop
2 = Constant Power Module error switching mode

Bit 0: CPCC_EN – Constant Power Constant/Current Module Enable

0 = Constant Power/Constant Current Module disabled (Default)
1 = Constant Power/Constant Current Module enabled

21.1.11 Constant Power Nominal Threshold Register (CPNOM)

Address 00120028

Bit Number	25:16	15:10	9:0
Bit Name	NOM_CURRENT_UPPER	RESERVED	NOM_CURRENT_LOWER
Access	R/W	-	R/W
Default	00_0000_0000	00_0000	00_0000_0000

Bits 25-16: NOM_CURRENT_UPPER – Configures I_{NOM} value used in Constant Power/Constant Current Calculations, when sensed value exceeds NOM_CURRENT_UPPER in Constant Voltage mode, setpoint will switch to Constant Power mode

Bits 15-10: RESERVED – Unused Bits

Bits 9-0: NOM_CURRENT_LOWER – Configures I_{NOM} value used in Constant Power/Constant Current Calculations, when sensed value falls below NOM_CURRENT_LOWER in Constant Power mode, setpoint will switch to Constant Voltage mode

21.1.12 Constant Power Max Threshold Register (CPMAX)

Address 0012002C

Bit Number	25:16	15:10	9:0
Bit Name	MAX_CURRENT_UPPER	RESERVED	MAX_CURRENT_LOWER
Access	R/W	-	R/W
Default	00_0000_0000	00_0000	00_0000_0000

Bits 25-16: MAX_CURRENT_UPPER – Configures I_{MAX} value used in Constant Power/Constant Current Calculations, when sensed value exceeds MAX_CURRENT_UPPER in Constant Power mode, setpoint will switch to Max Current mode

Bits 15-10: RESERVED – Unused Bits

Bits 9-0: MAX_CURRENT_LOWER – Configures I_{MAX} value used in Constant Power/Constant Current Calculations, when sensed value falls below

MAX_CURRENT_LOWER in Max Current mode, setpoint will switch to Constant Power mode

21.1.13 Constant Power Configuration Register (CPCONFIG)

Address 00120030

Bit Number	25:16	15:10	9:0
Bit Name	MAX_CURRENT	RESERVED	NOM_VOLTAGE
Access	R/W	-	R/W
Default	00_0000_0000	00_0000	00_0000_0000

Bits 25-16: MAX_CURRENT – Configures I_{MAX} setpoint used in Constant Power/Constant Current Calculations in Max Current mode
Bits 15-10: RESERVED – Unused Bits
Bits 9-0: NOM_VOLTAGE – Configures V_{NOM} setpoint used in Constant Power/Constant Current Calculations in Constant Voltage mode (Loop Oring configuration selected)

21.1.14 Constant Power Max Power Register (CPMAXPWR)

Address 00120034

Bit Number	19:0
Bit Name	MAX_POWER
Access	R/W
Default	0000_0000_0000_0000_0000

Bits 19-0: MAX_POWER – Configures P_{MAX} value used in Constant Power/Constant Current calculations in Constant Power mode

21.1.15 Constant Power Integrator Threshold Register (CPINTTHRESH)

Address 00120038

Bit Number	23:0
Bit Name	INT_THRESH
Access	R/W
Default	0000_0000_0000_0000_0000

Bits 23-0: INT_THRESH – 24-bit signed value added to Current Loop Duty value to determine when to freeze Current Loop Integrator

21.1.16 Constant Power Firmware Divisor Register (CPFWDIVISOR)

Address 0012003C

Bit Number	9:0
Bit Name	FW_DIVISOR
Access	R/W
Default	00_0000_0000

Bits 9-0: FW_DIVISOR– 10-bit value used in Constant Power calculation when firmware value is selected in Bit 17 of Constant Power Control Register

21.1.17 Constant Power Status Register (CPSTAT)

Address 00120040

Bit Number	8	7	6
Bit Name	CONSTANT_CUR	CONSTANT_PWR	CONSTANT_VOLT
Access	R	R	R
Default	-	-	-

Bit Number	5	4	3
Bit Name	CC_TO_CV_INT	CV_TO_CC_INT	CC_TO_CP_INT
Access	R	R	R
Default	-	-	-

Bit Number	2	1	0
Bit Name	CP_TO_CC_INT	CP_TO_CV_INT	CV_TO_CP_INT
Access	R	R	R
Default	-	-	-

Bit 8: CONSTANT_CUR – Constant Current Mode Indication
0 = Constant Current Mode not enabled
1 = Constant Current Mode enabled
Bit 7: CONSTANT_PWR – Constant Power Mode Indication
0 = Constant Power Mode not enabled
1 = Constant Power Mode enabled
Bit 6: CONSTANT_VOLT – Constant Voltage Mode Indication
0 = Constant Voltage Mode not enabled
1 = Constant Voltage Mode enabled
Bit 5: CC_TO_CV_INT – Constant Current Mode to Constant Voltage Mode latched status, cleared on read
0 = No transition from Constant Current to Constant Voltage detected
1 = Transition from Constant Current to Constant Voltage detected
Bit 4: CV_TO_CC_INT – Constant Voltage Mode to Constant Current Mode latched status, cleared on read
0 = No transition from Constant Voltage to Constant Current detected
1 = Transition from Constant Voltage to Constant Current detected
Bit 3: CC_TO_CP_INT – Constant Current Mode to Constant Power Mode latched status, cleared on read
0 = No transition from Constant Current to Constant Power detected
1 = Transition from Constant Current to Constant Power detected
Bit 2: CP_TO_CC_INT – Constant Power Mode to Constant Current Mode latched status, cleared on read
0 = No transition from Constant Power to Constant Current detected
1 = Transition from Constant Power to Constant Current detected
Bit 1: CP_TO_CV_INT – Constant Power Mode to Constant Voltage Mode latched status, cleared on read
0 = No transition from Constant Power to Constant Voltage detected
1 = Transition from Constant Power to Constant Voltage detected
Bit 0: CV_TO_CP_INT – Constant Voltage Mode to Constant Power Mode latched status, cleared on read
0 = No transition from Constant Voltage to Constant Power detected
1 = Transition from Constant Voltage to Constant Power detected

21.1.18 Cycle Adjustment Control Register (CYCADJCTRL)

Address 00120044

Bit Number	9:7	6:5
Bit Name	CYC_ADJ_GAIN	CYC_ADJ_SYNC
Access	R/W	R/W
Default	000	00

Bit Number	4:3	2:1	0
Bit Name	SECOND_SAMPLE_SEL	FIRST_SAMPLE_SEL	CYC_ADJ_EN
Access	R/W	R/W	R/W
Default	00	00	0

Bits 9-7: CYC_ADJ_GAIN – Configures gain of Cycle Adjustment calculation
- 0 = 1x gain (Default)
- 1 = 2x gain
- 2 = 4x gain
- 3 = 8x gain
- 4 = 16x gain
- 5 = 32x gain
- 6 = 64x gain
- 7 = 128x gain

Bits 6-5: CYC_ADJ_SYNC – Selects which DPWM trigger synchronizes cycle adjustment calculation, first 2 samples after receipt of DPWM trigger will be used for Cycle Adjustment Calculation.
- 0 = DPWM-0 frame sync trigger selected (Default)
- 1 = DPWM-1 frame sync trigger selected
- 2 = DPWM-2 frame sync trigger selected
- 3 = DPWM-3 frame sync trigger selected

Bits 4-3: SECOND_SAMPLE_SEL – Configures Front End Module Data used for Second Sample of Cycle Adjustment Calculation
- 0 = Front End Module 0 Error Data selected (Default)
- 1 = Front End Module 1 Error Data selected
- 2 = Front End Module 2 Error Data selected

Bits 2-1: FIRST_SAMPLE_SEL – Configures Front End Module Data used for First Sample of Cycle Adjustment Calculation
- 0 = Front End Module 0 Error Data selected (Default)
- 1 = Front End Module 1 Error Data selected
- 2 = Front End Module 2 Error Data selected

Bit 0: CYC_ADJ_EN – Cycle Adjustment Calculation Enable
- 0 = Cycle Adjustment Calculation disabled (Default)
- 1 = Cycle Adjustment Calculation enabled

21.1.19 Cycle Adjustment Limit Register (CYCADJLIM)

Address 00120048

Bit Number	28:16	15:13	12:0
Bit Name	CYC_ADJ_UPPER_LIMIT	RESERVED	CYC_ADJ_LOWER_LIM
Access	R/W	-	R/W
Default	0_0000_0000_0000	000	0_0000_0000_0000

Bits 28-16: CYC_ADJ_UPPER_LIMT – Cycle Adjustment Calculation signed upper limit value, output of Cycle Adjustment Calculation is clamped at the upper limit, if calculated result exceeds the upper limit. LSB resolution equals High Frequency Oscillator period/16.
Bits 15-13: RESERVED – Unused Bits
Bits 12-0: CYC_ADJ_LOWER_LIMT – Cycle Adjustment Calculation signed lower limit value, output of Cycle Adjustment Calculation is clamped at the lower limit, if calculated result falls below the lower limit. LSB resolution equals High Frequency Oscillator period/16.

21.1.20 Cycle Adjustment Status Register (CYCADJSTAT)

Address 0012004C

Bit Number	28:16	15:10	9:0
Bit Name	CYC_ADJ_CALC	RESERVED	CYC_ADJ_ERROR
Access	R	-	R
Default	-	00_0000	-

Bits 28-16: CYC_ADJ_CALC – 13-bit signed value representing calculated Cycle Adjustment provided to DPWM module based on first 2 error samples
Bits 15-10: RESERVED – Unused Bits
Bits 9-0: CYC_ADJ_ERROR – 10-bit signed value representing calculated error of the first 2 error samples received

21.1.21 Global Enable Register (GLBEN)

Address 00120050

Bit Number	10	9	8	7:4
Bit Name	FE_CTRL2_EN	FE_CTRL1_EN	FE_CTRL0_EN	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	0000

Bit Number	3	2	1	0
Bit Name	DPWM3_EN	DPWM2_EN	DPWM1_EN	DPWM0_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 10: FE_CTRL2_EN – Global Firmware Enable for Front End Control 2 Module
0 = Front End Control 2 Module Disabled (Default)
1 = Front End Control 2 Module Enabled
Bit 9: FE_CTRL1_EN – Global Firmware Enable for Front End Control 1 Module
0 = Front End Control 1 Module Disabled (Default)
1 = Front End Control 1 Module Enabled
Bit 8: FE_CTRL0_EN – Global Firmware Enable for Front End Control 0 Module

0 = Front End Control 0 Module Disabled (Default)
1 = Front End Control 0 Module Enabled

Bits 7-4: RESERVED – Unused Bits

Bit 3: DPWM3_EN – Global Firmware Enable for DPWM 3 Module
0 = DPWM 3 Module Disabled (Default)
1 = DPWM 3 Module Enabled

Bit 2: DPWM2_EN – Global Firmware Enable for DPWM 2 Module
0 = DPWM 2 Module Disabled (Default)
1 = DPWM 2 Module Enabled

Bit 1: DPWM1_EN – Global Firmware Enable for DPWM 1 Module
0 = DPWM 1 Module Disabled (Default)
1 = DPWM 1 Module Enabled

Bit 0: DPWM0_EN – Global Firmware Enable for DPWM 0 Module
0 = DPWM 0 Module Disabled (Default)
1 = DPWM 0 Module Enabled

21.1.22 PWM Global Period Register (PWMGLBPRD)

Address 00120054

Bit Number	17:4	3:0
Bit Name	PRD	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bits 17-4: PRD – Global PWM Period value, overriding DPWM Period settings when global PWM period is selected within each DPWM module

Bits 3-0: RESERVED – Unused Bits

21.1.23 Sync Control Register (SYNCCTRL)

Address 00120058

Bit Number	5	4:2	1	0
Bit Name	SYNC_IN	SYNC_MUX_SEL	SYNC_OUT	SYNC_DIR
Access	R	R/W	R/W	R/W
Default	-	000	1	1

Bit 5: SYNC_IN – Value of Sync pin
0 = Logic level low present on Sync pin
1 = Logic level high present on Sync pin
Bits 4-2: SYNC_MUX_SEL – Selects which module controls Sync pin output
000 = DPWM 0 Sync Output (Default)
001 = DPWM 1 Sync Output
010 = DPWM 2 Sync Output
011 = DPWM 3 Sync Output
100 = Value from SYNC_OUT (Bit 1)
101 = Value from CLKOUT signal in TSAR Module (See Section 15.1)
110 = Low-Frequency Oscillator Clock Output
111 = Driven low
Bit 1: SYNC_OUT – Configure output value for Sync pin, if used as an output
0 = Sync pin driven low in output mode
1 = Sync pin driven high in output mode (Default)
Bit 0: SYNC_DIR – Configure direction of Sync pin
0 = Sync pin configured as an output pin
1 = Sync pin configured as an input pin (Default)

21.1.24 Light Load Control Register (LLCTRL)

Address 0012005C

Bit Number	25:8	7:4	3	2:1	0
Bit Name	DPWM_ON_TIME	RESERVED	CYCLE_CNT_EN	LL_FILTER_SEL	LL_EN
Access	R/W	-	R/W	R/W	R/W
Default	00_0000_0000_0000_0000	0000	0	00	0

Bits 25-8: DPWM_ON_TIME – DPWM pulse width used for EADC-based light load mode operation, when selected Filter data exceeds TURN_ON_THRESH value
Bits 7-3: RESERVED – Unused Bits
Bit 3: CYCLE_CNT_EN – Enables Switching Cycle Counter for enabling constant pulse widths when configured in Light Load operation
0 = Switching Cycle Counter disabled (Default)
1 = Switching Cycle Counter enabled
Bits 2-1: LL_FILTER_SEL – Configures source of filter data for Light Load comparisons
0 = Filter 0 data selected (Default)
1 = Filter 1 data selected
2 = Filter 2 data selected
Bit 0: LL_EN – Light Load Mode Enable
0 = Mode disabled (Default)
1 = Mode enabled

21.1.25 Light Load Enable Threshold Register (LLENTHRESH)

Address 00120060

Bit Number	31:24	23:18	17:0
Bit Name	CYCLE_CNT_THRESH	RESERVED	TURN_ON_THRESH
Access	R/W	-	R/W
Default	0000_0000	0000_00	00_0000_0000_0000_0000

Bits 31-24: CYCLE_CNT_THRESH – Switching Cycle threshold where constant width DPWM pulses are enabled when number of switching cycles without pulses exceeds threshold
Bits 23-18: RESERVED – Unused Bits
Bits 17-0: TURN_ON_THRESH – Filter data threshold where constant width DPWM pulses are enabled when filter data exceeds threshold

21.1.26 Light Load Disable Threshold Register (LLDISTHRESH)

Address 00120064

Bit Number	17:0
Bit Name	TURN_OFF_THRESH
Access	R/W
Default	00_0000_0000_0000_0000

Bits 17-0: TURN_OFF_THRESH – Filter data threshold where constant width DPWM pulses are disabled when filter data falls below threshold

21.1.27 Analog Peak Current Mode Control Register (APCMCTRL)

Address 00120068

Bit Number	5:4	3	2:1	0
Bit Name	PCM_FILTER_SEL	PCM_LATCH_EN	PCM_FE_SEL	PCM_EN
Access	R/W	R/W	R/W	R/W
Default	00	0	00	0

Bits 5-4: PCM_FILTER_SEL – Selects source of Peak Current Slope Compensation Ramp Start
0 = Filter 0 data selected (Default)
1 = Filter 1 data selected
2 = Filter 2 data selected
3 = Constant Power/Constant Current data selected
Bit 3: PCM_LATCH_EN – Enables latching of Peak Current Flag to end of frame
0 = PCM Flag is not latched to end of PCM Frame (Default)
1 = PCM Flag is latched to end of PCM Frame
Bits 2-1: PCM_FE_SEL – Selects source of Front End Comparator output for Analog Peak Current Mode Control
0 = Front End Control 0 Comparator output selected (Default)
1 = Front End Control 1 Comparator output selected
2 = Front End Control 2 Comparator output selected
Bit 0: PCM_EN – Analog Peak Current Mode Control Module Enable
0 = Analog Peak Current Mode Control Module disabled (Default)
1 = Analog Peak Current Mode Control Module enabled

21.2 *Fault Mux Registers*

21.2.1 Analog Comparator Control 0 Register (ACOMPCTRL0)

Address 00130000

Bit Number	30:24	23:22	21:19	18
Bit Name	ACOMP_B_THRESH	RESERVED	ACOMP_B_SEL	ACOMP_B_POL
Access	R/W	-	R/W	R/W
Default	000_0000	00	000	1

Bit Number	17	16:15	14:8	7:6
Bit Name	ACOMP_B_INT_EN	RESERVED	ACOMP_A_THRESH	RESERVED
Access	R/W	-	R/W	-
Default	0	00	000_0000	00

Bit Number	5:3	2	1	0
Bit Name	ACOMP_A_SEL	ACOMP_A_POL	ACOMP_A_INT_EN	ACOMP_EN
Access	R/W	R/W	R/W	R/W
Default	000	1	0	0

Bits 30-24: ACOMP_B_THRESH – Configures Analog Comparator B Threshold value
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bits 23-22: RESERVED – Unused bits
Bits 21-19: ACOMP_B_SEL – Configures Analog Comparator B Threshold
0 = Analog Comparator B Threshold set by ACOMP_B_THRESH (Default)
1 = Analog Comparator B Threshold set by Comparator Ramp 0
2 = Analog Comparator B Threshold set by Filter 0 Output
3 = Analog Comparator B Threshold set by Filter 1 Output
4 = Analog Comparator B Threshold set by Filter 2 Output
Bit 18: ACOMP_B_POL – Analog Comparator B Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)
Bit 17: ACOMP_B_INT_EN – Analog Comparator B Interrupt Enable
0 = Disables Analog Comparator B Interrupt generation (Default)
1 = Enables Analog Comparator B Interrupt generation
Bits 16-15: RESERVED – Unused bits
Bits 14-8: ACOMP_A_THRESH – Configures Analog Comparator A Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bits 7-6: RESERVED – Unused bits
Bits 5-3: ACOMP_A_SEL – Configures Analog Comparator A Threshold
0 = Analog Comparator A Threshold set by ACOMP_A_THRESH (Default)
1 = Analog Comparator A Threshold set by Comparator Ramp 0
2 = Analog Comparator A Threshold set by Filter 0 Output
3 = Analog Comparator A Threshold set by Filter 1 Output
4 = Analog Comparator A Threshold set by Filter 2 Output
Bit 2: ACOMP_A_POL – Analog Comparator A Polarity

0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_A_INT_EN – Analog Comparator A Interrupt Enable
0 = Disables Analog Comparator A Interrupt generation (Default)
1 = Enables Analog Comparator A Interrupt generation

Bit 0: ACOMP_EN – Analog Comparators Enable
0 = Analog Comparators Disabled (Default)
1 = Analog Comparators Enabled

21.2.2 Analog Comparator Control 1 Register (ACOMPCTRL1)

Address 00130004

Bit Number	30:24	23:22	21:19	18
Bit Name	ACOMP_D_THRESH	RESERVED	ACOMP_D_SEL	ACOMP_D_POL
Access	R/W	-	R/W	R/W
Default	000_0000	00	000	1

Bit Number	17	16	15	14:8
Bit Name	ACOMP_D_INT_EN	ACOMP_D_OUT_EN	RESERVED	ACOMP_C_THRESH
Access	R/W	R/W	-	R/W
Default	0	0	0	000_0000

Bit Number	7:6	5:3	2	1	0
Bit Name	RESERVED	ACOMP_C_SEL	ACOMP_C_POL	ACOMP_C_INT_EN	RESERVED
Access	-	R/W	R/W	R/W	-
Default	00	000	1	0	0

Bits 30-24: ACOMP_D_THRESH – Configures Analog Comparator D Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V

Bits 23-22: RESERVED – Unused bits

Bits 21-19: ACOMP_D_SEL – Configures Analog Comparator D Threshold
0 = Analog Comparator D Threshold set by ACOMP_D_THRESH (Default)
1 = Analog Comparator D Threshold set by Comparator Ramp 0
2 = Analog Comparator D Threshold set by Filter 0 Output
3 = Analog Comparator D Threshold set by Filter 1 Output
4 = Analog Comparator D Threshold set by Filter 2 Output

Bit 18: ACOMP_D_POL – Analog Comparator D Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 17: ACOMP_D_INT_EN – Analog Comparator D Interrupt Enable
0 = Disables Analog Comparator D Interrupt generation (Default)
1 = Enables Analog Comparator D Interrupt generation

Bit 16: ACOMP_D_OUT_EN – Analog Comparator D DAC Output Enable
0 = Disables output of Comparator DAC D onto AD pin (Default)
1 = Enables output of Comparator DAC D onto AD pin

Bit 15: RESERVED – Unused bit

Bits 14-8: ACOMP_C_THRESH – Configures Analog Comparator C Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..

127 = Comparator Reference of 2.5 V

Bits 7-6: RESERVED – Unused bits

Bits 5-3: ACOMP_C_SEL – Configures Analog Comparator C Threshold

0 = Analog Comparator C Threshold set by ACOMP_C_THRESH (Default)
1 = Analog Comparator C Threshold set by Comparator Ramp 0
2 = Analog Comparator C Threshold set by Filter 0 Output
3 = Analog Comparator C Threshold set by Filter 1 Output
4 = Analog Comparator C Threshold set by Filter 2 Output

Bit 2: ACOMP_C_POL – Analog Comparator C Polarity

0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_C_INT_EN – Analog Comparator C Interrupt Enable

0 = Disables Analog Comparator C Interrupt generation (Default)
1 = Enables Analog Comparator C Interrupt generation

Bit 0: RESERVED – Unused bit

21.2.3 Analog Comparator Control 2 Register (ACOMPCTRL2)

Address 00130008

Bit Number	30:24	23	22	21:19
Bit Name	ACOMP_F_THRESH	RESERVED	ACOMP_F_REF_SEL	ACOMP_F_SEL
Access	R/W	-	R/W	R/W
Default	000_0000	0	0	000

Bit Number	18	17	16	15
Bit Name	ACOMP_F_POL	ACOMP_F_INT_EN	ACOMP_F_OUT_EN	RESERVED
Access	R/W	R/W	R/W	-
Default	1	0	0	0

Bit Number	14:8	7:6	5:3
Bit Name	ACOMP_E_THRESH	RESERVED	ACOMP_E_SEL
Access	R/W	-	R/W
Default	000_0000	00	000

Bit Number	2	1	0
Bit Name	ACOMP_E_POL	ACOMP_E_INT_EN	ACOMP_E_OUT_EN
Access	R/W	R/W	R/W
Default	1	0	0

Bits 30-24: ACOMP_F_THRESH – Configures Analog Comparator F Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V
Bit 23: RESERVED – Unused bit
Bit 22: ACOMP_F_REF_SEL – Analog Comparator F Reference Select
0 = Selects internal DAC reference (Default)
1 = Selects reference driven from AD-07 pin
Bits 21-19: ACOMP_F_SEL – Configures Analog Comparator F Threshold
0 = Analog Comparator F Threshold set by ACOMP_F_THRESH (Default)
1 = Analog Comparator F Threshold set by Comparator Ramp 0
2 = Analog Comparator F Threshold set by Filter 0 Output
3 = Analog Comparator F Threshold set by Filter 1 Output
4 = Analog Comparator F Threshold set by Filter 2 Output
Bit 18: ACOMP_F_POL – Analog Comparator F Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)
Bit 17: ACOMP_F_INT_EN – Analog Comparator F Interrupt Enable
0 = Disables Analog Comparator F Interrupt generation (Default)
1 = Enables Analog Comparator F Interrupt generation
Bit 16: ACOMP_F_OUT_EN – Analog Comparator F DAC Output Enable
0 = Disables output of Comparator DAC F onto AD pin (Default)
1 = Enables output of Comparator DAC F onto AD pin
Bit 15: RESERVED – Unused bit
Bits 14-8: ACOMP_E_THRESH – Configures Analog Comparator E Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV

……..
127 = Comparator Reference of 2.5 V

Bits 7-6: RESERVED – Unused bits

Bits 5-3: ACOMP_E_SEL – Configures Analog Comparator E Threshold
0 = Analog Comparator E Threshold set by ACOMP_E_THRESH (Default)
1 = Analog Comparator E Threshold set by Comparator Ramp 0
2 = Analog Comparator E Threshold set by Filter 0 Output
3 = Analog Comparator E Threshold set by Filter 1 Output
4 = Analog Comparator E Threshold set by Filter 2 Output

Bit 2: ACOMP_E_POL – Analog Comparator E Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_E_INT_EN – Analog Comparator E Interrupt Enable
0 = Disables Analog Comparator E Interrupt generation (Default)
1 = Enables Analog Comparator E Interrupt generation

Bit 0: ACOMP_E_OUT_EN – Analog Comparator E DAC Output Enable
0 = Disables output of Comparator DAC E onto AD pin (Default)
1 = Enables output of Comparator DAC E onto AD pin

21.2.4 Analog Comparator Control 3 Register (ACOMPCTRL3)

Address 0013000C

Bit Number	14:8	7:6	5:3
Bit Name	ACOMP_G_THRESH	RESERVED	ACOMP_G_SEL
Access	R/W	-	R/W
Default	000_0000	00	000

Bit Number	2	1	0
Bit Name	ACOMP_G_POL	ACOMP_G_INT_EN	ACOMP_G_OUT_EN
Access	R/W	R/W	R/W
Default	1	0	0

Bits 14-8: ACOMP_G_THRESH – Configures Analog Comparator G Threshold
0 = Comparator Reference of 19.53125 mV (Default)
1 = Comparator Reference of 39.0625 mV
……..
127 = Comparator Reference of 2.5 V

Bits 7-6: RESERVED – Unused bits

Bits 5-3: ACOMP_G_SEL – Configures Analog Comparator G Threshold
0 = Analog Comparator G Threshold set by ACOMP_G_THRESH (Default)
1 = Analog Comparator G Threshold set by Comparator Ramp 0
2 = Analog Comparator G Threshold set by Filter 0 Output
3 = Analog Comparator G Threshold set by Filter 1 Output
4 = Analog Comparator G Threshold set by Filter 2 Output

Bit 2: ACOMP_G_POL – Analog Comparator G Polarity
0 = Comparator result enabled when input falls below threshold
1 = Comparator result enabled when input exceeds threshold (Default)

Bit 1: ACOMP_G_INT_EN – Analog Comparator G Interrupt Enable
0 = Disables Analog Comparator G Interrupt generation (Default)
1 = Enables Analog Comparator G Interrupt generation

Bit 0: ACOMP_G_OUT_EN – Analog Comparator G DAC Output Enable
0 = Disables output of Comparator DAC G onto AD pin (Default)
1 = Enables output of Comparator DAC G onto AD pin

21.2.5 External Fault Control Register (EXTFAULTCTRL)

Address 00130010

Bit Number	11	10	9	8
Bit Name	FAULT3_POL	FAULT2_POL	FAULT1_POL	FAULT0_POL
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit Number	7	6	5	4
Bit Name	FAULT3_INT_EN	FAULT2_INT_EN	FAULT1_INT_EN	FAULT0_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FAULT3_DET_EN	FAULT2_DET_EN	FAULT1_DET_EN	FAULT0_DET_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 11: FAULT3_POL – Polarity configuration for FAULT[3] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 10: FAULT2_POL – Polarity configuration for FAULT[2] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 9: FAULT1_POL – Polarity configuration for FAULT[1] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 8: FAULT0_POL – Polarity configuration for FAULT[0] pin
0 = Fault detection enabled on falling edge
1 = Fault detection enabled on rising edge (Default)
Bit 7: FAULT3_INT_EN – FAULT[3] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 6: FAULT2_INT_EN – FAULT[2] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 5: FAULT1_INT_EN – FAULT[1] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 4: FAULT0_INT_EN – FAULT[0] Pin Interrupt Enable
0 = Disables Fault Detection Interrupt generation (Default)
1 = Enables Fault Detection Interrupt generation
Bit 3: FAULT3_DET_EN – FAULT[3] Pin Detection Enable
0 = Fault Detection Disabled (Default)
1 = Fault Detection Enabled
Bit 2: FAULT2_DET_EN – FAULT[2] Pin Detection Enable
0 = Fault Detection Disabled (Default)
1 = Fault Detection Enabled
Bit 1: FAULT1_DET_EN – FAULT[1] Pin Detection Enable
0 = Fault Detection Disabled (Default)
1 = Fault Detection Enabled
Bit 0: FAULT0_DET_EN – FAULT[0] Pin Detection Enable
0 = Fault Detection Disabled (Default)

1 = Fault Detection Enabled

21.3 *Fault Mux Interrupt Status Register (FAULTMUXINTSTAT)*

Address 00130014

Bit Number	16	15	14	13	12
Bit Name	DCOMP3	DCOMP2	DCOMP1	DCOMP0	LFO_FAIL
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit Number	11	10	9	8	7	6
Bit Name	FAULT3	FAULT2	FAULT1	FAULT0	DCM_DETECT	ACOMP_G
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit Number	5	4	3	2	1	0
Bit Name	ACOMP_F	ACOMP_E	ACOMP_D	ACOMP_C	ACOMP_B	ACOMP_A
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit 16: DCOMP3 – Digital Comparator 3 Interrupt Stat15us, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled
Bit 15: DCOMP2 – Digital Comparator 2 Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled
Bit 14: DCOMP1 – Digital Comparator 1 Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled
Bit 13: DCOMP0 – Digital Comparator 0 Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled
Bit 12: LFO_FAIL– Low Frequency Oscillator Failure Interrupt Status, cleared by read of status register
0 = Low Frequency Oscillator operational
1 = Low Frequency Oscillator failure detected
Bit 11: FAULT3 – External FAULT[2] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 10: FAULT2 – External FAULT[2] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 9: FAULT1 – External FAULT[1] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 8: FAULT0 – External FAULT[0] Interrupt Detection
0 = No External GPIO detection found
1 = External GPIO detection found
Bit 7: DCM_DETECT – Discontinuous Conduction Mode Interrupt Status, cleared by read of status register
0 = Discontinuous Conduction Mode detected
1 = Discontinuous Conduction Mode not detected
Bit 6: ACOMP_G – Analog Comparator G Interrupt Status, cleared by read of status register

0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

Bit 5: ACOMP_F – Analog Comparator F Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

Bit 4: ACOMP_E – Analog Comparator E Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

Bit 3: ACOMP_D – Analog Comparator D Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

Bit 2: ACOMP_C – Analog Comparator C Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

Bit 1: ACOMP_B – Analog Comparator B Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

Bit 0: ACOMP_A – Analog Comparator A Interrupt Status, cleared by read of status register
0 = Comparator threshold interrupt disabled
1 = Comparator threshold interrupt enabled

21.3.1 Fault Mux Raw Status Register (FAULTMUXRAWSTAT)

Address 00130018

Bit Number	16	15	14	13	12
Bit Name	DCOMP3	DCOMP2	DCOMP1	DCOMP0	LFO_FAIL
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit Number	11	10	9	8	7	6
Bit Name	FAULT3	FAULT2	FAULT1	FAULT0	DCM_DETECT	ACOMP_G
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit Number	5	4	3	2	1	0
Bit Name	ACOMP_F	ACOMP_E	ACOMP_D	ACOMP_C	ACOMP_B	ACOMP_A
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit 16: DCOMP3 – Digital Comparator 3 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 15: DCOMP2 – Digital Comparator 2 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 14: DCOMP1 – Digital Comparator 1 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 13: DCOMP0 – Digital Comparator 0 Raw Status
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 12: LFO_FAIL – Low Frequency Oscillator Failure Raw Status
0 = Low Frequency Oscillator operational

1 = Low Frequency Oscillator failure detected

Bit 11: FAULT3 – External Fault Detection on FAULT[3] pin
0 = No External FAULT[2] detection found
1 = External GPIO detection found

Bit 10: FAULT2 – External Fault Detection on FAULT[2] pin
0 = No External FAULT[2] detection found
1 = External GPIO detection found

Bit 9: FAULT1 – External Fault Detection on FAULT[1] pin
0 = No External FAULT[1] detection found
1 = External GPIO detection found

Bit 8: FAULT0 – External Fault Detection on FAULT[0] pin
0 = No External FAULT[0] detection found
1 = External GPIO detection found

Bit 7: DCM_DETECT – Discontinuous Conduction Mode Raw Status
0 = Discontinuous Conduction Mode detected
1 = Discontinuous Conduction Mode not detected

Bit 6: ACOMP_G – Analog Comparator G Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 5: ACOMP_F – Analog Comparator F Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 4: ACOMP_E – Analog Comparator E Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 3: ACOMP_D – Analog Comparator D Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 2: ACOMP_C – Analog Comparator C Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 1: ACOMP_B – Analog Comparator B Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

Bit 0: ACOMP_A – Analog Comparator A Raw Result
0 = Comparator threshold not exceeded
1 = Comparator threshold exceeded

21.3.2 Comparator Ramp Control 0 Register (COMPRAMP0)

Address 0013001C

Bit Number	31:28	27:10
Bit Name	START_VALUE_SEL	STEP_SIZE
Access	R/W	R/W
Default	0000	00_0000_0000_0000_0000

Bit Number	9:5	4	3
Bit Name	CLKS_PER_STEP	DPWM3_TRIG_EN	DPWM2_TRIG_EN
Access	R/W	R/W	R/W
Default	0_0000	0	00

Bit Number	2	1	0
Bit Name	DPWM1_TRIG_EN	DPWM0_TRIG_EN	RAMP_EN
Access	R/W	R/W	R/W
Default	00	00	0

Bits 31-28: START_VALUE_SEL – Configures comparator ramp starting value
0 = Filter 0 Output (Bits 17-11) (Default)
1 = Filter 1 Output (Bits 17-11)
2 = Filter 2 Output (Bits 17-11)
3 = Analog Comparator Threshold A Value
4 = Analog Comparator Threshold B Value
5 = Analog Comparator Threshold C Value
6 = Analog Comparator Threshold D Value
7 = Analog Comparator Threshold E Value
8 = Analog Comparator Threshold F Value
9 = Analog Comparator Threshold G Value

Bits 27-10: STEP_SIZE - Programmable 18-bit unsigned comparator step with Bits 27:24 representing the integer portion of the comparator step (0-15 Comparator steps of 19.5mV each) and Bits 23:10 representing the fractional portion of the comparator step

Bits 9-5: CLKS_PER_STEP – Selects number of MCLK (HFO_OSC/8) clock cycles per comparator step where number of subcycles can vary from 1 to 32
0 = 1 MCLK clock cycles per step (Default)
1 = 2 MCLK clock cycles per step
2 = 3 MCLK clock cycles per step
…….
31 = 32 MCLK clock cycles per step

Bit 4: DPWM3_TRIG_EN – Enables DPWM Trigger from DPWM 3 to Analog Comparator Ramp 0
0 = DPWM 3 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 3 trigger routed to Analog Comparator Ramp 0

Bit 3: DPWM2_TRIG_EN – Enables DPWM Trigger from DPWM 2 to Analog Comparator Ramp 0
0 = DPWM 2 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 2 trigger routed to Analog Comparator Ramp 0

Bit 2: DPWM1_TRIG_EN – Enables DPWM Trigger from DPWM 1 to Analog Comparator Ramp 0
0 = DPWM 1 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 1 trigger routed to Analog Comparator Ramp 0

Bit 1: DPWM0_TRIG_EN – Enables DPWM Trigger from DPWM 0 to Analog Comparator Ramp 0

0 = DPWM 0 trigger not routed to Analog Comparator Ramp 0 (Default)
1 = DPWM 0 trigger routed to Analog Comparator Ramp 0

Bit 0: RAMP_EN – Enable for Analog Comparator Ramp 0

0 = Analog Comparator Ramp disabled (Default)
1 = Analog Comparator Ramp enabled

21.3.3 Digital Comparator Control 0 Register (DCOMPCTRL0)

Address 0x00130020

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0
Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault

Bits 23-19: RESERVED – Unused bits

Bit 18: COMP_POL – Digital Comparator 0 Polarity

0 = Digital Comparator result asserted if value below threshold (Default)
1 = Digital Comparator result asserted if value above threshold

Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold

0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected

Bit 14: CNT_CLR – Comparator Detection Counter clear

0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault

Bit 13: CNT_CONFIG – Comparator Detection Counter configuration

0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold

Bit 12: INT_EN – Comparator Interrupt Enable

0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation

Bit 11: COMP_EN – Digital Comparator 0 Enable

0 = Disables Digital Comparator 0 (Default)
1 = Enables Digital Comparator 0

Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

21.3.4 Digital Comparator Control 1 Register (DCOMPCTRL1)

Address 0x00130024

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0
Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault
Bits 23-19: RESERVED – Unused bits
Bit 18: COMP_POL – Digital Comparator 1 Polarity
0 = Digital Comparator result asserted if value below threshold (Default)
1 = Digital Comparator result asserted if value above threshold
Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold
0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected
Bit 14: CNT_CLR – Comparator Detection Counter clear
0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault
Bit 13: CNT_CONFIG – Comparator Detection Counter configuration
0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
Bit 12: INT_EN – Comparator Interrupt Enable
0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation
Bit 11: COMP_EN – Digital Comparator 1 Enable
0 = Disables Digital Comparator 1 (Default)
1 = Enables Digital Comparator 1
Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

21.3.5 Digital Comparator Control 2 Register (DCOMPCTRL2)

Address 0x00130028

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0

Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault
Bits 23-19: RESERVED – Unused bits
Bit 18: COMP_POL – Digital Comparator 1 Polarity
0 = Digital Comparator result asserted if value below threshold (Default)
1 = Digital Comparator result asserted if value above threshold
Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold
0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected
Bit 14: CNT_CLR – Comparator Detection Counter clear
0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault
Bit 13: CNT_CONFIG – Comparator Detection Counter configuration
0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold
Bit 12: INT_EN – Comparator Interrupt Enable
0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation
Bit 11: COMP_EN – Digital Comparator 2 Enable
0 = Disables Digital Comparator 2 (Default)
1 = Enables Digital Comparator 2
Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

21.3.6 Digital Comparator Control 3 Register (DCOMPCTRL3)

Address 0x0013002C

Bit Number	31:24	23:19	18	17:15	14
Bit Name	CNT_THRESH	RESERVED	COMP_POL	FE_SEL	CNT_CLR
Access	R/W	-	R/W	R/W	R/W
Default	0000_0000	0000_0	0	000	0

Bit Number	13	12	11	10:0
Bit Name	CNT_CONFIG	INT_EN	COMP_EN	THRESH
Access	R/W	R/W	R/W	R/W
Default	0	0	0	000_0000_0000

Bits 31-24: CNT_THRESH – Sets the number of received comparator events before declaring a fault
Bits 23-19: RESERVED – Unused bits
Bit 18: COMP_POL – Digital Comparator 1 Polarity
0 = Digital Comparator result asserted if value below threshold (Default)

1 = Digital Comparator result asserted if value above threshold

Bits 17-15: FE_SEL – Selects which Front End absolute data is used for Digital Comparison with threshold

0 = Front End 0 absolute data selected (Default)
1 = Front End 1 absolute data selected
2 = Front End 2 absolute data selected
3 = Front End 0 error data selected
4 = Front End 1 error data selected
5 = Front End 2 error data selected

Bit 14: CNT_CLR – Comparator Detection Counter clear

0 = No clear of Comparator Detection Counter (Default)
1 = Clear Comparator Detection counter and associated fault

Bit 13: CNT_CONFIG – Comparator Detection Counter configuration

0 = Counter clears upon receipt of sample which does not exceed comparator threshold (Default)
1 = Counter decrements by 1 upon receipt of sample which does not exceed comparator threshold

Bit 12: INT_EN – Comparator Interrupt Enable

0 = Disables Comparator Interrupt generation (Default)
1 = Enables Comparator Interrupt generation

Bit 11: COMP_EN – Digital Comparator 3 Enable

0 = Disables Digital Comparator 3 (Default)
1 = Enables Digital Comparator 3

Bits 10-0: THRESH – Sets the digital comparator threshold, 11-bit signed value with resolution of 1.5625mV/bit

21.3.7 Digital Comparator Counter Status Register (DCOMPCNTSTAT)

Address 0x00130030

Bit Number	31:24	31:24	31:24	31:24
Bit Name	DCOMP3_CNT	DCOMP2_CNT	DCOMP1_CNT	DCOMP0_CNT
Access	R	R	R	R
Default	-	-	-	-

Bits 31-24: DCOMP3_CNT – Current value of Digital Comparator 3 detection counter
Bits 23-16: DCOMP2_CNT – Current value of Digital Comparator 2 detection counter
Bits 15-8: DCOMP1_CNT – Current value of Digital Comparator 1 detection counter
Bits 7-0: DCOMP0_CNT – Current value of Digital Comparator 0 detection counter

21.3.8 DPWM 0 Current Limit Control Register (DPWM0CLIM)

Address 0x00130034

Bit Number	15	14	13
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	8	7	6	5	4

Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 15: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 0 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 0 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)

1 = Analog Comparator result enabled for current limit

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

21.3.9 DPWM 0 Fault AB Detection Register (DPWM0FLTABDET)

Address 0x00130038

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection

Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection

Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection

Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection

Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 0 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection

Bit 6: ACOMP_A_EN – Enables Analog Comparator G result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

21.3.10 DPWM 0 Fault Detection Register (DPWM0FAULTDET)

Address 0x0013003C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN

Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 0 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 15: RESERVED – Unused bit
Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 0 PWM-A Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 0 PWM-A Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 0 PWM-A Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 0 PWM-A Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 10: PWMA_FAULT3_EN – Enables FAULT[3] pin for DPWM 0 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 0 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 0 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 0 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 0 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 0 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 0 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 0 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

21.3.11 DPWM 0 IDE Detection Register (DPWM0IDEDET)

Address 0x00130040

Bit Number	6	5	4	3
Bit Name	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	2	1	0
Bit Name	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 6: ACOMP_6_EN – Enables Analog Comparator G result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 5: ACOMP_5_EN – Enables Analog Comparator F result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 4: ACOMP_4_EN – Enables Analog Comparator E result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 3: ACOMP_3_EN – Enables Analog Comparator D result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 2: ACOMP_2_EN – Enables Analog Comparator C result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 1: ACOMP_1_EN – Enables Analog Comparator B result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 0: ACOMP_0_EN – Enables Analog Comparator A result for DPWM 0 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

21.3.12 DPWM 1 Current Limit Control Register (DPWM1CLIM)

Address 0x00130044

Bit Number	15	14	13
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	8	7	6	5	4
Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 15: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 1 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 1 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit

Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

21.3.13 DPWM 1 Fault AB Detection Register (DPWM1FLTABDET)

Address 0x00130048

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 1 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 Fault AB detection

0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

21.3.14 DPWM 1 Fault Detection Register (DPWM1FAULTDET)

Address 0x0013004C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6

Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 1 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 PWM-B Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 15: RESERVED – Unused bit

Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection

Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection

Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection

Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 1 PWM-A Fault Detection

0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection

Bit 10: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 1 PWM-A Fault Detection

0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection

Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 1 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

21.3.15 DPWM 1 IDE Detection Register (DPWM1IDEDET)

Address 0x00130050

Bit Number	6	5	4	3
Bit Name	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	2	1	0
Bit Name	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 6: ACOMP_6_EN – Enables Analog Comparator G result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 5: ACOMP_5_EN – Enables Analog Comparator F result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 4: ACOMP_4_EN – Enables Analog Comparator E result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 3: ACOMP_3_EN – Enables Analog Comparator D result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 2: ACOMP_2_EN – Enables Analog Comparator C result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 1: ACOMP_1_EN – Enables Analog Comparator B result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 0: ACOMP_0_EN – Enables Analog Comparator A result for DPWM 1 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

21.3.16 DPWM 2 Current Limit Control Register (DPWM2CLIM)

Address 0x00130054

Bit Number	15	14	13
Bit Name	ANALOG_PCM_EN	DCOMP3_EN	DCOMP2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	12	11	10	9
Bit Name	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	8	7	6	5	4
Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 15: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 2 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 2 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit

Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

21.3.17 DPWM 2 Fault AB Detection Register (DPWM2FLTABDET)

Address 0x00130058

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 2 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 Fault AB detection

0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

21.3.18 DPWM 2 Fault Detection Register (DPWM2FAULTDET)

Address 0x0013005C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN

Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	5	4	3
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	2	1	0
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 2 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 15: RESERVED – Unused bit
Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 2 PWM-A Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 2 PWM-A Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 2 PWM-A Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 2 PWM-A Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 10: PWMA_FAULT3_EN – Enables FAULT[3] pin for DPWM 2 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 2 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 2 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 2 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 2 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 2 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 2 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 2 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

21.3.19 DPWM 2 IDE Detection Register (DPWM2IDEDET)

Address 0x00130060

Bit Number	6	5	4	3
Bit Name	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	2	1	0
Bit Name	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 6: ACOMP_6_EN – Enables Analog Comparator G result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 5: ACOMP_5_EN – Enables Analog Comparator F result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 4: ACOMP_4_EN – Enables Analog Comparator E result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 3: ACOMP_3_EN – Enables Analog Comparator D result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 2: ACOMP_2_EN – Enables Analog Comparator C result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 1: ACOMP_1_EN – Enables Analog Comparator B result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

Bit 0: ACOMP_0_EN – Enables Analog Comparator A result for DPWM 2 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

21.3.20 DPWM 3 Current Limit Control Register (DPWM3CLIM)

Address 0x00130064

Bit Number	15	14
Bit Name	ANALOG_PCM_EN	DCOMP3_EN
Access	R/W	R/W
Default	0	0

Bit Number	13	12	11	10	9
Bit Name	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN	FAULT2_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5	4
Bit Name	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	3	2	1	0
Bit Name	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 15: ANALOG_PCM_EN – Enables Analog Peak Current detection result for DPWM 2 Current Limit
0 = Analog Peak Current detection disabled for current limit (Default)
1 = Analog Peak Current detection enabled for current limit
Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 Current Limit
0 = Digital Comparator 3 result disabled for current limit (Default)
1 = Digital Comparator 3 result enabled for current limit
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 Current Limit
0 = Digital Comparator 2 result disabled for current limit (Default)
1 = Digital Comparator 2 result enabled for current limit
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 Current Limit
0 = Digital Comparator 1 result disabled for current limit (Default)
1 = Digital Comparator 1 result enabled for current limit
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 Current Limit
0 = Digital Comparator 0 result disabled for current limit (Default)
1 = Digital Comparator 0 result enabled for current limit
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 3 Current Limit
0 = External Fault pin disabled for current limit (Default)
1 = External Fault pin enabled for current limit

Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit
Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 Current Limit
0 = Analog Comparator result disabled for current limit (Default)
1 = Analog Comparator result enabled for current limit

21.3.21 DPWM 3 Fault AB Detection Register (DPWM3FLTABDET)

Address 0x00130068

Bit Number	14	13	12	11	10
Bit Name	DCOMP3_EN	DCOMP2_EN	DCOMP1_EN	DCOMP0_EN	FAULT3_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	9	8	7	6	5
Bit Name	FAULT2_EN	FAULT1_EN	FAULT0_EN	ACOMP_G_EN	ACOMP_F_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	ACOMP_E_EN	ACOMP_D_EN	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 14: DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 3 disabled for Fault AB detection (Default)
1 = Digital Comparator 3 enabled for Fault AB detection
Bit 13: DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 2 disabled for Fault AB detection (Default)
1 = Digital Comparator 2 enabled for Fault AB detection
Bit 12: DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 1 disabled for Fault AB detection (Default)
1 = Digital Comparator 1 enabled for Fault AB detection
Bit 11: DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 Fault AB Detection
0 = Digital Comparator 0 disabled for Fault AB detection (Default)
1 = Digital Comparator 0 enabled for Fault AB detection
Bit 10: FAULT3_EN – Enables FAULT[3] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 9: FAULT2_EN – Enables FAULT[2] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 8: FAULT1_EN – Enables FAULT[1] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 7: FAULT0_EN – Enables FAULT[0] pin for DPWM 3 Fault AB detection
0 = External Fault pin disabled for Fault AB detection (Default)
1 = External Fault pin enabled for Fault AB detection
Bit 6: ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 5: ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 4: ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection
Bit 3: ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 Fault AB detection

0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 2: ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 1: ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

Bit 0: ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 Fault AB detection
0 = Analog Comparator result disabled for Fault AB detection (Default)
1 = Analog Comparator result enabled for Fault AB detection

21.3.22 DPWM 3 Fault Detection Register (DPWM3FAULTDET)

Address 0x0013006C

Bit Number	30	29	28
Bit Name	PWMB_DCOMP3_EN	PWMB_DCOMP2_EN	PWMB_DCOMP1_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	27	26	25
Bit Name	PWMB_DCOMP0_EN	PWMB_FAULT3_EN	PWMB_FAULT2_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	24	23	22
Bit Name	PWMB_FAULT1_EN	PWMB_FAULT0_EN	PWMB_ACOMP_G_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	21	20	19
Bit Name	PWMB_ACOMP_F_EN	PWMB_ACOMP_E_EN	PWMB_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18	17	16
Bit Name	PWMB_ACOMP_C_EN	PWMB_ACOMP_B_EN	PWMB_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	15	14
Bit Name	RESERVED	PWMA_DCOMP3_EN
Access	-	R/W
Default	0	0

Bit Number	13	12	11
Bit Name	PWMA_DCOMP2_EN	PWMA_DCOMP1_EN	PWMA_DCOMP0_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10	9
Bit Name	PWMA_FAULT3_EN	PWMA_FAULT2_EN
Access	R/W	R/W
Default	0	0

Bit Number	8	7	6
Bit Name	PWMA_FAULT1_EN	PWMA_FAULT0_EN	PWMA_ACOMP_G_EN

Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	**5**	**4**	**3**
Bit Name	PWMA_ACOMP_F_EN	PWMA_ACOMP_E_EN	PWMA_ACOMP_D_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	**2**	**1**	**0**
Bit Name	PWMA_ACOMP_C_EN	PWMA_ACOMP_B_EN	PWMA_ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 30: PWMB_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 29: PWMB_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 28: PWMB_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 27: PWMB_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 PWM-B Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 26: PWMB_FAULT3_EN – Enables FAULT[3] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 25: PWMB_FAULT2_EN – Enables FAULT[2] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 24: PWMB_FAULT1_EN – Enables FAULT[1] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 23: PWMB_FAULT0_EN – Enables FAULT[0] pin for DPWM 3 PWM-B Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 22: PWMB_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 21: PWMB_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 20: PWMB_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 19: PWMB_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 18: PWMB_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 17: PWMB_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 16: PWMB_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 PWM-B Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 15: RESERVED – Unused bit
Bit 14: PWMA_DCOMP3_EN – Enables Digital Comparator 3 result for DPWM 3 PWM-A Fault Detection
0 = Digital Comparator 3 disabled for fault detection (Default)
1 = Digital Comparator 3 enabled for fault detection
Bit 13: PWMA_DCOMP2_EN – Enables Digital Comparator 2 result for DPWM 3 PWM-A Fault Detection
0 = Digital Comparator 2 disabled for fault detection (Default)
1 = Digital Comparator 2 enabled for fault detection
Bit 12: PWMA_DCOMP1_EN – Enables Digital Comparator 1 result for DPWM 3 PWM-A Fault Detection
0 = Digital Comparator 1 disabled for fault detection (Default)
1 = Digital Comparator 1 enabled for fault detection
Bit 11: PWMA_DCOMP0_EN – Enables Digital Comparator 0 result for DPWM 3 PWM-A Fault Detection
0 = Digital Comparator 0 disabled for fault detection (Default)
1 = Digital Comparator 0 enabled for fault detection
Bit 10: PWMA_FAULT3_EN – Enables FAULT[3] pin for DPWM 3 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 9: PWMA_FAULT2_EN – Enables FAULT[2] pin for DPWM 3 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 8: PWMA_FAULT1_EN – Enables FAULT[1] pin for DPWM 3 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 7: PWMA_FAULT0_EN – Enables FAULT[0] pin for DPWM 3 PWM-A Fault Detection
0 = External Fault pin disabled for fault detection (Default)
1 = External Fault pin enabled for fault detection
Bit 6: PWMA_ACOMP_G_EN – Enables Analog Comparator G result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 5: PWMA_ACOMP_F_EN – Enables Analog Comparator F result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection
Bit 4: PWMA_ACOMP_E_EN – Enables Analog Comparator E result for DPWM 3 PWM-A Fault detection
0 = Analog Comparator result disabled for fault detection (Default)

1 = Analog Comparator result enabled for fault detection

Bit 3: PWMA_ACOMP_D_EN – Enables Analog Comparator D result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 2: PWMA_ACOMP_C_EN – Enables Analog Comparator C result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 1: PWMA_ACOMP_B_EN – Enables Analog Comparator B result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

Bit 0: PWMA_ACOMP_A_EN – Enables Analog Comparator A result for DPWM 3 PWM-A Fault detection

0 = Analog Comparator result disabled for fault detection (Default)
1 = Analog Comparator result enabled for fault detection

21.3.23 DPWM 3 IDE Detection Register (DPWM3IDEDET)

Address 0x00130070

Bit Number	6	5	4	3
Bit Name	ACOMP_G_EN	ACOMP_F_EN	ACOMP_E_EN	ACOMP_D_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	2	1	0
Bit Name	ACOMP_C_EN	ACOMP_B_EN	ACOMP_A_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit 6: ACOMP_6_EN – Enables Analog Comparator G result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection
Bit 5: ACOMP_5_EN – Enables Analog Comparator F result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection
Bit 4: ACOMP_4_EN – Enables Analog Comparator E result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection
Bit 3: ACOMP_3_EN – Enables Analog Comparator D result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection
Bit 2: ACOMP_2_EN – Enables Analog Comparator C result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection
Bit 1: ACOMP_1_EN – Enables Analog Comparator B result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection
Bit 0: ACOMP_0_EN – Enables Analog Comparator A result for DPWM 3 IDE detection
0 = Analog Comparator result disabled for IDE detection (Default)
1 = Analog Comparator result enabled for IDE detection

21.3.24 HFO Fail Detect Register (HFOFAILDET)

Address 0x00130074

Bit Number	17:1	0
Bit Name	HFO_FAIL_THRESH	HFO_DETECT_EN
Access	R/W	R/W
Default	0_0000_0000_1111_1111	0

Bits 17-1: HFO_FAIL_THRESH – Configures threshold where a clear flag is used to clear a counter in the Low Frequency Oscillator domain (if LFO counter overflows, a reset will be generated), resolution of threshold equals High Frequency Oscillator period
Bit 0: HFO_DETECT_EN – Enables High Frequency Oscillator Failure Detection logic, device will be reset upon detection of an oscillator failure
0 = Disables High Frequency Oscillator Failure Detection (Default)
1 = Enables High Frequency Oscillator Failure Detection

21.3.25 LFO Fail Detect Register (LFOFAILDET)

Address 0x00130078

Bit Number	6:2	1	0
Bit Name	LFO_FAIL_THRESH	LFO_FAIL_INT_EN	LFO_DETECT_EN
Access	R/W	R/W	R/W
Default	0_0011	0	0

Bits 6-2: LFO_FAIL_THRESH – Configures threshold where a clear flag is used to clear a counter in the High Frequency Oscillator domain (if HFO counter overflows, a reset will be generated), resolution of threshold equals Low Frequency Oscillator period
Bit 1: LFO_FAIL_INT_EN – Low Frequency Oscillator Fail Interrupt Enable
0 = Disables Interrupt Generation upon LFO Failure Detection (Default)
1 = Enables Interrupt Generation upon LFO Failure Detection
Bit 0: LFO_DETECT_EN – Enables Low Frequency Oscillator Failure Detection logic, interrupt will be generated upon detection of an oscillator failure
0 = Disables Low Frequency Oscillator Failure Detection (Default)
1 = Enables Low Frequency Oscillator Failure Detection

21.3.26 IDE Control Register (IDECTRL)

Address 0013007C

Bit Number	31:24	23:16
Bit Name	DCM_LIMIT_H	DCM_LIMIT_L
Access	R/W	R/W
Default	0000_0000	0000_0000

Bit Number	15:14	13	12:0
Bit Name	RESERVED	DCM_INT_EN	IDE_KD
Access	-	R/W	R/W
Default	00	0	0_0000_0000_0000

Bits 31-24: DCM_LIMIT_H – Value added to 1-Da value to provide hysteresis for exiting DCM mode
Bits 23-16: DCM_LIMIT_L – Value subtracted from 1-Da value to provide hysteresis for entering DCM mode
Bit 15-14: RESERVED – Unused Bits
Bit 13: DCM_INT_EN – Enables Discontinuous Conduction Mode (DCM) interrupt generation based on selected Filter outputs
0 = Disables DCM Detection Interrupt (Default)
1 = Enables DCM Detection Interrupt
Bits 12-0: IDE_KD – 13-bit unsigned value used to calculate the DPWM B Pulse width when configured in IDE Mode. IDE_KD is configured in 4.9 format, with the integer portion of the KD value ranging from 0 to 15 and 9 fractional bits available for the pulse width calculation.

21.4 *RTC – Real Time Clock Interface*

21.4.1 RTC Control Register (RTCCTRL)

Address FFF7E400

Bit Number	3:2	1	0
Bit Name	CONFIG_INCL	RESERVED	PRESET_EN
Access	R/W	R	R/W
Default	11	0	0

Bit 3-2: CONFIG_INCL – For analog configuration only
00 = invalid value
01 = invalid value
10 = enables external 1.8V clock input on XTAL_IN pin or 3.3V clock input on TCK, depending on value in RTC_CLK_IN_SEL bit in IOMUX register
11 = disable
Bit 1: Reserved
Bit 0: PRESET_EN – Counter preset enable
0 = RTC Preset Disabled (Default)
1 = RTC Preset Enabled

21.4.2 RTC Counter Register (RTCCOUNT)

Address FFF7E404

Bit Number	27:17	16:12	11:6	5:0
Bit Name	DAYS	HOURS	MINS	SECS
Access	R	R	R	R
Default	0	0	0	0

Bit 27:17: DAYS – Current count of days
Bit 16:12: HOURS – Current count of hours
Bit 11:6: MINS – Current count of minutes
Bit 5:0: SECS – Current count of seconds

21.4.3 RTC Preset Register (RTCPRESET)

Address FFF7E408

Bit Number	27:17	16:12	11:6	5:0
Bit Name	DAYS	HOURS	MINS	SECS
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 27:17: DAYS – Preset value of days
Bit 16:12: HOURS – Preset value of hours
Bit 11:6: MINS – Preset value of minutes
Bit 5:0: SECS – Preset value of seconds

21.4.4 RTC Interrupt Enable Register (RTCINTEN)

Address FFF7E40C

Bit Number	3	2	1	0
Bit Name	SEC60	SEC30	SEC10	SEC
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 3: 60SEC – Enable interrupts every 60 seconds
Bit 2: 30SEC – Enable interrupts every 30 seconds
Bit 1: 10SEC – Enable interrupts every 10 seconds
Bit 0: 1SEC – Enable interrupts every 1 second

21.4.5 RTC Interrupt Status Register (RTCINTSTAT)

Address FFF7E410

Bit Number	3	2	1	0
Bit Name	SEC60	SEC30	SEC10	SEC
Access	R	R	R	R
Default	0	0	0	0

Bit 3: 60SEC – Interrupt flag for 60 seconds
Bit 2: 30SEC – Interrupt flag for 30 seconds
Bit 1: 10SEC – Interrupt flag for 10 seconds
Bit 0: 1SEC – Interrupt flag for 1 second

21.4.6 RTC Prescale Register (RTCPRESCALE)

Address FFF7E414

Bit Number	9:0
Bit Name	PRESCALE
Access	R/W
Default	0

Bit 9:0: PRESCALE – Prescaler value
Optimal value for 10Mhz XTAL is 0x2CF. Minor adjustments can be made between 0x1CF and 0x3CF.

21.5 *SPI – Serial Peripheral Interface*

21.5.1 SPI Control Register (SPICTRL)

Address FFF7E800

Bit Number	23:21
Bit Name	CLKRATE
Access	R/W
Default	000

Bit Number	20:16	15:11	10:7	6	5
Bit Name	FRMLEN	RXCNT	TXCNT	WRSTORE	WRSTART
Access	R/W	R/W	R/W	R/W	R/W
Default	00000	00000	0000	0	0

Bit Number	4	3	2	1	0
Bit Name	POL	PHA	INTEN	MODE	SPIEN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 23:21: CLKRATE – Master clock rate relative to ICLK
- 0 = SCK is ICLK/2 (Default)
- 1 = SCK is ICLK/4 (Default)
- 2 = SCK is ICLK/8 (Default)
- 3 = SCK is ICLK/16 (Default)

Bit 20:16: FRMLEN – Sets the number of messages (TXCNT + RXCNT) to hold CS low.
Bit 15:11: RXCNT – Sets the number bytes to receive after TXCNT bytes have been transmitted
Bit 10:7: TXCNT – Sets the bytes to transmit from the SPITX registers
Bit 6: WRSTORE – Places or discards data received during TXCNT
- 0 = Data received during TXCNT discarded (Default)
- 1 = Data received during TXCNT placed in RXBUF

Bit 5: WRSTART- Sets which WRREG initiates transfer
- 0 = Write to SPITX-0 starts message transfer (Default)
- 1 = Write to SPITX-1 starts message transfer

Bit 4: POL – The polarity bit, together with the phase bit, determines the transfer-mode.
Bit 3: PHA – The phase bit, together with the polarity bit, determines the transfer-mode.
Bit 2: INTEN – Enable interrupt generation to the CPU
- 0 = Disabled (Default)
- 1 = Enabled

Bit 1: MODE – Configures SPI mode
- 0 = Master Mode (Default)
- 1 = Slave mode

Bit 0: SPIEN – Enable for SPI Module
- 0 = Disabled (Default)
- 1 = Enabled

21.5.2 SPI Status Register (SPISTAT)

Address FFF7E804

Bit Number		7:3	2	1	0
Bit Name		FRMCNT	WRCOL	BUSY	SPIF
Access		R	R	R	R
jDefault		0	0	0	0

Bit 12:4: FRMCNT – Indicates the number of messages remaining in the FRMLEN before SCS will go inactive.

Bit 2: WCOL – SPI interface is busy

Bit 1: BUSY – SPI interface is busy

Bit 0: SPIF – SPI Flag, write to clear

21.5.3 SPI Pin Function Register (SPIFUNC)

Address FFF7E808

Bit Number	3	2	1	0
Bit Name	MISO	MOSI	SCS	SCK
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

21.5.4 SPI Pin Direction Register (SPIDIR)

Address FFF7E80C

Bit Number	3	2	1	0
Bit Name	MISO	MOSI	SCS	SCK
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

21.5.5 SPI Pin GP Out Register (SPIGPOUT)

Address FFF7E810

Bit Number	3	2	1	0
Bit Name	MISO	MOSI	SCS	SCK
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

21.5.6 SPI Pin GP In Register (SPIGPIN)

Address FFF7E814

Bit Number	3	2	1	0
Bit Name	MISO	MOSI	SCS	SCK
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

21.5.7 SPI TX Buffer Register (SPITX0)

Address FFF7E818

Bit Number	31:0
Bit Name	DATA
Access	R/W
Default	0

21.5.8 SPI TX Buffer Register (SPITX1)

Address FFF7E81C

Bit Number	31:0
Bit Name	DATA
Access	R/W
Default	0

21.5.9 SPI Read Buffer Register (SPIRX0)

Address FFF7E820

Bit Number	31:0
Bit Name	DATA
Access	R
Default	0

21.5.10 SPI Read Buffer Register (SPIRX1)

Address FFF7E824

Bit Number	31:0
Bit Name	DATA
Access	R
Default	0

21.5.11 SPI Read Buffer Register (SPIRX2)

Address FFF7E828

Bit Number	31:0
Bit Name	DATA
Access	R
Default	0

21.5.12 SPI Read Buffer Register (SPIRX3)

Address FFF7E82C

Bit Number	31:0
Bit Name	DATA
Access	R
Default	0

21.6 *UART Registers*

21.6.1 UART Control Register 0 (UARTCTRL0)

Address FFF7EC00 – UART 0 Control Register 0
Address FFF7ED00 – UART 1 Control Register 0

Bit Number	7	6	5
Bit Name	STOP	PARITY	PARITY_ENA
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	4	3	2:0
Bit Name	SYNC_MODE	ADDR_MODE	DATA_SIZE
Access	R/W	R/W	R/W
Default	0	0	000

Bit 7: STOP – Configures stop bits for each frame
0 = One STOP bit included in each frame (Default)
1 = Two STOP bits included in each frame
Bit 6: PARITY – Sets odd or even parity
0 = Odd parity (Default)
1 = Even parity
Bit 5: PARITY_ENA - Enables parity transmission
0 = No parity bit included in each frame (Default)
1 = One parity bit included in each frame
Bit 4: SYNC_MODE – Selects between Synchronous mode and Asynchronous mode
0 = Asynchronous (Default)
1 = Synchronous
Bit 3: ADDR_MODE – Selects between Idle and Address Bit Mode
0 = IDLE Line mode with no Address bit (Default)
1 = Address Bit mode with one Address bit
Bits 2-0: DATA_SIZE – Determines the TX and RX byte size
000 = No Data (Default)
001 = 1 bit of data
010 = 2 bits of data
011 = 3 bits of data
100 = 4 bits of data
101 = 5 bits of data
110 = 6 bits of data
111 = 7 bits of data

21.6.2 UART Receive Status Register (UARTRXST)

Address FFF7EC04 – UART 0 Receive Status Register
Address FFF7ED04 – UART 1 Receive Status Register

Bit Number	4	3	2	1	0
Bit Name	RX_IDLE	SLEEP	RX_RDY	RX_WAKE	RX_ENA
Access	R	R/W	R	R	R/W
Default	-	0	-	-	0

Bit 4: RX_IDLE –RX Idle status bit

0 = Not in Rx Idle State
1 = Rx Idle detected

Bit 3: SLEEP – Sleep Mode Configuration
0 = Sleep Mode disabled (Default)
1 = Sleep Mode enabled

Bit 2: RX_RDY – UART Receiver ready status bit
0 = UART Receiver not ready
1 = UART Receiver ready

Bit 1: RX_WAKE – UART Receiver wake status bit
0 = UART Receiver has not entered wakeup state
1 = UART Receiver has entered wakeup state

Bit 0: RX_ENA – Turns on UART Receiver
0 = UART Receiver disabled (Default)
1 = UART Receiver enabled

21.6.3 UART Transmit Status Register (UARTTXST)

Address FFF7EC08 – UART 0 Transmit Status Register
Address FFF7ED08 – UART 1 Transmit Status Register

Bit Number	7	6	5:4
Bit Name	CONTINUE	LOOPBACK	RESERVED
Access	R/W	R/W	-
Default	0	0	00

Bit Number	3	2	1	0
Bit Name	TX_EMPTY	TX_RDY	TX_WAKE	TX_ENA
Access	R	R	R/W	R/W
Default	-	-	0	0

Bit 7: CONTINUE – Configure operation in suspend mode
0 = Stop transmitting on suspend (Default)
1 = Continue transmitting after initiation of suspend

Bit 6: LOOPBACK – Loopback Mode Configuration
0 = Normal mode (Default)
1 = Loopback Mode

Bit 5-4: RESERVED – Unused bits – Default to 00

Bit 3: TX_EMPTY – Transmit buffer status
0 = Transmit buffer is not empty
1 = Transmit buffer is empty

Bit 2: TX_RDY – Transmitter Ready
0 = UART Transmitter is not ready
1 = UART Transmitter is ready to transmit data

Bit 1: TX_WAKE – TX wake control bit
0 = UART Transmitter Wakeup disabled (Default)
1 = UART Transmitter Wakeup enabled

Bit 0: TX_ENA – Turns on TX module
0 = UART Transmitter Disabled (Default)
1 = UART Transmitter Enabled

21.6.4 UART Control Register 3 (UARTCTRL3)

Address FFF7EC0C – UART 0 Control Register 3
Address FFF7ED0C – UART 1 Control Register 3

Bit Number	7	6	5	4

Bit Name	SW_RESET	POWERDOWN	CLOCK	RX_INT_ENA
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	TX_INT_ENA	WAKEUP_INT_ENA	BRKDT_INT_ENA	ERR_INT_ENA
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 7: SW_RESET – Software reset for UART Transmitter/Receiver
0 = Disables Software Reset (Default)
1 = Enables Software Reset
Bit 6: POWERDOWN – Power-down Transmitter/Receiver Control
0 = Disables Power-down mode (Default)
1 = Enables Power-down mode
Bit 5: CLOCK_ENA – UART Clock Select
0 = Selects external clock (Default)
1 = Selects internal clock
Bit 4: RX_INT_ENA – Enables the interrupts from UART Receiver
0 = Disables interrupts from UART Receiver (Default)
1 = Enables interrupts from UART Receiver
Bit 3: TX_INT_ENA – Enables the interrupts from UART Transmitter
0 = Disables interrupts from UART Transmitter (Default)
1 = Enables interrupts from UART Transmitter
Bit 2: WAKEUP_INT_ENA – Enables the wakeup interrupt from UART
0 = Disables Wakeup Interrupt (Default)
1 = Enables Wakeup Interrupt
Bit 1: BRKDT_INT_ENA – Enables the Broken Circuit interrupt from UART Receiver
0 = Disables Broken Circuit Interrupt (Default)
1 = Enables Broken Circuit Interrupt
Bit 0: ERR_INT_ENA – Enables UART Receiver Error Interrupt
0 = Disables UART Receiver Error Interrupt (Default)
1 = Enables UART Receiver Error Interrupt

21.6.5 UART Interrupt Status Register (UARTINTST)

Address FFF7EC10 – UART 0 Interrupt Status Register
Address FFF7ED10 – UART 1 Interrupt Status Register

Bit Number	7	6	5	4
Bit Name	BUS_BUSY	RESERVED	FRAME_ERR	OVERRUN_ERR
Access	R	-	R	R
Default	-	0	-	-

Bit Number	3	2	1	0
Bit Name	PARITY_ERR	WAKEUP_INT	BRKDT_INT	RX_ERR
Access	R	R	R	R
Default	-	-	-	-

Bit 7: BUS_BUSY – UART Receiver Busy Indicator
0 = UART Receiver ready to accept new frame
1 = UART Receiver currently processing message
Bit 6: RESERVED – Unused bit – Default to 0
Bit 5: FRAME_ERR – UART Receiver Framing Error
0 = No framing error found within incoming data message
1 = Indicates the incoming data message had a framing error
Bit 4: OVERRUN_ERR – UART Receiver Buffer Overflow
0 **=** No overflow condition found in receive buffer
1 = Indicates the receive buffer has overflowed
Bit 3: PARITY_ERR – UART Receiver Parity Error
0 = No parity error found on the incoming data message
1 = Indicates a parity error found on the incoming data message
Bit 2: WAKEUP_INT – UART Receiver Wakeup Interrupt
0 = No Wakeup Interrupt received from UART Receiver
1 = Wakeup Interrupt received from UART Receiver
Bit 1: BRKDT_INT – UART Receiver Broken Circuit Interrupt
0 = No Broken Circuit interrupt received from UART Receiver
1 = Indicates a Broken Circuit interrupt received from UART Receiver
Bit 0: RX_ERR – UART Receiver Error
0 = No UART Receiver Errors detected
1 = Frame Error or Overrun error or Parity Error or Broken Circuit error received from UART Receiver

21.6.6 UART Baud Divisor High Byte Register (UARTHBAUD)

Address FFF7EC14 – UART 0 Baud Divisor High Byte Register
Address FFF7ED14 – UART 1 Baud Divisor High Byte Register

Bit Number	7:0
Bit Name	BAUD_DIV_H
Access	R/W
Default	0000_0000

Bits 7-0: BAUD_DIV_H - Sets the high byte of the 24 bit baud rate selector

21.6.7 UART Baud Divisor Middle Byte Register (UARTMBAUD)

Address FFF7EC18 – UART 0 Baud Divisor Middle Byte Register
Address FFF7ED18 – UART 1 Baud Divisor Middle Byte Register

Bit Number	7:0
Bit Name	BAUD_DIV_M
Access	R/W
Default	0000_0000

Bits 7-0: BAUD_DIV_M - Sets the middle byte of the 24 bit baud rate selector

21.6.8 UART Baud Divisor Low Byte Register (UARTLBAUD)

Address FFF7EC1C – UART 0 Baud Divisor Low Byte Register
Address FFF7ED1C – UART 1 Baud Divisor Low Byte Register

Bit Number	7:0
Bit Name	BAUD_DIV_L
Access	R/W
Default	0000_0000

Bits 7-0: BAUD_DIV_L - Sets the low byte of the 24 bit baud rate selector

21.6.9 UART Receive Buffer (UARTRXBUF)

Address FFF7EC24 – UART 0 Receive Buffer
Address FFF7ED24 – UART 1 Receive Buffer

Bit Number	7:0
Bit Name	RXDAT
Access	R
Default	-

Bits 7-0: RXDAT – Contains the last data byte received from the UART Receiver

21.6.10 UART Transmit Buffer (UARTTXBUF)

Address FFF7EC28 – UART 0 Transmit Buffer
Address FFF7ED28 – UART 1 Transmit Buffer

Bit Number	7:0
Bit Name	TXDAT
Access	R/W
Default	0000_0000

Bits 7-0: TXDAT – Contains the data byte to be transmitted by the UART Transmitter

21.6.11 UART I/O Control Register (UARTIOCTRLSCLK, UARTIOCTRLRX, UARTIOCTRLTX)

Address FFF7EC2C – UART 0 I/O (SCLK) Control Register
Address FFF7ED2C – UART 1 I/O (SCLK) Control Register
Address FFF7EC30 – UART 0 I/O (RX) Control Register
Address FFF7ED30 – UART 1 I/O (RX) Control Register
Address FFF7EC34 – UART 0 I/O (TX) Control Register
Address FFF7ED34 – UART 1 I/O (TX) Control Register

Bit Number	3	2	1	0
Bit Name	DATA_IN	DATA_OUT	IO_FUNC	IO_DIR
Access	R	R/W	R/W	R/W
Default	-	0	0	0

Bit 3: DATA_IN – Data received from pin when configured as GPIO
Bit 2: DATA_OUT – Data transmitted to pin when configured as GPIO
Bit 1: IO_FUNC – Selects the function for UART pins
0 = GPIO mode (Default)
1 = Baud Clock for SCLK, Normal operation for SCI_RX/SCI_TX
Bit 0: IO_DIR – Pin direction when configured as GPIO
0 = Input (Default)
1 = Output

21.7 *ADC Registers*

21.7.1 ADC Control Register (ADCCTRL)

Address 00140000

Bit Number	31:24	23	22
Bit Name	EXT_TRIG_DLY	EXT_TRIG_GPIO_VAL	EXT_TRIG_GPIO_DIR
Access	R/W	R/W	R/W
Default	0000_0000	0	0

Bit Number	21	20	19:16	15:13
Bit Name	EXT_TRIG_GPIO_EN	EXT_TRIG_EN	EXT_TRIG_SEL	SAMPLING_SEL
Access	R/W	R/W	R/W	R/W
Default	0	0	0000	000

Bit Number	12	11	10:8	7:4
Bit Name	ADC_SEL_REF	ADC_ROUND	BYPASS_EN	MAX_CONV
Access	R/W	R/W	R/W	R/W
Default	0	0	111	0000

Bit Number	3	2	1	0
Bit Name	SINGLE_SWEEP	SW_START	ADC_INT_EN	ADC_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bits 31-24: EXT_TRIG_DLY – 8-bit External ADC Trigger Delay configuration, LSB bit resolution equals period of ADC Clock (High Frequency Oscillator Frequency divided by 4)
Bit 23: EXT_TRIG_GPIO_VAL – Output value of ADC_EXT_TRIG pin when configured in GPIO mode
0 = ADC_EXT_TRIG pin driven low (Default)
1 = ADC_EXT_TRIG pin driven high
Bit 22: EXT_TRIG_GPIO_DIR – Direction of ADC_EXT_TRIG pin when configured in GPIO mode
0 = ADC_EXT_TRIG pin configured as input (Default)
1 = ADC_EXT_TRIG pin configured as output
Bit 21: EXT_TRIG_GPIO_EN – Configuration of ADC_EXT_TRIG pin
0 = ADC_EXT_TRIG pin configured in functional mode (Default)
1 = ADC_EXT_TRIG pin configured in GPIO mode
Bit 20: EXT_TRIG_EN – External Trigger Enable, conversions are started using the external trigger as selectable by the **EXT_TRIG_SEL** bits.
0 = Disable External Trigger capability (Default)
1 = Enable External Trigger capability

Bits 19-16: EXT_TRIG_SEL – Selects which external trigger can start a conversion loop.
0 = HS Loop1 Event 1 (DPWMA Low Resolution Edge) (Default)
1 = HS Loop1 Event 3 (DPWMB Low Resolution Edge)
2 = HS Loop2 Event 1 (DPWMA Low Resolution Edge)
3 = HS Loop2 Event 3 (DPWMB Low Resolution Edge)
4 = HS Loop3 Event 1 (DPWMA Low Resolution Edge)
5 = HS Loop3 Event 3 (DPWMB Low Resolution Edge)

6 = HS Loop4 Event 1 (DPWMA Low Resolution Edge)
7 = HS Loop4 Event 3 (DPWMB Low Resolution Edge)
8 = ADC_EXT_TRIG pin
9 = Analog Comparator A Output
A = Analog Comparator B Output
B = Analog Comparator C Output
C = Analog Comparator D Output
D = Analog Comparator E Output
E = Analog Comparator F Output
F = Analog Comparator G Output

Bits 15-13: SAMPLING_SEL - Defines ADC sampling and hold timing setup, refer to ADC Specification for details on timing options

111 = 1008KS/s
110 = 268KS/s (Default)
101 = 1008KS/s
100 = 538KS/s
011 = 504KS/s
010 = 744KS/s
001 = 744KS/s
000 = 268KS/s

Bit 12: ADC_SEL_REF – ADC Voltage Reference Select

0 = Selects Internal ADC voltage reference (Default)
1 = Selects AVDD as ADC voltage reference

Bit 11: ADC_ROUND – Enables rounding of ADC Result to 10 bits

0 = ADC Results are not rounded (Default)
1 = ADC Results are rounded to 10 most significant bits

Bits 10-8: BYPASS_EN – Enables dual sample/hold for specific channels. There are only four valid settings:

011 = Dual Sample/Hold enabling on Channel 2
101 = Dual Sample/Hold enabling on Channel 1
110 = Dual Sample/Hold enabling on Channel 0
111 = Dual Sample/Hold Disabled (Default)

Bits 7-4: MAX_CONV – Maximum number of conversion done in one conversion loop

0x0 = 1 conversion selection converted in the loop (Default)
0xF = All 16 conversion selections converted in the loop

Bit 3: SINGLE_SWEEP – ADC Conversion Mode

0 = Continuous conversion loop runs (Default)
1 = Single conversion loop run

Bit 2: SW_START - Firmware ADC Conversion Start, bit will be cleared automatically by hardware at end of ADC conversion

0 = Conversions not initiated by firmware (Default)
1 = Initiate an ADC conversion loop

Bit 1: ADC_INT_EN – End-of-conversion Interrupt Enable

0 = Disable End-of-Conversion Interrupt (Default)
1 = Enable End-of-Conversion Interrupt

Bit 0: ADC_EN – ADC12 Enable Control

0 = Disables ADC Immediately (Default)
1 = Enables ADC

21.7.2 ADC Status Register (ADCSTAT)

Address 00140004

Bit Number	6:3	2	1	0
Bit Name	CURRENT_CH	ADC_EXT_TRIG_VAL	ADC_INT_RAW	ADC_INT
Access	R	R	R	R

Default	-	-	-	-

Bits 6-3: CURRENT_CH – Register shows the currently converting channel
Bit 2: ADC_EXT_TRIG_VAL – ADC_EXT_TRIG pin value
0 = ADC_EXT_TRIG pin driven low
1 = ADC_EXT_TRIG pin driven high
Bit 1: ADC_INT_RAW – End-of-conversion interrupt flag, raw version
0 = No End-of-conversion interrupt detected
1 = End-of-conversion interrupt found
Bit 0: ADC_INT – End-of-conversion interrupt flag, latched version
0 = No End-of-conversion interrupt detected
1 = End-of-conversion interrupt found

21.7.3 ADC Test Control Register (ADCTSTCTRL)

Address 00140008

Bit Number	1	0
Bit Name	ADC_SH_BUFFER_EN	Reserved
Access	R/W	
Default	0	0

Bit 1: ADC_SH_BUFFER_EN - ADC Sample and Hold Buffer Enable
0 = Disables ADC Sample and Hold Buffer for use without Sample and Hold(Default)
1 = Enables ADC Sample and Hold Buffer
Bit 0: RESERVED

Note: Other bits in this register are used for device test. All the other bits should be kept at a zero value during normal operation

21.7.4 ADC Sequence Select Register 0 (ADCSEQSEL0)

Address 0014000C

Bit Number	28	27:24	23:21	20	19:16
Bit Name	SEQ3_SH	SEQ3	RESERVED	SEQ2_SH	SEQ2
Access	R/W	R/W	-	R/W	R/W
Default	0	0000	000	0	0000

Bit Number	15:13	12	11:8	7:5	4	3:0
Bit Name	RESERVED	SEQ1_SH	SEQ1	RESERVED	SEQ0_SH	SEQ0
Access	-	R/W	R/W	-	R/W	R/W
Default	000	0	0000	000	0	0000

Bit 28: SEQ3_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling
Bits 27-24: SEQ3 - Channel to be converted fourth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected
Bits 23-21: RESERVED – Unused bits
Bit 20: SEQ2_SH – Dual channel sequence select

0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 19-16: SEQ2 - Channel to be converted third
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

Bits 15-13: RESERVED – Unused bits

Bit 12: SEQ1_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 11-8: SEQ1 - Channel to be converted second
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

Bits 7-5: RESERVED – Unused bits

Bit 4: SEQ0_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 3-0: SEQ0 - Channel to be converted first
0000 = Channel 0 selected (Default
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

21.7.5 ADC Sequence Select Register 1 (ADCSEQSEL1)

Address 00140010

Bit Number	28	27:24	23:21	20	19:16
Bit Name	SEQ7_SH	SEQ7	RESERVED	SEQ6_SH	SEQ6
Access	R/W	R/W	-	R/W	R/W
Default	0	0000	000	0	0000

Bit Number	15:13	12	11:8	7:5	4	3:0
Bit Name	RESERVED	SEQ5_SH	SEQ5	RESERVED	SEQ4_SH	SEQ4
Access	-	R/W	R/W	-	R/W	R/W
Default	000	0	0000	000	0	0000

Bit 28 SEQ7_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 27-24: SEQ7- Channel to be converted eighth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

Bits 23-21: RESERVED – Unused bits

Bit 20: SEQ6_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 19-16: SEQ6 - Channel to be converted seventh
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected

…….
1111 = Temp Sensor selected
Bits 15-13: RESERVED – Unused bits
Bit 12: SEQ5_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling
Bits 11-8: SEQ5 - Channel to be converted sixth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected
Bits 7-5: RESERVED – Unused bits
Bit 4: SEQ4_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling
Bits 3-0: SEQ4 - Channel to be converted fifth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

21.7.6 ADC Sequence Select Register 2 (ADCSEQSEL2)

Address 00140014

Bit Number	28	27:24	23:21	20	19:16
Bit Name	SEQ11_SH	SEQ11	RESERVED	SEQ10_SH	SEQ10
Access	R/W	R/W	-	R/W	R/W
Default	0	0000	000	0	0000

Bit Number	15:13	12	11:8	7:5	4	3:0
Bit Name	RESERVED	SEQ9_SH	SEQ9	RESERVED	SEQ8_SH	SEQ8
Access	-	R/W	R/W	-	R/W	R/W
Default	000	0	0000	000	0	00000

Bit 28: SEQ11_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling
Bits 27-24: SEQ11 - Channel to be converted twelth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected
Bits 23-21: RESERVED – Unused bits
Bit 20: SEQ10_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling
Bits 19-16: SEQ10 - Channel to be converted eleventh
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected
Bits 15-13: RESERVED – Unused bits
Bit 12: SEQ9_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)

1 = Selected for Dual Sampling

Bits 11-8: SEQ9 - Channel to be converted tenth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

Bits 7-5: RESERVED – Unused bits

Bit 4: SEQ8_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 3-0: SEQ8 - Channel to be converted ninth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

21.7.7 ADC Sequence Select Register 3 (ADCSEQSEL3)

Address 00140018

Bit Number	28	27:24	23:21	20	19:16
Bit Name	SEQ15_SH	SEQ15	RESERVED	SEQ14_SH	SEQ14
Access	R/W	R/W	-	R/W	R/W
Default	0	0000	000	0	0000

Bit Number	15:13	12	11:8	7:5	4	3:0
Bit Name	RESERVED	SEQ13_SH	SEQ13	RESERVED	SEQ12_SH	SEQ12
Access	-	R/W	R/W	-	R/W	R/W
Default	000	0	0000	000	0	0000

Bit 28: SEQ15_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 27-24: SEQ15 - Channel to be converted sixteenth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

Bits 23-21: RESERVED – Unused bits

Bit 20: SEQ14_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 19-16: SEQ14 - Channel to be converted fifteenth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….
1111 = Temp Sensor selected

Bits 15-13: RESERVED – Unused bits

Bit 12: SEQ13_SH – Dual channel sequence select
0 = Not selected for Dual Sampling (Default)
1 = Selected for Dual Sampling

Bits 11-8: SEQ13 - Channel to be converted fourteenth
0000 = Channel 0 selected (Default)
0001 = Channel 1 selected
…….

1111 = Temp Sensor selected

Bits 7-5: RESERVED – Unused bits

Bit 4: SEQ12_SH – Dual channel sequence select

0 = Not selected for Dual Sampling (Default)

1 = Selected for Dual Sampling

Bits 3-0: SEQ12 - Channel to be converted thirteenth

0000 = Channel 0 selected (Default)

0001 = Channel 1 selected

…….

1111 = Temp Sensor selected

21.7.8 ADC Result Registers 0-15 (ADCRESULTx, x=0:15)

Address 0014001C – ADC Result Register 0
Address 00140020 – ADC Result Register 1
Address 00140024 – ADC Result Register 2
Address 00140028 – ADC Result Register 3
Address 0014002C – ADC Result Register 4
Address 00140030 – ADC Result Register 5
Address 00140034 – ADC Result Register 6
Address 00140038 – ADC Result Register 7
Address 0014003C – ADC Result Register 8
Address 00140040 – ADC Result Register 9
Address 00140044 – ADC Result Register 10
Address 00140048 – ADC Result Register 11
Address 0014004C – ADC Result Register 12
Address 00140050 – ADC Result Register 13
Address 00140054 – ADC Result Register 14
Address 00140058 – ADC Result Register 15

Bit Number	11:0
Bit Name	RESULT
Access	R
Default	-

Bits 11-0: RESULT – Each sequence has a dedicated result register**.**

21.7.9 ADC Averaged Result Registers 0-5 (ADCAVGRESULTx, x=0:15)

Address 0014005C – ADC Averaged Result Register 0
Address 00140060 – ADC Averaged Result Register 1
Address 00140064 – ADC Averaged Result Register 2
Address 00140068 – ADC Averaged Result Register 3
Address 0014006C – ADC Averaged Result Register 4
Address 00140070 – ADC Averaged Result Register 5

Bit Number	11:0
Bit Name	RESULT
Access	R
Default	-

Bits 11-0: RESULT – First 6 ADC Results have an averaged result

21.7.10 ADC Digital Compare Limits Register 0-5 (ADCCOMPLIMx, x=0:5)

Address 00140074 – ADC Digital Compare Limits Register 0
Address 00140078 – ADC Digital Compare Limits Register 1
Address 0014007C – ADC Digital Compare Limits Register 2
Address 00140080 – ADC Digital Compare Limits Register 3
Address 00140084 – ADC Digital Compare Limits Register 4
Address 00140088 – ADC Digital Compare Limits Register 5

Bit Number	27:16	15:12	11:0
Bit Name	UPPER_LIMIT	RESERVED	LOWER_LIMIT
Access	R/W	-	R/W
Default	1111_1111_1111	0000	0000_0000_0000

Bits 27-16: UPPER_LIMIT – Configures the upper limit value. If the ADC conversion selected is equal or greater than the limit, the Digital Compare Interrupt Flag is set (bit 22 of ADC Control Register 1). Results of comparison can be read from the ADC Digital Compare Results Register (see Section 4.12).
Bits 15-12: RESERVED – Unused bits – Default to 0000
Bits 11-0: LOWER_LIMIT – Configures the lower limit value. If the ADC conversion selected is equal or less than the limit, the Digital Compare Interrupt Flag is set (bit 22 of ADC Control Register 1). Results of comparison can be read from the ADC Digital Compare Results Register (see Section 4.12).

21.7.11 ADC Digital Compare Enable Register (ADCCOMPEN)

Address 0014008C

Bit Number	27	26	25	24
Bit Name	COMP5_UP_INT_EN	COMP5_LO_INT_EN	COMP4_UP_INT_EN	COMP4_LO_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	23	22	21	20
Bit Name	COMP3_UP_INT_EN	COMP3_LO_INT_EN	COMP2_UP_INT_EN	COMP2_LO_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	19	18	17	16
Bit Name	COMP1_UP_INT_EN	COMP1_LO_INT_EN	COMP0_UP_INT_EN	COMP0_LO_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	15:14	13	12	11
Bit Name	RESERVED	COMP5_DATA_SEL	COMP4_DATA_SEL	COMP3_DATA_SEL
Access	-	R/W	R/W	R/W
Default	00	0	0	0

Bit Number	10	9	8	7:6
Bit Name	COMP2_DATA_SEL	COMP1_DATA_SEL	COMP0_DATA_SEL	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	00

Bit Number	5	4	3	2	1	0
Bit Name	COMP5_EN	COMP4_EN	COMP3_EN	COMP2_EN	COMP1_EN	COMP0_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0

Bit 27: COMP5_UP_INT_EN – Digital Comparator 5 Upper Limit Interrupt Enable
0 = Interrupt generation disabled on result above upper limit (Default)
1 = Interrupt generation enabled on result above upper limit
Bit 26: COMP5_LO_INT_EN – Digital Comparator 5 Lower Limit Interrupt Enable
0 = Interrupt generation disabled on result below lower limit (Default)
1 = Interrupt generation enabled on result below lower limit
Bit 25: COMP4_UP_INT_EN – Digital Comparator 4 Upper Limit Interrupt Enable
0 = Interrupt generation disabled on result above upper limit (Default)
1 = Interrupt generation enabled on result above upper limit
Bit 24: COMP4_LO_INT_EN – Digital Comparator 4 Lower Limit Interrupt Enable
0 = Interrupt generation disabled on result below lower limit (Default)
1 = Interrupt generation enabled on result below lower limit
Bit 23: COMP3_UP_INT_EN – Digital Comparator 3 Upper Limit Interrupt Enable
0 = Interrupt generation disabled on result above upper limit (Default)
1 = Interrupt generation enabled on result above upper limit

Bit 22: COMP3_LO_INT_EN – Digital Comparator 3 Lower Limit Interrupt Enable
0 = Interrupt generation disabled on result below lower limit (Default)
1 = Interrupt generation enabled on result below lower limit
Bit 21: COMP2_UP_INT_EN – Digital Comparator 2 Upper Limit Interrupt Enable
0 = Interrupt generation disabled on result above upper limit (Default)
1 = Interrupt generation enabled on result above upper limit
Bit 20: COMP2_LO_INT_EN – Digital Comparator 2 Lower Limit Interrupt Enable
0 = Interrupt generation disabled on result below lower limit (Default)
1 = Interrupt generation enabled on result below lower limit
Bit 19: COMP1_UP_INT_EN – Digital Comparator 1 Upper Limit Interrupt Enable
0 = Interrupt generation disabled on result above upper limit (Default)
1 = Interrupt generation enabled on result above upper limit
Bit 18: COMP1_LO_INT_EN – Digital Comparator 1 Lower Limit Interrupt Enable
0 = Interrupt generation disabled on result below lower limit (Default)
1 = Interrupt generation enabled on result below lower limit
Bit 17: COMP0_UP_INT_EN – Digital Comparator 0 Upper Limit Interrupt Enable
0 = Interrupt generation disabled on result above upper limit (Default)
1 = Interrupt generation enabled on result above upper limit
Bit 16: COMP0_LO_INT_EN – Digital Comparator 0 Lower Limit Interrupt Enable
0 = Interrupt generation disabled on result below lower limit (Default)
1 = Interrupt generation enabled on result below lower limit
Bits 15-14: RESERVED – Unused bits
Bit 13: COMP5_DATA_SEL – Digital Comparator 5 Data Select
0 = Raw ADC Result 5 used for comparison (Default)
1 = Averaged ADC Result 5 used for comparison
Bit 12: COMP4_DATA_SEL – Digital Comparator 4 Data Select
0 = Raw ADC Result 4 used for comparison (Default)
1 = Averaged ADC Result 4 used for comparison
Bit 11: COMP3_DATA_SEL – Digital Comparator 3 Data Select
0 = Raw ADC Result 3 used for comparison (Default)
1 = Averaged ADC Result 3 used for comparison
Bit 10: COMP2_DATA_SEL – Digital Comparator 2 Data Select
0 = Raw ADC Result 2 used for comparison (Default)
1 = Averaged ADC Result 2 used for comparison
Bit 9: COMP1_DATA_SEL – Digital Comparator 1 Data Select
0 = Raw ADC Result 1 used for comparison (Default)
1 = Averaged ADC Result 1 used for comparison
Bit 8: COMP0_DATA_SEL – Digital Comparator 0 Data Select
0 = Raw ADC Result 0 used for comparison (Default)
1 = Averaged ADC Result 0 used for comparison
Bits 7-6: RESERVED – Unused bits
Bit 5: COMP5_EN – Digital Comparator 5 Enable
0 = Comparator Disabled (Default)
1 = Comparator Enabled
Bit 4: COMP4_EN – Digital Comparator 4 Enable
0 = Comparator Disabled (Default)
1 = Comparator Enabled
Bit 3: COMP3_EN – Digital Comparator 3 Enable
0 = Comparator Disabled (Default)
1 = Comparator Enabled
Bit 2: COMP2_EN – Digital Comparator 2 Enable
0 = Comparator Disabled (Default)
1 = Comparator Enabled
Bit 1: COMP1_EN – Digital Comparator 1 Enable
0 = Comparator Disabled (Default)
1 = Digital Comparator 1 Enabled

Bit 0: COMP0_EN – Digital Comparator 0 Enable
0 = Comparator Disabled (Default)
1 = Comparator Enabled

21.7.12 ADC Digital Compare Results Register (ADCCOMPRESULT)

Address 00140090

Bit Number	27	26	25	24
Bit Name	DCOMP5_UP_RAW	DCOMP5_LO_RAW	DCOMP4_UP_RAW	DCOMP4_LO_RAW
Access	R	R	R	R
Default	-	-	-	-

Bit Number	23	22	21	20
Bit Name	DCOMP3_UP_RAW	DCOMP3_LO_RAW	DCOMP2_UP_RAW	DCOMP2_LO_RAW
Access	R	R	R	R
Default	-	-	-	-

Bit Number	19	18	17	16
Bit Name	DCOMP1_UP_RAW	DCOMP1_LO_RAW	DCOMP0_UP_RAW	DCOMP0_LO_RAW
Access	R	R	R	R
Default	-	-	-	-

Bit Number	15:12	11	10	9
Bit Name	RESERVED	DCOMP5_UP_INT	DCOMP5_LO_INT	DCOMP4_UP_INT
Access	-	R	R	R
Default	0000	-	-	-

Bit Number	8	7	6	5
Bit Name	DCOMP4_LO_INT	DCOMP3_UP_INT	DCOMP3_LO_INT	DCOMP2_UP_INT
Access	R	R	R	R
Default	-	-	-	-

Bit Number	4	3	2	1
Bit Name	DCOMP2_LO_INT	DCOMP1_UP_INT	DCOMP1_LO_INT	DCOMP0_UP_INT
Access	R	R	R	R
Default	-	-	-	-

Bit Number	0
Bit Name	DCOMP0_LO_INT
Access	R
Default	-

Bit 27: DCOMP5_UP_RAW – Digital Comparator 5 Upper Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded

Bit 26: DCOMP5_LO_RAW – Digital Comparator 5 Lower Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded

Bit 25: DCOMP4_UP_RAW – Digital Comparator 4 Upper Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded

Bit 24: DCOMP4_LO_RAW – Digital Comparator 4 Lower Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 23: DCOMP3_UP_RAW – Digital Comparator 3 Upper Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 22: DCOMP3_LO_RAW – Digital Comparator 3 Lower Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 21: DCOMP2_UP_RAW – Digital Comparator 2 Upper Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 20: DCOMP2_LO_RAW – Digital Comparator 2 Lower Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 19: DCOMP1_UP_RAW – Digital Comparator 1 Upper Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 18: DCOMP1_LO_RAW – Digital Comparator 1 Lower Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 17: DCOMP0_UP_RAW – Digital Comparator 0 Upper Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bit 16: DCOMP0_LO_RAW – Digital Comparator 0 Lower Limit Raw Result
0 = Limit not exceeded
1 = Limit exceeded
Bits 15-12: RESERVED – Unused bits
Bit 11: DCOMP5_UP_INT – Digital Comparator 5 Upper Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 10: DCOMP5_LO_INT – Digital Comparator 5 Lower Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 9: DCOMP4_UP_INT – Digital Comparator 4 Upper Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 8: DCOMP4_LO_INT – Digital Comparator 4 Lower Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 7: DCOMP3_UP_INT – Digital Comparator 3 Upper Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 6: DCOMP3_LO_INT – Digital Comparator 3 Lower Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 5: DCOMP2_UP_INT – Digital Comparator 2 Upper Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 4: DCOMP2_LO_INT – Digital Comparator 2 Lower Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 3: DCOMP1_UP_INT – Digital Comparator 1 Upper Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded
Bit 2: DCOMP1_LO_INT – Digital Comparator 1 Lower Limit Interrupt Result, cleared on read

0 = Limit not exceeded
1 = Limit exceeded

Bit 1: DCOMP0_UP_INT – Digital Comparator 0 Upper Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded

Bit 0: DCOMP0_LO_INT – Digital Comparator 0 Lower Limit Interrupt Result, cleared on read
0 = Limit not exceeded
1 = Limit exceeded

21.7.13 ADC Averaging Control Register (ADCAVGCTRL)

Address 00140094

Bit Number	22:21	20	19	18:17	16
Bit Name	AVG5_CONFIG	AVG5_EN	RESERVED	AVG4_CONFIG	AVG4_EN
Access	R/W	R/W	-	R/W	R/W
Default	00	0	0	00	0

Bit Number	15	14:13	12	11
Bit Name	RESERVED	AVG3_CONFIG	AVG3_EN	RESERVED
Access	-	R/W	R/W	-
Default	0	00	0	0

Bit Number	10:9	8	7	6:5
Bit Name	AVG2_CONFIG	AVG2_EN	RESERVED	AVG1_CONFIG
Access	R/W	R/W	-	R/W
Default	00	0	0	00

Bit Number	4	3	2:1	0
Bit Name	AVG1_EN	RESERVED	AVG0_CONFIG	AVG0_EN
Access	R/W	-	R/W	R/W
Default	0	0	00	0

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Bits 22-21: AVG5_CONFIG – ADC Averaging Module 5 Configuration
0 = Moving average of 4 samples (Default)
1 = Moving average of 8 samples
2 = Moving average of 16 samples
3 = Moving average of 32 samples
Bit 20: AVG5_EN – ADC Averaging Module 5 Enable
0 = ADC Averaging Disabled (Default)
1 = ADC Averaging Enabled
Bit 19: RESERVED – Unused bit
Bits 18-17: AVG4_CONFIG – ADC Averaging Module 4 Configuration
0 = Moving average of 4 samples (Default)
1 = Moving average of 8 samples
2 = Moving average of 16 samples
3 = Moving average of 32 samples
Bit 16: AVG4_EN – ADC Averaging Module 4 Enable
0 = ADC Averaging Disabled (Default)
1 = ADC Averaging Enabled
Bit 15: RESERVED – Unused bit
Bits 14-13: AVG3_CONFIG – ADC Averaging Module 3 Configuration
0 = Moving average of 4 samples (Default)
1 = Moving average of 8 samples
2 = Moving average of 16 samples
3 = Moving average of 32 samples
Bit 12: AVG3_EN – ADC Averaging Module 3 Enable
0 = ADC Averaging Disabled (Default)
1 = ADC Averaging Enabled
Bit 11: RESERVED – Unused bit
Bits 10-9: AVG2_CONFIG – ADC Averaging Module 2 Configuration

0 = Moving average of 4 samples (Default)
1 = Moving average of 8 samples
2 = Moving average of 16 samples
3 = Moving average of 32 samples

Bit 8: AVG2_EN – ADC Averaging Module 4 Enable
0 = ADC Averaging Disabled (Default)
1 = ADC Averaging Enabled

Bit 7: RESERVED – Unused bit

Bits 6-5: AVG1_CONFIG – ADC Averaging Module 1 Configuration
0 = Moving average of 4 samples (Default)
1 = Moving average of 8 samples
2 = Moving average of 16 samples
3 = Moving average of 32 samples

Bit 4: AVG1_EN – ADC Averaging Module 1 Enable
0 = ADC Averaging Disabled (Default)
1 = ADC Averaging Enabled

Bit 3: RESERVED – Unused bit

Bits 2-1: AVG0_CONFIG – ADC Averaging Module 0 Configuration
0 = Moving average of 4 samples (Default)
1 = Moving average of 8 samples
2 = Moving average of 16 samples
3 = Moving average of 32 samples

Bit 0: AVG0_EN – ADC Averaging Module 0 Enable
0 = ADC Averaging Disabled (Default)
1 = ADC Averaging Enabled

21.8 *DPWM 0-3 Registers*

21.8.1 DPWM Control Register 0 (DPWMCTRL0)

Address 00150000 – DPWM 3 Control Register 0
Address 00170000 – DPWM 2 Control Register 0
Address 001A0000 – DPWM 1 Control Register 0
Address 001D0000 – DPWM 0 Control Register 0

Bit Number	31:28	27:24	23
Bit Name	PWM_B_INTRA_MUX	PWM_A_INTRA_MUX	CBC_PWM_C_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	22:21	20	19
Bit Name	RESERVED	CBC_PWM_AB_EN	CBC_ADV_CNT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	18:17	16	15
Bit Name	MIN_DUTY_MODE	RESERVED	MSYNC_SLAVE_EN
Access	R/W	R/W	R/W
Default	00	0	0

Bit Number	14	13
Bit Name	D_ENABLE	RESERVED
Access	R/W	R/W
Default	0	0

Bit Number	12	11	10
Bit Name	RESON_MODE_FIXED_DUTY_EN	PWM_B_FLT_POL	PWM_A_FLT_POL
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	9	8	7:4
Bit Name	BLANK_B_EN	BLANK_A_EN	PWM_MODE
Access	R/W	R/W	R/W
Default	0	0	0010

Bit Number	3	2	1	0
Bit Name	PWM_B_INV	PWM_A_INV	CLA_EN	PWM_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	1	0

Bits 31-28: PWM_B_INTRA_MUX – Interchanges DPWM signals post edge generation
0 = Pass-through (Default)
1 = Edge-gen output, this module

2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bits 27-24: PWM_A_INTRA_MUX – Combines DPWM signals are prior to HR module
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bit 23: CBC_PWM_C_EN – Sets if Fault CBC changes output waveform for PWM-C
0 = PWM-C unaffected by Fault CBC (Default)
1 = PWM-C affected by Fault CBC

Bit 21:22: RESERVED

Bit 20: CBC_PWM_AB_EN – Sets if Fault CBC changes output waveform for PWM-A and PWM-B
0 **=** PWM-A and PWM-B unaffected by Fault CBC (Default)
1 **=** PWM-A and PWM-B affected by Fault CBC

Bit 19: CBC_ADV_CNT_EN – Selects cycle-by-cycle of operation
Normal Mode
0 = CBC disabled (Default)
1 = CBC enabled
Multi and Resonant Modes
0 = PWM-A and PWM-B operate independently (Default)
1 = PWM-A and PWM-B pulse matching enabled

Bits 18-17: MIN_DUTY_MODE – Minimum Duty Cycle Mode
00 = Suppression of minimum duty cycles is disabled (Default)
01 = CLA value is clamped to zero when below input value is less than MIN_DUTY_LOW
10 = CLA value is clamped to MIN_DUTY_LOW register value when input value is less than MIN_DUTY_LOW

Bit 16: RESERVED

Bit 15: MSYNC_SLAVE_EN – Multi-Sync Slave Mode Control
0 = PWM not synchronized to another PWM channel (Default)
1 = Enable Multi-Sync Slave Mode, current channel will be slaved from corresponding channel

Bit 14: D_ENABLE – Converts CLA duty value to DPWM as period-CLA duty value
0 = Value used for event calculations if CLA Duty (Default)
1 = Value used for event calculations is period minus CLA duty value

Bit 13: RESERVED

Bit 12: RESON_MODE_FIXED_DUTY_EN – Configures how duty cycle is controlled in Resonance Mode

0 = Resonant mode duty cycle set by Filter duty (Default)
1 = Resonant mode duty cycle set by Auto Switch High Register

Bit 11: PWM_B_FLT_POL – Sets the fault output polarity during a disable condition (that is, fault or module disabled)
0 = PWM B fault output polarity is set to low (Default)
1 = PWM B fault output polarity is set to high

Bit 10: PWM_A_FLT_POL – Sets the fault output polarity during a disable condition (that is, fault or module disabled)
0 = PWM A fault output polarity is set to low (Default)
1 = PWM A fault output polarity is set to high

Bit 9: BLANK_B_EN – Comparator Blanking Window B Enable
0 = Comparator Blanking Window for PWM-B Disabled (Default)
1 = Comparator Blanking Window for PWM-B Enabled

Bit 8: BLANK_A_EN – Comparator Blanking Window A Enable
0 = Comparator Blanking Window for PWM-A Disabled (Default)
1 = Comparator Blanking Window for PWM-B Enabled

Bits 7-4: PWM_MODE – DPWM Mode
0 = Normal Mode
1 = Resonant Mode
2 = Multi-Output Mode
3 = Triangular Mode
4 = Leading Mode

Bit 3: PWM_B_INV – PWM B Output Polarity Control
0 = Non-inverted PWM B output (Default)
1 = Inverts PWM B output

Bit 2: PWM_A_INV – PWM A Output Polarity Control
0 = Non-inverted PWM A output (Default)
1 = Inverted PWM A output

Bit 1: CLA_EN– CLA Processing Enable
0 = Generate PWM waveforms from PWM Register values (Default)
1 = Enable CLA input

Bit 0: PWM_EN – PWM Processing Enable
0 = Disable PWM module, outputs zero (Default)
1 = Enable PWM operation

21.8.2 DPWM Control Register 1 (DPWMCTRL1)

Address 00150004 – DPWM 3 Control Register 1
Address 00170004 – DPWM 2 Control Register 1
Address 001A0004 – DPWM 1 Control Register 1
Address 001D0004 – DPWM 0 Control Register 1

Bit Number	31	30	29
Bit Name	PRESET_EN	SYNC_FET_EN	BURST_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	28	27:24	23:21
Bit Name	CLA_DUTY_ADJ_EN	SYNC_OUT_DIV_SEL	CLA_SCALE
Access	R/W	R/W	R/W
Default	0	000	000

Bit Number	20	19	18
Bit Name	EXT_SYNC_EN	CBC_BSIDE_ACTIVE EN	AUTO_MODE_SEL
Access	R/W	R/W	R/W
Default	1	1	0

Bit Number	17	16	15	14
Bit Name	RESERVED	EVENT_UP_SEL	CHECK_OVERRIDE	GLOBAL_PERIOD_EN
Access	R/W	R/W	R/W	R/W
Default	0	1	1	0

Bit Number	13	12	11	10	9
Bit Name	PWM_B_OE	PWM_A_OE	GPIO_B_VAL	GPIO_B_EN	GPIO_A_VAL
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	8	7	6	5
Bit Name	GPIO_A_EN	PWM_HR_MULTI_OUT_EN	SFRAME_EN	PWM_B_PROT_DIS
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	4	3:2	1	0
Bit Name	PWM_A_PROT_DIS	HIRES_SCALE	RESERVED	HIRES_DIS
Access	R/W	R/W	R/W	R/W
Default	0	00	1	0

Bit 31: PRESET_EN – Counter Preset Enable
0 = Counter reset to 0 upon detection of sync (Default)
1 = Counter preset to Preset Count Value upon detection of sync
Bit 30: SYNC_FET_EN – SyncFET Mode Enabled
0 = SyncFET Mode Disabled (Default)
1 = SyncFET Mode Enabled (Default)

Bit 29: BURST_EN – Burst (Light Load) Mode Detection Enable
0 = Burst Mode (Light Load) Detection disabled (Default)
1 = Burst Mode (Light Load) Detection enabled
Bit 28: CLA_DUTY_ADJ_EN – Enables CLA Duty Adjust from Current/Flux Balancing
0 = CLA Duty Adjust not enabled (Default)
1 = CLA Duty Adjust enabled
Bits 27-24: SYNC_OUT_DIV_SEL – Sets the divider for generating the Sync Out pulse.
0000 = Sync Out generated on every switching cycle (Default)
0001 = Sync Out generated once every 2 switching cycles
0010 = Sync Out generated once every 3 switching cycles
…….
1111 = Sync Out generated once every 16 switching cycles
Bits 23-21: CLA_SCALE – Scaling for CLA Input Data
000 = CLA Value (Default)
001 = CLA Value multiplied by 2
010 = CLA Value divided by 2
011 = CLA Value multiplied by 4
100 = CLA Value divided by 4
101 = CLA Value multiplied by 8
110 = CLA Value divided by 8
111 = CLA Value
Bit 20: EXT SYNC_EN – Slave DPWM to external sync
0 = DPWM not synchronized to external sync (Default)
1 = Slave DPWM to external sync

Bit 19: CBC_BSIDE_ACTIVE_EN – Sets if CBC responds to Fault CBC when PWM-B is active, only available in Multi and Reson modes
0 = Response to Fault CBC when PWM-A active (Default)
1 = Response to Fault CBC when PWM-A or PWM-B active

Bit 18: AUTO_MODE_SEL – Auto Switching Mode Select
0 = Auto Switching Mode disabled (Default)
1 = Auto Switching Mode enabled
Bits 17: RESERVED
Bits 16: EVENT_UP_SEL – Update End Period Mode
0 = Events updated anytime (Default)
1 = Events updated at End of Period
Bit 15: CHECK_OVERRIDE – PWM Check Override
0 = DPWM checks mathematical settings within module, correct placement of Event settings/period settings. Invalid configurations are not allowed. (Default)
1 = Overrides checking for invalid configurations and turns off PWM mathematical checking functions
Bit 14: GLOBAL_PERIOD_EN
0 = Event calculations use DPWM Period register (Default)
1 = Event calculations use Global Period register
Bit 13: PWM_B_OE – Direction for PWM B pin
0 = PWM B configured as output (Default)
1 = PWM B configured as input
Bit 12: PWM_A_OE – Direction for PWM A pin
0 = PWM A configured as output (Default)
1 = PWM A configured as input
Bit 11: GPIO_B_VAL – Sets value of PWM B output in GPIO mode
0 = PWM B driven low in GPIO mode (Default)
1 = PWM B driven high in GPIO mode
Bit 10: GPIO_B_EN – Enables GPIO mode for PWM B output
0 = PWM B in DPWM mode (Default)

1 = PWM B in GPIO mode

Bit 9: GPIO_A_VAL – Sets value of PWM A output in GPIO mode
0 = PWM A driven low in GPIO mode (Default)
1 = PWM A driven high in GPIO mode

Bit 8: GPIO_A_EN – Enables GPIO mode for PWM A output
0 = PWM A in DPWM mode (Default)
1 = PWM A in GPIO mode

Bit 7: PWM_HR_MULT_OUT_EN – Control bit for Hi-Res Block
0 = Disabled (Default)
1 = Enabled

Bit 6: SFRAME_EN – PWM Single Step Frame Mode Enable
0 = Disable Single Frame Mode (Default)
1 = Enable Single Step Frame Mode. One EADC sample is requested, CLA then Filters, then one PWM duty cycle performed, then wait on Single Frame Trigger toggle before advancing to next frame.

Bit 5: PWM_B_PROT_DIS – PWM B Asynchronous Protection Disable
0 = Allows asynchronous protection to turn off PWM B Output (Default)
1 = Disables asynchronous protection from turning off PWM B Output

Bit 4: PWM_A_PROT_DIS – PWM A Asynchronous Protection Disable
0 = Allows asynchronous protection to turn off PWM A Output (Default)
1 = Disables asynchronous protection from turning off PWM A Output

Bits 3-2: HIRES_SCALE – Determines resolution of high resolution steps
00 = Resolution of 16 phases. Full resolution enabled. Resolution step = PCLK/16 (Default)
01 = Resolution of 8 phases. Resolution step = PCLK/8
10 = Resolution of 4 phases. Resolution step = PCLK/4
11 = Resolution of 2 phases. Resolution step = PCLK/2

Bit 1: RESERVED

Bit 0: HIRES_DIS – PWM High Resolution Disable
0 **=** Enable High Resolution logic (Default)
1 **=** Disable High Resolution logic

21.8.3 DPWM Control Register 2 (DPWMCTRL2)

Address 00150008 – DPWM 3 Control Register 2
Address 00170008 – DPWM 2 Control Register 2
Address 001A0008 – DPWM 1 Control Register 2
Address 001D0008 – DPWM 0 Control Register 2

Bit Number	16	15:12	11:10
Bit Name	BLANK_PCM_EN	SYNC_IN_DIV_RATIO	RESERVED
Access	R/W	R/W	R/W
Default	0	0000	0

Bit Number	9:8	7	6
Bit Name	FILTER_DUTY_SEL	IDE_DUTY_B_EN	IDE_DETECT_EN
Access	R/W	R/W	R/W
Default	00	0	0

Bit Number	5:4	3:2
Bit Name	SAMPLE_TRIG1_OVERSAMPLE	SAMPLE_TRIG1_MODE
Access	R/W	R/W
Default	00	000

Bit Number	1	0
Bit Name	SAMPLE_TRIG_2_EN	SAMPLE_TRIG_1_EN
Access	R/W	R/W
Default	0	1

Bit 16: BLANK_PCM_EN – Comparator Blanking Window B Enable for PCM
0 = Comparator Blanking A Window Disabled (Default)
1 = Comparator Blanking A Window for PWM-B Enabled
Bits 15-12: SLAVE_SYNC_IN_DIV_RATIO – Sets the number of syncs to be masked before a resync
Bit 11-10: Reserved
Bits 9-8: FILTER_DUTY_SEL – Sets which register is used for the max duty calculation at the Filter in RESON and MESH modes.
0 = PWM Period Register (Default)
1 = Event 2
2 = PWM Period Adjust Register (Bits 13:0)
Bit 7: IDE_DUTY_B_EN – IDE Duty Cycle Side B Enable
0 = Disabled (Default)
1 = Enabled
Bit 6: IDE_DETECT_EN – IDE Detect Enable
0 = Disabled (Default)
1 = Enabled
Bits 5-4: SAMPLE_TRIG1_OVERSAMPLE – Oversample Select for Sample Trigger 1
00 = Trigger an EADC sample at DPWMSAMPTRIG1 (PWM Sample Trig Register value) (Default)
01 = Trigger EADC samples at (1* DPWMSAMPTRIG1) and at ((1/2)*DPWMSAMPTRIG1)
10 = Trigger EADC samples at (1* DPWMSAMPTRIG1) , ((3/4)*DPWMSAMPTRIG1), ((1/2)*DPWMSAMPTRIG1) and at ((1/4)*DPWMSAMPTRIG1)

11 = Trigger EADC samples at (1* DPWMSAMPTRIG1) , ((7/8)*DPWMSAMPTRIG1), ((3/4)*DPWMSAMPTRIG1), ((5/8)*DPWMSAMPTRIG1) , ((1/2)* DPWMSAMPTRIG1) , ((3/8)*DPWMSAMPTRIG1), ((1/4)*DPWMSAMPTRIG1) and at ((1/8)*DPWMSAMPTRIG1)

Bits 3-2: SAMPLE_TRIG1_MODE – Mode select for Sample Trigger 1
0 = Trigger value is set using PWM Sample Trig Register value (Default)
1 = Trigger value is adaptive midpoint (EV1+CLA_DUTY/2 + Adaptive Offset) and uses current CLA value at update event
2 = Trigger value is adaptive midpoint (EV1+CLA_DUTY + Adaptive Offset) and uses current CLA value at update event
3 = Trigger value is adaptive based on previous CBC location + Adaptive Offset

Bit 1: SAMPLE_TRIG_2_EN – Sample Trigger 2 Enable
0 = Disable Sample Trigger 2 (Default)
1 = Enable Sample Trigger 2

Bit 0: SAMPLE_TRIG_1_EN – Sample Trigger 1 Enable
0 = Disable Sample Trigger 1 (Default)
1 = Enable Sample Trigger 1

21.8.4 DPWM Period Register (DPWMPRD)

Address 0015000C – DPWM 3 Period Register
Address 0017000C – DPWM 2 Period Register
Address 001A000C – DPWM 1 Period Register
Address 001D000C – DPWM 0 Period Register

Bit Number	17:4	3:0
Bit Name	PRD	RESERVED
Access	R/W	-
Default	00_0011_0100_0001	0000

Bits 17-4: PRD – PWM Period. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.5 DPWM Event 1 Register (DPWMEV1)

Address 00150010 – DPWM 3 Event 1 Register
Address 00170010 – DPWM 2 Event 1 Register
Address 001A0010 – DPWM 1 Event 1 Register
Address 001D0010 – DPWM 0 Event 1 Register

Bit Number	17:4	3:0
Bit Name	EVENT1	RESERVED
Access	R/W	-
Default	00_0000_0001_0100	0000

Bits 17-4: EVENT1 – Configures the location of Event 1. Low resolution register, last 4 bits are unused. Refer to DPWM app note for additional information.
Bits 3-0: RESERVED – Unused bits

21.8.6 DPWM Event 2 Register (DPWMEV2)

Address 00150014 – DPWM 3 Event 2 Register
Address 00170014 – DPWM 2 Event 2 Register
Address 001A0014 – DPWM 1 Event 2 Register
Address 001D0014 – DPWM 0 Event 2 Register

Bit Number	17:0
Bit Name	EVENT2
Access	R/W
Default	0_0000_0011_0000_0000

Bits 17-0: EVENT2 – Configures the location of Event 2. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0 (dependent on Bits 3:2 of DPWM Control Register 2). Refer to DPWM app note for additional information.

21.8.7 DPWM Event 3 Register (DPWMEV3)

Address 00150018 – Loop 4 DPWM Event 3 Register
Address 00170018 – Loop 3 DPWM Event 3 Register
Address 001A0018 – Loop 2 DPWM Event 3 Register
Address 001D0018 – Loop 1 DPWM Event 3 Register

Bit Number	17:0
Bit Name	EVENT3
Access	R/W
Default	00_0000_0011_1110_0000

Bits 17-0: EVENT3 – Configures the location of Event 3. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0. Refer to DPWM app note for additional information.

21.8.8 DPWM Event 4 Register (DPWMEV4)

Address 0015001C – Loop 4 DPWM Event 4 Register
Address 0017001C – Loop 3 DPWM Event 4 Register
Address 001A001C – Loop 2 DPWM Event 4 Register
Address 001D001C – Loop 1 DPWM Event 4 Register

Bit Number	17:0
Bit Name	EVENT4
Access	R/W
Default	00_0000_0111_0000_0000

Bits 17-0: EVENT4 – Configures the location of Event 4. Value equals number of PCLK clock periods in Bits 17:4 and number of high resolution clock phases of PCL in Bits 3:0. Refer to DPWM app note for additional information.

21.8.9 DPWM Sample Trigger 1 Register (DPWMSAMPTRIG1)

Address 00150020 – DPWM 3 Sample Trigger 1 Register
Address 00170020 – DPWM 2 Sample Trigger 1 Register
Address 001A0020 – DPWM 1 Sample Trigger 1 Register
Address 001D0020 – DPWM 0 Sample Trigger 1 Register

Bit Number	17:6	5:0
Bit Name	SAMPLE_TRIGGER	RESERVED
Access	R/W	-
Default	0000_0000_0100	00_0000

Bits 17-6: SAMPLE_TRIGGER – Configures the location of the sample trigger within a PWM period. Value equals the number of PCLK clock periods. Enables start of conversion for EADC. Refer to DPWM app note for additional information. Low resolution register, last 6 bits are read-only.
Bits 5-0: RESERVED – Unused bits

21.8.10 DPWM Sample Trigger 2 Register (DPWMSAMPTRIG2)

Address 00150024 – DPWM 3 Sample Trigger 1 Register
Address 00170024 – DPWM 2 Sample Trigger 1 Register
Address 001A0024 – DPWM 1 Sample Trigger 1 Register
Address 001D0024 – DPWM 0 Sample Trigger 1 Register

Bit Number	17:6	5:0
Bit Name	SAMPLE_TRIGGER	RESERVED
Access	R/W	-
Default	0000_0000_0100	00_0000

Bits 17-6: SAMPLE_TRIGGER – Configures the location of the sample trigger within a PWM period. Value equals the number of PCLK clock periods. Enables start of conversion for EADC. Refer to DPWM app note for additional information. Low resolution register, last 6 bits are read-only.
Bits 5-0: RESERVED – Unused bits

21.8.11 DPWM Phase Trigger Register (DPWMPHASETRIG)

Address 00150028 – DPWM 3 Phase Trigger Register
Address 00170028 – DPWM 2 Phase Trigger Register
Address 001A0028 – DPWM 1 Phase Trigger Register
Address 001D0028 – DPWM 0 Phase Trigger Register

Bit Number	17:4	3:0
Bit Name	PHASE_TRIGGER	RESERVED
Access	R/W	-
Default	0	0

Bits 17-4: PHASE_TRIGGER – Configures the phase trigger delay within multi-output mode. Value equals the number of PCLK clock periods. Refer to DPWM app note for additional information. Low resolution register, last 4 bits are read-only
Bits 3-0: RESERVED – Unused bits

21.8.12 DPWM Cycle Adjust A Register (DPWMCYCADJA)

Address 0015002C – DPWM 3 Cycle Adjust A Register
Address 0017002C – DPWM 2 Cycle Adjust A Register
Address 001A002C – DPWM 1 Cycle Adjust A Register
Address 001D002C – DPWM 0 Cycle Adjust A Register

Bit Number	15:0
Bit Name	CYCLE_ADJUST_A
Access	R/W
Default	0

Bits 15-0: CYCLE_ADJUST_A – Adjusts PWM A output signal. 16-bit signed number allows output signal to be delayed or sped up. Refer to DPWM app note for additional information.

21.8.13 DPWM Cycle Adjust B Register (DPWMCYCADJB)

Address 00150030 – DPWM 3 Cycle Adjust B Register
Address 00170030 – DPWM 2 Cycle Adjust B Register
Address 001A0030 – DPWM 1 Cycle Adjust B Register
Address 001D0030 – DPWM 0 Cycle Adjust B Register

Bit Number	15:0
Bit Name	CYCLE_ADJUST_B
Access	R/W
Default	0

Bits 15-0: CYCLE_ADJUST_B – Adjusts the PWM B output signal. 16-bit signed number allows output signal to be delayed or sped up. Refer to DPWM app note for additional information.

21.8.14 DPWM Resonant Duty Register (DPWMRESDUTY)

Address 00150034 – DPWM 3 Resonant Duty Register
Address 00170034 – DPWM 2 Resonant Duty Register
Address 001A0034 – DPWM 1 Resonant Duty Register
Address 001D0034 – DPWM 0 Resonant Duty Register

Bit Number	13:0
Bit Name	RESONANT_DUTY
Access	R/W
Default	0

Bits 15-0: FILTER_REF – Sets the filter reference value sent to the filter.

21.8.15 DPWM Fault Control Register (DPWMFLTCTRL)

Address 00150038 – DPWM 3 Fault Control Register
Address 00170038 – DPWM 2 Fault Control Register
Address 001A0038 – DPWM 1 Fault Control Register
Address 001D0038 – DPWM 0 Fault Control Register

Bit Number	31	30	29	28
Bit Name	RESERVED	ALL_FAULT_EN	CBC_FAULT_EN	CBC_FAULT_MODE
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	27:21	20:14	13:7	6:0
Bit Name	CBC_MAX_COUNT	AB_MAX_COUNT	B_MAX_COUNT	A_MAX_COUNT
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bits 31: RESERVED – Unused bits
Bit 30: ALL_FAULT_EN – DPWM Fault Module enable
0 = All DPWM Fault Modules disabled (Default)
1 = All DPWM Fault Modules enabled
Bit 29: CBC_FAULT_EN – CBC Fault Module enable
0 = CBC Fault Modules disabled (Default)
1 = CBC Fault Modules enabled
Bit 28: CBC_FAULT_MODE – CBC Fault Mode
0 = CBC Fault input set to raw CBC fault
1 = CBC Fault input set to output of CBC module
Bits 27-21: CBC_MAX_COUNT – Cycle-by-Cycle Fault Count, sets the number of received sequential faults on Cycle-by-Cycle Fault input before asserting the fault
Bits 20-14: AB_MAX_COUNT – Fault AB Count, sets the number of received sequential faults on Fault AB input before asserting the fault
Bits 13-7: B_MAX_COUNT – Fault B Count, sets the number of received sequential faults on Fault B input before asserting the fault
Bits 6-0: A_MAX_COUNT – Fault A Count, sets the number of received sequential faults on Fault A input before asserting the fault

21.8.16 DPWM Overflow Register (DPWMOVERFLOW)

Address 0015003C – DPWM 3 Overflow Register
Address 0017003C – DPWM 2 Overflow Register
Address 001A003C – DPWM 1 Overflow Register
Address 001D003C – DPWM 0 Overflow Register

Bit Number	7	6	5	4	3:0
Bit Name	PWM_B_CHECK	PWM_A_CHECK	GPIO_B_IN	GPIO_A_IN	OVERFLOW
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit 7: PWM_B_CHECK – Value of PWM B internal check
0 = Passed checks
1 = Failed checks (override required to enable output)
Bit 6: PWM_A_CHECK – Value of PWM B input
0 = Passed check
1 = Failed check (override required to enable output)
Bit 5: GPIO_B_IN0 – Value of PWM B input
0 = Low signal on PWM B
1 = High signal on PWM B
Bit 4: GPIO_A_IN – Value of PWM A input
0 = Low signal on PWM A
1 = High value on PWM A
Bit 3: OVERFLOW – PWM Event 4 Overflow Status
0 = CLA Event 4 has not overflowed
1 = Overflow condition found on CLA Event 4
Bit 2: OVERFLOW[2] – CLA Event 4 Overflow Status
0 = PWM Event 4 has not overflowed
1 = Overflow condition found on PWM Event 4
Bit 1: OVERFLOW[1] – CLA Event 3 Overflow Status
0 = CLA Event 3 has not overflowed
1 = Overflow condition found on CLA Event 3
Bit 0: OVERFLOW[0] – CLA Event 2 Overflow Status
0 = CLA Event 2 has not overflowed
1 = Overflow condition found on CLA Event 2

21.8.17 DPWM Interrupt Register (DPWMINT)

Address 00150040 – DPWM 3 Interrupt Register
Address 00170040 – DPWM 2 Interrupt Register
Address 001A0040 – DPWM 1 Interrupt Register
Address 001D0040 – DPWM 0 Interrupt Register

Bit Number	22	21	20	19	18	17	16
Bit Name	MODE_SWITCH	FLT_A	FLT_B	FLT_AB	FLT_CBC	PRD	INT
Access	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-

Bit Number	15:12	11	10
Bit Name	RESERVED	MODE_SWITCH_FLAG_CLR	MODE_SWITCH_FLAG_EN
Access	-	R/W	R/W
Default	0000	0	0

Bit Number	9	8	7
Bit Name	MODE_SWITCH_INT_EN	FLT_A_INT_EN	FLT_B_INT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	6	5	4	3:0
Bit Name	FLT_AB_INT_EN	FLT_CBC_INT_EN	PRD_INT_EN	PRD_INT_SCALE
Access	R/W	R/W	R/W	R/W
Default	0	0	0	1111

Bit 22: MODE_SWITCH – Mode Switching Flag
0 = Flag is not asserted
1 = Flag is set
Bit 21: FLT_A – Fault A Flag
0 = Flag is not asserted
1 = Flag is set
Bit 20: FLT_B – Fault B Flag
0 = Flag is not asserted
1 = Flag is set
Bit 19: FLT_AB – Fault AB Flag
0 = Flag is not asserted
1 = Flag is set
Bit 18: FLT_CBC – Fault Cycle-by-Cycle Flag
0 = Flag is not asserted
1 = Flag is set
Bit 17: PRD – PWM Period Interrupt Flag
0 = PWM Period Interrupt Flag is not asserted
1 = PWM Period Interrupt Flag is set
Bit 16: INT– Interrupt Out
0 = INT is not asserted
1 = INT is set
Bits 15-12: RESERVED – Unused bits
Bit 11: MODE_SWITCH_FLAG_CLR– Mode Switching Flag Clear
0 = (Default)
1 = Risedge 0-1 clears flag generated.

Bit 10: MODE_SWITCH_FLAG_EN– Mode Switching Flag Enable
0 = Disables generation of flag for Mode Switching (Default)
1 = Enables generation of flag for Mode Switching.
Bit 9: MODE_SWITCH_INT_EN – Mode Switching Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 8: FLT_A_INT_EN – Fault A Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 7: FLT_B_INT_EN – Fault B Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 6: FLT_AB_INT_EN – Fault AB Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 5: FLT_CBC_INT_EN – Fault Cycle-by-Cycle Flag Interrupt Enable
0 = Interrupt is not enabled (Default)
1 = Interrupt is enabled
Bit 4: PRD_INT_EN – PWM Period Interrupt Enable
0 = Disables generation of periodic PWM interrupt (Default)
1 = Enables generation of periodic PWM interrupt
Bits 3-0: PRD_INT_SCALE – This value scales the period interrupt signal from an interrupt every switching cycle to 16 switching cycles
0000 = Period Interrupt generated every switching cycle (Default)
0001 = Period Interrupt generated once every 2 switching cycles
0010 = Period Interrupt generated once every 4 switching cycles
0011 = Period Interrupt generated once every 6 switching cycles
0100 = Period Interrupt generated once every 8 switching cycles
0101 = Period Interrupt generated once every 16 switching cycles
0110 = Period Interrupt generated once every 32 switching cycles
0111 = Period Interrupt generated once every 48 switching cycles
1000 = Period Interrupt generated once every 64 switching cycles
1001 = Period Interrupt generated once every 80 switching cycles
1010 = Period Interrupt generated once every 96 switching cycles
1011 = Period Interrupt generated once every 128 switching cycles
1100 = Period Interrupt generated once every 160 switching cycles
1101 = Period Interrupt generated once every 192 switching cycles
1110 = Period Interrupt generated once every 224 switching cycles
1111 = Period Interrupt generated once every 256 switching cycles

21.8.18 DPWM Counter Preset Register (DPWMCNTPRE)

Address 00150044 – DPWM 3 Counter Preset Register
Address 00170044 – DPWM 2 Counter Preset Register
Address 001A0044 – DPWM 1 Counter Preset Register
Address 001D0044 – DPWM 0 Counter Preset Register

Bit Number	17:4	3:0
Bit Name	PRESET	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: PRESET – Counter preset value, counter reset to this value upon detection of sync when PRESET_EN bit in DPWMCTRL1 is enabled. Low resolution register, last 4 bits are read-only
Bits 3-0: RESERVED – Unused bits

21.8.19 DPWM Blanking A Begin Register (DPWMBLKABEG)

Address 00150048 – DPWM 3 Blanking A Begin Register
Address 00170048 – DPWM 2 Blanking A Begin Register
Address 001A0048 – DPWM 1 Blanking A Begin Register
Address 001D0048 – DPWM 0 Blanking A Begin Register

Bit Number	17:4	3:0
Bit Name	BLANK_A_BEGIN	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_A_BEGIN – Configures start of Comparator Blanking Window for PWM A**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.20 DPWM Blanking A End Register (DPWMBLKAEND)

Address 0015004C – DPWM 3 Blanking A End Register
Address 0017004C – DPWM 2 Blanking A End Register
Address 001A004C – DPWM 1 Blanking A End Register
Address 001D004C – DPWM 0 Blanking A End Register

Bit Number	17:4	3:0
Bit Name	BLANK_A_END	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_A_END – Configures end of Comparator Blanking Window for PWM A**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.21 DPWM Blanking B Begin Register (DPWMBLKBBEG)

Address 00150050 – DPWM 3 Blanking B Begin Register
Address 00170050 – DPWM 2 Blanking B Begin Register
Address 001A0050 – DPWM 1 Blanking B Begin Register
Address 001D0050 – DPWM 0 Blanking B Begin Register

Bit Number	17:4	3:0
Bit Name	BLANK_B_BEGIN	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_B_BEGIN – Configures start of Comparator Blanking Window for PWM B**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.22 DPWM Blanking B End Register (DPWMBLKBEND)

Address 00150054 – DPWM 3 Blanking B End Register
Address 00170054 – DPWM 2 Blanking B End Register
Address 001A0054 – DPWM 1 Blanking B End Register
Address 001D0054 – DPWM 0 Blanking B End Register

Bit Number	17:4	3:0
Bit Name	BLANK_B_END	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: BLANK_B_END – Configures end of Comparator Blanking Window for PWM B**.** Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.23 DPWM Minimum Duty Cycle High Register (DPWMMINDUTYHI)

Address 00150058 – DPWM 3 Minimum Duty Cycle High Register
Address 00170058 – DPWM 2 Minimum Duty Cycle High Register
Address 001A0058 – DPWM 1 Minimum Duty Cycle High Register
Address 001D0058 – DPWM 0 Minimum Duty Cycle High Register

Bit Number	17:4	3: 0
Bit Name	MIN_DUTY_HIGH	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: MIN_DUTY_HIGH– Configures upper threshold for minimum duty cycle logic. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.24 DPWM Minimum Duty Cycle Low Register (DPWMMINDUTYLO)

Address 0015005C – DPWM 3 Minimum Duty Cycle Low Register
Address 0017005C – DPWM 2 Minimum Duty Cycle Low Register
Address 001A005C – DPWM 1 Minimum Duty Cycle Low Register
Address 001D005C – DPWM 0 Minimum Duty Cycle Low Register

Bit Number	17:4	3: 0
Bit Name	MIN_DUTY_LOW	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: MIN_DUTY_LOW– Configures lower threshold for minimum duty cycle logic. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.25 DPWM Adaptive Sample Register (DPWMADAPTIVE)

Address 00150060 – DPWM 3 Adaptive Sample Register
Address 00170060 – DPWM 2 Adaptive Sample Register
Address 001A0060 – DPWM 1 Adaptive Sample Register
Address 001D0060 – DPWM 0 Adaptive Sample Register

Bit Number	11:0
Bit Name	ADAPT_SAMP
Access	R/W
Default	0000_0000_0000

Bit 13-0: ADAPT_SAMP – Configures Adaptive Sample Adjust

21.8.26 DPWM Fault Status (DPWMFLTSTAT)

Address 00150064 – DPWM 3 Fault Input Status Register
Address 00170064 – DPWM 2 Fault Input Status Register
Address 001A0064 – DPWM 1 Fault Input Status Register
Address 001D0064 – DPWM 0 Fault Input Status Register

Bit Number	5	4	3	2	1	0
Bit Name	BURST	IDE_DETECT	FLT_A	FLT_B	FLT_AB	FLT_CBC
Access	R	R	R	R	R	R
Default	-	-	-	-	-	-

Bit 5: BURST – Burst Mode Detection Status
0 = Burst Mode Detection is not asserted
1 = Burst Mode Detection is set
Bit 4: IDE_DETECT – IDE Detection Status (from Analog Comparators)
0 = IDE Detection is not asserted
1 = IDE Detection is set
Bit 3: FLT_A – Fault A Detection Status
0 = Fault A Detection is not asserted
1 = Fault A Detection is set
Bit 2: FLT_B – Fault B Detection Status
0 = Fault B Detection is not asserted
1 = Fault B Detection is set
Bit 1: FLT_AB – Fault AB Detection Status
0 = Fault AB Detection is not asserted

1 = Fault AB Detection is set

Bit 0: FLT_CBC – Current Limit Detection Status
0 = Current Limit Detection is not asserted
1 = Current Limit Detection is set

21.8.27 DPWM Auto Switch High Upper Thresh Register (DPWMAUTOSWHIUPTHRESH)

Address 00150068 – DPWM 3 Auto Switch High Upper Thresh Register
Address 00170068 – DPWM 2 Auto Switch High Upper Thresh Register
Address 001A0068 – DPWM 1 Auto Switch High Upper Thresh Register
Address 001D0068 – DPWM 0 Auto Switch High Upper Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_HIGH_UPPER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: AUTO_SWITCH_HIGH_UPPER– Configures upper threshold for Auto Switch Mode High operation. Mode switching does not occur between Auto Switch High Upper and Auto Switch High Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.28 DPWM Auto Switch High Lower Thresh Register (DPWMAUTOSWHILOWTHRESH)

Address 0015006C – DPWM 3 Auto Switch High Lower Thresh Register
Address 0017006C – DPWM 2 Auto Switch High Lower Thresh Register
Address 001A006C – DPWM 1 Auto Switch High Lower Thresh Register
Address 001D006C – DPWM 0 Auto Switch High Lower Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_HIGH_LOWER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 17-4: AUTO_SWITCH_HIGH_LOWER– Configures lower threshold for Auto Switch Mode High operation. Mode switching does not occur between Auto Switch High Upper and Auto Switch High Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.29 DPWM Auto Switch Low Upper Thresh Register (DPWMAUTOSWLOUPTHRESH)

Address 00150070 – DPWM 3 Auto Switch Low Upper Thresh Register
Address 00170070 – DPWM 2 Auto Switch Low Upper Thresh Register
Address 001A0070 – DPWM 1 Auto Switch Low Upper Thresh Register
Address 001D0070 – DPWM 0 Auto Switch Low Upper Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_LOW_UPPER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 29-16: AUTO_SWITCH_LOW_UPPER– Configures upper threshold for Auto Switch Mode Low operation. Mode switching does not occur between Auto Switch Low Upper and Auto Switch Low Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.30 DPWM Auto Switch Low Lower Thresh Register (DPWMAUTOSWLOLOWTHRESH)

Address 00150074 – DPWM 3 Auto Switch Low Lower Thresh Register
Address 00170074 – DPWM 2 Auto Switch Low Lower Thresh Register
Address 001A0074 – DPWM 1 Auto Switch Low Lower Thresh Register
Address 001D0074 – DPWM 0 Auto Switch Low Lower Thresh Register

Bit Number	17:4	3:0
Bit Name	AUTO_SWITCH_LOW_LOWER	RESERVED
Access	R/W	-
Default	00_0000_0000_0000	0000

Bit 29-16: AUTO_SWITCH_LOW_LOWER– Configures lower threshold for Auto Switch Mode Low operation. Mode switching does not occur between Auto Switch Low Upper and Auto Switch Low Lower thresholds. Low resolution register, last 4 bits are read-only.
Bits 3-0: RESERVED – Unused bits

21.8.31 DPWM Auto Config Max Register (DPWMAUTOMAX)

Address 00150078 – DPWM 3 Auto Config Max Register
Address 00170078 – DPWM 2 Auto Config Max Register
Address 001A0078 – DPWM 1 Auto Config Max Register
Address 001D0078 – DPWM 0 Auto Config Max Register

Bit Number	31:28	27:24
Bit Name	PWM_B_INTRA_MUX	PWM_A_INTRA_MUX
Access	R/W	R/W
Default	0	0

Bit Number	23	22:21	20
Bit Name	CBC_PWM_C_EN	RESERVED	CBC_PWM_AB_EN
Access	R/W	-	R/W
Default	0	0	0

Bit Number	19	18:13	12
Bit Name	CBC_ADV_CNT_EN	RESERVED	RESON_MODE_FIXED_DUTY_EN
Access	R/W	R	R/W
Default	0	0	0

Bit Number	11:8	7:4	3:2	1	0
Bit Name	RESERVED	PWM_MODE	RESERVED	CLA_EN	RESERVED
Access	-	R/W	-	R/W	-
Default	0	0	0	0	0

Bits 31-28: PWM_B_INTRA_MUX – Interchanges DPWM signals post edge generation
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bits 27-24: PWM_A_INTRA_MUX – Combines DPWM signals are prior to HR module
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bit 23: CBC_PWM_C_EN – Sets if Fault CBC changes output waveform for PWM-C

0 = PWM-C unaffected by Fault CBC (Default)
1 = PWM-C affected by Fault CBC

Bit 22:21: RESERVED – Unused Bit

Bit 20: CBC_PWM_AB_EN – Sets if Fault CBC changes output waveform for PWM-A and PWM-B

0 **=** PWM-A and PWM-B unaffected by Fault CBC (Default)
1 **=** PWM-A and PWM-B affected by Fault CBC

Bit 19: CBC_ADV_CNT_EN – Selects cycle-by-cycle of operation

Normal Mode
0 = CBC disabled (Default)
1 = CBC enabled
Multi and Resonant Modes
0 = PWM-A and PWM-B operate independently (Default)
1 = PWM-A and PWM-B pulse matching enabled

Bits 18-13: RESERVED – Unused Bits

Bit 12: RESON_MODE_FIXED_DUTY_EN – Configures how duty cycle is controlled in Resonance Mode

0 = Resonant mode duty cycle set by Filter duty (Default)
1 = Resonant mode duty cycle set by Auto Switch High Register

Bits 11-8: RESERVED – Unused Bits

Bits 7-4: PWM_MODE – DPWM Mode

0 = Normal Mode
1 = Resonant Mode
2 = Multi-Output Mode
3 = Triangular Mode
4 = Leading Mode

Bits 3-2: RESERVED – Unused Bits

Bit 1: CLA_EN– CLA Processing Enable

0 = Generate PWM waveforms from PWM Register values (Default)
1 = Enable CLA input

Bit 0: RESERVED – Unused bit

21.8.32 DPWM Auto Config Mid Register (DPWMAUTOMID)

Address 0015007C – DPWM 3 Auto Config Mid Register
Address 0017007C – DPWM 2 Auto Config Mid Register
Address 001A007C – DPWM 1 Auto Config Mid Register
Address 001D007C – DPWM 0 Auto Config Mid Register

Bit Number	31:28	27:24
Bit Name	PWM_B_INTRA_MUX	PWM_A_INTRA_MUX
Access	R/W	R/W
Default	0	0

Bit Number	23	22:21	20
Bit Name	CBC_PWM_C_EN	RESERVED	CBC_PWM_AB_EN
Access	R/W	-	R/W
Default	0	0	0

Bit Number	19	18:13	12
Bit Name	CBC_ADV_CNT_EN	RESERVED	RESON_MODE_FIXED_DUTY_EN
Access	R/W	R	R/W
Default	0	0	0

Bit Number	11:8	7:4	3:2	1	0
Bit Name	RESERVED	PWM_MODE	RESERVED	CLA_EN	RESERVED
Access	-	R/W	-	R/W	-
Default	0	0	0	0	0

Bits 31-28: PWM_B_INTRA_MUX – Interchanges DPWM signals post edge generation
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bits 27-24: PWM_A_INTRA_MUX – Combines DPWM signals are prior to HR module
0 = Pass-through (Default)
1 = Edge-gen output, this module
2 = PWM-C, this module
3 = Crossover, this module
4 = Pass-through below A
5 = Pass-through below B
6 = Pass-through below C
7 = Pass-through below level-2 C
8 = Pass-through below level-3 C

Bit 23: CBC_PWM_C_EN – Sets if Fault CBC changes output waveform for PWM-C
0 = PWM-C unaffected by Fault CBC (Default)
1 = PWM-C affected by Fault CBC
Bit 22:21: RESERVED – Unused Bit
Bit 20: CBC_PWM_AB_EN – Sets if Fault CBC changes output waveform for PWM-A and PWM-B
0 **=** PWM-A and PWM-B unaffected by Fault CBC (Default)
1 **=** PWM-A and PWM-B affected by Fault CBC
Bit 19: CBC_ADV_CNT_EN – Selects cycle-by-cycle of operation
Normal Mode
0 = CBC disabled (Default)
1 = CBC enabled
Multi and Resonant Modes
0 = PWM-A and PWM-B operate independently (Default)
1 = PWM-A and PWM-B pulse matching enabled
Bits 18-13: RESERVED – Unused Bits
Bit 12: RESON_MODE_FIXED_DUTY_EN – Configures how duty cycle is controlled in Resonance Mode
0 = Resonant mode duty cycle set by Filter duty (Default)
1 = Resonant mode duty cycle set by Auto Switch High Register
Bits 11-8: RESERVED – Unused Bits
Bits 7-4: PWM_MODE – DPWM Mode
0 = Normal Mode
1 = Resonant Mode
2 = Multi-Output Mode
3 = Triangular Mode

4 = Leading Mode

Bits 3-2: RESERVED – Unused Bits

Bit 1: CLA_EN– CLA Processing Enable

0 = Generate PWM waveforms from PWM Register values (Default)

1 = Enable CLA input

Bit 0: RESERVED – Unused bit

21.8.33 DPWM Edge PWM Generation Control Register (DPWMEDGEGEN)

Address 00150080 – DPWM 3 Edge PWM Generation Control Register
Address 00170080 – DPWM 2 Edge PWM Generation Control Register
Address 001A0080 – DPWM 1 Edge PWM Generation Control Register
Address 001D0080 – DPWM 0 Edge PWM Generation Control Register

Bit Number	16	15	14:12	11
Bit Name	EDGE_EN	RESERVED	A_ON_EDGE	RESERVED
Access	R/W	-	R/W	-
Default	0	0	000	0

Bit Number	10:8	7	6:4	3	2:0
Bit Name	A_OFF_EDGE	RESERVED	B_ON_EDGE	RESERVED	B_OFF_EDGE
Access	R/W	-	R/W	-	R/W
Default	01	0	10	0	11

Bit 16: EDGE_EN – Enables edge generate module. When combining dpwm's, all modules must have this bit enabled.

Bits 14-12: A_ON_EDGE – Select input edge to trigger A ON output edge

0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B

Bit 15: RESERVED – Unused bit

Bits 10-8: A_OFF_EDGE – Select input edge to trigger A OFF output edge

0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B

Bit 7: RESERVED – Unused bit

Bits 6-4: B_ON_EDGE – Select input edge to trigger B ON output edge

0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B

Bit 3: RESERVED – Unused bit
Bit 2-0: B_OFF_EDGE – Select input edge to trigger B OFF output edge
0 = Current DPWM posedge A
1 = Current DPWM negedge A
2 = Current DPWM posedge B
3 = Current DPWM negedge B
4 = Below (n+1) DPWM posedge A
5 = Below (n+1) DPWM negedge A
6 = Below (n+1) DPWM posedge B
7 = Below (n+1) DPWM negedge B

21.8.34 DPWM Filter Duty Read Register (DPWMFILTERDUTYREAD)

Address 00150084 – DPWM 3 Filter Duty Read Register
Address 00170084 – DPWM 2 Filter Duty Read Register
Address 001A0084 – DPWM 1 Filter Duty Read Register
Address 001D0084 – DPWM 0 Filter Duty Read Register

Bit Number	17:0
Bit Name	FILTER_DUTY
Access	R
Default	-

Bits 17-0: FILTER_DUTY – Filter Duty value received by DPWM Module

21.8.35 DPWM CBC Location (DPWMCBCLOCATION)

Address 00150088 – DPWM 3 CBC Location Register
Address 00170088 – DPWM 2 CBC Location Register
Address 001A0088 – DPWM 1 CBC Location Register
Address 001D0088 – DPWM 0 CBC Location Register

Bit Number	13:0
Bit Name	CBC_LOCATION
Access	R
Default	-

Bits 14-0: CBC_LOCATION – Holds counter value of last CBC event.

21.9 *Filter Registers*

Registers for Filter Modules 0-2 are identical in their bit definitions.

21.9.1 Filter Status Register (FILTERSTATUS)

Address 00160000 – Filter 2 Status Register
Address 00190000 – Filter 1 Status Register
Address 001C0000 – Filter 0 Status Register

Bit Number	4	3	2
Bit Name	FILTER_BUSY	YN_LOW_CLAMP	YN_HIGH_CLAMP
Access	R	R	R
Default	-	-	-

Bit Number	1	0
Bit Name	KI_YN_LOW_CLAMP	KI_YN_HIGH_CLAMP
Access	R	R
Default	-	-

Bit 4: FILTER_BUSY – Filter Busy Indicator
0 = Filter is waiting for new data
1 = Filter busy calculating
Bit 3: YN_LOW_CLAMP – PID Output Low Rail Indicator
0 = PID Output not equal to low rail
1 = PID Output equal to low rail
Bit 2: YN_HIGH_CLAMP – PID Output High Rail Indicator
0 = PID Output not equal to high rail
1 = PID Output equal to high rail
Bit 1: KI_YN_LOW_CLAMP – KI Feedback Low Rail Indicator
0 = KI Feedback not equal to low rail
1 = KI Feedback equal to low rail
Bit 0: KI_YN_HIGH_CLAMP – KI Feedback High Rail Indicator
0 = KI Feedback not equal to high rail
1 = KI Feedback equal to high rail

21.9.2 Filter Control Register (FILTERCTRL)

Address 00160004 – Filter 2 Control Register
Address 00190004 – Filter 1 Control Register
Address 001C0004 – Filter 0 Control Register

Bit Number	15	14	13:12
Bit Name	KI_ADDER_MODE	PERIOD_MULT_SEL	OUTPUT_MULT_SEL
Access	R/W	R/W	R/W
Default	1	0	00

Bit Number	11:9	8	7	6	5
Bit Name	YN_SCALE	NL_MODE	KD_STALL	KI_STALL	KP_OFF
Access	R/W	R/W	R/W	R/W	R/W
Default	000	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	KD_OFF	KI_OFF	FORCE_START	USE_CPU_SAMPLE	FILTER_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1

Bit 15: KI_ADDER_MODE – Configures addition of Xn and Xn-1 in Integral branch
0 = Only Xn used for addition (Xn + 0)
1 = Xn + Xn-1 used for addition (Default)

Bit 14: PERIOD_MULT_SEL – Selects output multiplicand used for multiplying with filter output to calculate DPWM Period value in Resonant Mode
0 = Switching period received from Loop Mux module (Default)
1 = KComp received from Loop Mux module

Bits 13-12: OUTPUT_MULT_SEL – Selects output multiplicand used for multiplying with filter output to calculate DPWM Duty value
0 = KComp received from Loop Mux module (Default)
1 = Switching period received from Loop Mux module
2 = Feed-Forward value received from Loop Mux module
3 = Resonant Duty value received from DPWM Module

Bit 11-9: YN_SCALE – Controls scaling of Yn value to compensate for filter coefficient scaling
0 = Filter output (Yn) not scaled (Default)
1 = Filter output (Yn) right shifted by 1
2 = Filter output (Yn) right shifted by 2
3 = Filter output (Yn) right shifted by 3
4 = Filter output (Yn) left shifted by 4
5 = Filter output (Yn) left shifted by 3
6 = Filter output (Yn) left shifted by 2
7 = Filter output (Yn) left shifted by 1

Bit 8: NL_MODE – Sets non-linear gain table configuration. Coefficient Bin mapping is controlled by Coefficient Configuration Register. Limit configuration is controlled by the Filter Nonlinear Limit Registers (See Sections 8.16-8.18)
0 = Non-symmetric mode (Default)
1 = Symmetric mode

Bit 7: KD_STALL – Freezes KD Branch, KD_YN remains at current value
0 = KD_YN recalculated on each filter update (Default)
1 = KD_YN stalled at present value

Bit 6: KI_STALL – Freezes KI Branch, KI_YN remains at current value
0 = KI_YN recalculated on each filter update (Default)

1 = KI_YN stalled at present value

Bit 5: KP_OFF – Turns off the KP branch
0 = KP branch calculating new outputs (Default)
1 = KP branch turned off

Bit 4: KD_OFF – Turns off the KD branch, KD_YN cleared to zero
0 = KD branch calculating new outputs (Default)
1 = KD branch turned off

Bit 3: KI_OFF – Turns off the KI branch, KI_YN cleared to zero
0 = KI branch calculating new outputs (Default)
1 = KI branch halted

Bit 2: FORCE_START – Initiates a filter calculation under firmware control
0 = No calculation started (Default)
1 = Calculation started

Bit 1: USE_CPU_SAMPLE – Forces filter to use error sample from CPU XN register (Section 8.3)
0 = Filter Mode, input data received from EADC (Default)
1 = CPU Mode, input data based on CPU XN register

Bit 0: FILTER_EN – Filter Enable
0 = Disables Filter operation
1 = Enables Filter operation (Default)

21.9.3 CPU XN Register (CPUXN)

Address 00160008 – Filter 2 CPU XN Register
Address 00190008 – Filter 1 CPU XN Register
Address 001C0008 – Filter 0 CPU XN Register

Bit Number	8:0
Bit Name	CPU_SAMPLE
Access	R/W
Default	0_0000_0000

Bits 8-0: CPU_SAMPLE – Forced X_n value, allows processor to use filter as ALU. Set Bit 2 of Filter Control Register to '1' to force CPU_SAMPLE as input to Filter.

21.9.4 Filter XN Read Register (FILTERXNREAD)

Address 0016000C – Filter 2 XN Read Register
Address 0019000C – Filter 1 XN Read Register
Address 001C000C – Filter 0 XN Read Register

Bit Number	24:16	15:9	8:0
Bit Name	XN_M1	RESERVED	XN
Access	R	-	R
Default	-	000_0000	-

Bits 24-16: XN_M1 – 9-bit signed XN_M1 register value, read-only
Bits 15-9: RESERVED
Bits 8-0: XN – 9-bit signed XN register value, read-only

21.9.5 Filter KI_YN Read Register (FILTERKIYNREAD)

Address 00160010 – Filter 2 KI_YN Read Register
Address 00190010 – Filter 1 KI_YN Read Register
Address 001C0010 – Filter 0 KI_YN Read Register

Bit Number	23:0
Bit Name	KI_YN
Access	R
Default	-

Bits 23-0: KI_YN – 24-bit signed KI_YN register value, read-only

21.9.6 Filter KD_YN Read Register (FILTERKDYNREAD)

Address 00160014 – Filter 2 KD_YN Register
Address 00190014 – Filter 1 KD_YN Register
Address 001C0014 – Filter 0 KD_YN Register

Bit Number	23:0
Bit Name	KD_YN
Access	R
Default	-

Bits 23-0: KD_YN – 24-bit signed KD_YN register value, read-only

21.9.7 Filter YN Read Register (FILTERYNREAD)

Address 00160018 – Filter 2 YN Read Register
Address 00190018 – Filter 1 YN Read Register
Address 001C0018 – Filter 0 YN Read Register

Bit Number	23:0
Bit Name	YN
Access	R
Default	-

Bits 23-0: YN – 24-bit signed YN register value, read-only

21.9.8 Coefficient Configuration Register (COEFCONFIG)

Address 0016001C – Filter 2 Coefficient Configuration Register
Address 0019001C – Filter 1 Coefficient Configuration Register
Address 001C001C – Filter 0 Coefficient Configuration Register

Bit Number	27	26:24	23	22:20
Bit Name	BIN6_ALPHA	BIN6_CONFIG	BIN5_ALPHA	BIN5_CONFIG
Access	R/W	R/W	R/W	R/W
Default	0	000	0	000

Bit Number	19	18:16	15	14:12	11
Bit Name	BIN4_ALPHA	BIN4_CONFIG	BIN3_ALPHA	BIN3_CONFIG	BIN2_ALPHA
Access	R/W	R/W	R/W	R/W	R/W
Default	0	000	0	000	0

Bit Number	10:8	7	6:4	3	2:0
Bit Name	BIN2_CONFIG	BIN1_ALPHA	BIN1_CONFIG	BIN0_ALPHA	BIN0_CONFIG
Access	R/W	R/W	R/W	R/W	R/W
Default	000	0	000	0	000

Bit 27: BIN6_ALPHA – Selects which alpha value to use in Bin 6 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample
0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
Bits 26-24: BIN6_CONFIG – Selects which coefficient set to place in Bin 6 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.
0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected
Bit 23: BIN5_ALPHA – Selects which alpha value to use in Bin 5 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample
0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected
Bits 22-20: BIN5_CONFIG – Selects which coefficient set to place in Bin 5 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 19: BIN4_ALPHA – Selects which alpha value to use in Bin 4 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 18-16: BIN4_CONFIG – Selects which coefficient set to place in Bin 4 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 15: BIN3_ALPHA – Selects which alpha value to use in Bin 3 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 14-12: BIN3_CONFIG – Selects which coefficient set to place in Bin 3 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 11: BIN2_ALPHA – Selects which alpha value to use in Bin 2 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 10-8: BIN2_CONFIG – Selects which coefficient set to place in Bin 2 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 7: BIN1_ALPHA – Selects which alpha value to use in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 6-4: BIN1_CONFIG – Selects which coefficient set to place in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected

4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

Bit 3: BIN0_ALPHA – Selects which alpha value to use in Bin 0 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample

0 = Bank 0 KD Alpha (KD_ALPHA_0) selected (Default)
1 = Bank 1 KD Alpha (KD_ALPHA_1) selected

Bits 2-0: BIN0_CONFIG – Selects which coefficient set to place in Bin 1 of Non-Linear Table. These bits are shadowed and updated to filter when filter is not processing an EADC sample.

0 = Coefficient Set A Selected (Default)
1 = Coefficient Set B Selected
2 = Coefficient Set C Selected
3 = Coefficient Set D Selected
4 = Coefficient Set E Selected
5 = Coefficient Set F Selected
6 = Coefficient Set G Selected

21.9.9 Filter KP Coefficient 0 Register (FILTERKPCOEF0)

Address 00160020 – Filter 2 KP Coefficient 0 Register
Address 00190020 – Filter 1 KP Coefficient 0 Register
Address 001C0020 – Filter 0 KP Coefficient 0 Register

Bit Number	31:16	15:0
Bit Name	KP_COEF_1	KP_COEF_0
Access	R/W	R/W
Default	0000_0000_0000_0000	0100_0010_0011_0100

Bits 31-16: KP_COEF_1 – KP Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KP_COEF_0 – KP Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

21.9.10 Filter KP Coefficient 1 Register (FILTERKPCOEF1)

Address 00160024 – Filter 2 KP Coefficient 1 Register
Address 00190024 – Filter 1 KP Coefficient 1 Register
Address 001C0024 – Filter 0 KP Coefficient 1 Register

Bit Number	15:0
Bit Name	KP_COEF_2
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: KP_COEF_2 – KP Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

21.9.11 Filter KI Coefficient 0 Register (FILTERKICOEF0)

Address 00160028 – Filter 2 KI Coefficient 0 Register
Address 00190028 – Filter 1 KI Coefficient 0 Register
Address 001C0028 – Filter 0 KI Coefficient 0 Register

Bit Number	31:16	15:0
Bit Name	KI_COEF_1	KI_COEF_0
Access	R/W	R/W
Default	0000_0000_0000_0000	0010_0100_0001_0010

Bits 31-16: KI_COEF_1 – KI Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KI_COEF_0 – KI Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

21.9.12 Filter KI Coefficient 1 Register (FILTERKICOEF1)

Address 0016002C – Filter 2 KI Coefficient 1 Register
Address 0019002C – Filter 1 KI Coefficient 1 Register
Address 001C002C – Filter 0 KI Coefficient 1 Register

Bit Number	31:16	15:0
Bit Name	KI_COEF_3	KI_COEF_2
Access	R/W	R/W
Default	0000_0000_0000_0000	0000_0000_0000_0000

Bits 31-16: KI_COEF_3 – KI Coefficient 3, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KI_COEF_2 – KI Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

21.9.13 Filter KD Coefficient 0 Register (FILTERKDCOEF0)

Address 00160030 – Filter 2 KD Coefficient 0 Register
Address 00190030 – Filter 1 KD Coefficient 0 Register
Address 001C0030 – Filter 0 KD Coefficient 0 Register

Bit Number	31:16	15:0
Bit Name	KD_COEF_1	KD_COEF_0
Access	R/W	R/W
Default	0000_0000_0000_0000	1100_0100_0000_0001

Bits 31-16: KD_COEF_1 – KD Coefficient 1, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register
Bits 15-0: KD_COEF_0 – KD Coefficient 0, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

21.9.14 Filter KD Coefficient 1 Register (FILTERKDCOEF1)

Address 00160034 – Filter 2 KD Coefficient 1 Register
Address 00190034 – Filter 1 KD Coefficient 1 Register
Address 001C0034 – Filter 0 KD Coefficient 1 Register

Bit Number	15:0
Bit Name	KD_COEF_2
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: KD_COEF_2 – KD Coefficient 2, 16-bit signed coefficient, configurable to any bin using the Coefficient Control Register

21.9.15 Filter KD Alpha Register (FILTERKDALPHA)

Address 00160038 – Filter 2 KD Alpha Register
Address 00190038 – Filter 1 KD Alpha Register
Address 001C0038 – Filter 0 KD Alpha Register

Bit Number	24:16	15:9	8:0
Bit Name	KD_ALPHA_1	RESERVED	KD_ALPHA_0
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_0101_0010

Bits 24-16: KD_ALPHA_1 – Bank 1 KD Alpha, 9-bit signed value, configurable to any bin using the Coefficient Control Register
Bits 15-9: RESERVED
Bits 8-0: KD_ALPHA_0 – Bank 0 KD Alpha, 9-bit signed value, configurable to any bin using the Coefficient Control Register

21.9.16 Filter Nonlinear Limit Register 0 (FILTERNL0)

Address 0016003C – Filter 2 Nonlinear Limit Register 0
Address 0019003C – Filter 1 Nonlinear Limit Register 0
Address 001C003C – Filter 0 Nonlinear Limit Register 0

Bit Number	24:16	15:9	8:0
Bit Name	LIMIT1	RESERVED	LIMIT0
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_1111_1111

Bits 24-16: LIMIT1 – Configures LIMIT1 in Nonlinear Coefficient tables
Bits 15-9: RESERVED
Bits 8-0: LIMIT0 – Configures LIMIT0 in Nonlinear Coefficient tables

21.9.17 Filter Nonlinear Limit Register 1 (FILTERNL1)

Address 00160040 – Filter 2 Nonlinear Limit Register 1
Address 00190040 – Filter 1 Nonlinear Limit Register 1
Address 001C0040 – Filter 0 Nonlinear Limit Register 1

Bit Number	24:16	15:9	8:0
Bit Name	LIMIT3	RESERVED	LIMIT2
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_0000_0000

Bits 24-16: LIMIT3 – Configures LIMIT3 in Nonlinear Coefficient tables
Bits 15-9: RESERVED
Bits 8-0: LIMIT2 – Configures LIMIT2 in Nonlinear Coefficient tables

21.9.18 Filter Nonlinear Limit Register 2 (FILTERNL2)

Address 00160044 – Filter 2 Nonlinear Limit Register 2
Address 00190044 – Filter 1 Nonlinear Limit Register 2
Address 001C0044 – Filter 0 Nonlinear Limit Register 2

Bit Number	24:16	15:9	8:0
Bit Name	LIMIT5	RESERVED	LIMIT4
Access	R/W	-	R/W
Default	0_0000_0000	000_0000	0_0000_0000

Bits 24-16: LIMIT5 – Configures LIMIT5 in Nonlinear Coefficient tables
Bits 15-9: RESERVED
Bits 8-0: LIMIT4 – Configures LIMIT4 in Nonlinear Coefficient tables

21.9.19 Filter KI Feedback Clamp High Register (FILTERKICLPHI)

Address 00160048 – Filter 2 KI Feedback Clamp High Register
Address 00190048 – Filter 1 KI Feedback Clamp High Register
Address 001C0048 – Filter 0 KI Feedback Clamp High Register

Bit Number	23:0
Bit Name	KI_CLAMP_HIGH
Access	R/W
Default	0111_1111_1111_1111_1111_1111

Bits 23-0: KI_CLAMP_HIGH – Sets the upper limit of KI_YN value. If calculated KI_YN exceeds this threshold, the KI_YN register will be set to KI_CLAMP_HIGH

21.9.20 Filter KI Feedback Clamp Low Register (FILTERKICLPLO)

Address 0016004C– Filter 2 KI Feedback Clamp Low Register
Address 0019004C– Filter 1 KI Feedback Clamp Low Register
Address 001C004C – Filter 0 KI Feedback Clamp Low Register

Bit Number	23:0
Bit Name	KI_CLAMP_LOW
Access	R/W
Default	0000_0000_0000_0000_0000_0000

Bits 23-0: KI_CLAMP_LOW – Sets the lower limit of KI_YN value. If calculated KI_YN falls below this threshold, the KI_YN register will be set to KI_CLAMP_LOW

21.9.21 Filter YN Clamp High Register (FILTERYNCLPHI)

Address 00160050 – Filter 2 YN Clamp High Register
Address 00190050 – Filter 1 YN Clamp High Register
Address 001C0050 – Filter 0 YN Clamp High Register

Bit Number	23:0
Bit Name	YN_CLAMP_HIGH
Access	R/W
Default	0111_1111_1111_1111_1111_1111

Bits 23-0: YN_CLAMP_HIGH – Sets the upper limit of YN value. If calculated YN exceeds this threshold, the YN register will be set to YN_CLAMP_HIGH

21.9.22 Filter YN Clamp Low Register (FILTERYNCLPLO)

Address 00160054 – Filter 2 YN Clamp Low Register
Address 00190054 – Filter 1 YN Clamp Low Register
Address 001C0054 – Filter 0 YN Clamp Low Register

Bit Number	23:0
Bit Name	YN_CLAMP_LOW
Access	R/W
Default	0000_0000_0000_0000_0000_0000

Bits 23-0: YN_CLAMP_LOW – Sets the lower limit of YN value. If calculated YN falls below this threshold, the YN register will be set to YN_CLAMP_LOW

21.9.23 Filter Output Clamp High Register (FILTEROCLPHI)

Address 00160058 – Filter 2 Output Clamp High Register
Address 00190058 – Filter 1 Output Clamp High Register
Address 001C0058 – Filter 0 Output Clamp High Register

Bit Number	17:0
Bit Name	OUTPUT_CLAMP_HIGH
Access	R/W
Default	11_1111_1111_1111_1111

Bits 17-0: OUTPUT_CLAMP_HIGH – Sets the upper limit of filter output value. If calculated filter output exceeds this threshold, the filter output will be set to OUTPUT_CLAMP_HIGH

21.9.24 Filter Output Clamp Low Register (FILTEROCLPLO)

Address 0016005C – Filter 2 Output Clamp Low Register
Address 0019005C – Filter 1 Output Clamp Low Register
Address 001C005C – Filter 0 Output Clamp Low Register

Bit Number	17:0
Bit Name	OUTPUT_CLAMP_LOW
Access	R/W
Default	00_0000_0000_0000_0000

Bits 17-0: OUTPUT_CLAMP_LOW – Sets the lower limit of filter output value. If calculated filter output falls below this threshold, the filter output will be set to OUTPUT_CLAMP_LOW

21.9.25 Filter Preset Register (FILTERPRESET)

Address 00160060 – Filter 2 Filter Preset Register
Address 00190060 – Filter 1 Filter Preset Register
Address 001C0060 – Filter 0 Filter Preset Register

Bit Number	27	26:24	23:0
Bit Name	PRESET_EN	PRESET_REG_SEL	PRESET_VALUE
Access	R/W	R/W	R/W
Default	00	000	0000_0000_0000_0000_0000_0000

Bit 27: PRESET_EN – Set to '1' to initiate write of internal filter register (Self cleared by hardware after successful programming)
Bits 26-24: PRESET_REG_SEL – Selects internal filter register to preset by processor
0 = XN_M1 Register (only bits 10:0 of PRESET_VALUE will be programmed into register)
1 = KI_YN Register
2 = KD_YN Register
3 = YN Register
4 = 18-bit Filter Data Register (after multiplication)
Bits 23-0: PRESET_VALUE – Value to preset into selected register

21.10 *Front End Control Registers*

Registers for Front End Control modules 0-2 are identical in their bit definitions

21.10.1 Ramp Control Register (RAMPCTRL)

Address 0x0018_0000 – Front End Control 2 Ramp Control Register
Address 0x001B_0000 – Front End Control 1 Ramp Control Register
Address 0x001E_0000 – Front End Control 0 Ramp Control Register

Bit Number	29:16	15:13	12
Bit Name	SYNC_FET_RAMP_START	RESERVED	RAMP_SAT_EN
Access	R/W	-	R/W
Default	00_0000_0000_0000	00	0

Bit Number	11	10	9
Bit Name	RAMP_COMP_INT_EN	RAMP_DLY_INT_EN	PREBIAS_INT_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	8	7	6:5	4
Bit Name	PCM_START_SEL	SYNC_FET_EN	MASTER_SEL	SLAVE_COMP_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	00	0

Bit Number	3	2	1	0
Bit Name	SLAVE_DELAY_EN	CONTROL_EN	FIRMWARE_START	RAMP_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bits 29-16: SYNC_FET_RAMP_START – Provides the starting value for the SyncFET Ramp with a resolution of High Frequency Oscillator Period/bit
Bits 15-13: RESERVED – Unused Bits
Bit 12: RAMP_SAT_EN – Enables addition or subtraction of DAC Saturation Step when EADC is in saturation.

0 = DAC Saturation Step logic is disabled, DAC incremented/decremented by value calculated by Ramp logic when EADC is in saturation (Default)
1 = DAC Saturation Step logic is enabled, DAC incremented/decremented by value stored in DAC Saturation Step register when EADC is in saturation

Bit 11: RAMP_COMP_INT_EN – Enables Ramp I/F Interrupt when soft-start/power-down ramp procedure is complete

0 = Soft-start/Power-Down Ramp Complete Interrupt is disabled (Default)
1 = Soft-start/Power-Down Ramp Complete Interrupt is enabled

Bit 10: RAMP_DLY_INT_EN – Enables Ramp I/F Interrupt when ramp delay procedure is complete

0 = Soft-start/Power-Down Ramp Delay Complete Interrupt is disabled (Default)
1 = Soft-start/Power-Down Ramp Delay Complete Interrupt is enabled

Bit 9: PREBIAS_INT_EN – Enables Ramp I/F Interrupt when Pre-Bias procedure is completed

0 = Pre-bias Complete Interrupt is disabled (Default)
1 = Pre-bias Complete Interrupt is enabled

Bit 8: PCM_START_SEL – Peak Current Mode Ramp Start Value Select

0 = Ramp starts from value programmed in DAC_VALUE bits in EADC_DAC_VALUE Register (Default)
1 = Ramp starts from filter output selected by PCM_SEL bits in Front End Control Mux Register

Bit 7: SYNC_FET_EN – Enables SyncFET Ramp Operation
0 = SyncFET Ramp Operation disabled (Default)
1 = SyncFET Ramp Operation enabled

Bits 6-5: MASTER_SEL – Selects Master Ramp I/F in slave mode
0 = Front End Control 0 acts as master (Default)
1 = Front End Control 1 acts as master
2 = Front End Control 2 acts as master

Bit 4: SLAVE_COMP_EN – Enables syncing of ramp start to Master Ramp I/F Complete pulse
0 = Ramp initiated by Master Ramp Complete pulse disabled (Default)
1 = Ramp initiated by Master Ramp Complete pulse enabled

Bit 3: SLAVE_DELAY_EN – Enables syncing of ramp start to Master Ramp I/F Delay Complete pulse
0 = Ramp initiated by Master Ramp Delay Complete pulse disabled (Default)
1 = Ramp initiated by Master Ramp Delay Complete pulse enabled

Bit 2: CONTROL_EN – Enables PMBus Control line to initiate ramp
0 = PMBus Control does not initiate ramp (Default)
1 = PMBus Control initiates ramp

Bit 1: FIRMWARE_START – Ramp start bit, self-clearing by ramp logic
0 = No ramp sequence initiated by firmware (Default)
1 = Ramp sequence initiated by firmware

Bit 0: RAMP_EN – Enable Ramp Logic (Pre-biasing should be disabled before asserting ramp, bit 16 of Pre-Bias Control Register)
0 = No soft start or power-down ramp controlled by hardware (Default)
1 = Enables hardware control of soft start or power-down ramp

21.10.2 Ramp Status Register (RAMPSTAT)

Address 0x0018_0004 – Front End Control 2 Ramp Status Register
Address 0x001B_0004 – Front End Control 1 Ramp Status Register
Address 0x001E_0004 – Front End Control 0 Ramp Status Register

Bit Number	11	10	9
Bit Name	EADC_DONE_RAW	RAMP_COMP_INT_STATUS	RAMP_DLY_INT_STATUS
Access	R	R	R
Default	-	-	-

Bit Number	8	7	6
Bit Name	PREBIAS_INT_STATUS	EADC_SAT_HIGH	EADC_SAT_LOW
Access	R	R	R
Default	-	-	-

Bit Number	5	4	3
Bit Name	EADC_EOC	PREBIAS_BUSY	RAMP_BUSY
Access	R	R	R
Default	-	-	-

Bit Number	2	1	0
Bit Name	RAMP_COMP_STATUS	RAMP_DLY_STATUS	PREBIAS_STATUS
Access	R	R	R
Default	-	-	-

Bit 11: EADC_DONE_RAW – EADC Conversion Done Raw Status
0 = EADC Conversion has not completed
1 = EADC Conversion has completed
Bit 10: RAMP_COMP_INT_STATUS – Ramp Complete latched status
0 = No Ramp Complete has been declared
1 = Ramp Complete has been declared
Bit 9: RAMP_DLY_INT_STATUS – Ramp Delay Complete latched status
0 = No Ramp Delay Complete has been declared
1 = Ramp Delay Complete has been declared
Bit 8: PREBIAS_INT_STATUS – Pre-Bias Complete latched status
0 = No Pre-Bias Complete has been declared
1 = Pre-Bias Complete has been declared
Bit 7: EADC_SAT_HIGH – EADC Saturation High Indicator
0 = EADC output is not saturated at high limit
1 = EADC output is saturated at high limit
Bit 6: EADC_SAT_LOW – EADC Saturation Low Indicator
0 = EADC output is not saturated at low limit
1 = EADC output is saturated at low limit
Bit 5: EADC_EOC – Indicates EADC end of conversion
Bit 4: PRE_BIAS_BUSY – Pre-Bias Busy
0 = Pre-Bias is not in progress
1 = Pre-Bias in progress
Bit 3: RAMP_BUSY – Ramp Busy
0 = Soft-Start/Power-Down Ramp is not in progress
1 = Soft-Start/Power-Down Ramp is in progress
Bit 2: RAMP_COMP_STATUS – Ramp Complete, Raw Status

0 = Ramp procedure is not complete
1 = Ramp procedure is complete

Bit 1: RAMP_DLY_STATUS – Ramp Delay Complete, Raw Status
0 = Ramp delay procedure is not complete
1 = Ramp delay procedure is complete

Bit 0: PRE_BIAS_STATUS – Pre-Bias Complete, Raw Status
0 = Pre-Bias is not completed
1 = Pre-Bias is completed

21.10.3 Ramp Cycle Register (RAMPCYCLE)

Address 0x0018_0008 – Front End Control 2 Ramp Cycle Register
Address 0x001B_0008 – Front End Control 1 Ramp Cycle Register
Address 0x001E_0008 – Front End Control 0 Ramp Cycle Register

Bit Number	23:8	7	6:0
Bit Name	DELAY_CYCLES	RESERVED	SWITCH_CYC_PER_STEP
Access	R/W	-	R/W
Default	0000_0000_0000_0000	0	000_0000

Bits 23-8: DELAY_CYCLES – Configures the number of delay cycles before an initiation of ramp sequence. Each delay cycle consists of n switching cycles, as specified by SWITCH_CYC_PER_STEP (Bits 6-0). Number of delay cycles can vary from 0 to 65535
0 = Ramp starts without delay (Default)
1 = Ramp starts after (1*SWITCH_CYC_PER_STEP) switching cycles
2 = Ramp starts after (2*SWITCH_CYC_PER_STEP) switching cycles
…….
65535 = Ramp starts after (65535*SWITCH_CYC_PER_STEP) switching cycles

Bit 7: RESERVED

Bits 6-0: SWITCH_CYC_PER_STEP – Selects number of switching cycles per DAC step. Number of subcycles can vary from 1 to 128.
0 = 1 switching cycle per step (Default)
1 = 2 subcycles per cycle
2 = 3 subcycles per cycle
…….
127 = 128 subcycles per cycle

21.10.4 EADC DAC Value Register (EADCDAC)

Address 0x0018_000C – Front End Control 2 EADC DAC Value Register
Address 0x001B_000C – Front End Control 1 EADC DAC Value Register
Address 0x001E_000C– Front End Control 0 EADC DAC Value Register

Bit Number	16	15	14	13:0
Bit Name	DAC_DITHER_ON_SAMPLE	DAC_DITHER_EN	RESERVED	DAC_VALUE
Access	R/W	R/W	-	R/W
Default	0	0	0	00_1111_1111_0000

Bit 16: DAC_DITHER_ON_SAMPLE – DAC Dithering on based on Sample Trigger
0 = DAC Dithering disabled on input sample trigger (Default)
1 = DAC Dithering enabled on input sample trigger
Bit 15: DAC_DITHER_EN – DAC Dithering Enable
0 = DAC Dithering disabled (Default)
1 = DAC Dithering enabled
Bit 15: RESERVED
Bits 13-0: DAC_VALUE - Programmable DAC Value, effective LSB equals 0.09765625mV

21.10.5 Ramp DAC Ending Value Register (RAMPDACEND)

Address 0x0018_0010 – Front End Control 2 Ramp DAC Ending Register
Address 0x001B_0010 – Front End Control 1 Ramp DAC Ending Register
Address 0x001E_0010 – Front End Control 0 Ramp DAC Ending Register

Bit Number	13:0
Bit Name	RAMP_DAC_VALUE
Access	R/W
Default	00_0000_0000_0000

Bits 13-0: RAMP_DAC_VALUE – Programmable Ramp Ending DAC Value, LSB equals 0.09765625mV

21.10.6 DAC Step Register (DACSTEP)

Address 0x0018_0014 – Front End Control 2 DAC Step Register
Address 0x001B_0014 – Front End Control 1 DAC Step Register
Address 0x001E_0014 – Front End Control 0 DAC Step Register

Bit Number	17:0
Bit Name	DAC_STEP
Access	R/W
Default	00_0000_0000_0000_0000

Bits 17-0: DAC_STEP – Programmable 18-bit unsigned DAC Step. Bits 17:10 represent the real portion of the DAC Step (0-255 DAC counts at bit resolution of 0.09765625mV). Bits 9:0 represent the fractional portion of the DAC Step.

21.10.7 DAC Saturation Step Register (DACSATSTEP)

Address 0x0018_0018 – Front End Control 2 DAC Saturation Step Register
Address 0x001B_0018 – Front End Control 1 DAC Saturation Step Register
Address 0x001E_0018 – Front End Control 0 DAC Saturation Step Register

Bit Number	13:0
Bit Name	DAC_SAT_STEP
Access	R/W
Default	00_0000_0000_0000

Bits 13-0: DAC_SAT_STEP – Programmable DAC Saturation Step, LSB equals 0.009765625mV
0 = DAC not adjusted on EADC saturation during ramp (Default)
1 = DAC adjusted by 1 DAC count on EADC saturation during ramp
…..
1023 = DAC adjusted by 1023 DAC counts on EADC saturation during ramp

21.10.8 EADC Control Register (EADCCTRL)

Address 0x0018_0020 – Front End Control 2 EADC Control Register
Address 0x001B_0020 – Front End Control 1 EADC Control Register
Address 0x001E_0020 – Front End Control 0 EADC Control Register

Bit Number	28	27	26
Bit Name	D2S_COMP_EN	EN_HYST_HIGH	EN_HYST_LOW
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	25:22	21	20
Bit Name	SAMP_TRIG_SCALE	FRAME_SYNC_EN	SCFE_CNT_RST
Access	R/W	R/W	R/W
Default	0000	0	0

Bit Number	19:16	15	14
Bit Name	SCFE_CNT_INIT	EADC_INV	AUTO_GAIN_SHIFT_MODE
Access	R/W	R/W	R/W
Default	0000	0	0

Bit Number	13	12	11
Bit Name	AUTO_GAIN_SHIFT_EN	AVG_WEIGHT_EN	AVG_SPATIAL_EN
Access	R/W	R/W	R/W
Default	0	0	0

Bit Number	10:9	8:6	5:4
Bit Name	AVG_MODE_SEL	EADC_MODE	AFE_GAIN
Access	R/W	R/W	R/W
Default	00	000	11

Bit Number	3	2	1	0
Bit Name	SCFE_GAIN_FILTER_SEL	SCFE_CLK_DIV_2	SCFE_ENA	EADC_ENA

Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit 28: D2S_COMP_EN – Analog Front End Ramp Comparator Enable
0 = Analog Front End Ramp Comparator disabled (Default)
1 = Analog Front End Ramp Comparator enabled
Bit 27: EN_HYST_HIGH – Increase comparator trip point by ~70mV
0 = Disables increase of ramp comparator trip point (Default)
1 = Enables increase of ramp comparator trip point
Bit 26: EN_HYST_LOW – Decrease comparator trip point by ~70mV
0 = Disables decrease of ramp comparator trip point (Default)
1 = Enables decrease of ramp comparator trip point

Bits 25-22: SAMP_TRIG_SCALE – Provides capability to mask incoming sample triggers to Front End Control
0 = EADC conversion initiated on every received sample trigger (Default)
1 = EADC conversion initiated once every 2 received sample triggers
2 = EADC conversion initiated once every 3 received sample triggers
…..
15 = EADC conversion initiated once every 16 received sample triggers
Bit 21: FRAME_SYNC_EN – Enable synchronization of switched cap front end counter to Switching Cycle Frame boundary
0 = Switch Cap Front End Counter not synchronized to frame (Default)
1 = Switch Cap Front End Counter synchronized to frame boundary
Bit 20: SCFE_CNT_RST – Force reset of Switched Cap Front End Counter
0 = Switch Cap Front End Counter operational (Default)
1 = Switch Cap Front End Counter reset
Bits 19-16: SCFE_CNT_INIT – Configures initial Switched Cap Front End Counter value out of reset or at start of switching cycle in Peak Current mode
Bit 15: EADC_INV – Enables EADC Data Inversion on data to filter module
0 = EADC Data is not inverted (Default)
1 = EADC Data Inverted
Bit 14: AUTO_GAIN_SHIFT_MODE – Configures Automatic Gain Shifting mode
0 = Fixed mode, gain shifting dependent on saturation of EADC for decreasing gain and less than 1/4 of dynamic range for increasing gain (Default)
1 = NL mode, gain shifting dependent on Non-Linear limit thresholds
Bit 13: AUTO_GAIN_SHIFT_EN – Enables Automatic Gain Shifting mode
0 = Automatic Gain Shifting Mode disabled (Default)
1 = Automatic Gain Shifting Mode enabled
Bit 12: AVG_WEIGHT_EN – Enables weighted averaging in EADC averaging mode, only applicable in 4x and 8x averaging mode. For 4x averaging, two oldest samples are each weighted by 1/8, the next oldest sample has a weight of ¼ and the newest sample is weighted by ½. For 8x averaging, the four oldest samples are each weighted by 1/16, the next 2 oldest samples are weighted by 1/8, the next oldest sample is weighted by ¼ and the newest sample is weighted by ½.
0 = Weighted averaging disabled (Default)
1 = Weighted averaging enabled
Bit 11: AVG_SPATIAL_EN – Enables spatial mode in EADC averaging mode
0 = Consecutive EADC samples averaged based on every received sample trigger from DPWM modules (Default)

1 = EADC samples averaged based on received sample triggers from DPWM modules. 2 sample triggers required for a single averaged sample to filter. 4 sample triggers required for a single averaged sample to filter module

Bit 10-9: AVG_MODE_SEL – Averaging Mode Configuration
0 = 2x Averaging (Default)
1 = 4x Averaging
2 = 8x Averaging

Bits 8-6: EADC_MODE – Selects EADC Mode Operation
0 = Standard mode, EADC samples based on sample triggers from DPWM module (Default)
1 = Averaging Mode, configured by AVG_MODE_SEL
2 = Non-continuous SAR Mode
3 = Continuous SAR Mode
4 = Reserved
5 = Peak Current Mode
6 = Constant Power/Constant Current Control Mode (CPCC module controls switching between Standard Mode and Non-Continuous SAR Mode)
7 = Constant Power/Constant Current Control 2 Mode (CPCC module controls switching between Standard mode and Continuous SAR Mode)

Bits 5-4: AFE_GAIN – AFE Front End Gain Setting
0 = 1x Gain, 8mV/LSB
1 = 2x Gain, 4mV/LSB
2 = 4x Gain, 2mV/LSB
3 = 8x Gain, 1mV/LSB (Default)

Bit 3: SCFE_GAIN_FILTER_SEL – Switched Cap Noise Filter Enable
0 = Disables Switch Cap Noise Filter
1 = Enables Switch Cap Noise Filter (Default)

Bit 2: SCFE_CLK_DIV_2 – Switched Cap Front End Clock Divider Select
0 = Switch Cap Clock divide by 1
1 = Switch Cap Clock divide by 2 (Default)

Bit 1: SCFE_ENA – Switch Cap Front Enable
0 = Disables Switch Cap Front End logic
1 = Enables Switch Cap Front End logic (Default)

Bit 0: EADC_ENA – EADC Enable
0 = Disables EADC
1 = Enables EADC (Default)

21.10.9 Pre-Bias Control Register 0 (PREBIASCTRL0)

Address 0x0018_0028 – Front End Control 2 Pre-Bias Control Register 0
Address 0x001B_0028 – Front End Control 1 Pre-Bias Control Register 0
Address 0x001E_0028 – Front End Control 0 Pre-Bias Control Register 0

Bit Number	17	16	15:8	7:0
Bit Name	PRE_BIAS_POL	PRE_BIAS_EN	PRE_BIAS_RANGE	PRE_BIAS_LIMIT
Access	R/W	R/W	R/W	R/W
Default	0	0	1111_1111	0000_0000

Bit 17: PRE_BIAS_POL – Configures polarity of received error voltage
0 = Error equals Vref-Vin (Default)
1 = Error equals Vin-Vref

Bit 16: PRE_BIAS_EN – Enable Pre-Biasing of Error ADC (Ramp should be disabled during pre-biasing, bit 0 of Ramp Control Register)
0 = Pre-Biasing has not been initiated (Default)
1 = Pre-Biasing by hardware has been enabled

Bits 15-8: PRE_BIAS_RANGE – Sets the acceptable range around the zero error point. If Error

ADC value stays in range for number of samples specified by **PRE_BIAS_LIMIT** (Bits 7:0), **PREBIAS_STATUS** (Bit 0 of Ramp Status Register) is enabled. Range will be +/- **PRE_BIAS_RANGE** around zero error point.
Bits 7-0: PRE_BIAS_LIMIT – Sets the acceptable number of samples in which the Error ADC value stays in range before asserting **PREBIAS_STATUS** (Bit 0 of Ramp Status Register). Counter limit ranges from 0 to 255. If **PREBIAS_STATUS** is set, it will take **PRE_BIAS_LIMIT** samples outside of acceptable range before clearing **PREBIAS_STATUS**.

21.10.10 Pre-Bias Control Register 1 (PREBIASCTRL1)

Address 0x0018_002C – Front End Control 2 Pre-Bias Control Register 1
Address 0x001B_002C – Front End Control 1 Pre-Bias Control Register 1
Address 0x001E_002C – Front End Control 0 Pre-Bias Control Register 1

Bit Number	23:16	15:14	13:0
Bit Name	SAMPLES_PER_ADJ	RESERVED	MAX_DAC_ADJ
Access	R/W	-	R/W
Default	0000_0000	00	00_0000_0000_0000

Bits 23-16: SAMPLES_PER_ADJ – Configures the number of EADC samples between Pre-Bias DAC setpoint adjustments
0 = DAC Setpoint adjustment on each EADC sample
1 = DAC Setpoint adjustment after 2 EADC sample
2 = DAC Setpoint adjustment after 3 EADC samples
…….
255 = DAC Setpoint adjustment after 256 EADC samples
Bits 15-14: RESERVED – Unused Bits
Bits 13-0: MAX_DAC_ADJ – Configures the maximum DAC setpoint adjustment step

21.10.11 SAR Control Register (SARCTRL)

Address 0x0018_0030 – Front End Control 2 SAR Control Register
Address 0x001B_0030 – Front End Control 1 SAR Control Register
Address 0x001E_0030 – Front End Control 0 SAR Control Register

Bit Number	31:24	23:16	15:8
Bit Name	EADC_WINDOW_2	EADC_WINDOW_1	SAR_RANGE
Access	R/W	R/W	R/W
Default	0010_1000	0110_0000	0000_0000

Bit Number	7:2	1:0
Bit Name	RESERVED	SAR_RESOLUTION
Access	-	R/W
Default	0000_00	00

Bits 31-24: EADC_WINDOW_2 – Configures acceptable range of error values to transition to AFE Gain of 2 during SAR process
Bits 23-16: EADC_WINDOW_1 – Configures acceptable range of error values to transition to AFE Gain of 1 during SAR process
Bits 15-8: SAR_RANGE – Configures acceptable range of error values before declaring SAR completion
Bits 7-2: RESERVED – Unused bits
Bits 1-0: SAR_RESOLUTION – Configures the final resolution for SAR Conversions
0 = 8mV Resolution, 1x AFE Gain

1 = 4mV Resolution, 2x AFE Gain
2 = 2mV Resolution, 4x AFE Gain
3 = 1mV Resolution, 8x AFE Gain

21.10.12 SAR Timing Register (SARTIMING)

Address 0x0018_0034 – Front End Control 2 SAR Timing Register
Address 0x001B_0034– Front End Control 1 SAR Timing Register
Address 0x001E_0034 – Front End Control 0 SAR Timing Register

Bit Number	10:8	7
Bit Name	SAR_TIMING_UPPER	RESERVED
Access	R/W	-
Default	100	0

Bit Number	6:4	3	2:0
Bit Name	SAR_TIMING_MID	RESERVED	SAR_TIMING_LOWER
Access	R/W	-	R/W
Default	011	0	010

Bits 10-8: SAR_TIMING_UPPER – Configures timing for Bits 9:8 of DAC setpoint for SAR Algorithm
Bit 7: RESERVED – Unused bit
Bits 6-4: SAR_TIMING_MID – Configures timing for Bits 7:6 of DAC setpoint for SAR Algorithm
Bit 3: RESERVED – Unused bit
Bits 2-0: SAR_TIMING_LOWER – Configures timing for Bits 5:0 of DAC setpoint for SAR Algorithm

21.10.13 EADC Value Register (EADCVALUE)

Address 0x0018_0038 – Front End Control 2 EADC Value Register
Address 0x001B_0038 – Front End Control 1 EADC Value Register
Address 0x001E_0038 – Front End Control 0 EADC Value Register

Bit Number	25:16	15	14
Bit Name	ABS_VALUE	EADC_SAT_HIGH	EADC_SAT_HIGH
Access	R	R	R
Default	-	-	-

Bit Number	13:9	8:0
Bit Name	RESERVED	ERROR_VALUE
Access	-	R
Default	00_000	-

Bits 25-16: ABS_VALUE – 10-bit Absolute Value calculated by Front End Control Module with a resolution of 1.5625mV/bit
Bit 15: EADC_SAT_HIGH – EADC Saturation High Indicator
0 = EADC output is not saturated at high limit
1 = EADC output is saturated at high limit
Bit 14: EADC_SAT_LOW – EADC Saturation Low Indicator
0 = EADC output is not saturated at low limit
1 = EADC output is saturated at low limit
Bits 13-9: RESERVED – Unused bits
Bits 8-0: ERROR_VALUE – Signed 9-bit Error value measured by Front End Control Module with a resolution of 1mV/bit

21.10.14 EADC Raw Value Register (EADCRAWVALUE)

Address 0x0018_003C – Front End Control 2 EADC Raw Value Register
Address 0x001B_003C – Front End Control 1 EADC Raw Value Register
Address 0x001E_003C – Front End Control 0 EADC Raw Value Register

Bit Number	8:0
Bit Name	RAW_ERROR_VALUE
Access	R
Default	-

Bits 8-0: RAW_ERROR_VALUE – Signed 9-bit Error value measured by Front End Control Module with a resolution of 1mV/bit. Value is raw EADC data before averaging.

21.10.15 DAC Status Register (DACSTAT)

Address 0x0018_0040 – Front End Control 2 DAC Status Register
Address 0x001B_0040 – Front End Control 1 DAC Status Register
Address 0x001E_0040 – Front End Control 0 DAC Status Register

Bit Number	9:0
Bit Name	DAC_VALUE
Access	R
Default	00_0000_0000

Bits 9-0: DAC_VALUE – Current 10-bit Value sent to DAC

21.11 *Miscellaneous Analog Control*

The Miscellaneous Analog Control module provides control signals to the oscillator and AFE blocks.

21.11.1 Clock Trim Register (CLKTRIM)

Address FFF7F000

Bit Number	16	15:12	11:8	7:0
Bit Name	RESET_DISABLE	HFO_FINE_TRIM	HFO_COARSE_TRIM	RESERVED
Access	R/W	R/W	R/W	
Default	0	1000	0110	

Bits 16: RESET_DISABLE - Firmware disable of RESET pin
Bits 15-12: HFO_FINE_TRIM - High Frequency Oscillator Clock Fine Trim Bits. Register will be programmed during device test. Changing this value will change the clock speed. It should only be changed in conjunction with the coarse trim and with an additional clock reference for comparison
Bits 11-8: HFO_COARSE_TRIM - High Frequency Oscillator Clock Coarse Trim Bits. Register will be programmed during device test. Changing this value will change the clock speed. It should only be changed in conjunction with the fine trim and with an additional clock reference for comparison
Bits 7-0: **RESERVED** – These bits are reserved for TI use and should be preserved in whatever state the device starts up in. Modifying the contents of these bits may cause the UCD3138A64 to move out of specification.

21.11.2 Package ID Register (PKGID)

Address FFF7F010

Bit Number	1:0
Bit Name	PKG_ID
Access	R/W
Default	00

Bits 1-0: PKG_ID – Represents package type of device
0 = 80-pin package (Default)

21.11.3 Brownout Register (BROWNOUT)

Address FFF7F014

Bit Number	2	1	0
Bit Name	INT	INT_EN	COMP_EN
Access	R	R/W	R/W
Default	-	0	0

Bit 2: INT – Brownout Interrupt Status
0 = No Brownout Condition observed
1 = Brownout Condition observed
Bit 1: INT_EN – Brownout Interrupt Enable
0 = Brownout Interrupt disabled (Default)
1 = Brownout Interrupt enabled
Bit 0: COMP_EN – Brownout Comparator Enable
0 = Brownout comparator logic disabled (Default)
1 = Brownout comparator logic enabled

21.11.4 Global I/O EN Register (GLBIOEN)

Address FFF7F018

Bit Number	31:0
Bit Name	GLOBAL_IO_EN
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 31-0: GLOBAL_IO_EN – This register enables the global control of digital I/O pins
0 = Control of IO is done by the functional block assigned to the IO (Default)
1 = Control of IO is done by Global IO registers.

Bit assignment is done by this table:

BIT	PIN_NAME
31	TMR_PWM[2]
30	TMR_PWM[3]
29	FAULT[3]
28	ADC_EXT_TRIG
27	TCK
26	TDO
25	TMS
24	TDI
23	SCI_TX[1]
22	SCI_TX[0]
21	SCI_RX[1]
20	SCI_RX[0]
19	TMR_CAP[0]
18	TMR_PWM[1]
17	TMR_PWM[0]
16	TMR_CAP[1]
15	I2C-DATA
14	CONTROL
13	ALERT
12	EXT_INT
11	FAULT[2]
10	FAULT[1]
9	FAULT[0]
8	SYNC
7	DPWM3B
6	DPWM3A
5	DPWM2B
4	DPWM2A
3	DPWM1B
2	DPWM1A
1	DPWM0B
0	DPWM0A

21.11.5 Global I/O OE Register (GLBIOOE)

Address FFF7F01C

Bit Number	31:0
Bit Name	GLOBAL_IO_OE
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 31-0: GLOBAL_IO_OE – This register controls the output enable signals for all digital I/O pins

0 = Input (Default)
1 = Output

Bit assignment is done by this table:

BIT	PIN_NAME
31	TMR_PWM[2]
30	TMR_PWM[3]
29	FAULT[3]
28	ADC_EXT_TRIG
27	TCK
26	TDO
25	TMS
24	TDI
23	SCI_TX[1]
22	SCI_TX[0]
21	SCI_RX[1]
20	SCI_RX[0]
19	TMR_CAP[0]
18	TMR_PWM[1]
17	TMR_PWM[0]
16	TMR_CAP[1]
15	I2C-DATA
14	CONTROL
13	ALERT
12	EXT_INT
11	FAULT[2]
10	FAULT[1]
9	FAULT[0]
8	SYNC
7	DPWM3B
6	DPWM3A
5	DPWM2B
4	DPWM2A
3	DPWM1B
2	DPWM1A
1	DPWM0B
0	DPWM0A

21.11.6 Global I/O Open Drain Control Register (GLBIOOD)

Address FFF7F020

Bit Number	31:0
Bit Name	GLOBAL_IO_OD
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 31-0: GLOBAL_IO_OD – This register controls if the global IO is configured as an open drain. This bit multiplexes the GLOBAL_IO_VALUE register to the OE signals

0 = Normal I/O (Default)
1 = Open Drain

Bit assignment is done by this table:

BIT	PIN_NAME
31	TMR_PWM[2]
30	TMR_PWM[3]
29	FAULT[3]
28	ADC_EXT_TRIG
27	TCK
26	TDO
25	TMS
24	TDI
23	SCI_TX[1]
22	SCI_TX[0]
21	SCI_RX[1]
20	SCI_RX[0]
19	TMR_CAP[0]
18	TMR_PWM[1]
17	TMR_PWM[0]
16	TMR_CAP[1]
15	I2C-DATA
14	CONTROL
13	ALERT
12	EXT_INT
11	FAULT[2]
10	FAULT[1]
9	FAULT[0]
8	SYNC
7	DPWM3B
6	DPWM3A
5	DPWM2B
4	DPWM2A
3	DPWM1B
2	DPWM1A
1	DPWM0B
0	DPWM0A

21.11.7 Global I/O Value Register (GLBIOVAL)

Address FFF7F024

Bit Number	31:0
Bit Name	GLOBAL_IO_VALUE
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 31-0: GLOBAL_IO_VALUE – This register set the output value of the digital I/O pins when configured as outputs

0 = Digital I/O pin configured as low in output mode (Default)
1 = Digital I/O pin configured as high in output mode

Bit assignment is done by this table:

BIT	PIN_NAME
31	TMR_PWM[2]
30	TMR_PWM[3]
29	FAULT[3]
28	ADC_EXT_TRIG
27	TCK
26	TDO
25	TMS
24	TDI
23	SCI_TX[1]
22	SCI_TX[0]
21	SCI_RX[1]
20	SCI_RX[0]
19	TMR_CAP[0]
18	TMR_PWM[1]
17	TMR_PWM[0]
16	TMR_CAP[1]
15	I2C-DATA
14	CONTROL
13	ALERT
12	EXT_INT
11	FAULT[2]
10	FAULT[1]
9	FAULT[0]
8	SYNC
7	DPWM3B
6	DPWM3A
5	DPWM2B
4	DPWM2A
3	DPWM1B
2	DPWM1A
1	DPWM0B
0	DPWM0A

21.11.8 Global I/O Read Register (GLBIOREAD)

Address FFF7F028

Bit Number	31:0
Bit Name	GLOBAL_IO_READ
Access	R
Default	-

Bits 31-0: GLOBAL_IO_READ – This register provides the value on these signals after I/O muxing

0 = Digital I/O pin low (Default)
1 = Digital I/O pin high

Bit assignment is done by this table:

BIT	PIN_NAME
31	TMR_PWM[2]
30	TMR_PWM[3]
29	FAULT[3]
28	ADC_EXT_TRIG
27	TCK
26	TDO
25	TMS
24	TDI
23	SCI_TX[1]
22	SCI_TX[0]
21	SCI_RX[1]
20	SCI_RX[0]
19	TMR_CAP[0]
18	TMR_PWM[1]
17	TMR_PWM[0]
16	TMR_CAP[1]
15	I2C-DATA
14	CONTROL
13	ALERT
12	EXT_INT
11	FAULT[2]
10	FAULT[1]
9	FAULT[0]
8	SYNC
7	DPWM3B
6	DPWM3A
5	DPWM2B
4	DPWM2A
3	DPWM1B
2	DPWM1A
1	DPWM0B
0	DPWM0A

21.11.9 RTCCTRLI/O Mux Control Register (IOMUX)

Address FFF7F030

Bit Number	7:6	5:4	3
Bit Name	TCAP1_MUX_SEL	TCAP0_MUX_SEL	RESERVED
Access	R/W	R/W	R
Default	00	00	0

Bit Number	2	1	0
Bit Name	JTAG_MUX_SEL	RTC_CLK_IN_SEL	RTC_CLK_OUT_SEL
Access	R/W	R/W	R/W
Default	See below	0	0

Bits 7-6: TCAP1_MUX_SEL – Pin Mux Select
0: TMR_CAP_1 function utilized via the TMR_CAP_1 pin
1: TMR_CAP_1 function utilized via the TDI pin
2: TMR_CAP_1 function utilized via the TDO pin
3: TMR_CAP_1 function utilized via the TMR_CAP_0 pin

Bits 5-4: TCAP0_MUX_SEL – Pin Mux Select
0: TMR_CAP_0 function utilized via the TMR_CAP_0 pin
1: TMR_CAP_0 function utilized via the TDI pin
2: TMR_CAP_0 function utilized via the TDO pin
3: TMR_CAP_0 function utilized via the TMR_CAP_1 pin

Bit 3: RESERVED

Bit 2: JTAG_MUX_SEL
0: JTAG pins function as JTAG port. TCK/TMS/TDI/TDO
1: JTAG pins disabled
JTAG port functions as SPI port in this mode.
TCK -> SPI_CLK
TMS -> SPI_CS
TDI -> SPI_MISO
TDO -> SPI_MOSI
This bit will be set to a 1 if there is a valid checksum in program flash and ROM jumps to directly to program flash on power up. If there is no valid checksum, and the ROM program stays in ROM mode for program download, this bit will be a 0.

Bit 1: RTC_CLK_IN_SEL – Pin Mux Select
0: Input to RTC module clock connected to XTAL_CLK_IN
1: Input to RTC module clock connected to TCK

Bit 0: RTC_CLK_OUT_SEL – Pin Mux Select
0: Output of RTC reference clock disabled
1: Output of RTC reference clock connected to TCK

21.11.10 Current Sharing Control Register (CSCTRL)

Address FFF7F038

Bit Number	23:16	15:8	7:4	3:0
Bit Name	DPWM_DUTY	DPMW_PERIOD	RESERVED	TEST_MODE
Access	R/W	R/W	-	R/W
Default	0000_0000	0000_0000	0000	0000

Bits 23-16: DPWM_DUTY – Configures Pulse Width/Duty Cycle for DPWM output to Current Sharing circuit. Resolution of LSB equals period of MCLK clock
Bits 15-8: DPWM_PERIOD – Configures Period for DPWM output to Current Sharing circuit. Output period equals DPWM_PERIOD+1 * LSB resolution. Resolution of LSB equals period of MCLK clock
Bits 7-4: RESERVED – Unused bits
Bits 3-0: TEST_MODE – Controls Current Sharing Operation

Test Mode	EN_SW1	EN_SW2	DIS_RES	DPWM	EN_HALF_CURR
0000	0	0	1	0	0
0001	1	0	0	ACTIVE	0
0010	0	0	1	0	0
0011	0	1	1	0	0
01XX	1	0	1	1	0
10XX	0	0	0	0	0
11XX	1	0	0	1	1

21.11.11 Temperature Reference Register (TEMPREF)

Address FFF7F03C

Bit Number	11:0
Bit Name	TEMP_REF
Access	R/W
Default	0000_0000_0000

Bits 11-0: TEMP_REF – Reference measurement taken during factory trim, ADC12 measurement of the internal temperature sensor at room temperature for use in offset calibration

21.11.12 Power Disable Control Register (PWRDISCTRL)

Address FFF7F040

Bit Number	20	19	18
Bit Name	RTC_CLK_EN	I2C_CLK_EN	SPI_CLK_EN
Access	R/W	R/W	R/W
Default	1	1	1

Bit Number	17	16	15
Bit Name	PCM_CLK_EN	CPCC_CLK_EN	FILTER2_CLK_EN
Access	R/W	R/W	R/W
Default	1	1	1

Bit Number	14	13	12	11
Bit Name	FILTER1_CLK_EN	FILTER0_CLK_EN	FE_CTRL2_CLK_EN	FE_CTRL1_CLK_EN
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit Number	10	9	8
Bit Name	FE_CTRL0_CLK_EN	DPWM3_CLK_EN	DPWM2_CLK_EN
Access	R/W	R/W	R/W
Default	1	1	1

Bit Number	7	6	5	4
Bit Name	DPWM1_CLK_EN	DPWM0_CLK_EN	SCI1_CLK_EN	SCI0_CLK_EN
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit Number	3	2	1	0
Bit Name	ADC12_CLK_EN	PMBUS_CLK_EN	GIO_CLK_EN	TIMER_CLK_EN
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit 17: PCM_CLK_EN – Clock Enable for Digital Peak Current Control Module
0 = Disables clocks to Digital Peak Current Control Module
1 = Enables clocks to Digital Peak Current Control Module (Default)
Bit 16: CPCC_CLK_EN – Clock Enable for Constant Power/Constant Current Module
0 = Disables clocks to Constant Power/Constant Current Module

1 = Enables clocks to Constant Power/Constant Current Module (Default)

Bit 15: FILTER2_CLK_EN – Clock Enable for Filter 2 Module
0 = Disables clocks to Filter 2 Module
1 = Enables clocks to Filter 2 Module (Default)

Bit 14: FILTER1_CLK_EN – Clock Enable for Filter 1 Module
0 = Disables clocks to Filter 1 Module
1 = Enables clocks to Filter 1 Module (Default)

Bit 13: FILTER0_CLK_EN – Clock Enable for Filter 0 Module
0 = Disables clocks to Filter 0 Module
1 = Enables clocks to Filter 0 Module (Default)

Bit 12: FE_CTRL2_CLK_EN – Clock Enable for Front End Control 2 Module
0 = Disables clocks to Front End Control 2 Module
1 = Enables clocks to Front End Control 2 Module (Default)

Bit 11: FE_CTRL1_CLK_EN – Clock Enable for Front End Control 1 Module
0 = Disables clocks to Front End Control 1 Module
1 = Enables clocks to Front End Control 1 Module (Default)

Bit 10: FE_CTRL0_CLK_EN – Clock Enable for Front End Control 0 Module
0 = Disables clocks to Front End Control 0 Module
1 = Enables clocks to Front End Control 0 Module (Default)

Bit 9: DPWM3_CLK_EN – Clock Enable for DPWM 3 Module
0 = Disables clocks to DPWM 3 Module
1 = Enables clocks to DPWM 3 Module (Default)

Bit 8: DPWM2_CLK_EN – Clock Enable for DPWM 2 Module
0 = Disables clocks to DPWM 2 Module
1 = Enables clocks to DPWM 2 Module (Default)

Bit 7: DPWM1_CLK_EN – Clock Enable for DPWM 1 Module
0 = Disables clocks to DPWM 1 Module
1 = Enables clocks to DPWM 1 Module (Default)

Bit 6: DPWM0_CLK_EN – Clock Enable for DPWM 0 Module
0 = Disables clocks to DPWM 0 Module
1 = Enables clocks to DPWM 0 Module (Default)

Bit 5: SCI1_CLK_EN – Clock Enable for SCI/UART 1Module
0 = Disables clocks to SCI/UART 1 Module
1 = Enables clocks to SCI/UART 1 Module (Default)

Bit 4: SCI0_CLK_EN – Clock Enable for SCI/UART 0 Module
0 = Disables clocks to SCI/UART 0 Module
1 = Enables clocks to SCI/UART 0 Module (Default)

Bit 3: ADC12_CLK_EN – Clock Enable for ADC12 Control Module
0 = Disables clocks to ADC12 Control Module
1 = Enables clocks to ADC12 Control Module (Default)

Bit 2: PMBUS_CLK_EN – Clock Enable for PMBus Interface Module
0 = Disables clocks to PMBus Interface Module
1 = Enables clocks to PMBus Interface Module (Default)

Bit 1: GIO_CLK_EN – Clock Enable for GIO Module
0 = Disables clocks to GIO Module
1 = Enables clocks to GIO Module (Default)

Bit 0: TIMER_CLK_EN – Clock Enable for Timer Module
0 = Disables clocks to Timer Module
1 = Enables clocks to Timer Module (Default)

21.12 *PMBus Interface*

21.12.1 PMBUS Control Register 1 (PMBCTRL1)

PMBus Address FFF7F600
PMBus1 Address FFF7F700

Bit Number	20	19	18	17
Bit Name	PRC_CALL	GRP_CMD	PEC_ENA	EXT_CMD
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	16	15:8	7:1	0
Bit Name	CMD_ENA	BYTE_COUNT	SLAVE_ADDR	RW
Access	R/W	R/W	R/W	R/W
Default	0	0000_0000	000_0000	0

Bit 20: PRC_CALL – Master Process Call Message Enable
0 = Default state for all messages besides Process Call message (Default)
1 = Enables transmission of Process Call message
Bit 19: GRP_CMD – Master Group Command Message Enable
0 = Default state for all messages besides Group Command message (Default)
1 = Enables transmission of Group Command message
Bit 18: PEC_ENA – Master PEC Processing Enable
0 = Disables PEC processing (Default)
1 = Enables PEC byte transmission/reception
Bit 17: EXT_CMD – Master Extended Command Code Enable
0 = Use 1 byte for Command Code (Default)
1 = Use 2 bytes for Command Code
Bit 16: CMD_ENA – Master Command Code Enable
0 = Disables use of command code on Master initiated messages (Default)
1 = Enables use of command code on Master initiated messages
Bits 15-8: BYTE_COUNT – Indicates number of data bytes transmitted in current message. Byte count does not include any device addresses, command words or block lengths in block messages. In block messages, the PMBus Interface automatically inserts the block length into the message based on the byte count setting. The firmware only needs to load the address, command words and data to be transmitted. PMBus Interface supports byte writes up to 255 bytes.
Bits 7-1: SLAVE_ADDR – Specifies the address of the slave to which the current message is directed towards.
Bit 0: RW – Indicates if current Master initiated message is read operation or write operation.
0 = Message is a write transaction (data from Master to Slave) (Default)
1 = Message is a read transaction (data from Slave to Master)

21.12.2 PMBus Transmit Data Buffer (PMBTXBUF)

PMBus Address FFF7F604
PMBus1 Address FFF7F704

Bit Number	31:24	23:16	15:8	7:0
Bit Name	BYTE3	BYTE2	BYTE1	BYTE0
Access	R/W	R/W	R/W	R/W
Default	0000_0000	0000_0000	0000_0000	0000_0000

Bits 31-24: BYTE3 – Last data byte transmitted from Transmit Data Buffer
Bits 23-16: BYTE2 – Third data byte transmitted from Transmit Data Buffer
Bits 15-8: BYTE1 – Second data byte transmitted from Transmit Data Buffer
Bits 7-0: BYTE0 – First data byte transmitted from Transmit Data Buffer

21.12.3 PMBus Receive Data Register (PMBRXBUF)

PMBus Address FFF7F608
PMBus1 Address FFF7F708

Bit Number	31:24	23:16	15:8	7:0
Bit Name	BYTE3	BYTE2	BYTE1	BYTE0
Access	R	R	R	R
Default	-	-	-	-

Bits 31-24: BYTE3 – Last data byte received in Receive Data Buffer
Bits 23-16: BYTE2 – Third data byte received in Receive Data Buffer
Bits 15-8: BYTE1 – Second data byte received in Receive Data Buffer
Bits 7-0: BYTE0 – First data byte received in Receive Data Buffer

21.12.4 PMBus Acknowledge Register (PMBACK)

PMBus Address FFF7F60C
PMBus1 Address FFF7F70C

Bit Number	0
Bit Name	ACK
Access	R/W
Default	0

Bit 0: ACK – Allows firmware to acknowledge or not acknowledge received data
0 = NACK received data (Default)
1 = Acknowledge received data, bit clears upon issue of ACK on PMBus

21.12.5 PMBus Status Register (PMBST)

PMBus Address FFF7F610

PMBus1 Address FFF7F710

Bit Number	21	20	19	18
Bit Name	SCL_RAW	SDA_RAW	CONTROL_RAW	ALERT_RAW
Access	R	R	R	R
Default	-	-	-	-

Bit Number	17	16	15
Bit Name	CONTROL_EDGE	ALERT_EDGE	MASTER
Access	R	R	R
Default	-	-	-

Bit Number	14	13	12	11	10
Bit Name	LOST_ARB	BUS_FREE	UNIT_BUSY	RPT_START	SLAVE_ADDR_READY
Access	R	R	R	R	R
Default	-	-	-	-	-

Bit Number	9	8	7	6
Bit Name	CLK_HIGH_TIMEOUT	CLK_LOW_TIMEOUT	PEC_VALID	NACK
Access	R	R	R	R
Default	-	-	-	-

Bit Number	5	4	3	2:0
Bit Name	EOM	DATA_REQUEST	DATA_READY	RD_BYTE_COUNT
Access	R	R	R	R
Default	-	-	-	-

Bit 21: SCL_RAW – PMBus Clock Pin Real Time Status
0 = PMBus clock pin observed at logic level low
1 = PMBus clock pin observed at logic level high

Bit 20: SDA_RAW – PMBus Data Pin Real Time Status
0 = PMBus data pin observed at logic level low
1 = PMBus data pin observed at logic level high

Bit 19: CONTROL_RAW – Control Pin Real Time Status – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Control pin observed at logic level low
1 = Control pin observed at logic level high

Bit 18: ALERT_RAW – Alert Pin Real Time Status – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Alert pin observed at logic level low
1 = Alert pin observed at logic level high

Bit 17: CONTROL_EDGE – Control Edge Detection Status – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Control pin has not transitioned
1 = Control pin has been asserted by another device on PMBus

Bit 16: ALERT_EDGE – Alert Edge Detection Status – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Alert pin has not transitioned
1 = Alert pin has been asserted by another device on PMBus
Bit 15: MASTER – Master Indicator
0 = PMBus Interface in Slave Mode or Idle Mode
1 = PMBus Interface in Master Mode
Bit 14: LOST_ARB – Lost Arbitration Flag
0 = Master has attained control of PMBus
1 = Master has lost arbitration and control of PMBus
Bit 13: BUS_FREE – PMBus Free Indicator
0 = PMBus processing current message
1 = PMBus available for new message
Bit 12: UNIT_BUSY – PMBus Busy Indicator
0 = PMBus Interface is idle, ready to transmit/receive message
1 = PMBus Interface is busy, processing current message
Bit 11: RPT_START – Repeated Start Flag
0 = No Repeated Start received by interface
1 = Repeated Start condition received by interface
Bit 10: SLAVE_ADDR_READY – Slave Address Ready
0 = Indicates no slave address is available for reading
1 = Slave address ready to be read from Receive Data Register (Bits 6:0)
Bit 9: CLK_HIGH_DETECTED – Clock High Detection Status
0 = No Clock High condition detected
1 = Clock High exceeded 50us during message
Bit 8: CLK_LOW_TIMEOUT – Clock Low Timeout Status
0 = No clock low timeout detected
1 = Clock low timeout detected, clock held low for greater than 35ms
Bit 7: PEC_VALID – PEC Valid Indicator
0 = Received PEC not valid (if EOM is asserted)
1 = Received PEC is valid
Bit 6: NACK – Not Acknowledge Flag Status
0 = Data transmitted has been accepted by receiver
1 = Receiver has not accepted transmitted data
Bit 5: EOM – End of Message Indicator
0 = Message still in progress or PMBus in idle state.
1 = End of current message detected
Bit 4: DATA_REQUEST – Data Request Flag
0 = No data needed by PMBus Interface
1 = PMBus Interface request additional data. PMBus clock stretching enabled to stall bus until firmware provides transmit data.
Bit 3: DATA_READY – Data Ready Flag
0 = No data available for reading by processor
1 = PMBus Interface read buffer full, firmware required to read data prior to further bus activity. PMBus clock stretching enabled to stall bus until data is read by firmware.
Bits 2-0: RD_BYTE_COUNT – Number of Data Bytes available in Receive Data Register
0 = No received data
1 = 1 byte received. Data located in Receive Data Register, Bits 7-0
2 = 2 bytes received. Data located in Receive Data Register, Bits 15-0
3 = 3 bytes received. Data located in Receive Data Register, Bits 23-0
4 = 4 bytes received. Data located in Receive Data Register, Bits 31-0

21.12.6 PMBus Interrupt Mask Register (PMBINTM)

PMBus Address FFF7F614
PMBus1 Address FFF7F714

Bit Number	9	8	7	6
Bit Name	CLK_HIGH_TIMEOUT	LOST_ARB	CONTROL	ALERT
Access	R/W	R/W	R/W	R/W
Default	1	1	1	1

Bit Number	5	4	3
Bit Name	EOM	SLAVE_ADDR_READY	DATA_REQUEST
Access	R/W	R/W	R/W
Default	1	1	1

Bit Number	2	1	0
Bit Name	DATA_READY	BUS_LOW_TIMEOUT	BUS_FREE
Access	R/W	R/W	R/W
Default	1	1	1

Bit 9: CLK_HIGH_TIMEOUT – Clock High Timeout Interrupt Mask
0 = Generates interrupt if clock high exceeds 50us during message
1 = Disables interrupt generation for Clock High Timeout (Default)
Bit 8: LOST_ARB – Lost Arbitration Interrupt Mask
0 = Generates interrupt upon assertion of Lost Arbitration flag
1 = Disables interrupt generation upon assertion of Lost Arbitration flag (Default)
Bit 7: CONTROL – Control Detection Interrupt Mask – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Generates interrupt upon assertion of Control flag
1 = Disables interrupt generation upon assertion of Control flag (Default)
Bit 6: ALERT – Alert Detection Interrupt Mask – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Generates interrupt upon assertion of Alert flag
1 = Disables interrupt generation upon assertion of Alert flag (Default)
Bit 5: EOM – End of Message Interrupt Mask
0 = Generates interrupt upon assertion of End of Message flag
1 = Disables interrupt generation upon assertion of End of Message flag (Default)
Bit 4: SLAVE_ADDR_READY – Slave Address Ready Interrupt Mask
0 = Generates interrupt upon assertion of Slave Address Ready flag
1 = Disables interrupt generation upon assertion of Slave Address Ready flag (Default)
Bit 3: DATA_REQUEST – Data Request Interrupt Mask
0 = Generates interrupt upon assertion of Data Request flag
1 = Disables interrupt generation upon assertion of Data Request flag (Default)
Bit 2: DATA_READY – Data Ready Interrupt Mask
0 = Generates interrupt upon assertion of Data Ready flag
1 = Disables interrupt generation upon assertion of Data Ready flag (Default)
Bit 1: BUS_LOW_TIMEOUT – Clock Low Timeout Interrupt Mask
0 = Generates interrupt upon assertion of Clock Low Timeout flag
1 = Disables interrupt generation upon assertion of Clock Low Timeout flag (Default)
Bit 0: BUS_FREE – Bus Free Interrupt Mask
0 = Generates interrupt upon assertion of Bus Free flag
1 = Disables interrupt generation upon assertion of Bus Free flag (Default)

21.12.7 PMBus Control Register 2 (PMBCTRL2)

PMBus Address FFF7F618

PMBus1 Address FFF7F718

Bit Number	30	29:23
Bit Name	SLAVE_ADDR_2_EN	SLAVE_ADDR_2
Access	R/W	R/W
Default	0	110_0000

Bit Number	22:21	20	19	18:16
Bit Name	RX_BYTE_ACK_CNT	MAN_CMD	TX_PEC	TX_COUNT
Access	R/W	R/W	R/W	R/W
Default	11	0	0	000

Bit Number	15	14:8	7	6:0
Bit Name	PEC_ENA	SLAVE_MASK	MAN_SLAVE_ACK	SLAVE_ADDR
Access	R/W	R/W	R/W	R/W
Default	0	111_1111	0	111_1100

Bit 30: SLAVE_ADDR_2_EN – Enable auto detection of the 2nd slave address.
0 = 2nd slave address disabled (default)
1 = 2nd slave address enabled

Bits 29-23: SLAVE_ADDR_2 – Configures the second device address of the slave. Used in automatic slave address acknowledge mode (default mode).

Bit 22-21: RX_BYTE_ACK_CNT – Configures number of data bytes to automatically acknowledge when receiving data in slave mode.
00 = 1 byte received by slave. Firmware is required to manually acknowledge every received byte.
01 = 2 bytes received by slave. Hardware automatically acknowledges the first received byte. Firmware is required to manually acknowledge after the second received byte.
10 = 3 bytes received by slave. Hardware automatically acknowledges the first 2 received bytes. Firmware is required to manually acknowledge after the third received byte.
11 = 4 bytes received by slave. Hardware automatically acknowledges the first 3 received bytes. Firmware is required to manually acknowledge after the fourth received byte (Default)

Bit 20: MAN_CMD – Manual Command Acknowledgement Mode
0 = Slave automatically acknowledges received command code (Default)
1 = Data Request flag generated after receipt of command code, firmware required to issue ACK to continue message

Bit 19: TX_PEC – Asserted when the slave needs to send a PEC byte at end of message. PMBus Interface will transmit the calculated PEC byte after transmitting the number of data bytes indicated by TX Byte Cnt(Bits 19:17).
0 = No PEC byte transmitted (Default)
1 = PEC byte transmitted at end of current message

Bit 18-16: TX_COUNT– Number of valid bytes in Transmit Data Register
0 = No bytes valid (Default)
1 = One byte valid, Byte #0 (Bits 7:0 of Receive Data Register)
2 = Two bytes valid, Bytes #0 and #1 (Bits 15:0 of Receive Data Register)
3 = Three bytes valid, Bytes #0-2 (Bits 23:0 of Receive Data Register)
4 = Four bytes valid, Bytes #0-3 (Bits 31:0 of Receive Data Register)

Bit 15: PEC_ENA – PEC Processing Enable
0 = PEC processing disabled (Default)
1 = PEC processing enabled
Bit 14-8: SLAVE_MASK – Used in address detection, the slave mask enables acknowledgement of multiple device addresses by the slave. Writing a '0' to a bit within the slave mask enables the corresponding bit in the slave address to be either '1' or '0' and still allow for a match. Writing a '0' to all bits in the mask enables the PMBus Interface to acknowledge any device address. Upon power-up, the slave mask defaults to 7Fh, indicating the slave will only acknowledge the address programmed into the Slave Address (Bits 6-0). Not applicable to the 2nd Slave Address.
Bit 7: MAN_SLAVE_ACK– Manual Slave Address Acknowledgement Mode
0 = Slave automatically acknowledges device address specified in SLAVE_ADDR, Bits 6-0 (Default)
1 = Enables the Manual Slave Address Acknowledgement Mode. Firmware is required to read received address and acknowledge on every message
Bits 6-0: SLAVE_ADDR – Configures the current device address of the slave. Used in automatic slave address acknowledge mode (default mode). The PMBus Interface will compare the received device address with the value stored in the Slave Address bits and the mask configured in the Slave Mask bits. If matching, the slave will acknowledge the device address.

21.12.8 PMBus Hold Slave Address Register (PMBHSA)

PMBus Address FFF7F61C
PMBus1 Address FFF7F71C

Bit Number	7:1	0
Bit Name	SLAVE_ADDR	SLAVE_RW
Access	R	R
Default	-	-

Bits 7-1: SLAVE_ADDR – Stored device address acknowledged by the slave
Bit 0: SLAVE_RW – Stored R/W bit from address acknowledged by the slave
0 = Write Access
1 = Read Access

21.12.9 PMBus Control Register 3 (PMBCTRL3)

PMBus Address FFF7F620

PMBus1 Address FFF7F720

Bit Number	24	23
Bit Name	I2C_MODE_EN	CLK_HI_DIS
Access	R/W	R/W
Default	0	1

Bit Number	22	21	20	19	18
Bit Name	MASTER_EN	SLAVE_EN	CLK_LO_DIS	IBIAS_B_EN	IBIAS_A_EN
Access	R/W	R/W	R/W	R/W	R/W
Default	0	1	0	0	0

Bit Number	17	16	15	14	13
Bit Name	SCL_DIR	SCL_VALUE	SCL_MODE	SDA_DIR	SDA_VALUE
Access	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit Number	12	11	10	9
Bit Name	SDA_MODE	CNTL_DIR	CNTL_VALUE	CNTL_MODE
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	8	7	6	5
Bit Name	ALERT_DIR	ALERT _VALUE	ALERT_MODE	CNTL_INT_EDGE
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	4	3	2	1	0
Bit Name	Reserved	FAST_MODE	BUS_LO_INT_EDGE	ALERT_EN	RESET
Access	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0

Bit 21: I2C_MODE_EN – I2C Mode Enable – Utilized for Master mode only
0 = I2C Mode Disabled (Default)
1 = I2C Mode Enabled

Bit 20: CLK_HI_DIS – Clock High Timeout Disable
0 = Clock High Timeout Enabled
1 = Clock High Timeout Disabled (Default)

Bit 22: MASTER_EN – PMBus Master Enable
0 = Disables PMBus Master capability (Default)
1 = Enables PMBus Master capability
Bit 21: SLAVE_EN – PMBus Slave Enable
0 = Disables PMBus Slave capability
1 = Enables PMBus Slave capability (Default)
Bit 20: CLK_LO_DIS – Clock Low Timeout Disable
0 = Clock Low Timeout Enabled (Default)
1 = Clock Low Timeout Disabled
Bit 19: IBIAS_B_EN – PMBus Current Source B Control – This bit is only valid on PMBusRegs. The second interface, PMBusRegs1, is not connected to the ADC
0 = Disables Current Source for PMBUS address detection thru ADC (Default)
1 = Enables Current Source for PMBUS address detection thru ADC
Bit 18: IBIAS_A_EN – PMBus Current Source A Control – see note above for IBIAS_B_EN
0 = Disables Current Source for PMBUS address detection thru ADC (Default)
1 = Enables Current Source for PMBUS address detection thru ADC
Bit 17: SCL_DIR – Configures direction of PMBus clock pin in GPIO mode
0 = PMBus clock pin configured as output (Default)
1 = PMBus clock pin configured as input
Bit 16: SCL_VALUE – Configures output value of PMBus clock pin in GPIO Mode
0 = PMBus clock pin driven low in GPIO Mode (Default)
1 = PMBus clock pin driven high in GPIO Mode
Bit 15: SCL_MODE – Configures mode of PMBus Clock pin
0 = PMBus clock pin configured in functional mode (Default)
1 = PMBus clock pin configured as GPIO
Bit 14: SDA_DIR – Configures direction of PMBus data pin in GPIO mode
0 = PMBus data pin configured as output (Default)
1 = PMBus data pin configured as input
Bit 13: SDA_VALUE – Configures output value of PMBus data pin in GPIO Mode
0 = PMBus data pin driven low in GPIO Mode (Default)
1 = PMBus data pin driven high in GPIO Mode
Bit 12: SDA_MODE – Configures mode of PMBus Data pin
0 = PMBus data pin configured in functional mode (Default)
1 = PMBus data pin configured as GPIO
Bit 11: CNTL_DIR – Configures direction of Control pin in GPIO mode – this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Control pin configured as output (Default)
1 = Control pin configured as input
Bit 10: CNTL_VALUE – Configures output value of Control pin in GPIO Mode– this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Control pin driven low in GPIO Mode (Default)
1 = Control pin driven high in GPIO Mode
Bit 9: CNTL_MODE – Configures mode of Control pin– this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Control pin configured in functional mode (Default)
1 = Control pin configured as GPIO
Bit 8: ALERT_DIR – Configures direction of Alert pin in GPIO mode– this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Control pin configured as output (Default)
1 = Control pin configured as input
Bit 7: ALERT_VALUE – Configures output value of Alert pin in GPIO Mode– this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Alert pin driven low in GPIO Mode (Default)
1 = Alert pin driven high in GPIO Mode
Bit 6: ALERT_MODE – Configures mode of Alert pin– this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin

0 = Alert pin configured in functional mode (Default)
1 = Aler3 pin configured as GPIO

Bit 5: CNTL_INT_EDGE – Control Interrupt Edge Select– this is only valid on PMBusRegs, not on PMBus1Regs, because only PMBusRegs is connected to the device pin
0 = Interrupt generated on falling edge of Control (Default)
1 = Interrupt generated on rising edge of Control

Bit 3: FAST_MODE – Fast Mode Enable
0 = Standard 100 KHz mode enabled (Default)
1 = Fast Mode enabled (400KHz operation on PMBus)

Bit 2: BUS_LO_INT_EDGE – Clock Low Timeout Interrupt Edge Select
0 = Interrupt generated on rising edge of clock low timeout (Default)
1 = Interrupt generated on falling edge of clock low timeout

Bit 1: ALERT_EN – Slave Alert Enable
0 = PMBus Alert is not driven by slave, pulled up high on PMBus (Default)
1 = PMBus Alert driven low by slave

Bit 0: RESET – PMBus Interface Synchronous Reset
0 = No reset of internal state machines (Default)
1 = Control state machines are reset to initial states

21.13 *GIO – General Purpose Input/Output Module*

GIO Registers have the following attributes:

- Addresses placed on word boundaries
- Byte, Half-word and Word Writes are permitted
- All Registers can be read in any mode
- All Registers are writeable

21.13.1 Fault IO Direction Register (FAULTDIR)

Address FFF7FA00

Bit Number	7	6	5	4
Bit Name	GIO_D_DIR	GIO_C_DIR	GIO_B_DIR	GIO_A_DIR
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_DIR	FLT2_DIR	FLT1_DIR	FLT0_DIR
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 7: GIO_D_DIR – GIO_D Pin Configuration
0 = GIO_D pin configured as an input pin in GPIO mode (Default)
1 = GIO_D pin configured as an output pin in GPIO mode
Bit 6: GIO_C_DIR – GIO_C Pin Configuration
0 = GIO_C pin configured as an input pin in GPIO mode (Default)
1 = GIO_C pin configured as an output pin in GPIO mode
Bit 5: GIO_B_DIR – GIO_B Pin Configuration
0 = GIO_B pin configured as an input pin in GPIO mode (Default)
1 = GIO_B pin configured as an output pin in GPIO mode
Bit 4: GIO_A_DIR – GIO_A Pin Configuration
0 = GIO_A pin configured as an input pin in GPIO mode (Default)
1 = GIO_A pin configured as an output pin in GPIO mode
Bit 3: FLT3_DIR – FAULT[3] Pin Configuration
0 = FAULT[3] pin configured as an input pin (Default)
1 = FAULT[3] pin configured as an output pin
Bit 2: FLT2_DIR – FAULT[2] Pin Configuration
0 = FAULT[2] pin configured as an input pin (Default)
1 = FAULT[2] pin configured as an output pin
Bit 1: FLT1_DIR – FAULT[1] Pin Configuration
0 = FAULT[1] pin configured as an input pin (Default)
1 = FAULT[1] pin configured as an output pin
Bit 0: FLT0_DIR – FAULT[0] Pin Configuration
0 = FAULT[0] pin configured as an input pin (Default)
1 = FAULT[0] pin configured as an output pin

21.13.2 Fault Input Register (FAULTIN)

Address FFF7FA04

Bit Number	7	6	5	4
Bit Name	GIO_D_IN	GIO_C_IN	GIO_B_IN	GIO_A_IN
Access	R	R	R	R
Default	-	-	-	-

Bit Number	3	2	1	0
Bit Name	FLT3_IN	FLT2_IN	FLT1_IN	FLT0_IN
Access	R	R	R	R
Default	-	-	-	-

Bit 7: GIO_D_IN – Input Value of GIO_D Pin
0 = GIO_D pin driven low in GPIO mode
1 = GIO_D pin driven high in GPIO mode
Bit 6: GIO_C_IN – Input Value of GIO_C Pin
0 = GIO_C pin driven low in GPIO mode
1 = GIO_C pin driven high in GPIO mode
Bit 5: GIO_B_IN – Input Value of GIO_B Pin
0 = GIO_B pin driven low in GPIO mode
1 = GIO_B pin driven high in GPIO mode
Bit 4: GIO_A_IN – Input Value of GIO_A Pin
0 = GIO_A pin driven low in GPIO mode
1 = GIO_A pin driven high in GPIO mode
Bit 3: FLT3_IN – Input Value of FAULT[3] Pin
0 = FAULT[3] pin driven low
1 = FAULT[3] pin driven high
Bit 2: FLT2_IN – Input Value of FAULT[2] Pin
0 = FAULT[2] pin driven low
1 = FAULT[2] pin driven high
Bit 1: FLT1_IN – Input Value of FAULT[1] Pin
0 = FAULT[1] pin driven low
1 = FAULT[1] pin driven high
Bit 0: FLT0_IN – Input Value of FAULT[0] Pin
0 = FAULT[0] pin driven low
1 = FAULT[0] pin driven high

21.13.3 Fault Output Register (FAULTOUT)

Address FFF7FA08

Bit Number	7	6	5	4
Bit Name	GIO_D_OUT	GIO_C_OUT	GIO_B_OUT	GIO_A_OUT
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_OUT	FLT2_OUT	FLT1_OUT	FLT0_OUT
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 7: GIO_D_OUT – GIO_D Pin Output Value
0 = GIO_D pin driven low when configured as output in GPIO mode (Default)
1 = GIO_D pin driven high when configured as output in GPIO mode
Bit 6: GIO_C_OUT – GIO_C Pin Output Value
0 = GIO_C pin driven low when configured as output in GPIO mode (Default)
1 = GIO_C pin driven high when configured as output in GPIO mode
Bit 5: GIO_B_OUT – GIO_B Pin Output Value
0 = GIO_B pin driven low when configured as output in GPIO mode (Default)
1 = GIO_B pin driven high when configured as output in GPIO mode
Bit 4: GIO_A_OUT – GIO_A Pin Output Value
0 = GIO_A pin driven low when configured as output in GPIO mode (Default)
1 = GIO_A pin driven high when configured as output in GPIO mode
Bit 3: FLT3_OUT – FAULT[3] Pin Output Value
0 = FAULT[3] pin driven low when configured as output (Default)
1 = FAULT[3] pin driven high when configured as output
Bit 2: FLT2_OUT – FAULT[2] Pin Output Value
0 = FAULT[2] pin driven low when configured as output (Default)
1 = FAULT[2] pin driven high when configured as output
Bit 1: FLT1_OUT – FAULT[1] Pin Output Value
0 = FAULT[1] pin driven low when configured as output (Default)
1 = FAULT[1] pin driven high when configured as output
Bit 0: FLT0_OUT – FAULT[0] Pin Output Value
0 = FAULT[0] pin driven low when configured as output (Default)
1 = FAULT[0] pin driven high when configured as output

21.13.4 Fault Interrupt Enable Register (FAULTINTENA)

Address FFF7FA14

Bit Number	7	6	5	4
Bit Name	GIO_D_INT_EN	GIO_C_INT_EN	GIO_B_INT_EN	GIO_A_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_INT_EN	FLT2_INT_EN	FLT1_INT_EN	FLT0_INT_EN
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 7: GIO_D_INT_EN – GIO_D Interrupt Enable
0 = Interrupt disabled for GIO_D pin (Default)
1 = Interrupt enabled for GIO_D pin in GPIO mode
Bit 6: GIO_C_INT_EN – GIO_C Interrupt Enable
0 = Interrupt disabled for GIO_C pin (Default)
1 = Interrupt enabled for GIO_C pin in GPIO mode
Bit 5: GIO_B_INT_EN – GIO_B Interrupt Enable
0 = Interrupt disabled for GIO_B pin (Default)
1 = Interrupt enabled for GIO_B pin in GPIO mode
Bit 4: GIO_A _INT_EN – GIO_A Interrupt Enable
0 = Interrupt disabled for GIO_A pin (Default)
1 = Interrupt enabled for GIO_A pin in GPIO mode
Bit 3: FLT3_INT_EN – FAULT[3] Interrupt Enable
0 = Interrupt disabled for FAULT[3] pin (Default)
1 = Interrupt enabled for FAULT[3] pin
Bit 2: FLT2_INT_EN – FAULT[2] Interrupt Enable
0 = Interrupt disabled for FAULT[2] pin (Default)
1 = Interrupt enabled for FAULT[2] pin
Bit 1: FLT1_INT_EN – FAULT[1] Interrupt Enable
0 = Interrupt disabled for FAULT[1] pin (Default)
1 = Interrupt enabled for FAULT[1] pin
Bit 0: FLT0_INT_EN – FAULT[0] Interrupt Enable
0 = Interrupt disabled for FAULT[0] pin (Default)
1 = Interrupt enabled for FAULT[0] pin

21.13.5 Fault Interrupt Polarity Register (FAULTINTPOL)

Address FFF7FA18

Bit Number	7	6	5	4
Bit Name	GIO_D_INT_POL	GIO_C_INT_POL	GIO_B_INT_POL	GIO_A_INT_POL
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_INT_POL	FLT2_INT_POL	FLT1_INT_POL	FLT0_INT_POL
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 7: GIO_D_INT_POL – GIO_D Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 6: GIO_C_INT_POL – GIO_C Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 5: GIO_B_INT_POL – GIO_B Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 4: GIO_A_INT_POL – GIO_A Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 3: FLT3_INT_POL – FAULT[3] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 2: FLT2_INT_POL – FAULT[2] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 1: FLT1_INT_POL – FAULT[1] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge
Bit 0: FLT0_INT_POL – FAULT[0] Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge

21.13.6 Fault Interrupt Pending Register (FAULTINTPEND)

Address FFF7FA1C

Bit Number	7	6	5	4
Bit Name	GIO_D_INT_PEND	GIO_C_INT_PEND	GIO_B_INT_PEND	GIO_A_INT_PEND
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit Number	3	2	1	0
Bit Name	FLT3_INT_PEND	FLT2_INT_PEND	FLT1_INT_PEND	FLT0_INT_PEND
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 7: GIO_D_INT_PEND – GIO_D has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 6: GIO_C_INT_PEND – GIO_C has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 5: GIO_B_INT_PEND – GIO_B has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 4: GIO_A_INT_PEND – GIO_A has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 3: FLT3_INT_PEND – FAULT[3] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 2: FLT2_INT_PEND – FAULT[2] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 1: FLT1_INT_PEND – FAULT[1] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

Bit 0: FLT0_INT_PEND – FAULT[0] has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag
0 = No Interrupt detected (Default)
1 = Interrupt pending

21.13.7 External Interrupt Direction Register (EXTINTDIR)

Address FFF7FA20

Bit Number	0
Bit Name	EXT_INT_DIR
Access	R/W
Default	0

Bit 0: EXT_INT_DIR – EXT-INT Pin Configuration
0 = EXT-INT pin configured as an input pin (Default)
1 = EXT-INT pin configured as an output pin

21.13.8 External Interrupt Input Register (EXTINTIN)

Address FFF7FA24

Bit Number	0
Bit Name	EXT_INT_IN
Access	R
Default	-

Bit 0: EXT_INT_IN – Input Value of EXT-INT Pin
0 = EXT-INT pin driven low in GPIO mode
1 = EXT-INT pin driven high in GPIO mode

21.13.9 External Interrupt Output Register (EXTINTOUT)

Address FFF7FA28

Bit Number	0
Bit Name	EXT_INT_OUT
Access	R/W
Default	0

Bit 0: EXT_INT_OUT – EXT-INT Pin Output Value
0 = EXT-INT pin driven low (Default)
1 = EXT-INT pin driven high

21.13.10 External Interrupt Enable Register (EXTINTENA)

Address FFF7FA34

Bit Number	0
Bit Name	EXT_INT_EN
Access	R/W
Default	0

Bit 0: EXT_INT_EN – EXT-INT Interrupt Enable
0 = Interrupt disabled for EXT-INT pin (Default)
1 = Interrupt enabled for EXT-INT pin

21.13.11 External Interrupt Polarity Register (EXTTINTPOL)

Address FFF7FA38

Bit Number	0
Bit Name	EXT_INT_POL
Access	R/W
Default	0

Bit 0: EXT_INT_POL – EXT-INT Interrupt Polarity Select
0 = Interrupt generated on falling edge (Default)
1 = Interrupt generated on rising edge

21.13.12 External Interrupt Pending Register (EXTINTPEND)

Address FFF7FA3C

Bit Number	0
Bit Name	EXT_INT_PEND
Access	R/W
Default	0

Bit 0: EXT_INT_PEND – EXT-INT has caused an interrupt. Writing a 1 to a bit will clear the interrupt flag.

21.14 *Timer Module*

Timer Registers have the following attributes:

- 32-bit wide
- Addresses placed on word boundaries
- Byte, Half-Word and word writes permitted
- All Registers can be read in any mode
- All Registers, except for the Timer Powerdown Control Register, are writeable in any mode. The Timer Powerdown Control Register is writeable only in privilege mode.

21.14.1 24-bit Counter Data Register (T24CNTDAT)

Address FFF7FD00

Bit Number	23:0
Bit Name	CNT_DAT
Access	R
Default	-

Bits 23-0: CNT_DAT: – Contains the 24-bit counter value

21.14.2 24-bit Counter Control Register (T24CNTCTRL)

Address FFF7FD04

Bit Number	15:8	7:3	2	1	0
Bit Name	PRESCALE	RESERVED	EXT_CLK_SEL	OV_INT_ENA	OV_FLAG
Access	R/W	-	R/W	R/W	R
Default	0000_0000	00000	0	0	0

Bits 15-8: PRESCALE – Defines the prescaler value used to select the 24-bit counter resolution. The minimum divider ratio is 4, prescaler value less than 3 defaults to 3.

Counter Resolution = (Prescaler Value+1)*1/ICLK

Bits 7-3: RESERVED – Unused bits

Bit 2: EXT_CLK_SEL – External Clock Select

0 = Selects ICLK as clock for 24-bit counter (Default)

1 = Selects External Clock on FAULT-0 as clock for 24-bit counter

Bit 1: OV_INT_ENA – Counter Overflow Interrupt Enable

0 = Disables 24-bit Counter Overflow Interrupt (Default)

1 = Enables 24-bit Counter Overflow Interrupt

Bit 0: OV_FLAG – Indicates a counter overflow. Overflow event is cleared by writing a '1' to this bit. If a clear and an overflow event occur at the same time, the flag will remain high (set has priority versus clear).

0 = No counter overflow since last clear

1 = Counter overflow since last clear

21.14.3 24-bit Capture Channel Data Register x(T24CAPDATx)

Address FFF7FD08 – 24-bit Capture Data Register 0
Address FFF7FD0C – 24-bit Capture Data Register 1

Bit Number	23:0
Bit Name	CAP_DAT
Access	R
Default	-

Bits 23-0: CAP_DAT– Contains the 24-bit input capture value

21.14.4 24-bit Capture Channel Control Register x(T24CAPCTRLx)

Address FFF7FD14 – 24-bit Capture Channel Control Register 0
Address FFF7FD18 – 24-bit Capture Channel Control Register 1

Bit Number	5:4	3:2	1	0
Bit Name	CAP_SEL	EDGE	CAP_INT_ENA	CAP_INT_FLAG
Access	R/W	R/W	R/W	R/W
Default	00	00	0	0

Bits 5-4: CAP_SEL – Capture Pin Select
00 = TCAP-A pin (Default)
01 = SCI_RX[0] pin
10 = SCI_RX[1] pin
11 = SYNC pin
Bits 3-2: EDGE – Input Capture Edge Select
00 = No Capture (Default)
01 = Rising Edge
10 = Falling Edge
11 = Both Edges
Bit 1: CAP_INT_ENA – Input Capture Interrupt Enable
0 = Disables 24-bit input capture interrupt (Default)
1 = Enables 24-bit input capture interrupt
Bit 0: CAP_INT_FLAG – Flag which indicates a valid input capture event. This bit is cleared by writing a '1' to it or by reading the corresponding Capture Channel Data Register. If a clear and a valid capture event occur at the same time, the flag will remain high (set has priority versus clear).
0 = No valid capture event since last clear
1 = Valid capture event since last clear

21.14.5 24-bit Capture I/O Control and Data Register (T24CAPIO)

Address FFF7FD20

Bit Number	5	4	3	2	1	0
Bit Name	TCAP_1_IN	TCAP_1_OUT	TCAP_1_DIR	TCAP_0_IN	TCAP_0_OUT	TCAP_0_DIR
Access	R	R/W	R/W	R	R/W	R/W
Default	-	0	0	-	0	0

Bit 5: TCAP_1_IN – Input data for pin TCAP_1/TDI/TDO pin, when connected to chip I/O
0 = Logic level low detected on TCAP pin
1 = Logic level high detected on TCAP pin
Bit 4: TCAP_1_OUT – Output data for pin TCAP_1 pin, when connected to chip I/O
0 = Logic level low driven on TCAP_1 pin in output mode (Default)
1 = Logic level high driven on TCAP_1 pin in output mode

Bit 3: TCAP_1_DIR – Controls data direction for pin TCAP, when connected to chip I/O
0 = TCAP_1 pin configured as input (Default)
1 = TCAP_1 pin configured as output
Bit 2: TCAP_0_IN – Input data for pin TCAP_0/TDI/TDO pin, when connected to chip I/O
0 = Logic level low detected on TCAP pin
1 = Logic level high detected on TCAP pin
Bit 1: TCAP_0_OUT – Output data for pin TCAP_0 pin, when connected to chip I/O
0 = Logic level low driven on TCAP_0 pin in output mode (Default)
1 = Logic level high driven on TCAP_0 pin in output mode
Bit 0: TCAP_0_DIR – Controls data direction for pin TCAP_0, when connected to chip I/O
0 = TCAP_0 pin configured as input (Default)
1 = TCAP_0 pin configured as output

21.14.6 24-bit Output Compare Channel 0 Data Register (T24CMPDAT0)

Address FFF7FD24

Bit Number	23:0
Bit Name	CMP_DAT
Access	R/W
Default	0000_0000_0000_0000_0000_0000

Bits 23-0: CMP_DAT– Contains the 24-bit output comparison value

21.14.7 24-bit Output Compare Channel 1 Data Register (T24CMPDAT1)

Address FFF7FD28

Bit Number	23:0
Bit Name	CMP_DAT
Access	R/W
Default	0000_0000_0000_0000_0000_0000

Bits 23-0: CMP_DAT– Contains the 24-bit output comparison value

21.14.8 24-bit Output Compare Channel 0 Control Register (T24CMPCTRL0)

Address FFF7FD2C

Bit Number	1	0
Bit Name	CMP_INT_ENA	CMP_INT_FLAG
Access	R/W	R/W
Default	0	0

Bit 1: CMP_INT_ENA– Output Compare Channel Interrupt
0 = Disables Output Compare Channel Interrupt (Default)
1 = Enables Output Compare Channel Interrupt
Bit 0: CMP_INT_FLAG – Indicates a valid output compare event. Bit can be cleared by writing a '1' to the bit or by rewriting the 24-bit Output Compare Channel Data Register. If a clear and compare event occur at the same time, the flag will remain high (set has priority versus clear).
0 = No compare event since last clear
1 = Compare event since last clear

21.14.9 24-bit Output Compare Channel 1 Control Register (T24CMPCTRL1)

Address FFF7FD30

Bit Number	1	0
Bit Name	CMP_INT_ENA	CMP_INT_FLAG
Access	R/W	R/W
Default	0	0

Bit 1: CMP_INT_ENA– Output Compare Channel Interrupt
0 = Disables Output Compare Channel Interrupt (Default)
1 = Enables Output Compare Channel Interrupt

Bit 0: CMP_INT_FLAG – Indicates a valid output compare event. Bit can be cleared by writing a '1' to the bit or by rewriting the 24-bit Output Compare Channel Data Register. If a clear and compare event occur at the same time, the flag will remain high (set has priority versus clear).
0 = No compare event since last clear
1 = Compare event since last clear

21.14.10 PWMx Counter Data Register (T16PWMxCNTDAT)

Address FFF7FD34 – 16-bit PWM0 Counter Data Register
Address FFF7FD58 – 16-bit PWM1 Counter Data Register
Address FFF7FD6C – 16-bit PWM2 Counter Data Register
Address FFF7FD80 – 16-bit PWM3 Counter Data Register

Bit Number	15:0
Bit Name	CNT_DAT
Access	R
Default	-

Bits 15-0: CNT_DAT – Contains the 16-bit counter value. Read-only.

21.14.11 PWMx Counter Control Register (T16PWMxCNTCTRL)

Address FFF7FD38 – 16-bit PWM0 Counter Control Register
Address FFF7FD5C – 16-bit PWM1 Counter Control Register
Address FFF7FD70 – 16-bit PWM2 Counter Control Register
Address FFF7FD84 – 16-bit PWM3 Counter Control Register

Bit Number	15:8	7	6:5	4
Bit Name	PRESCALE	RESERVED	SYNC_SEL	SYNC_EN
Access	R/W	-	R/W	R/W
Default	0000_0000	0	00	0

Bit Number	3	2	1	0
Bit Name	SW_RESET	CMP_RESET_ENA	OV_INT_ENA	OV_INT_FLAG
Access	R/W	R/W	R/W	R/W
Default	0	0	0	0

Bit 15-8: PRESCALE – Defines the prescaler value to select the PWM counter resolution.
Counter Resolution = (Prescaler + 1) *1/ICLK
Bit 7: RESERVED – Unused bit
Bits 6:5: SYNC_SEL – Configures master PWM counter
0 = PWM0 Counter (Default)
1 = PWM1 Counter
2 = PWM2 Counter
3 = PWM3 Counter
Bit 4: SYNC_EN – PWM counter starts when master PWM counter is enabled
0 = PWM counter independent of other PWM counters (Default)
1 = PWM counter controlled by Master PWM counter
Bit 3: SW_RESET– PWM counter reset by software. This bit is cleared after reset and has to be set to run the PWM counter.
0 = PWM counter reset and counter stop (Default)
1 = PWM counter is running
Bit 2: CMP_RESET_ENA – Enables PWM counter reset by compare action of T16CMPxDR.
0 = Disable PWM counter reset by compare action (Default)
1 = Enable PWM counter reset by compare action
Bit 1: OV_INT_ENA– PWM Counter Overflow Interrupt Enable
0 = Disable PWM counter overflow interrupt (Default)
1 = Enable PWM counter overflow interrupt
Bit 0: OV_INT_FLAG – Flag which indicates a PWM counter overflow. This bit is cleared by writing '1' to it. If a clear and an overflow event occur at the same time, the flag will remain high (set has priority versus clear).
0 = No PWM counter overflow since last clear
1 = PWM counter overflow since last clear

21.14.12 PWMx 16-bit Compare Channel 0-1 Data Register (T16PWMxCMPyDAT)

Address FFF7FD3C – 16-bit PWM0 Compare Channel 0 Data Register
Address FFF7FD40 – 16-bit PWM0 Compare Channel 1 Data Register
Address FFF7FD60 – 16-bit PWM1 Compare Channel 0 Data Register
Address FFF7FD64 – 16-bit PWM1 Compare Channel 1 Data Register
Address FFF7FD74 – 16-bit PWM2 Compare Channel 0 Data Register
Address FFF7FD78 – 16-bit PWM2 Compare Channel 1 Data Register
Address FFF7FD88 – 16-bit PWM3 Compare Channel 0 Data Register
Address FFF7FD8C – 16-bit PWM3 Compare Channel 1 Data Register

Bit Number	15:0
Bit Name	CMP_DAT
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: CMP_DAT – Contains the 16-bit compare value. When in PWM mode, the value in the T16PWMxCMPyDAT is loaded after a match with the PWMx Counter Data Register. When in OC mode, it has to be written by the CPU. The mode is controlled by the bit SHADOW in the PWMx/Dual Compare Control Register. If both Registers T16PWMxCMP0DAT and T16PWMxCMP1DAT contain the same value, the interrupt and pin behavior is controlled by output compare channel 0 (T16PWMxCMP0DAT has priority over T16PWMxCMP1DAT).

21.14.13 PWM Compare Control Register (T16PWMxCMPCTRL)

Address FFF7FD44 – 16-bit PWM0 Compare Control Register
Address FFF7FD68 – 16-bit PWM1 Compare Control Register
Address FFF7FD7C – 16-bit PWM2 Compare Control Register
Address FFF7FD90 – 16-bit PWM3 Compare Control Register

Bit Number	12	11	10	9	8
Bit Name	SHADOW	PWM_IN	PWM_OUT	PWM_OUT_ENA	PWM_OUT_DRV
Access	R/W	R	R/W	R/W	R/W
Default	0	-	0	0	0

Bit Number	7:6	5:4	3
Bit Name	PWM_OUT_ACTION1	PWM_OUT_ACTION0	CMP1_INT_ENA
Access	R/W	R/W	R/W
Default	00	00	0

Bit Number	2	1	0
Bit Name	CMP1_INT_FLAG	CMP0_INT_ENA	CMP0_INT_FLAG
Access	R/W	R/W	R/W
Default	0	0	0

Bit 12: SHADOW – Controls the update of the 16-bit output compare Registers.
0 = PWM output compare Registers immediately written (Default)
1 = PWM output compare Registers updated through the buffers T16PWMxCMPyDAT after a match occurs in the corresponding Register T16PWMxCMPyDAT.

Bit 11: PWM_IN – Input value of PWM pin when configured in PWM mode
0 = Logic level low detected on PWM pin
1 = Logic level high detected on PWM pin

Bit 10: PWM_OUT – Data to be written into the output latch when PWM_OUT_DRV is high.
0 = Output latch is cleared when PWM_OUT_DRV=1 (Default)
1 = Output latch is set when PWM_OUT_DRV=1

Bit 9: PWM_OUT_ENA – FAN-PWM pin configuration
0 = FAN-PWM configured as an input pin (Default)
1 = FAN-PWM configured as an output pin

Bit 8: PWM_OUT_DRV – Causes the value of the bit PWM_OUT to be written into the output latch. So it is possible to preload the output latch or to use the pin as GPIO. The compare action has priority before the preload function. This bit is always read as '0'.
0 = Output latch not affected by the value of PWM_OUT (Default)
1 = Value of OUT written into the output latch

Bits 7-6: PWM_OUT_ACTION1 – These 2 bits select the output action when a compare equal is detected on T16CMP1DAT
00 = No action (Default)
01 = Set pin
10 = Clear pin
11 = Toggle pin

Bits 5-4: PWM_OUT_ACTION0 – Selects the output action when a compare equal is detected on T16CMP0DAT.
00 = No action (Default)
01 = Set pin
10 = Clear pin
11 = Toggle pin

Bit 3: CMP1_INT_ENA– Compare 1 Interrupt Enable
0 = Disables Compare 1 Interrupt (Default)
1 = Enables Compare 1 Interrupt
Bit 2: CMP1_INT_FLAG – Flag which indicates a valid output compare 1 event. This bit is cleared by writing '1' to this bit or by rewriting T16PWMxCMP1DAT. If a clear and a compare event occurs at the same time, the flag will remain high (set has priority versus write clear).
0 = No compare event since last clear
1 = Compare event since last clear
Bit 1: CMP0_INT_ENA – Compare 0 Interrupt Enable
0 = Disables Compare 0 Interrupt (Default)
1 = Enables Compare 0 Interrupt
Bit 0: CMP0_INT_FLAG – Flag which indicates a valid output compare 1 event. This bit is cleared by writing '1' to this bit or by rewriting T16PWMxCMP0DAT. If a clear and a compare event occurs at the same time, the flag will remain high (set has priority versus write clear).
0 = No compare event since last clear
1 = Compare event since last clear

21.14.14 Watchdog Status (WDST)

Address FFF7FD94

Bit Number	3	2	1	0
Bit Name	WAKE_EV_RAW	WD_EV_RAW	WAKE_EV_INT	WD_EV_INT
Access	R	R	R	R
Default	-	-	-	-

Bit 3: WAKE_EV_RAW – Watchdog Wake Event Raw Status
0 = Watchdog Timer has not reached ½ of terminal count
1 = Watchdog Timer has reached ½ of terminal count
Bit 2: WD_EV_RAW – Watchdog Event Raw Status
0 = Watchdog Timer has not reached terminal count
1 = Watchdog Timer has reached terminal count
Bit 1: WAKE_EV_INT – Watchdog Wake Event Interrupt Status, cleared on read of Watchdog Status Register
0 = Watchdog Timer has not reached ½ of terminal count
1 = Watchdog Timer has reached ½ of terminal count
Bit 0: WD_EV_INT – Watchdog Event Interrupt Status, cleared on read of Watchdog Status Register
0 = Watchdog Timer has not reached terminal count
1 = Watchdog Timer has reached terminal count

21.14.15 Watchdog Control (WDCTRL)

Address FFF7FD98

Bit Number	14:8	7	6	5	4
Bit Name	WD_PERIOD	RESERVED	PROTECT	CPU_RESET_EN	WDRST_INT_EN
Access	R/W	-	R/W	R/W	R/W
Default	111_1111	0	1	0	0

Bit Number	3	2	1	0
Bit Name	WKEV_INT_EN	WKEV_EN	WDRST_EN	CNT_RESET
Access	R/W	R/W	R/W	R/W
Default	0	0	0	1

Bits 14-8: WD_PERIOD - Configures the time for the watchdog reset.
H'7F ~ 1.3s (minimum) (Default)
H'00 ~ 10ms (maximum)
Bit 7: RESERVED – Unused bits
Bit 6: PROTECT – Watchdog Protect Bit, Active Low
0 = Watchdog enable bits are protected, only can be cleared by POR. CPU_RESET_ENA (Bit 5), WDRST_ENA (Bit 2) and WKEV_ENA (Bit 1) are automatically set high when PROTECT is written low.
1 = Watchdog enable bits can be set by processor (Default)
Bit 5: CPU_RESET_EN – Enables Watchdog Reset Event to reset the CPU
0 = Watchdog Reset does not reset CPU (Default)
1 = Watchdog Reset does resets CPU
Bit 4: WDRST_INT_EN – Watchdog Reset Event Interrupt Enable
0 = Disables generation of Watchdog Reset Interrupt (Default)
1 = Enables generation of Watchdog Reset Interrupt
Bit 3: WKEN_INT_EN – Watchdog Wake Event Interrupt Enable
0 = Disables generation of Watchdog Wake Event Interrupt (Default)

1 = Enables generation of Watchdog Wake Event Interrupt

Bit 2: WKEV_EN – Watchdog Wake Event Comparator Enable

0 = Disables Watchdog Wake Event Comparator (Default)

1 = Enables Watchdog Wake Event Comparator

Bit 1: WDRST_EN – Watchdog Reset Event Comparator Enable

0 = Disables Watchdog Reset Event Comparator (Default)

1 = Enables Watchdog Reset Event Comparator

Bit 0: CNT_RESET – This bit resets the watchdog counters. This bit self clears and if the enables are set, the counters restart counting.

0 = Watchdog counters enabled (Default)

1 = Watchdog counters reset

21.15 *Memory Controller - MMC*

All MMC control Registers have the following attributes:

- 16-bit wide
- Addresses placed on word boundaries
- 16-bit data is placed on the least significant data bus D[15:0]
- Only half-word writes are permitted
- Registers are readable in any mode, but writeable only in privilege mode

21.15.1 Static Memory Control Register (SMCTRL)

Address FFFFFD00

Bit Number	13:12	11:9	7:4	3	1:0
Bit Name	LEAD	TRAIL	ACTIVE	ENDIAN	WIDTH
Access	R/W	R/W	R/W	R	R/W
Default	00	000	0000	-	00

Bits 13-12: LEAD – Address setup time cycles (write operations)
00 = No setup time required (Default)
01 = Write strobe is delayed one cycle
10 = Write strobe is delayed two cycles
11 = Write strobe is delayed three cycles

Bits 11-9: TRAIL – Number of Trailing wait states. Determine the trailing wait states after read and write operations to the memory associated with the chip select corresponding to the wait states.

Bit s 7-4: ACTIVE – Active Wait states (both read/write operations)
0000 = 0 Wait states (Default)
0001 = 1 Wait states
0010 = 2 Wait states
0011 = 3 Wait states
0100 = 4 Wait states
0101 = 5 Wait states
0110 = 6 Wait states
0111 = 7 Wait states
1000 = 8 Wait states
1001 = 9 Wait states
1010 = 10 Wait states
1011 = 11 Wait states
1100 = 12 Wait states
1101 = 13 Wait states
1110 = 14 Wait states
1111 = 15 Wait states

Bit 3: ENDIAN – Endian Mode Identification
0 = CPU configured in big endian mode
1 = CPU configured in little endian mode

Bits 1-0: WIDTH – Data Width for Memories
00 = 8 bits (Default)
01 = 16 bits
10 = 32 bits
11 = Reserved

21.15.2 Write Control Register (WCTRL)

Address FFFFFD2C

Bit Number	1	0
Bit Name	TRAIL_OVR	WBUF_ENA
Access	R/W	R/W
Default	0	0

Bit 1: TRAIL_OVR – Write trailing wait state override.
0 = At least one trailing wait state (Default)
1 = TRAIL sets trailing wait states
Bit 0: WBUF_ENA – Write buffer enable. When this bit is 1, the memory controller latches the data and control signals in the first cycle for write operations to the memories and peripherals on the expansion bus and lets the CPU perform other operations. However, the CPU starts a wait state if there is another request before the memory controller finishes.
0 = Write buffer disabled (Disabled)
1 = Write buffer enabled

21.15.3 Peripheral Control Register (PCTRL)

Address FFFFFD30

Bit Number	0
Bit Name	PBUF_ENA
Access	R/W
Default	0

Bit 0: PBUF_ENA – Write buffer enable. When this bit is set to 1, the memory controller latches the data and control signals in the first cycle for write operations to the memories and peripherals on the expansion bus and lets the CPU perform other operations. However, the CPU starts a wait state if there is another request before the memory controller finishes.
0 = Write buffer disabled (Default)
1 = Write buffer enabled

21.15.4 Peripheral Location Register (PLOC)

Address FFFFFD34

Bit Number	15:0
Bit Name	LOC
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: LOC – These 16 bits represent the peripheral location bits, which correspond to each of the 16 peripheral selects.
0 = Peripheral is internal (Default)
1 = Peripheral is external

21.15.5 Peripheral Protection Register (PPROT)

Address FFFFFD38

Bit Number	15:0
Bit Name	PROT
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: PROT – These 16 bits represent the peripheral protection bits, which correspond to each of the 16 peripheral selects.

0 = Peripheral is accessible in all modes (Default)

1 = Peripheral is accessible in privilege mode only

21.16 *DEC – Address Manager*

The DEC generates the memory selects and SAR peripheral select signals by decoding the address and control signals from the ARM processor. In addition, the DEC provides the control signals for the Program and Data Flash.

The assigned memory selects for Cyclone are as follows:

Memory Select 0 => Boot ROM (1Kx32)
Memory Select 1 => Program Flash 0(8Kx32)
Memory Select 2 => Data Flash (512x32)
Memory Select 3 => Data RAM (2Kx32)
Memory Select 4 => Loop Mux (1Kx32)
Memory Select 5 => Fault Mux (1Kx32)
Memory Select 6 => ADC12 Control (1Kx32)
Memory Select 7 => DPWM3 (1Kx32)
Memory Select 8 => Filter 2 (1Kx32)
Memory Select 9 => DPWM 2 (1Kx32)
Memory Select 10 => Front End Control 2 (1Kx32)
Memory Select 11 => Filter 1 (1Kx32)
Memory Select 12 => DPWM 1 (1Kx32)
Memory Select 13 => Front End Control 1 (1Kx32)
Memory Select 14 => Filter 0 (1Kx32)
Memory Select 15 => DPWM 0 (1Kx32)
Memory Select 16 => Front End Control 0 (1Kx32)
Memory Select 17 => Program Flash 1(8Kx32)

21.16.1 Memory Fine Base Address High Register 0 (MFBAHR0)

Address FFFFFE00

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.2 Memory Fine Base Address Low Register 0 (MFBALR0)

Address FFFFFE04

Bit Number	15:10	8	7:4	1	0
Bit Name	ADDRESS[15:10]	MS	BLOCK_SIZE	RONLY	PRIV
Access	R/W	R/W	R/W	R/W	R/W
Default	000000	0	0000	0	0

Bits15-10: ADDRESS[15:10] – 6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

Bit 8: MS – Memory Map Select

0 = Memory Map configuration not updated (Default)
1 = Enables the fine and coarse memory selects and activates the memory map

Bits 7-4: BLOCK_SIZE – Configures the size of the memory

0000 = Memory select is disabled (Default)
0001 = 1K Bytes

0010 = 2K Bytes
0011 = 4K Bytes
0100 = 8K Bytes
0101 = 16K Bytes
0110 = 32K Bytes
0111 = 64K Bytes
1000 = 128K Bytes
1001 = 256K Bytes
1010 = 512K Bytes
1011 = 1M Bytes
1100 = 2M Bytes
1101 = 4M Bytes
1110 = 8M Bytes
1111 = 16M Bytes

Bit 1: RONLY – Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory.

0 = Read/write access to memory (Default)
1 = Read accesses to memory only

Bit 0: PRIV – Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode.

0 = User/privilege mode accesses to memory (Default)
1 = Privilege mode accesses to memory only

21.16.3 Memory Fine Base Address High Register 1-3,17-19 (MFBAHRx)

Address FFFFFE08 – Memory Fine Base Address High Register 1
Address FFFFFE10– Memory Fine Base Address High Register 2
Address FFFFFE18 – Memory Fine Base Address High Register 3
Address FFFFFE88 – Memory Fine Base Address High Register 17
Address FFFFFEA8 – Memory Fine Base Address High Register 18 – only on UCD3138128
Address FFFFFEB0 – Memory Fine Base Address High Register 19 – only on UCD3138128

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0000_0000

Note: - The values shown for these bitfields are the reset values. The ROM will load other values into these bitfields to configure the memory map for ROM mode. Some of the bitfields will be changed again when the ROM jumps to FLASH mode.

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.4 Memory Fine Base Address Low Register 1-3,17-19 (MFBALRx)

Address FFFFFE0C – Memory Fine Base Address Low Register 1
Address FFFFFE14 – Memory Fine Base Address Low Register 2
Address FFFFFE1C – Memory Fine Base Address Low Register 3
Address FFFFFE8C – Memory Fine Base Address Low Register 17
Address FFFFFEAC – Memory Fine Base Address Low Register 18 – only on UCD3138128
Address FFFFFEB4 – Memory Fine Base Address Low Register 19 – only on UCD3138128

Bit Number	15:10	9	7:4	1	0
Bit Name	ADDRESS[15:10]	AW	BLOCK_SIZE	RONLY	PRIV
Access	R/W	R/W	R/W	R/W	R/W

Default	0000	0	0000	0	0

Note: - The values shown for these bitfields are the reset values. The ROM will load other values into these bitfields to configure the memory map for ROM mode. Some of the bitfields will be changed again when the ROM jumps to FLASH mode.

Bits 15-10: ADDRESS[15:10] – 6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

Bit 9: AW – Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles.

0 = Write operation is not supplemented with an additional cycle (Default)
1 = Write operation takes an additional cycle

Bits 7-4: BLOCK_SIZE – Configures the size of the memory

0000 = Memory select is disabled (Default)
0001 = 1K Bytes
0010 = 2K Bytes
0011 = 4K Bytes
0100 = 8K Bytes
0101 = 16K Bytes
0110 = 32K Bytes
0111 = 64K Bytes
1000 = 128K Bytes
1001 = 256K Bytes
1010 = 512K Bytes
1011 = 1M Bytes
1100 = 2M Bytes
1101 = 4M Bytes
1110 = 8M Bytes
1111 = 16M Bytes

Bit 1: RONLY – Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory.

0 = Read/write access to memory (Default)
1 = Read accesses to memory only

Bit 0: PRIV – Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode.

0 = User/privilege mode accesses to memory (Default)
1 = Privilege mode accesses to memory only

21.16.5 Memory Fine Base Address High Register 4 (MFBAHR4)

Address FFFFFE20 – Memory Fine Base Address High Register 4

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_0010

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.6 Memory Fine Base Address Low Register 4-16 (MFBALRx)

Address FFFFFE24 – Memory Fine Base Address Low Register 4
Address FFFFFE2C – Memory Fine Base Address Low Register 5
Address FFFFFE34 – Memory Fine Base Address Low Register 6

Address FFFFFE3C – Memory Fine Base Address Low Register 7
Address FFFFFE44 – Memory Fine Base Address Low Register 8
Address FFFFFE4C – Memory Fine Base Address Low Register 9
Address FFFFFE54 – Memory Fine Base Address Low Register 10
Address FFFFFE5C – Memory Fine Base Address Low Register 11
Address FFFFFE64 – Memory Fine Base Address Low Register 12
Address FFFFFE6C – Memory Fine Base Address Low Register 13
Address FFFFFE74 – Memory Fine Base Address Low Register 14
Address FFFFFE7C – Memory Fine Base Address Low Register 15
Address FFFFFE84 – Memory Fine Base Address Low Register 16

Bit Number	15:10	9	8:2	1	0
Bit Name	ADDRESS[15:10]	AW	RESERVED	RONLY	PRIV
Access	R/W	R/W	-	R/W	R/W
Default	000000	0	0_0000_00	0	0

Bits 15-10: ADDRESS[15:10] – 6 Least Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.
Bit 9: AW – Auto-wait-on-write. When this bit is set, any write operation on this memory select takes two system cycles.
0 = Write operation is not supplemented with an additional cycle (Default)
1 = Write operation takes an additional cycle
Bits 8-2: RESERVED – Unused bits
Bit 1: RONLY – Read-only protection. This bit sets read-only protection for the memory selected by the memory select. An illegal access exception is generated when a write is attempted to the memory.
0 = Read/write access to memory (Default)
1 = Read accesses to memory only
Bit 0: PRIV – Privilege mode protection. This bit sets privilege mode protection for the memory Registration selected by the memory select. An illegal access exception is generated on any access to memory protected by privilege mode.
0 = User/privilege mode accesses to memory (Default)
1 = Privilege mode accesses to memory only

21.16.7 Memory Fine Base Address High Register 5 (MFBAHR5)

Address FFFFFE28 – Memory Fine Base Address High Register 5

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_0011

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.8 Memory Fine Base Address High Register 6 (MFBAHR6)

Address FFFFFE30 – Memory Fine Base Address High Register 6

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_0100

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.9 Memory Fine Base Address High Register 7 (MFBAHR7)

Address FFFFFE38 – Memory Fine Base Address High Register 7

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_0101

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.10 Memory Fine Base Address High Register 8 (MFBAHR8)

Address FFFFFE40 – Memory Fine Base Address High Register 8

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_0110

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.11 Memory Fine Base Address High Register 9 (MFBAHR9)

Address FFFFFE48 – Memory Fine Base Address High Register 9

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_0111

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.12 Memory Fine Base Address High Register 10 (MFBAHR10)

Address FFFFFE50 – Memory Fine Base Address High Register 10

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1000

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.13 Memory Fine Base Address High Register 11 (MFBAHR11)

Address FFFFFE58 – Memory Fine Base Address High Register 11

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1001

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.14 Memory Fine Base Address High Register 12 (MFBAHR12)

Address FFFFFE60 – Memory Fine Base Address High Register 12

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1010

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.15 Memory Fine Base Address High Register 13 (MFBAHR13)

Address FFFFFE68 – Memory Fine Base Address High Register 13

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1011

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.16 Memory Fine Base Address High Register 14 (MFBAHR14)

Address FFFFFE70 – Memory Fine Base Address High Register 14

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1100

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.17 Memory Fine Base Address High Register 15 (MFBAHR15)

Address FFFFFE78 – Memory Fine Base Address High Register 15

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1101

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.18 Memory Fine Base Address High Register 16 (MFBAHR16)

Address FFFFFE80 – Memory Fine Base Address High Register 16

Bit Number	15:0
Bit Name	ADDRESS[31:16]
Access	R/W
Default	0000_0000_0001_1110

Bits 15-0: ADDRESS[31:16] – 16 Most Significant Bits of the Base Address. The Base Address sets the 22 most significant bits of the memory address.

21.16.19 Program Flash Control Register 0-3 (PFLASHCTRL_x)

Address FFFFFE90 - PFLASHCTRL_0
Address FFFFFE9C - PFLASHCTRL_1
Address FFFFFEA0 - PFLASHCTRL_2 – only on UCD3138128
Address FFFFFEA4 - PFLASHCTRL_3 – only on UCD3138128

Bit Number	11	10	9	8	7:5	4:0
Bit Name	BUSY	RESERVED	PAGE_ERASE	MASS_ERASE	RESERVED	PAGE_SEL
Access	R	-	R/W	R/W	-	R/W
Default	-	0	0	0	000	00000

Bit 11: BUSY – Program Flash Busy Indicator
0 = Program Flash available for read/write/erase access
1 = Program Flash unavailable for read/write/erase access
Bit 10: INFO_BLOCK_ENA – Program Flash Information Block Enable. Test use only.
0 = Access enabled to main memory block (Default)
1 = Access enabled to information block
Bit 9: PAGE_ERASE – Program Flash Page Erase Enable
0 = No Page Erase initiated on Program Flash (Default)

1 = Page Erase on Program Flash enabled. Page erased is based on PAGE_SEL (Bits 4-0). Interlock Key must be set in Flash Interlock Register (Section 17.21) to initiate Page Erase cycle. This bit is cleared upon completion of Page Erase cycle.

Bit 8: MASS_ERASE – Program Flash Mass Erase Enable
0 = No Mass Erase initiated on Program Flash (Default)
1 = Mass Erase of Program Flash enabled. Interlock Key must be set in Flash Interlock Register (Section 17.21) to initiate Mass Erase cycle. This bit is cleared upon completion of Mass Erase cycle.

Bits 4-0: PAGE_SEL – Selects page to be erased during Page Erase Cycle

21.16.20 Data Flash Control Register (DFLASHCTRL)

Address FFFFFE94

Bit Number	11	10	9	8	7:6	5:0
Bit Name	BUSY	RESERVED	PAGE_ERASE	MASS_ERASE	RESERVED	PAGE_SEL
Access	R	-	R/W	R/W	-	R/W
Default	-	-	0	0	-	000000

Bit 11: BUSY – Data Flash Busy Indicator
0 = Data Flash available for read/write/erase access
1 = Data Flash unavailable for read/write/erase access

Bit 9: PAGE_ERASE – Data Flash Page Erase Enable
0 = No Page Erase initiated on Data Flash (Default)
1 = Page Erase Cycle on Data Flash enabled. Page erased is based on PAGE_SEL (Bits 4-0). This bit is cleared upon completion of Page Erase cycle.

Bit 8: MASS_ERASE – Data Flash Mass Erase Enable
0 = No Mass Erase initiated on Data Flash (Default)
1 = Mass Erase of Data Flash enabled. Bit is cleared upon completion of mass erase.

Bits 5-0: PAGE_SEL – Selects page to be erased during Page Erase Cycle

21.16.21 Flash Interlock Register (FLASHILOCK)

Address FFFFFE98

Bit Number	31:0
Bit Name	INTERLOCK_KEY
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bit 31-0: INTERLOCK_KEY – Flash Interlock Key. Register must be set to: 0x42DC157E prior to every Data Flash write/mass erase/page erase or
0x42DC157E prior to every Program Flash#0 write/mass erase/page erase or
0x6C97D0C5 prior to every Program Flash#1 write/mass erase/page erase or
If the Interlock Key is not set, the write/erase cycle to the Flash will not initiate. This register will clear upon the completion of a write/erase cycle to the Flash modules.

21.17 *CIM – Central Interrupt Module*

CIM Registers have the following attributes:

- 32-bit wide
- Addresses placed on word boundaries
- Byte, half-word and word writes permitted
- All Registers have read/write access in any mode
- Interrupt Mask and FIQ/IRQ Program Control Registers are writeable in privilege mode only. A write in user mode to these Registers causes a peripheral illegal access exception.

21.17.1 IRQ Index Offset Vector Register (IRQIVEC)

Address FFFFFF20

Bit Number	7:0
Bit Name	IRQIVEC
Access	R
Default	-

Bits 7-0: IRQIVEC – Index of the IRQ Pending Interrupt (Cleared upon read)
0 = No interrupt pending
1 = Pending interrupt on Channel 0
2 = Pending interrupt on Channel 1
N = Pending interrupt on Channel N-1, where N <= 31

21.17.2 FIQ Index Offset Vector Register (FIQIVEC)

Address FFFFFF24

Bit Number	7:0
Bit Name	FIQIVEC
Access	R
Default	-

Bits 7-0: FIQIVEC – Index of the FIQ pending interrupt (Cleared upon read)
0 = No interrupt pending
1 = Pending interrupt on Channel 0
2 = Pending interrupt on Channel 1
N = Pending interrupt on Channel N-1, where N <= 31.

21.17.3 FIQ/IRQ Program Control Register (FIRQPR)

Address FFFFFF2C

A 32-bit FIQ/IRQ program control Register (FIRQPR) determines whether a given interrupt request will be FIQ or IRQ type.

Bit Number	31:0
Bit Name	FIRQPR
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 31-0: FIRQPR – These bits determine whether an interrupt request from a peripheral is of type FIQ or IRQ. Each bit corresponds to one request channel. This Register is writeable in privilege mode only.
0 = Interrupt request is of IRQ type (Default)
1 = Interrupt request is of FIQ type

21.17.4 Pending Interrupt Read Location Register (INTREQ)

Address FFFFFF30

Bit Number	31:0
Bit Name	INTREQ
Access	R
Default	-

Bits 31-0: INTREQ – Pending Interrupt Requests
0 = No interrupt has occurred
1 = Interrupt is pending

21.17.5 Interrupt Mask Register (REQMASK)

Address FFFFFF34

Bit Number	31:0
Bit Name	REQMASK
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 31-0: REQMASK – Interrupt Request Mask Select
0 = Interrupt request channel is disabled (Default)
1 = Interrupt request channel is enabled

21.18 *SYS – System Module*

SYS Registers have the following attributes:

- 16-bit wide
- Addresses placed on word boundaries
- Byte, half-word and word writes permitted
- All Registers can be read in any mode of operation.
- Global Control Register is writeable in privilege mode only. All other Registers are writeable in any mode.

21.18.1 Clock Control Register (CLKCNTL)

Address FFFFFFD0

The clock control Register configures the MCLK divider for low power modes and the clock multiplexer which drives the Sync pin when configured to output the CLKOUT signal. CLKCNTRL is accessible in user and privilege mode and supports byte, half-word and word accesses. Any access to this Register takes two SYSCLK cycles.

Bit Number	9:8	7	6:5	4	3	2:0
Bit Name	M_DIV_RATIO	RESERVED	CLKSR	RESERVED	CLKDOUT	RESERVED
Access	-	-	R/W	-	R/W	-
Default	00	0	00	0	0	000

Bits 9-8: M_DIV_RATIO – MCLK (Processor Clock) Divide Ratio
00 = MCLK frequency equals High Frequency Oscillator divided by 8 (Default)
01 = MCLK frequency equals High Frequency Oscillator divided by 16
10 = MCLK frequency equals High Frequency Oscillator divided by 32
11 = MCLK frequency equals High Frequency Oscillator divided by 64

Bit 7: RESERVED

Bit 6-5: CLKSR – These bits control the source/function of CLKOUT
00 = Driven by value in CLKDOUT (Bit 3) (Default)
01 = Driven by the interface clock (ICLK)
10 = Driven by the CPU clock (MCLK)
11 = Driven by the system clock (SYSCLK)

Bit 4: RESERVED – Unused bit

Bit 3: CLKDOUT – This pin represents the output value of CLKOUT
0 = CLKOUT driven to logic low in output mode (Default)
1 = CLKOUT driven to logic high in output mode

Bits 2-0: RESERVED

21.18.2 System Exception Control Register (SYSECR)

Address FFFFFFE0

The system exception control Register contains bits that allow the user to generate a software reset. The OVR bits disable some reset/abort conditions when TRST is high.

Bit Number	15:14	13:3	2	1	0
Bit Name	RESET	RESERVED	PACCOVR	ACCOVR	ILLOVR
Access	R/W	-	R/W	R/W	R/W
Default	01	-	0	0	0

Bits 15-14: RESET – Software Reset Enable. These bits always read as 01
01 = No reset
1X = Global system reset (X = don't care)
X0 = Global system reset (X = don't care)
Bits 13-3: RESERVED
Bit 2: PACCOVR – Peripheral Access Violation Override
0 = Peripheral access violation error causes a reset or abort (Default)
1 = No action taken on a peripheral access violation
Bit 1: ACCOVR – Memory Access Reset Override
0 = Memory access violation error causes a reset or abort (Default)
.
1 = No action taken on an illegal address
Bit 0: ILLOVR – Illegal Address Reset Override
0 = Illegal address causes a reset or abort (Default)
1 = No action taken on an illegal address

21.18.3 System Exception Status Register (SYSESR)

Address FFFFFFE4

The System Exception Status Register contains flags for different reset/abort sources. On power-up, all bits are cleared to 0. When a reset condition is recognized, the appropriate bit in the Register is set and the value of the bit is maintained through the reset. When a new reset condition occurs, the current contents of this Register are not cleared. The contents of this Register are cleared on a power-on reset or by software.

Bit Number	15	14	13	12	11	10
Bit Name	PORRST	CLKRST	WDRST	ILLMODE	ILLADR	ILLACC
Access	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0

Bit Number	9	8	7	6:0
Bit Name	PILLACC	ILLMAP	SWRST	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	000_0000

Bit 15: PORRST – Power-On reset flag. Set when power-on reset is asserted. Reset is asserted as long as power-on-reset is active. Whenever a device is powered, this bit is set.
User and privilege modes (read)
0 = Power-up reset has not occurred since the last clear
1 = Power-up reset has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect
Bit 14: CLKRST – This bit represents the clock fail flag. This bit indicates a clock fault condition

has occurred. After power-on-reset, the CLKRST is reset to 0. Value remains unchanged during other resets.

User and privilege modes (read)
0 = Clock failure has not occurred since the last clear
1 = Clock failure has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 13: WDRST – This bit represents the watchdog reset flag. This bit indicates that the last reset was caused by the watchdog.

User and privilege modes (read)
0 = Watchdog reset has not occurred since the last clear
1 = Watchdog reset has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 12: ILLMODE – This bit represents the illegal mode flag. This bit is set when the mode bits in the program status Register are set to an illegal value.

User and privilege modes (read)
0 = Illegal mode has not occurred since the last clear
1 = Illegal mode has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 11: ILLADR – This bit represents the illegal address access flag. This bit is set when an access to an unimplemented location in the memory map is detected in non-user mode.

User and privilege modes (read)
0 = Illegal address has not occurred since the last clear
1 = Illegal address has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 10: ILLACC – This bit represents the illegal memory access flag. This bit is set when an access to a protected location without permission rights is detected in non-user mode.

User and privilege modes (read)
0 = Illegal memory access has not occurred since the last clear
1 = Illegal memory access has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 9: PILLACC – This bit represents the peripheral illegal access flag. This bit is set when a peripheral access violation is detected in user mode.

User and privilege modes (read)
0 = Illegal peripheral access has not occurred since the last clear
1 = Illegal peripheral access has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 8: ILLMAP – This bit represents the illegal address map flag. This bit is set when the base addresses of one or more memories overlap. Reset occurs when the overlapped registration is accessed.

User and privilege modes (read)
0 = Illegal address mapping has not occurred since the last clear
1 = Illegal address mapping has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0

1 = No effect

Bit 7: SWRST – This bit represents the software reset flag. This bit is set when the last reset is caused by software writing the RESET bits.

User and privilege modes (read)
0 = Software reset has not occurred since the last clear
1 = Software reset has occurred since the last clear
User and privilege modes (write)
0 = Clears the corresponding bit to 0
1 = No effect

Bit 6-0: RESERVED

21.18.4 Abort Exception Status Register (ABRTESR)

Address FFFFFFE8

The Abort Exception Status Register shows the abort cause.

Bit Number	15	14	13	12:0
Bit Name	ADRABT	MEMABT	PACCVIO	RESERVED
Access	R/W	R/W	R/W	-
Default	0	0	0	0_0000_0000_0000

Bit 15: ADRABT – This bit represents the illegal address abort. An illegal address access was detected in user mode. An abort was generated due to an illegal address access from either the MPU or system

User and privilege modes (read)
0 = No illegal address
1 = Abort caused by an illegal address
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 14: MEMABT – This bit represents the memory access abort. This bit indicates an illegal memory access was detected in user mode. An abort was generated due to the illegal memory access from either the MPU or system.

User and privilege modes (read)
0 = No illegal memory access
1 = Abort caused by an illegal memory access
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 13: PACCVIO – This bit represents the peripheral access violation error. This bit indicates a peripheral access violation error was detected during a peripheral Register access in user mode. An abort was generated due to a peripheral access violation.

User and privilege modes (read)
0 = No peripheral access violation
1 = Abort caused by a peripheral access violation
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 12-0: RESERVED – Unused bits

21.18.5 Global Status Register (GLBSTAT)

Address FFFFFFEC

The Global Status Register specifies the module that triggered the illegal address, illegal access, abort or reset. When a new reset condition reset occurs, the current contents of this Register are not cleared. The contents of this Register are cleared on a power-on reset or by software.

Bit Number	7	6	5	4	3:0
Bit Name	SYSADDR	SYSACC	MPUADDR	MPUACC	RESERVED
Access	R/W	R/W	R/W	R/W	-
Default	0	0	0	0	0000

Bit 7: SYSADDR – This bit represents the system illegal address flag. This bit is set when the system detects an illegal address.
User and privilege modes (read)
0 = No system illegal address
1 = Abort or reset caused by a system illegal address
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 6: SYSACC – This bit represents the system illegal access flag. This bit is set when the system detects an illegal access.
User and privilege modes (read)
0 = No system illegal access
1 = Abort or reset caused by a system illegal access
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 5: MPUADDR – This bit represents the MPU illegal address flag. This bit is set when the memory protection unit detects an illegal address.
User and privilege modes (read)
0 = No MPU illegal address
1 = Abort or reset caused by a MPU illegal address
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 4: MPUACC – This bit represents the MPU illegal access flag. This bit is set when the MPU detects an illegal access.
User and privilege modes (read)
0 = No MPU illegal access
1 = Abort or reset caused by a MPU illegal access
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

Bit 3-0: RESERVED

21.18.6 Device Identification Register (DEV)

Address FFFFFFF0

The Device Identification Register contains device specification information that is hard coded during device manufacturing. This register is read-only.

Bit Number	15:0
Bit Name	DEV
Access	R
Default	0000_0100_0100_0111

Bits 15-0: DEV – These bits represent the device identification code.

21.18.7 System Software Interrupt Flag Register (SSIF)

Address FFFFFFF8

The System Software Interrupt Flag Register is set when a software interrupt is triggered. The flag allows the user to poll for a software interrupt.

Bit Number	0
Bit Name	SSIFLAG
Access	R/W
Default	0

Bit 0: SSIFLAG – This bit represents the system software interrupt flag. This bit is set when a correct SSKEY is written to the System Software Interrupt Flag Register. This bit is cleared only by software.

User and privilege modes (read)
0 = No IRQ/FIQ interrupt request has been generated since the last clear
1 = IRQ/FIQ interrupt request has been generated since the last clear
User and privilege modes (write)
0 = Clears bit to 0
1 = No effect

21.18.8 System Software Interrupt Request Register (SSIR)

Address FFFFFFFC

The System Software Interrupt Request Register contains a key sequence that triggers a software interrupt request to the CIM. Also, the Register contains an 8-bit data field.

Bit Number	15:8	7:0
Bit Name	SSKEY	SSDATA
Access	R/W	R/W
Default	0000_0000	0000_0000

Bits 15-8: SSKEY – These bits represent the system software interrupt request key. These write-only bits are executable in both user and privilege modes. A 0x75 written to these bits initiates IRQ/FIQ interrupts. Data in this field is always read as zero.
Bits 7-0: SSDATA – These bits represent the system software interrupt data. The SSDATA bits provide an 8-bit field that can be used for passing messages into the system software interrupt.

22 Converting UCD3138 programs to UCD3138A64

The main issue in converting programs from UCD3138 to UCD3138A64 is the changes in the memory map. There are also a few changes necessary because of the addition of an additional FLASH bank, and the related changes to register names for FLASH control.

22.1 *Change Linker Addresses*

To change the linker addresses, there are three files which need to change:

Cyclone.cmd
Cyclone_headers.cmd
Cyclone_global_variables_defs.c

All the files have the same name, but the contents are different. The simplest thing to do is to move the file to a new directory which contains the new files.

22.2 *Change Header Files Which Define Peripherals*

There are several header files which change. A new set of header files is available from TI. The new versions have the same names. This makes it unnecessary to change all the #include statements in all the source files. Normally the include files are all in a headers folder. Use the headers folder that has UCD3138A64 headers in it, and the program will compile properly.

22.3 *Changes to the Flash Control Registers*

The changes to the flash control registers are described in Section 2.4, 17 Register Changes for Program Flash Blocks . For programs which use the full features of the UCD3138A64, read that section, and look at TI example codes.

For a quick test of a 32K byte or less code, replace DecRegs.PFLASHCTRL with DecRegs.PFLASHCTRL0 wherever it occurs in the code.

22.4 *Set BLANK_PCM_EN for Peak Current Mode*

For Peak Current Mode, the BLANK_PCM_EN bit should be set in the appropriate DPWMCTRL2 registers that provide blanking for PCM.

PCM blanking provides blanking logic in the Front End, rather than in the DPWM. For more information, see the UCD3138064 manual.

22.5 *Update Parm Info/Parm Value Pointers*

The parm info/parm value PMBus commands are used by the GUI. They support memory accesses for the memory debugger and some of the filter design functions. The GUI is designed for a standard set of pointers. There is a list of memory areas. Each memory area has a start pointer and a length. The GUI accesses each memory area by sending the number for the area, and the offset within that area.

There are areas for RAM, DFLASH, PFLASH, one for each fast peripheral, and one for the block of slow peripherals at the end of the memory space. For conversion to the UCD3138A64, it is necessary to move some blocks to new addresses. In addition, the three added flash blocks get their own pointer values.

22.5.1 Changes in pmbus.h

It is necessary to change the parm info/parm value pointers in pmbus.h. The changes are marked in bold, italic, underline, and red:

```
//  Memory limits used by the PARM_INFO and PARM_VALUE commands.
#define RAM_START_ADDRESS  0x0006A000      // Beginning of RAM
#define RAM_END_ADDRESS              0x0006BFFF      // End of RAM
#define RAM_LENGTH                   (RAM_END_ADDRESS - RAM_START_ADDRESS + 1)
```

```
// Allow access to peripherals, but not core ARM regs.
#define REG_START_ADDRESS   0xFFF7E400      // Beginning of Register space
#define REG_END_ADDRESS             0xFFF7fdff      // End of Register space
#define REG_LENGTH                  (REG_END_ADDRESS - REG_START_ADDRESS + 1)

// Allow read-only access to Data Flash
#define DFLASH_START_ADDRESS        0x00069800      // Beginning of DFLASH
#define DFLASH_END_ADDRESS          0x00069FFF      // End of DFLASH
#define DFLASH_LENGTH                       (DFLASH_END_ADDRESS - DFLASH_START_ADDRESS +
1)

// Allow read-only access to Constants in Program Flash
#define PFLASH_0_CONST_START_ADDRESS    0x00000000      // Beginning of PFLASH_0 Constants
#define PFLASH_0_CONST_END_ADDRESS      0x00007FFF      // End of PFLASH Constants
#define PFLASH_0_CONST_LENGTH                   (((unsigned
short)PFLASH_0_CONST_END_ADDRESS) - PFLASH_0_CONST_START_ADDRESS + 1)

// Allow read-only access to Program in Program Flash
#define PFLASH_0_PROG_START_ADDRESS     0x00000000      // Beginning of PFLASH Program
#define PFLASH_0_PROG_END_ADDRESS       0x00007FFF      // End of PFLASH Program
#define PFLASH_0_PROG_LENGTH                (((unsigned short)PFLASH_0_PROG_END_ADDRESS) -
PFLASH_0_PROG_START_ADDRESS + 1)

 //fast peripherals
#define LOOP_MUX_START_ADDRESS  0x00120000
#define LOOP_MUX_LENGTH     0x00000070

#define FAULT_MUX_START_ADDRESS 0x00130000
#define FAULT_MUX_LENGTH    0x00000080

#define ADC_START_ADDRESS   0x00140000
#define ADC_LENGTH          0x00000098

#define DPWM3_START_ADDRESS     0x00150000
#define DPWM3_LENGTH            0x00000090

#define FILTER2_START_ADDRESS   0x00160000
#define FILTER2_LENGTH      0x00000064

#define DPWM2_START_ADDRESS     0x00170000
#define DPWM2_LENGTH            0x00000090

#define FE_CTRL2_START_ADDRESS  0x00180000
#define FE_CTRL2_LENGTH     0x00000044

#define FILTER1_START_ADDRESS   0x00190000
#define FILTER1_LENGTH      0x00000064
```

```
#define DPWM1_START_ADDRESS    0x001a0000
#define DPWM1_LENGTH           0x00000090

#define FE_CTRL1_START_ADDRESS  0x001b0000
#define FE_CTRL1_LENGTH        0x00000044

#define FILTER0_START_ADDRESS   0x001c0000
#define FILTER0_LENGTH         0x00000064

#define DPWM0_START_ADDRESS    0x001d0000
#define DPWM0_LENGTH           0x00000090

#define FE_CTRL0_START_ADDRESS  0x001e0000
#define FE_CTRL0_LENGTH        0x00000044

#define SYSTEM_REGS_START_ADDRESS 0xfffffd00
#define SYSTEM_REGS_LENGTH       0x2d0

// Allow read-only access to Program in Program Flash1
#define PFLASH_1_PROG_START_ADDRESS      0x00008000     // Beginning of PFLASH Program
#define PFLASH_1_PROG_END_ADDRESS        0x0000FFFF     // End of PFLASH Program
#define PFLASH_1_PROG_LENGTH             (((unsigned short)PFLASH_1_PROG_END_ADDRESS) -
PFLASH_1_PROG_START_ADDRESS + 1)

#define NUM_MEMORY_SEGMENTS      20       // 20 memory segments for Cyclone A64
```

22.5.2 Changes in Parm Info/Parm Value File

It is also necessary to add start and length for pflash 1 to the lists in the c file with parm info/parm value in it. These may be in different files in different codes.

```
    SYSTEM_REGS_START_ADDRESS,
    PFLASH_1_PROG_START_ADDRESS};
    SYSTEM_REGS_LENGTH,
    PFLASH_1_PROG_LENGTH };
```

In the same list, change the PFLASH names to PFLASH_0:

```
    PFLASH_0_CONST_START_ADDRESS,
    PFLASH_0_PROG_START_ADDRESS,
    PFLASH_0_CONST_LENGTH,
    PFLASH_0_PROG_LENGTH,
```

Generally the table holding the above will have some conditional compilation based on NUM_MEMORY_SEGMENTS. The if-statements can be removed, and the code which was compiled with NUM_MEMORY_SEGMENTS = 19 should be retained with the PFLASH2 segment added as above. The array sizes for these tables need to be changed from 19, either to 20 or to NUM_MEMORY_SEGMENTS.

```
        const Uint32        parm_mem_start[NUM_MEMORY_SEGMENTS] = {
```

```
const Uint16        parm_mem_length[NUM_MEMORY_SEGMENTS] = {    RAM_LENGTH,
```

22.6 Changes to load.asm

It is also necessary to change load.asm. The stack addresses and the ram address for ram clearing need to be changed to match the new RAM location. For clarity, and if dual processor compilation is desired, it might be good to rename load.asm to load_128.asm.

```
SUP_STACK_TOP       .equ    0x6bffc ;Supervisor mode (SWI stack) starts at top of memory
FIQ_STACK_TOP       .equ    0x6be00 ;allocate 256 bytes to supervisor stack, then do FIQ stack
IRQ_STACK_TOP       .equ    0x6bd00 ;allocate 256 bytes to fiq stack, then start irq stack
USER_STACK_TOP      .equ    0x6bb00 ;Allocate 512 bytes to irq stack, regular stack gets rest, down
to variables

    MOV     A2, #106  ;point at 0x6a000 - start of RAM
```

It is also necessary to change the counter for RAM clearing, because there are twice as many bytes of Ram in the UCD3138A64:

Instead of this:

```
MOV     A1, #255    ;loop counter
LSL     A1, A1, #2  ;almost all words cleared 1020 of 1024
```

Use this:

```
MOV     A1, #1      ;loop counter
LSL     A1, A1, #11 ;set to 2** 11 = 2048 words = 8192 bytes - all of RAM
```

Also in load.asm, it is probably necessary to comment out or change these lines:

```
;           LDR         r4,c_mfbalr1_half0 ;point r4 at program flash base address register
;           MOV         r0,#0x62 ;make block size 32K, address 0, read only
;           STRH        r0,[r4]; store it there
```

Commenting them out will work. Their main function is to make the program flash read only. This isn't as important as it was on the original UCD30xx devices because the FLASH key now also protects the program flash from writes. Executing the statements above is problematic because it is possible that the device is set up to have block2 in the address 0 position instead of block 0. This would occur in a multi-image system.

22.7 Changes to system_defines.h

Change data flash addresses in system_defines.h.

```
#define DATA_FLASH_START_ADDRESS        (0x69800)
#define DATA_FLASH_END_ADDRESS          (0x69fff)
```

It may also be necessary to change a constant which is written to the memory fine base address low register for data flash:

#define MFBALR2_HALF0_DATA_FLASH_BASE_ADDRESS (0x9800)

22.8 *Changes to Software Interrupt Addresses*

Change RAM addresses in the software interrupt for checksum clearing/flash erasure. This code is in interrupts.c

```
case 12: // clear integrity word.
        {
                {
                        register Uint32 * program_index = (Uint32 *) 0x6a000;
                        //store destination address for program
                        register Uint32 * source_index = (Uint32 *)zero_out_integrity_word;
                        //Set source address of PFLASH; ……
                {
                        register FUNC_PTR func_ptr;
                        func_ptr=(FUNC_PTR)0x6a000;    //Set function to 0x6a000
                        func_ptr();
                }     //execute erase checksum
```

22.9 *Changes to Data Flash Write in Software Interrupt*

This code is also in interrupts.c. The original code wrote the data flash address every time. This is not necessary, and the data flash has moved in the UCD3138A64, so it will cause a problem. Here is what to comment out:

```
        DecRegs.FLASHILOCK.all = 0x42DC157E; //unlock flash write

//      DecRegs.MFBALR2.bit.BLOCK_SIZE =2;
//      DecRegs.MFBALR2.bit.ADDRESS = 0x22;
        DecRegs.MFBALR2.bit.RONLY = 0;
```

22.10 *Changes to Device ID*

Change 0ISO to A64V in device ID:

#define DEVICE UCD310A64V1 //Device Name

And/or

#define DEVICE_ID "UCD310A64V1|0.0.35.0068|120227"

This tells the GUI that this is a UCD3138A64 instead of a UCD3138.

22.11 *DPWM Registers – Bits Removed*

When compiling a UCD3138 code converted to UCD3138A64, there will be error messages about bits missing from the DPWM registers. In general, the statement which writes to the missing bit can be removed, as it will not affect the functionality. The bits were removed because only one of the states was being used. The DPWM is now always in that state.

22.12 *Change APCMCTRL to PCMCTRL*

PCMCTRL has been removed, and its one bitfield has been moved to PCMCTRL. So all references to PCMCTRL will cause an error. Just change PCMCTRL to APCMCTRL.

22.13 *Changing to Fixed Frequency Sampling on LLC*

This is beyond the scope of this document. See the Reference code for LLC on UCD3138A64 available from TI.

23 Converting UCD3138064 Programs to UCD3138A64

Converting programs from UCD3138064 is very similar to converting from UCD3138. Here are the major differences

6. You start with 2 flash blocks instead of 1.
   - This means that the number of memory segments doesn't change
   - Note that PFLASH1 in the UCD3138064 is equivalent to PFLASH0 in the UCD3138A64
   - PFLASH 2 changes to PFLASH1 in the UCD3138A64
7. Data Flash and RAM still move, but from different places
8. The .cmd and cyclone_device.h files have different names.

Other than that, the same guidelines apply completely.

24 Converting UCD3138A64 Programs to UCD3138128

This conversion is very simple, because all that needs to be changed is the Device ID and the table for parm info/parm value. It may also be necessary to change the checksum location. Of course it is also necessary to use the '128 header and .cmd files.

These lines need to be added to the start and end section of pmbus.h:

```
// Allow read-only access to Program in Program Flash 1
#define PFLASH_1_PROG_START_ADDRESS 0x00008000     // Beginning of PFLASH Program
#define PFLASH_1_PROG_END_ADDRESS   0x0000FFFF     // End of PFLASH Program
#define PFLASH_1_PROG_LENGTH        ((unsigned
short)(PFLASH_1_PROG_END_ADDRESS - PFLASH_1_PROG_START_ADDRESS) + 1)


// Allow read-only access to Program in Program Flash 2
#define PFLASH_2_PROG_START_ADDRESS 0x00010000     // Beginning of PFLASH Program
#define PFLASH_2_PROG_END_ADDRESS   0x00017FFF     // End of PFLASH Program
#define PFLASH_2_PROG_LENGTH        ((unsigned
short)(PFLASH_2_PROG_END_ADDRESS - PFLASH_2_PROG_START_ADDRESS) + 1)
```

```
// Allow read-only access to Program in Program Flash 3
#define PFLASH_3_PROG_START_ADDRESS 0x00018000     // Beginning of PFLASH Program
#define PFLASH_3_PROG_END_ADDRESS   0x0001FFFF     // End of PFLASH Program
#define PFLASH_3_PROG_LENGTH        ((unsigned
short)(PFLASH_3_PROG_END_ADDRESS - PFLASH_3_PROG_START_ADDRESS) + 1)
```

The number of memory segments needs to be changed to 22 to cover the additional segments for the added flash blocks:

```
#define NUM_MEMORY_SEGMENTS   22       // 22 memory segments for Cyclone 128
```

In addition, it is necessary to add start and length for pflash 2 and 3 to the c file with parm info/parm value in it. Depending on the program, these may be in different files:

It is also necessary to add start and length for pflash 1 to 3 to the lists in the c file with parm info/parm value in it. These may be in different files in different codes.

```
SYSTEM_REGS_START_ADDRESS,
PFLASH_1_PROG_START_ADDRESS,
PFLASH_2_PROG_START_ADDRESS,
PFLASH_3_PROG_START_ADDRESS};
SYSTEM_REGS_LENGTH,
PFLASH_1_PROG_LENGTH,
PFLASH_2_PROG_LENGTH,
PFLASH_3_PROG_LENGTH   };
```

If it hasn't been done already, the array size value for the memory start and size arrays should be changed to NUM_MEMORY_SEGMENTS:

```
const Uint32    parm_mem_start[NUM_MEMORY_SEGMENTS] = {

const Uint16    parm_mem_length[NUM_MEMORY_SEGMENTS] = {    RAM_LENGTH,
```

Device ID also needs to be changed to show that it is a '128. Here is the correct Device ID:

```
#define DEVICE          UCD310128V1                          //Device Name
```

And/or

```
#define DEVICE_ID       "UCD310128V1|0.0.35.0068|120227"
```

25 References

1. UCD3138 Digital Power Peripherals Programmer's Manual (SLUU995).
2. UCD3138 ARM and Digital System Programmer's Manual (SLUU994).
3. UCD3138 Monitoring and Communications Programmer's Manual (SLUU996).
4. UCD3138 Device Datasheet (SLUSAP2).
5. UCD3138064 Device Datasheet (SLUSB27).
6. UCD3138064 Programmer's Manual (SLUUAD8).

Document Revision History

Version	Release Date	List of Changes
SLUUB54	July 2014	Initial Document
SLUUB54A	September 2014	Rev. A.
SLUUB54B	April 2016	Rev B.

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