Using the TPS56300 to Power DSPs

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ABSTRACT

The synchronous buck converter controllers (TPS56100, TPS56300, TPS56xx, and TPS5602) made by Texas Instruments are specifically designed to provide excellent transient response and high efficiency to the microprocessor power applications such as the TMS320C6000 and TMS320C5000 families from TI, as well as similar digital loads. In addition, hysteresis control method is used such that power supply designers do not have to worry about the stability and compensation issues.

1 Introduction

The TI TPS56300 features programmable dual channels (a synchronous buck controller and a LDO controller) with fast feedback control. The ripple regulator (synchronous buck converter) efficiently powers the TI DSP core voltage. The LDO controller drives an external N-channel power MOSFET. When the input supply voltage exceeds the required DSP I/O voltage, the MOSFET is controlled as a linear regulator. When the input supply voltage equals the required DSP I/O voltage (or, less than I/O voltage), the MOSFET is fully enhanced and used as a power distribution switch. The TPS56300 also includes inhibit, slow start, and under-voltage lockout features to aide in controlling power sequencing.

Many protection features are incorporated to ensure better system integrity. An open-drain output power good status circuit monitors both output voltages, and is pulled low if output falls below the threshold. An over current shutdown circuit protects the high-side power MOSFET against short-to-ground faults at load or the phase node, while overvoltage protection turns off the output drivers and LDO controller if output exceeds its threshold. Under voltage protection turns off the high-side and low-side MOSFET drivers and the LDO controller if output is 25% below V_{ref}. Lossless current-sensing is done by detecting the drain-source voltage drop across the high-side power MOSFET while it is conducting.

1.1 TPS56300 Operating Conditions

Table 1. Summary of the TI Synchronous Buck Converter Controller and EVM Characteristics

	V_I RANGE (POWER STAGE)	V_{CC} RANGE (CONTROLLER)	V_O RANGE (POWER STAGE)	$I_{O, MAX}$† (POWER STAGE)	DRIVER CURRENT (CONTROLLER)	OTHERS
TPS56100	4.5 ~ 6 V	4.5 ~ 6 V	1.3 to 2.6 V	7 A	2 A	1 channel
TPS56300	2.8 ~ 5.5 V	2.8 ~ 5.5 V	1.3 to 3.3 V	4 A for RR 6 A for LDO	2 A	2 channels
TPS56xx	4.5 ~ 6 V	12 V	1.5V,1.8 V, 2.5 V, or 3.3 V	8 A	2 A	1 channel
TPS5602	4.5 ~ 25 V	4.5 ~ 25 V	Adjustable	4 A/channel	1.2 A at V_O = 3 V	2 channels

† The current capability can be extended if the switching devices are added in parallel; see Table 2 in TI TPS56100/56300 data sheets.

1.2 Key Features

- Programmable Dual Output Controller
  - Switching Regulator Controls DSP Core Voltage
  - LDO Controller Regulates DSP I/O Voltage
- Programmable Slow-Start
- Simultaneous Power-Up of Both Outputs
- Power Good Output
- Efficiencies Greater Than 90% on Switching Regulator
- ±1.5% Reference Voltage Tolerance
- Overvoltage, Undervoltage, and Adjustable Overcurrent Protection
- Fully Compliant With TI DSP Power Requirements
- Evaluation Module TPS56300EVM–139 Available

2 Application Circuit

Figure 1 shows a typical circuit design using the TPS56300, which features a dual-channel output, a ripple regulator (1.8-V output) and an LDO (3.3-V output). During input voltage ranging from 2.8 to LDO_OUT (LDO output voltage), the LDO's power MOSFET looks like a small resistor (11 mΩ) and can be used as a power distribution switch. Over the input voltage range higher than the LDO_OUT, the LDO regulates the output at 3.3 V. The ripple regulator of TPS56300 regulates the DSP core voltage over the input range (2.8 V ~ 5.5 V). The two output voltages are independent and are easily set by voltage identification network (VID) pins. Tri-level VID pins set both regulated voltages to any of nine preset voltage pairs from 1.3 V to 3.3 V. Other voltages are possible by implementing an external voltage divider.

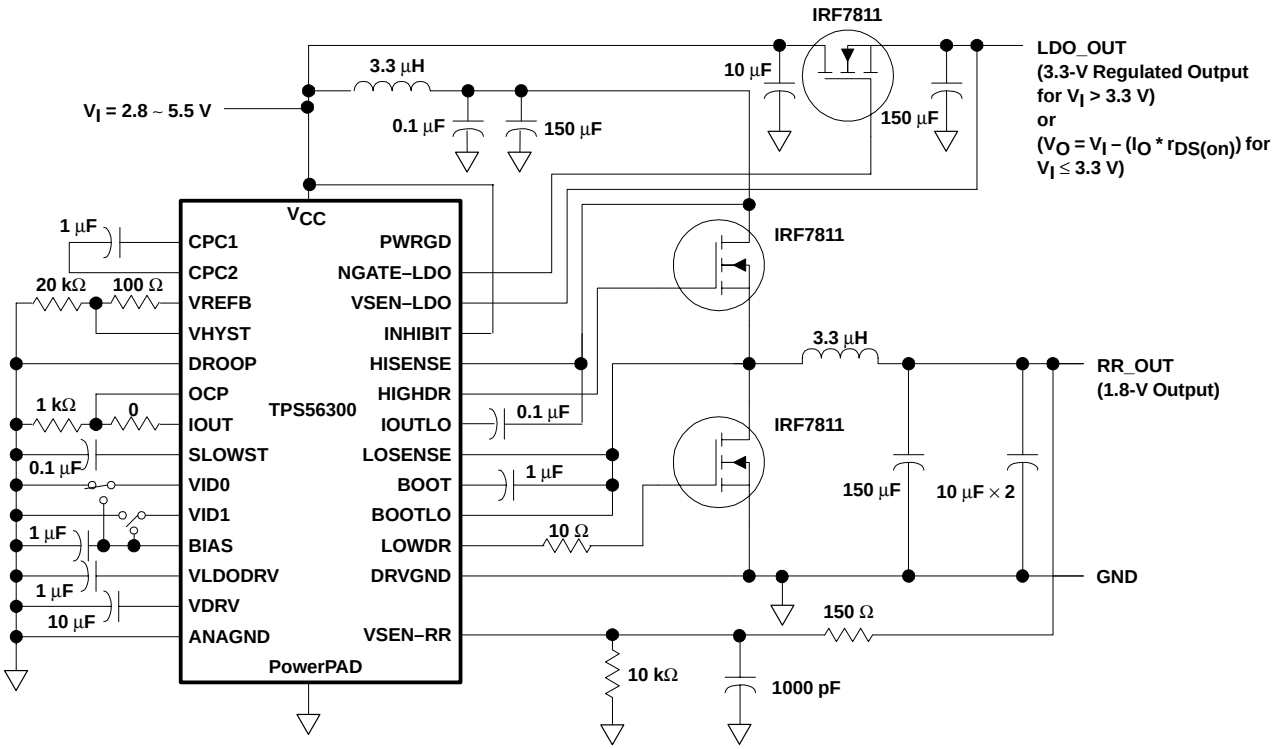

Figure 1. Typical Circuit Design Using the TPS56300

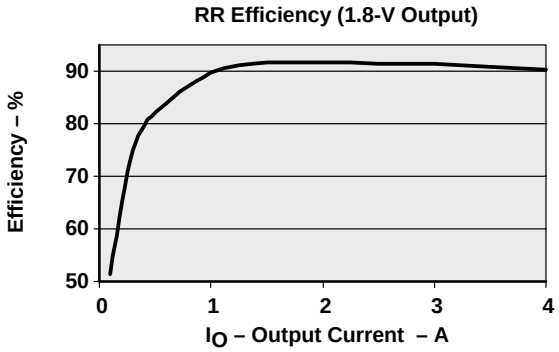

Figure 2. Efficiencies of Ripple Regulator (3.4-V Input)

Table 2 shows the setting values of TPS56300 to generate the output voltages 1.5 V, 1.8 V, 2.5 V, and 3.3 V for TI DSP power requirements. Figure 2 shows the efficiency of the ripple regulator.

Table 2. Summary of Setting Values for TPS56300 1.5/1.8/2.5/3.3-V Outputs

VID TERMINALS (0 = GND, 1 = FLOATING, 2 = $V_{(BIAS)}$)		V_O1	V_O2
VID1	VID0	(RR_OUT, Vdc)	(LDO_OUT, Vdc)
2	1	1.5	3.3
1	0	1.8	3.3
1	2	2.50	3.3

Most LDOs Power MOSFET manufacturers specify the maximum power dissipation allowable without damaging the device. The safe operating area for the LDO regulator using IRF7811 as the power MOSFET is shown in Figure 3. The LDO regulator must operate within this area. The LDO regulator power dissipation is calculated using equation 1.

$$P_D = (V_I - V_O) \times I_O \quad (1)$$

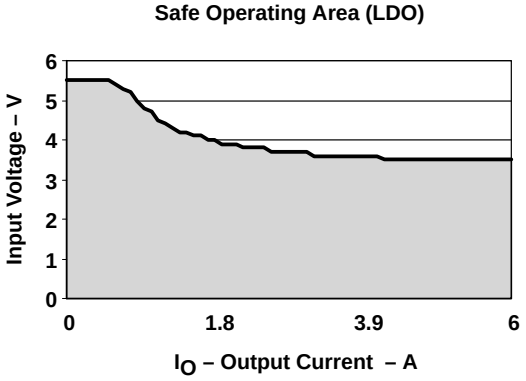

Figure 3. Safe Operating Area of the LDO (3.3-V Output, 3.4-V Input)

NOTE: TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long term reliability of the device. System level concerns, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers.

3 Power Supply Solutions

The power solution for 1.8-V core and 3.3-V I/O voltage using TPS56300 is shown in Figure 4. Both supplies (LDO and ripple regulator) will ramp up together to promote better system reliability during power up.

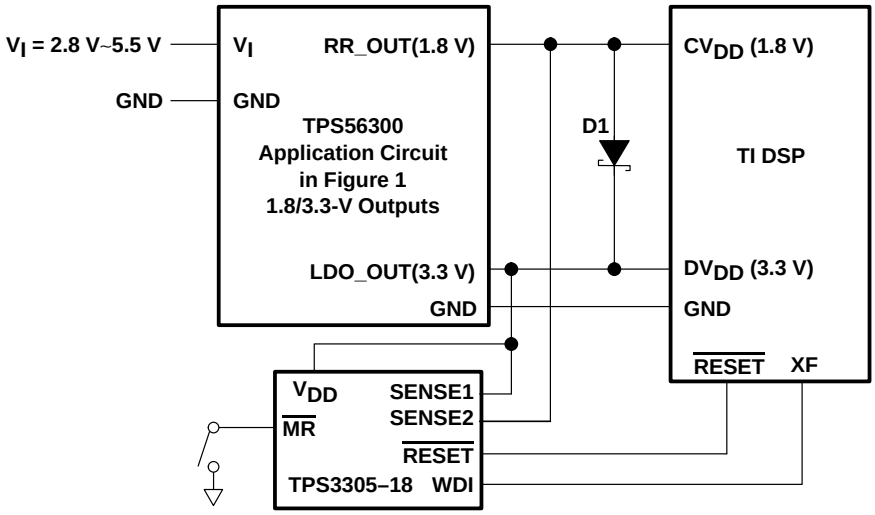

Figure 4. TI DSP Power Supply Solution Using the TPS56300

The Schottky diode (D1) provides a measure of protection during the power-down sequence and during other periods when the DV_{DD} supply is below the CV_{DD} supply by limiting the CV_{DD}–DV_{DD} voltage to the forward drop of D1.

The two power supplies should be placed close to the DSP to minimize the trace resistance and inductance, and to minimize the ground loop current between the two output grounds. This ground loop current can generate radiated EMI noise that can adversely affect any circuitry within the loop. The ground connection must be made directly on the DSP to help minimize the problem.

4 Evaluation Module

An EVM (evaluation module)—SLVP139—is available to provide a convenient method for evaluating the performance of the TPS56300. A completed and tested power supply is included in the EVM.

5 References

For detailed information:

1. Data sheet and EVM Board; http://www–s.ti.com/sc/psheets/slvs261a/slvs261a.pdf
2. EVM board order; http://www.ti.com/sc/docs/tools/analog/tps56300evm_139.html
3. SVS application note; http://www.ti.com/sc/docs/apps/analog/supervisory_circuits.html
4. Application note; http://www.ti.com/sc/docs/apps/analog/power_management.html

For general information:

5. TI Power Management Products; http://www.ti.com/sc/docs/products/msp/pwrmgmt/index.html

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