TPS43340-Q1 Family Design Checklist

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This application note is for TPS43340-Q1, a dual-buck regulator controller (Buck1, Buck2), single-buck regulator converter (Buck3), and linear regulator (LREG1), lists the connection details for each pin. The pin details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each pin on a system schematic. In addition to this list, customers are advised to use the information in the data sheet, (TI literature number SLVSB16).

Pin Details

Pin Name	Pin No.	Pin Group	I/O	Description	Expected Components and Connections	Function, if Not Used
BOOT1	48	Analog	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckA. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.	Connect a capacitor of several hundred nF (for example. 220 nF) between BOOT1 and PH1, use low resistance, low inductance (short, wide PCB trace) and a small loop. Avoid vias.	N/A
BOOT2	37	Analog	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckB. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.	Connect a capacitor of several hundred nF (for example. 220 nF) between BOOT2 and PH2, uselow resistance, low inductance (short, wide PCB trace) and a small loop. Avoid vias.	N/A
BOOT3	14	Analog	I	A capacitor between BOOT3 and PH3 acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck converter Buck3. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.	Connect a capacitor of several hundred nF (for example. 220 nF) between BOOT3 and PH3, use low resistance, low inductance (short, wide PCB trace) and a small loop. Avoid vias.	N/A
COMP1	8	Analog	O	Error amplifier output of Buck1 and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of Buck1. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.	Connect a Type2 compensation network, designed for a bandwidth of 1 / 6th to 1 / 10th of f_{SW}. Calculate per the Component Selection Tool.	N/A
COMP2	29	Analog	O	Error amplifier output of Buck2 and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of Buck2. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.	Connect a Type2 compensation network, designed for a bandwidth of 1 / 6th to 1 / 10th of f_{SW}. Calculate per the Component Selection Tool.	N/A
COMP3	18	Analog	O	Error amplifier output of Buck3 and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the inductor on PH3.	Connect a Type2 compensation network, designed for a bandwidth of 1 / 6th to 1 / 10th of f_{SW}. Calculate per the Component Selection Tool.	N/A

Pin Name	Pin No.	Pin Group	I/O	Description	Expected Components and Connections	Function, if Not Used
EN1	22	Digital	I	Enable input for Buck1 (active-high with an internal pullup current source with approximately 0.5 µA of current). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller.	Pull high for activation, low to de-activate. Hard-wired or µC-controlled	Buck1 is active.
EN2	21	Digital	I	Enable input for Buck2 (active-high with an internal pullup current source with approximately 0.5 µA of current). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller.	Pull high for activation, low to de-activate. Hard-wired or µC-controlled	Buck2 is active.
EN3	20	Digital	I	Enable input for Buck3 (active-high with an internal pullup current source with approximately 0.5 µA of current). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 0.7 V disables the controller.	Pull high for activation, low to de-activate. Hard-wired or µC-controlled	Buck3 is active.
EN4	47	Digital	I	Enable input for LREG1 (active-high with an internal pullup current source). An input voltage higher than VIH enables the regulator, whereas an input voltage lower than VIL disables the regulator. This input has an internal pullup with approximately 0.5 µA of current.	Pull high for activation, low to de-activate. Hard-wired or µC-controlled	LREG1 is active.
EXTSUP	40	Power	I	One can use EXTSUP to supply the VREG regulator from one of the TPS43340-Q1 buck regulator rails to reduce power dissipation in cases where there is an expectation of high VIN. If EXTSUP is unused, leave the pin open without a capacitor installed.	Connect to a permanent source supplying 4.6 V to VIN. If the source is not permanently on, insert a diode prior to the EXTSUP input. Decouple with approximately 100 nF.	Leave open
GL1	3	Power	O	External low-side N-channel MOSFET gate drive for buck regulator Buck1. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.	Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If necessary to slow FETs down, use a series resistor in this line (for example, 10 Ω).	N/A
GL2	34	Power	O	This output can drive the external low-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.	Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If necessary to slow FETs down, use a series resistor in this line (for example, 10 Ω).	N/A
GND	26	Analog	O	Analog ground reference	Provide a low-resistance, low-inductance (short, wide PCB trace, lots of vias) path to GND, ideally, to the GND-plane	N/A
GPULL	39	Analog	O	Gate-driver output to implement the reverse-battery protection by driving an external P-channel MOSFET.	Connect to gate of Diode-bypass-FET to reduce losses in the diode and improve efficiency.	Leave open
GU1	1	Power	O	External high-side N-channel MOSFET gate drive for buck regulator Buck1. The output provides high peak currents to drive capacitive loads. The gate-drive reference is a floating-ground reference provided by PH1 and has a voltage swing provided by BOOT1.	Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If necessary to slow FETs down, use a series resistor in this line (for example, 10 Ω).	N/A
GU2	36	Power	O	This output can drive an external high-side N-channel MOSFET for buck regulator Buck2. The output provides high peak currents to drive capacitive loads. The gate-drive reference is a floating-ground reference provided by PH2 and has a voltage swing provided by BOOT2.	Keep the trace to the gate of the FET short and low-impedance. Do not add extra capacitance. If necessary to slow FETs down, use a series resistor in this line (for example, 10 Ω).	N/A

Pin Name	Pin No.	Pin Group	I/O	Description	Expected Components and Connections	Function, if Not Used
LREG1	46	Power	O	Linear regulator output.	Decouple with a low-ESR ceramic output capacitor in the range of 1 µF to 47 µF connected from this terminal to ground.	N/A
PGND1	4	Analog	O	Power ground connection for the GL1 driver.	Connect solidly—low-resistance, low-inductance (short, wide PCB trace, lots of vias) to the GND plane.	N/A
PGND2	33	Analog	O	Power ground connection to the source of the low-side N-channel MOSFETs of Buck2	Connect solidly—low-resistance, low-inductance (short, wide PCB trace, lots of vias) to the GND plane.	N/A
PGND3	12	Analog	O	Buck3 power ground	Connect solidly—low-resistance, low-inductance (short, wide PCB trace, lots of vias) to the GND plane.	N/A
PH1	2	Power	O	Switching terminal of buck regulator Buck1, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous mode operation is desirable.	Keep trace to FETs and inductor short and low-impedance.	N/A
PH2	35	Power	O	Switching terminal of buck regulator Buck2, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous mode operation is desirable.	Keep trace to FETs and inductor short and low-impedance.	N/A
PH3	13	Power	O	Switching terminal of buck converter Buck3. Also provides a floating ground reference for the high-side MOSFET gate-driver circuitry	Keep trace to inductor short and low-impedance.	N/A
Rdelay	24	Analog	O	The capacitor at the Rdelay pin sets the power-good delay interval used to de-glitch the outputs of the power-good comparators. Leaving this pin open sets the power-good delay to an internal default value of 20 µs, typical.	Choose for desired delay time, for example, 1 nF for 1 ms. Calculate per the Component Selection Tool.	Defaults to 20 µs, typical.
RST1	9	Digital	O	Open-drain power-good output for Buck1, with a 50-kΩ pullup resistor to S2. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ (see data sheet) of the set value.	Connect to interrupt input of the processor; use for sequencing of the rails [requires Vout of the first rail to be higher than the enable voltage (>1.7 V)] or leave open. An additional pullup of, for example, 10 kΩ can strengthen the output.	Leave open
RST2	28	Digital	O	Open-drain power-good output for Buck2 with a 50 kΩ pullup resistor to S4. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ (see data sheet) of the set value.	Connect to interrupt input of the processor; use for sequencing of the rails [requires Vout of the first rail to be higher than the enable voltage (>1.7 V)] or leave open. An additional pullup of, for example, 10 kΩ can strengthen the output.	Leave open
RST3	16	Digital	O	Open-drain power-good output for Buck3. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ (see data sheet) of the set value.	Connect to interrupt input of the processor; use for sequencing of the rails [requires Vout of the first rail to be higher than the enable voltage (>1.7 V)] or leave open. An additional pullup of, for example, 10 kΩ can strengthen the output.	Leave open

Pin Name	Pin No.	Pin Group	I/O	Description	Expected Components and Connections	Function, if Not Used
RST4	44	Digital	O	Open-drain power-good indicator pin for LREG1, with a 50-kΩ pullup resistor to LREG1. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ (see data sheet) of the set value.	Connect to interrupt input of the processor; use for sequencing of the rails [requires Vout of the first rail to be higher than the enable voltage (>1.7 V)] or leave open. An additional pullup of, for example, 10 kΩ can strengthen the output.	Leave open
RT	25	Analog	O	Connecting a resistor to analog ground on this pin sets the operating switching frequency of the buck controllers and converter. Shorting this pin to ground or leaving it open defaults operation to 400 kHz for the buck controllers and the converter.	Connect a resistor to GND for the appropriate frequency, for example, 160 kΩ for 150 kHz, 40 kΩ for 600 kHz.	defaults to 400kHz typical for Bucks, 200kHz for boost
S1	6	Analog	I	High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for the Buck2 controller.	Connect to the current-sense resistor, chosen for adequate peak-current limit (consider slope-compensation). Calculate per the Component Selection Tool. Route S1 and S2 differentially. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (S1 positive node, S2 negative node). A capacitor between S1 and S2 can reduce noise; choose approximately 10 nF.	N/A
S2	5	Analog	I			N/A
S3	31	Analog	I	High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for the Buck2 controller.	Connect to the current-sense resistor, chosen for adequate peak-current limit (consider slope-compensation). Calculate per the Component Selection Tool. Route S3 and S4 differentially. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and VIN. (S3 positive node, S4 negative node). A capacitor between S3 and S4 can reduce noise; choose approximately 10 nF.	N/A
S4	32	Analog	I			N/A
SLEW	19	Analog	I	Slew rate (dV/dt) selector of the internal high-side switching MOSFET for Buck3.	connected from this terminal to ground.	
SS1	10	Analog	O	Soft-start or tracking input for buck controller Buck1. The buck controller regulates the VSENSE1 voltage to the lower of 0.8 V or the SS1 pin voltage. An internal pullup current source of typically 1 μA is present at the pin. Alternatively, this pin can be used for tracking another supply.	Connect a capacitor to GND for soft-start (calculate per the Component Selection Tool) or connect with a voltage divider to a leading supply to track that rail.	N/A
SS2	27	Analog	O	Soft-start or tracking input for buck controller Buck2. The buck controller regulates the VSENSE2 voltage to the lower of 0.8 V or the SS2 pin voltage. An internal pullup current source of typically 1 μA is present at the pin. Alternatively, this pin can be used for tracking another supply.	Connect a capacitor to GND for soft-start (calculate per the Component Selection Tool) or connect with a voltage divider to a leading supply to track that rail.	N/A

Pin Name	Pin No.	Pin Group	I/O	Description	Expected Components and Connections	Function, if Not Used
SS3	15	Analog	O	Soft-start or tracking input for buck converter Buck3. The buck converter regulates the VSENSE3 voltage to the lower of 0.8 V or the SS3 pin voltage. An internal pullup current source of typically 1 µA is present at the pin. Alternatively, this pin can be used for tracking another supply.	Connect a capacitor to GND for soft-start (calculate per the Component Selection Tool) or connect with a voltage divider to a leading supply to track that rail.	N/A
SYNC	23	Digital	I	PLL synchronization, low-power-mode (LPM) control pin. If an external clock is present on this pin, the device detects it and the internal PLL locks on to the external clock. This overrides the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz.	Tie high to force the device into always-continuous mode. Leave open or tie to GND to allow LPM. In both cases, the device switches at the frequency defined by the RT resistor. Apply an external clock to synchronize to a clocking system (150 kHz to 600 kHz)	Leaving it open allows LPM.
VIN	41	Power	I	Main Input pin. This is the buck-controller and buck-converter input pin. Additionally, it powers the internal control circuits of the device.	Decouple with a capacitance in the order of 10 µF, keep close to the IC with a low-resistance, low-inductance (short, wide PCB trace) path. Avoid vias.	N/A
VIN2SENSE	43	Analog	I	Supply-voltage sense input for the current mode of Buck2.	Connect to the drain of the high-side-FET of Buck2, for example, VBAT or Vout1 (S2).	N/A
VLR1	42	Power	I	The VLR1 pin is the input voltage source for the linear regulator supply.	Connect a capacitor on the order of 100 nF to ground to filter any noise present on the line.	N/A
VREG	38	Analog	O	Output pin of internal regulator to provide decoupling. This pin has current-limit protection; do not use it to drive any other loads.	Decouple with 3.3 µF to 10 µF, recommended is 4.7 µF, keep close to the IC with low-resistance, low-inductance (short, wide PCB trace) path. Avoid vias.	N/A
VSENSE1	7	Analog	I	Feedback voltage pin for Buck1. The buck controller regulates the feedback voltage to the internal reference of 0.8 V.	Choose a resistor network to set the VSENSE1 voltage to 0.8 V, allow for >10-µA current. For noise cancellation, a capacitor in the order of 47 pF to 100 pF in parallel with the lower resistor can help.	N/A
VSENSE2	30	Analog	I	Feedback voltage pin for Buck2. The buck controller regulates the feedback voltage to the internal reference of 0.8 V.	Choose a resistor network to set the VSENSE2 voltage to 0.8 V, allow for >10-µA current. For noise cancellation, a capacitor in the order of 47 pF to 100 pF in parallel with the lower resistor can help.	N/A
VSENSE3	17	Analog	I	Feedback voltage pin for Buck3. The buck controller regulates the feedback voltage to the internal reference of 0.8 V.	Choose a resistor network to set the VSENSE3 voltage to 0.8 V, allow for >10-µA current. For noise cancellation, a capacitor in the order of 47 pF to 100 pF in parallel with the lower resistor can help.	N/A
VSENSE4	45	Analog	I	Feedback voltage pin for linear regulator LREG1. LREG1 regulates the feedback voltage to the internal reference	Choose a resistor network to set the VSENSE3 voltage to 0.8 V, allow for >10-µA current. For noise cancellation, a capacitor in the order of 47 pF to 100 pF in parallel with the lower resistor can help.	N/A
VSUP	11	Power	I	Power supply for the Buck3 regulator.	Provide good decoupling to PGND3 with a ceramic capacitor close to the pins.	N/A

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