Introduction to the Series Capacitor Buck Converter

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ABSTRACT

The series capacitor buck converter is a dc-dc converter topology that uniquely merges a switched capacitor circuit and a multiphase buck converter. Many of the challenges faced by conventional buck converters are overcome by this converter topology. This enables efficient, high frequency operation and significantly smaller solution size. The series capacitor buck converter has beneficial characteristics such as lower switching loss, less inductor current ripple, automatic inductor current balancing, duty ratio extension, and soft charging of the series capacitor. Drawbacks include a maximum output voltage (or minimum input voltage) limit and the impracticality of phase shedding. This application report analyzes the topology and presents example experimental results from the TPS54A20 voltage regulator designed for 12 V input, 1.2 V output with 10 A full load current.

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1 Introduction

Shrinking power converter size is highly desirable in point-of-load voltage regulator applications. Voltage regulators take up a large percentage of circuit board space and system weight. Passive components (primarily inductors and capacitors) are usually the largest physical elements of a voltage regulator. To reduce inductance and capacitance requirements and free up board space, the converter switching frequency is often increased. This can be effective but also will increase switching power loss. The series capacitor buck converter, shown in Figure 1, overcomes many of the challenges faced by conventional buck converters and enables small, efficient, high frequency (multi-MHz) voltage regulators.
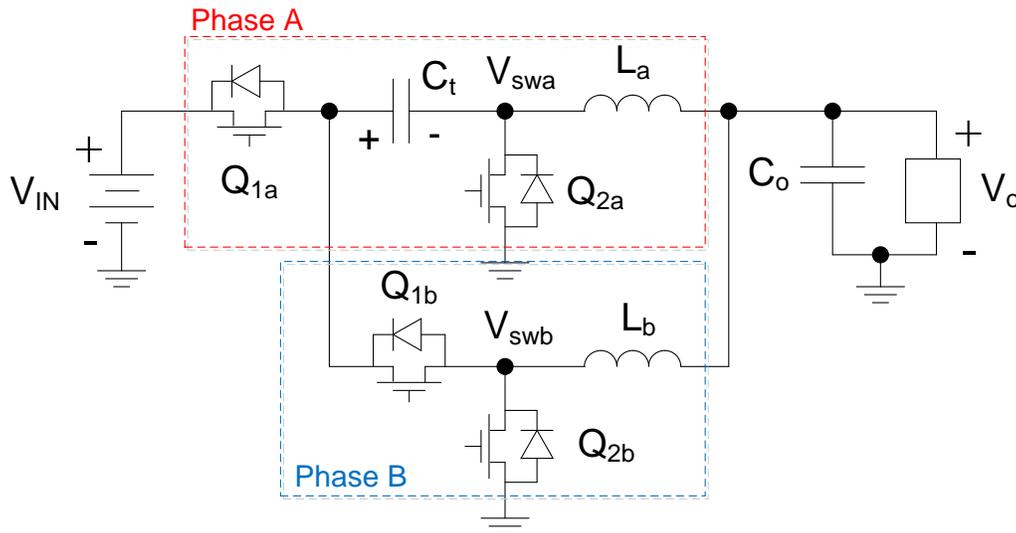

Figure 1. Two-phase Series Capacitor Buck Converter

The potential for inductor size reduction is shown in Figure 2. Inductors used in existing 10-A output buck converters operating at about 500-kHz switching frequency are shown on the left. Inductors used in a 10 A, two-phase series capacitor buck converter operating with 2-5MHz switching frequency per phase are shown on the right. The inductors on the right are 15 times smaller than the inductors on the left.
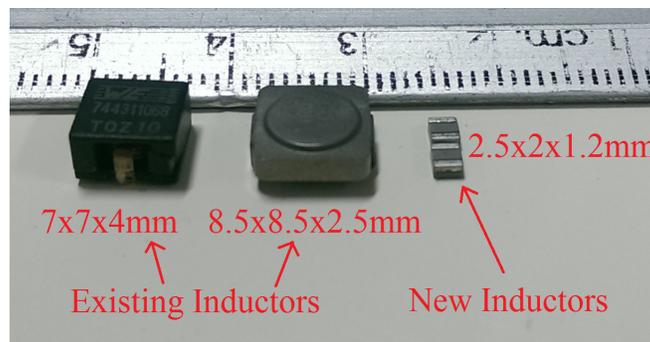

Figure 2. Inductor Size Comparison for a 10-A Application

2 High Frequency Buck Converter Challenges

The buck converter is a simple, established topology for point-of-load voltage regulators. Point-of-load converters are the last conversion stage in the power delivery system and directly supply power to the load (which is often an IC like a DSP, FPGA, ASIC, DDR memory, etc.). In high current applications, multiple buck converters operate in parallel in what is commonly referred to as a multiphase buck converter. For example, a two-phase buck converter is shown in Figure 3.
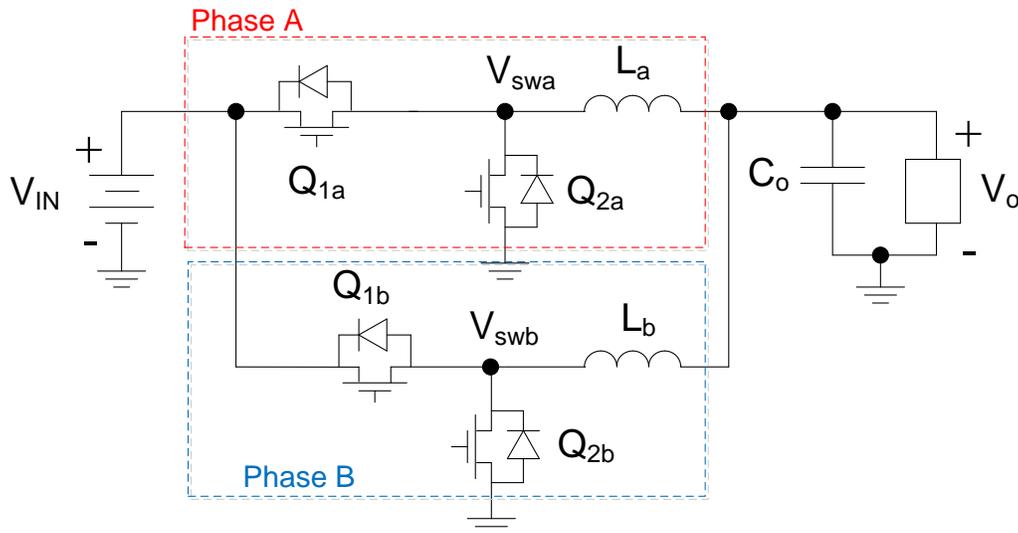
Figure 3. Two-phase Buck Converter

The two major challenges to high frequency operation of buck converters are excessive switching loss and narrow high side switch pulse width. If switching frequency is pushed into the MHz range, switching loss can become very large. This is primarily due to the fact that switching loss increases proportionally with switching frequency. High voltage conversion ratio (e.g. >5:1) and high current (e.g. >10 A) applications can struggle with a large portion of total loss being switching loss.

A very short on-time of the high side switch is challenging as well. Narrow pulse widths can be difficult to generate effectively without other time delays interfering with maintaining sufficient room for control. For example, many converters using peak current mode control find it difficult to generate short on-times because they must blank the initial portion of the high side on-time. Narrow pulse width is often a limiting factor in high voltage conversion ratio applications. Consider a buck converter with a 10:1 voltage conversion ratio operating at 5 MHz. As shown in Figure 4, the high side switch nominal on-time is 20ns. This short on-time is not achievable in many converters today.
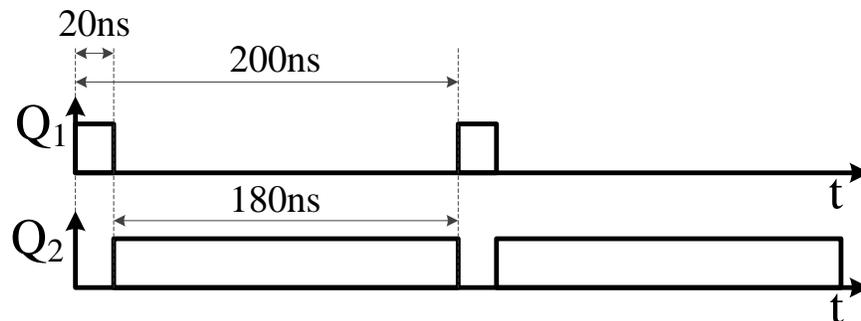

Figure 4. Narrow Pulse Width in High Frequency, High Conversion Ratio Buck Converter

There are various approaches that have been explored to address high frequency conversion challenges. Resonant and quasi-resonant converters enable soft switching which is beneficial as switching frequency increases, refer to Section 6 [1]. Drawbacks of this approach include resonant tank tuning requirements to achieve soft switching, restrictions in switching frequency, load current range of achieving soft switching, circulating current loss, increased switch ratings, and increased loss in passive components. The tapped inductor buck converter overcomes the voltage conversion ratio challenge but suffers from a large voltage spike that may require a clamp circuit and is non-minimum phase (i.e. has a right half plane zero in the

control-to-output transfer function), refer to Section 6 [2], [3]. Another approach is merging a switched capacitor circuit and an inductor based converter, refer to Section 6 [4]. Combining a switched capacitor circuit and a buck converter is advantageous because voltage conversion can be accomplished by the switched capacitor circuit and output regulation is achieved through the buck stage. This hybrid approach plays to the strengths of each circuit.

3 Series Capacitor Buck Converter

The series capacitor buck converter, shown in Figure 1, leverages the hybrid switched capacitor/inductor approach. It uniquely combines a switched capacitor circuit and a multiphase buck converter in a single conversion stage. Three or more phase versions are feasible but the focus of this report is on the two-phase implementation. This topology adds one energy transfer capacitor (the series capacitor) and can easily be compared to a two-phase buck converter, refer to Section 6 [5]. There are two key differences in the converter connection points. First, the series capacitor is inserted between the high side and low side switch of phase A. Second, the drain of the phase B high side switch is connected to the source of the phase A high side switch instead of the input supply. As will be seen, these small adjustments have considerable impact on converter operation and characteristics.

3.1 Steady-State Operation

The converter configurations and waveforms are very similar to an interleaved, two-phase buck converter, as shown in Figure 5 to Figure 10. Each phase is interleaved with 180 degrees phase shift, and inductor currents are triangular just like a two-phase buck converter. Waveforms for continuous conduction mode (CCM) are shown.

During the first time interval (t_1) shown in Figure 5, the phase A high side switch (Q_{1a}) is turned on. The phase A inductor current increases and the series capacitor is charged by the phase A inductor, as shown in Figure 8 and Figure 9. The phase B low side switch (Q_{2b}) is on and the phase B inductor current decreases. The switch node voltages are shown in Figure 10. This example assumes a 12-V input supply. The voltage across the series cap is nominally half the input voltage (i.e. 6 V). The series capacitor value is selected so that the voltage ripple is small. It mostly acts as a dc voltage source.
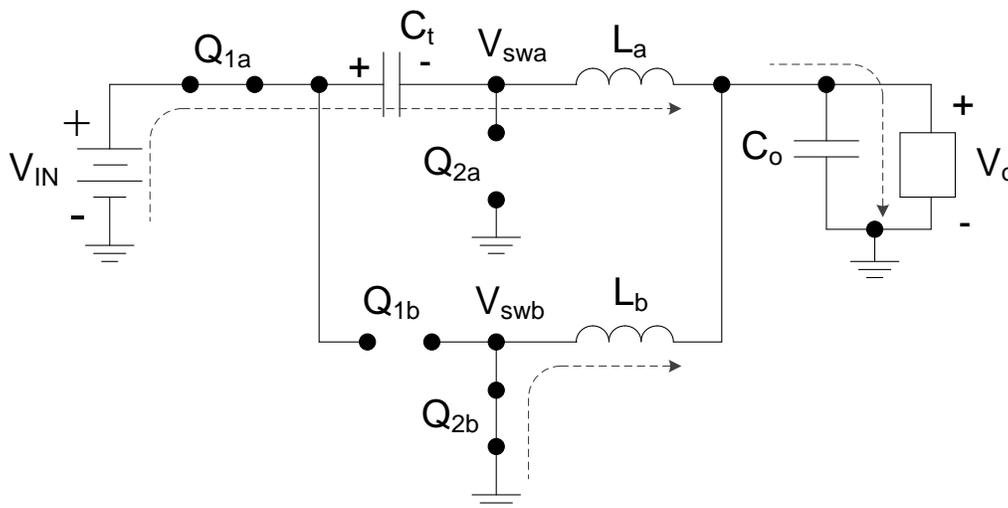

Figure 5. Interval 1: Phase A High Side Switch (Q1a) on

During the second (and fourth) time interval (t_2 and t_4) shown in Figure 6, both low side switches (Q_{2a} and Q_{2b}) are turned on. Both switch node voltages are at ground and both inductor currents decrease, as shown in Figure 8 and Figure 10. Because there is no current in the series capacitor, its voltage remains constant as shown in Figure 9.
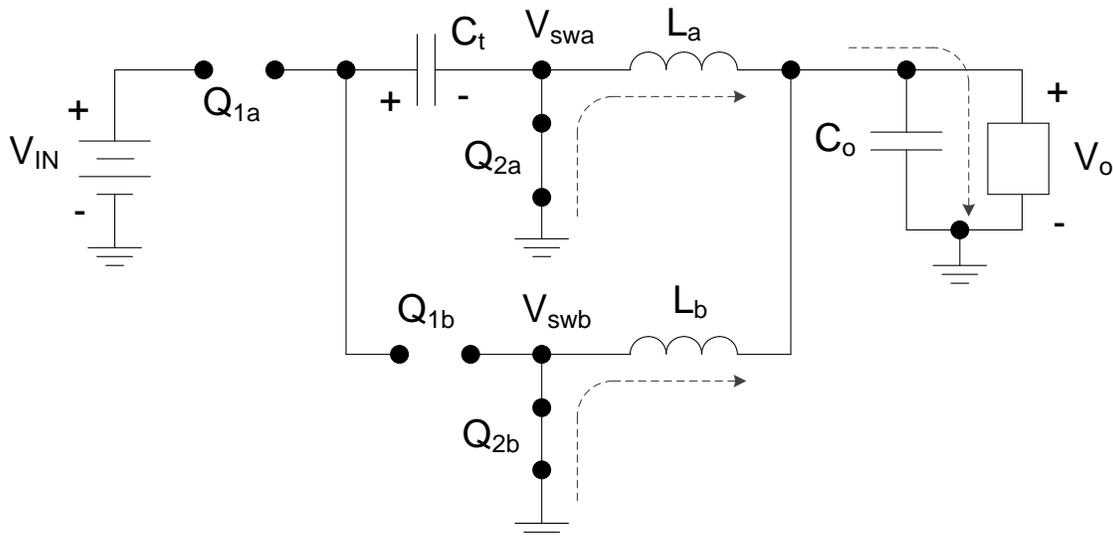
**Figure 6. Interval 2 and 4: Both Low Side Switches (Q2a, Q2b) on**
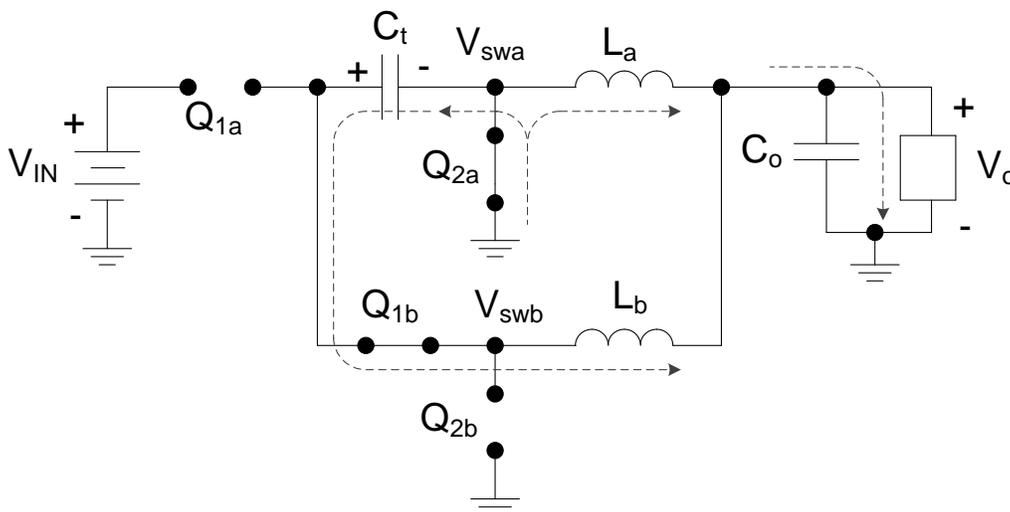
Figure 7. Interval 3: Phase B High Side Switch (Q1b) on

During the third time interval (t_3) shown in Figure 7, the phase B high side switch (Q_{1b}) is on. Because the phase A low side switch (Q_{2a}) is on, the negative side of the series capacitor is connected to ground. The series capacitor acts as an input capacitor to phase B and brings the phase B switch node up to approximately half the input voltage as shown in Figure 10. It is discharged a small amount by the phase B inductor current which rises during this interval as shown in Figure 8. The series capacitor voltage decreases slightly as shown in Figure 9.
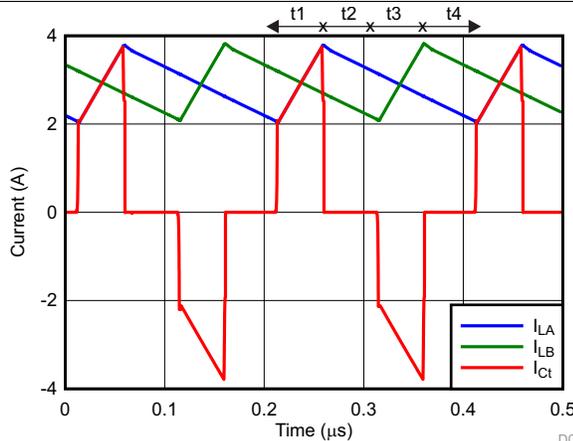
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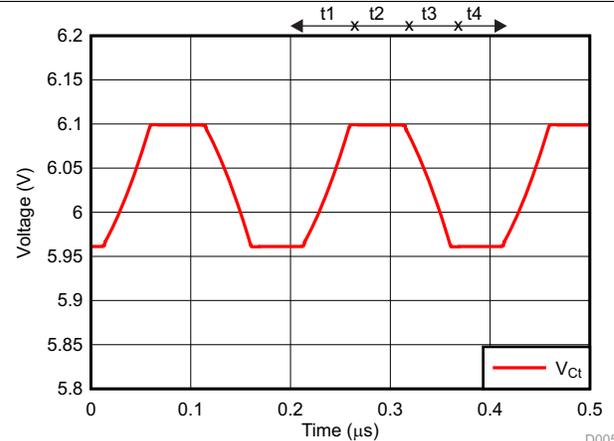
Figure 9. Series Capacitor Voltage (Differential)
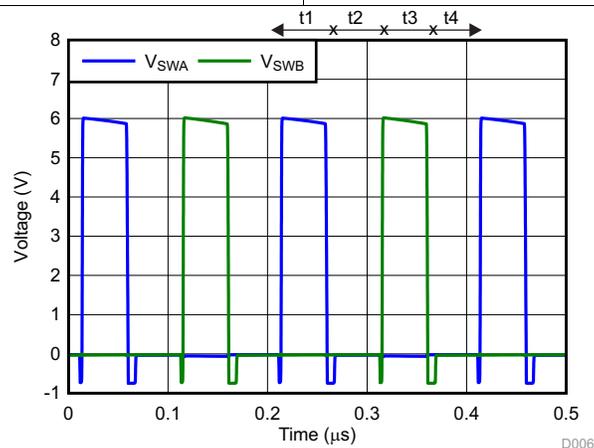
**Figure 10. Switch Node Voltages**

The main differences between the series capacitor buck converter and the conventional buck converter are that the duty ratio of the high side switches is doubled, switching occurs with half the drain-to-source voltage experienced by switches in a buck converter, inductor current balancing is automatic, and inductor current ripple is decreased. All these factors are favorable for high frequency and high conversion ratio converters.

A major drawback of the topology is a limitation of the theoretical maximum output voltage to $V_{IN}/4$. This is due to a 50% duty cycle limitation and the switch node voltage being $V_{IN}/2$ when the high side switches are on. Practically, the maximum output voltage is about $V_{IN}/5$ when converter losses are taken in to account. Another drawback is that phase shedding and adding is not practical.

3.2 *Steady-State Equations*

The equations that describe steady-state operation of the series capacitor buck converter are derived from the converter configurations. For simplicity, assume the converter is lossless (i.e. no resistive terms), the inductance values are matched (i.e. $L = L_A = L_B$), and the duty ratios are matched (that is, $D = D_A = D_B$). The large-signal average model for the inductor currents, series capacitor voltage, and output capacitor voltage is:

$$L\frac{dI_{LA}}{dt} = DV_{in} - DV_{Ct} - V_o \tag{1}$$

$$L\frac{dI_{LB}}{dt} = DV_{Ct} - V_o \tag{2}$$

$$C_t\frac{dV_{Ct}}{dt} = DI_{LA} - DI_{LB} \tag{3}$$

$$C_o\frac{dV_o}{dt} = I_{LA} + I_{LB} - I_o \tag{4}$$

where I_{LA} and I_{LB} are the average inductor currents, V_{Ct} is the average series capacitor voltage, V_O is the average output capacitor voltage, L is the inductance, C_t is the series capacitance, C_O is the output capacitance, D is the duty ratio, V_{IN} is the average input voltage, and I_O is the average output current. In steady state, all the time derivatives are set to zero (i.e. the left side of equations (1)-(4) are zero). Then, by equating Equation 1 and Equation 2 and simplifying, the series capacitor voltage in steady state is found to be:

$$V_{Ct} = \frac{V_{IN}}{2} \tag{5}$$

The ideal, steady-state duty ratio is obtained by substituting $V_{IN}/2$ for V_{Ct} in Equation 1 or Equation 2 and simplifying which results in:

$$D = \frac{2V_o}{V_{IN}} \tag{6}$$

This confirms that the duty ratio of the series capacitor buck converter is double that of a conventional buck converter for the same input-to-output voltage conversion ratio.

Because the series capacitor (C_t) is needed in each phase when its high side switch is on, both high side switches cannot be on simultaneously. Hence, the duty cycle is limited to 50%. The converter waveforms are similar to a switched capacitor circuit with a 2:1 conversion ratio followed by a buck converter. This inherent 2:1 step down combined with the 50% duty cycle limitation results in the theoretical maximum output voltage of the converter being limited to $V_{IN}/4$.

The average inductor currents are equal in steady state. This result is obtained by examining Equation 3 with the capacitor voltage time derivative set to zero which simplifies to:

$$I_{LA} = I_{LB} \tag{7}$$

The average inductor currents are matched because the charge balance on the series capacitor is maintained in steady state.

3.3 *Inductor Current Ripple Reduction*

The inductor current waveform in the series capacitor buck is similar to a conventional buck converter. The peak-to-peak current ripple in the series capacitor buck converter is:

$$\Delta i_L = \frac{V_o\left(1-2\dfrac{V_o}{V_{in}}\right)}{Lf_{sw}}$$

(8)

where Δ_{iL} is the peak-to-peak inductor current ripple and f_{sw} is the per phase switching frequency. For comparison, current ripple in a buck converter is:

$$\Delta i_{L,\,buck} = \frac{V_o\left(1-\dfrac{V_o}{V_{in}}\right)}{Lf_{sw}}$$

(9)

The series capacitor buck converter has lower peak-to-peak current ripple than a buck converter for the same voltage conversion ratio, inductance, and switching frequency. The ratio of the inductor ripple is:

$$\frac{\Delta i_L}{\Delta i_{L,Buck}} = \frac{\left(1-2\dfrac{V_o}{V_{in}}\right)}{\left(1-\dfrac{V_o}{V_{in}}\right)}$$

(10)

This ratio demonstrates the reduction of current ripple and is shown as a percent ripple reduction in Figure 11. This property is noteworthy because even meager reductions in inductor current ripple can result in significant savings in core loss. Another approach could be to design for the same inductor current ripple. This would result in lower inductance required in the series capacitor buck converter.
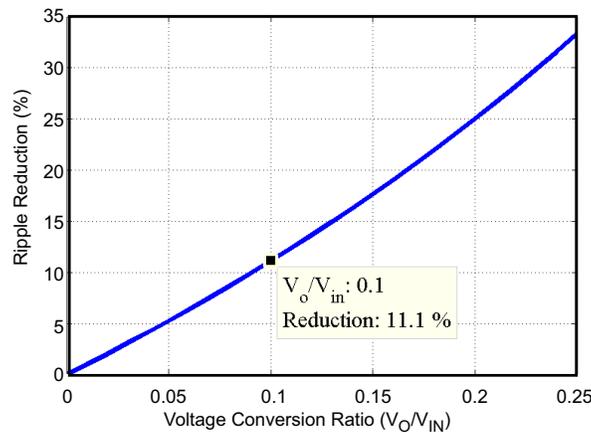
Figure 11. Peak-to-Peak Inductor Current Ripple Reduction

3.4 *Switching Loss Reduction*

Another key benefit of the series capacitor buck converter is reduced switching loss. Reduced voltage during switching reduces switching loss. This is advantageous since loss scales approximately linearly with frequency and quadratically with voltage. Because the series capacitor acts as a dc voltage source with half the input voltage across it, the switch drain-to-source voltage during switching is half of that experienced in a buck converter. This applies to all switches during both turn-on and turn-off in the series capacitor buck converter. Even though Q_{1b} must block the full input voltage when switch Q_{1a} is on, Q_{1b} has only half the input voltage across it during switching. This reduces the loss due to the overlap of switch current and voltage and the switch parasitic output capacitance loss. For example, if a given MOSFET switches at half the typical voltage, a 67% decrease in energy loss due to parasitic output capacitance can be achieved as shown in Figure 12. This graph takes the nonlinear nature of switch output capacitance into account and utilizes measured output capacitance data from TI NexFETs™.
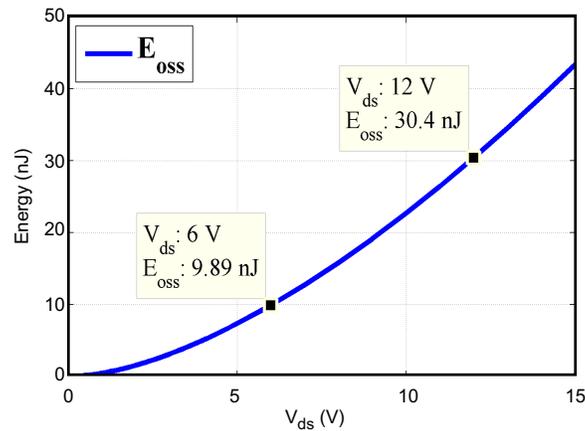
Figure 12. Reduction in Parasitic Capacitance Energy Loss During Switching

3.5 *Automatic Inductor Current Balancing*

A unique feature of the series capacitor buck topology is automatic inductor current balancing. This property is advantageous because accurate current sensing or estimation at high frequency can be challenging. It can eliminate a current sharing control loop that requires high performance circuits to balance phase currents.

Current balancing is achieved because the series capacitor charge must remain balanced (i.e. its average voltage in steady-state is constant). This provides an inherent feedback loop that ensures inductor current balance. If the inductor currents are not equal, the series capacitor voltage would drift up or down because charge balance would not be maintained. Only when charge balance exists does the average capacitor voltage remain constant.

For example, if a scenario exists where the average phase A inductor current is larger than the average phase B inductor current, the average series capacitor voltage would gradually increase. When the series capacitor voltage increases, the average phase A switch node voltage (V_{SWA}) decreases and the average phase B switch node voltage (V_{SWB}) increases. This, in turn, will force the average phase A inductor current to decrease and the average phase B inductor current to increase. The inductor currents eventually reach a level where they are both equal and the capacitor voltage is constant. The converter states are then in equilibrium. This passive correction mechanism also works in the opposite direction if phase B inductor current is larger than phase A inductor current. For a more detailed explanation, refer to Section 6 [6].

Variations in inductance do not impact the average inductor currents or series capacitor voltage. The reason variations in inductance do not negatively impact the current sharing mechanism is because the charge delivered to or removed from the series capacitor does not change with inductance, as shown in Figure 13. The area under the curves (denoted by areas Q_1 and Q_2) represents the charge added or removed from the series capacitor by the inductors. Variations in inductance change the peak-to-peak ripple of the inductor, but the area under the curve (the charge in/out of the series capacitor) does not change.
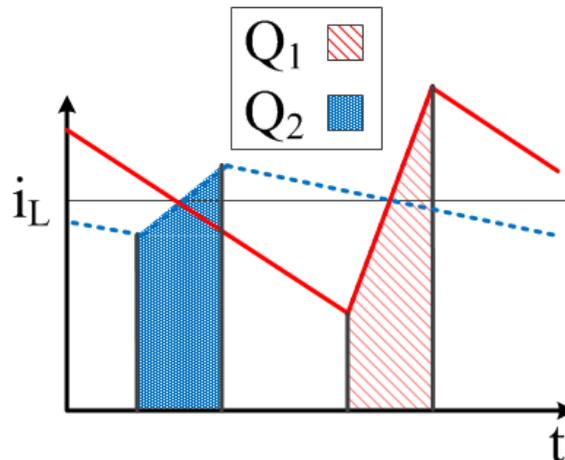

Figure 13. Inductance Variation Impact on Current Sharing

This is an important result because inductors often have up to 20% manufacturing variation in inductance. Inductance variation can also be caused by converter layout and different saturation profiles. This property demonstrates the robustness of the automatic current sharing mechanism.

4   Experimental Results

Sample experimental results are shown in the following sections to highlight the salient features of the series capacitor buck converter. The TPS54A20 integrated circuit was used to design a 12-V input, 1.2-V output voltage regulator with 10-A full load current capability. The converter components and layout are shown in Figure 14. The footprint shown is 15 mm x 14.6 mm, and the height is 1.2 mm. Even smaller footprints are possible with a more optimized layout.
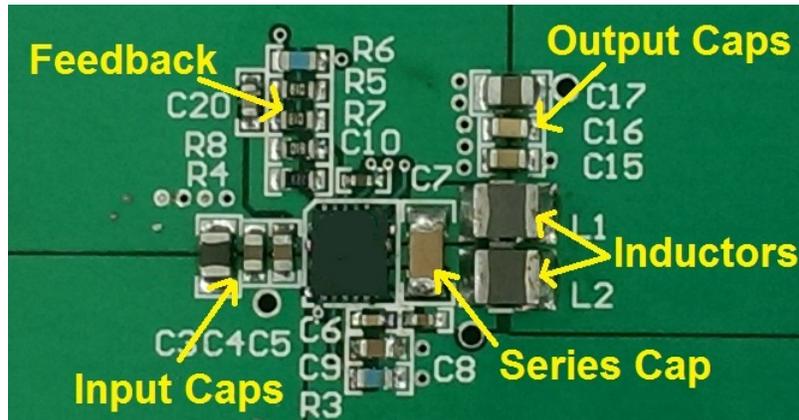

Figure 14. Series Capacitor Buck Converter Prototype Using TPS54A20

4.1   Steady-State Waveforms

The steady-state inductor currents and switch node voltages are shown in Figure 15. The converter is switching at 2 MHz per phase. The switch node voltages rise to approximately half the input voltage (6 V) when the high side switches are on. The inductor currents exhibit even current sharing. The phases are operated with 180 degrees of phase interleaving.
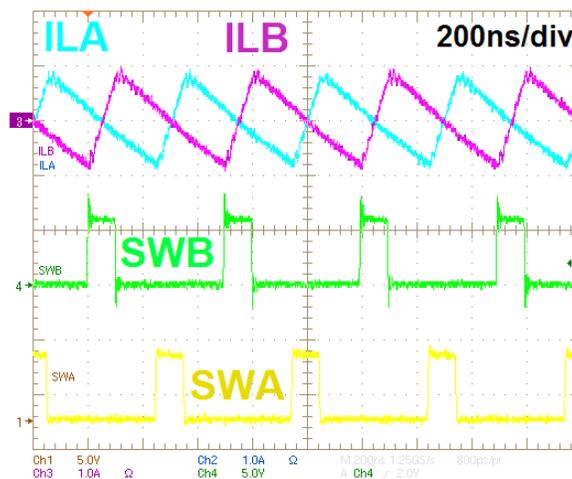
Figure 15. Steady-State Series Capacitor Buck Converter Waveforms

4.2 Efficiency and Power Loss

The prototype's efficiency and power loss graphs are shown in Figure 16 and Figure 17. The efficiency is compared to a 10-A buck converter operating under the same conditions (12-V input, 1.2-V output) with 530-kHz switching frequency. The efficiency of the series capacitor buck converter is higher for most of the load range even though its switching frequency is approximately four times higher. The lower efficiency at full load is attributed to the higher dc resistance in the inductors used in the series capacitor buck converter (9 mΩ vs. 3 mΩ in the buck converter). The buck converter also implements a light load mode that helps to reduce power loss. The series capacitor buck converter operated with forced continuous conduction mode over the load range and had an external supply for the gate driver.

Figure 16. Efficiency vs Output Current

Figure 17. Power Loss vs Output Current
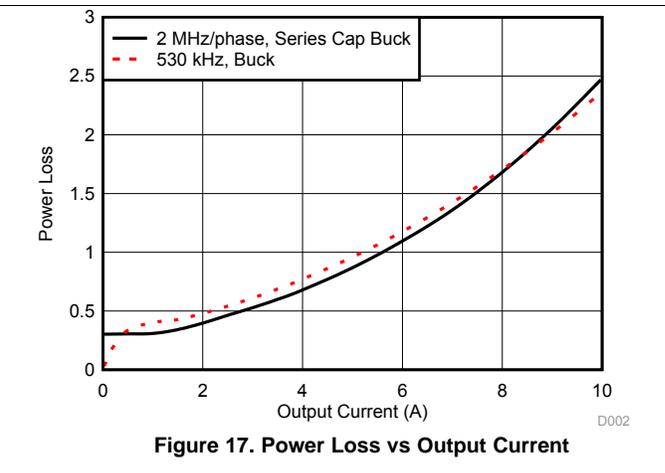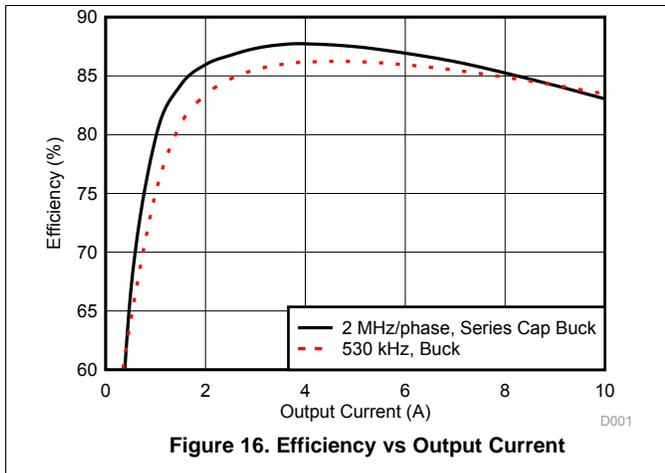
4.3 Load Transient Response

The converter response to 10-A load step up and down transients is shown in Figure 18. The load slew rate is 1 A/µs and the output capacitance is 91 µF. The top trace is the output voltage measured with ac coupling and 20 MHz bandwidth. The bottom two traces are the inductor currents. The output voltage deviation is limited to 50 mV (±4%) with a settling time of approximately 10 µs. Excellent dynamic current sharing between the inductor currents is observed throughout.
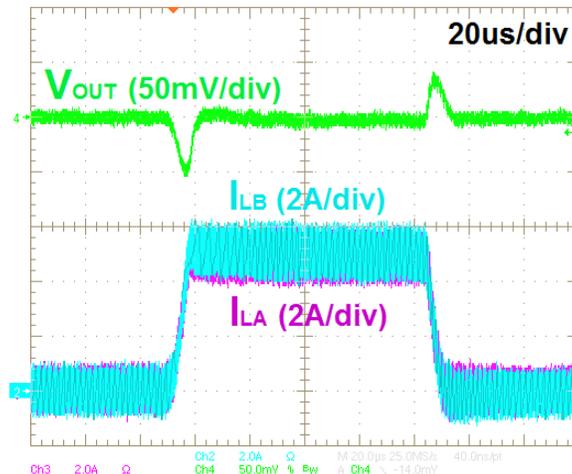
Figure 18. Load Transient Response

4.4 Bode Plot

The stability and small-signal response characteristics of the series capacitor buck converter can be observed from a measured bode plot. The loop response shown in Figure 19 demonstrates a high crossover frequency of 321 kHz and a phase margin of 53.6 degrees. The nominal operating point for this measurement was a 2.5-A load with an output capacitance of 91 µF. Conventional buck converters designed for the same application often have crossover frequencies in the tens of kHz range and require significantly more output capacitance to achieve similar transient response. This result demonstrates the high bandwidth and stable operation of the series capacitor buck converter.
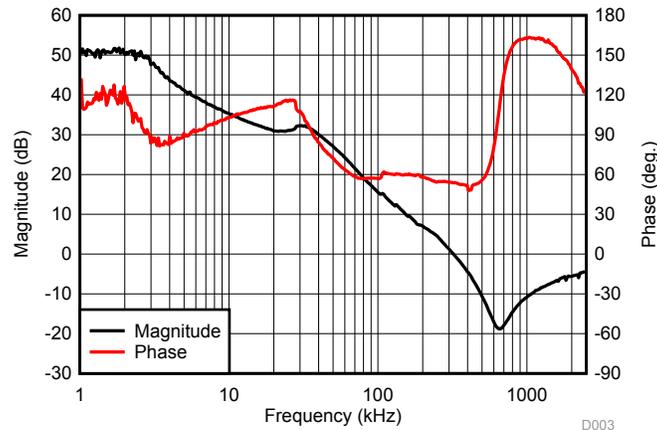
Figure 19. Bode Plot Showing Magnitude and Phase

4.5 Thermal Image

A thermal image of the converter prototype operating at 10 A is shown in Figure 20. The converter is operating at room temperature and no air flow is applied. The TPS54A20 IC has the highest temperature of around 67°C because most of the power loss (heat) is in the IC. The inductors are considerably cooler by comparison. This demonstrates that even though the inductor size has been significantly reduced due to high frequency operation, the converter is not thermally limited by this size reduction.
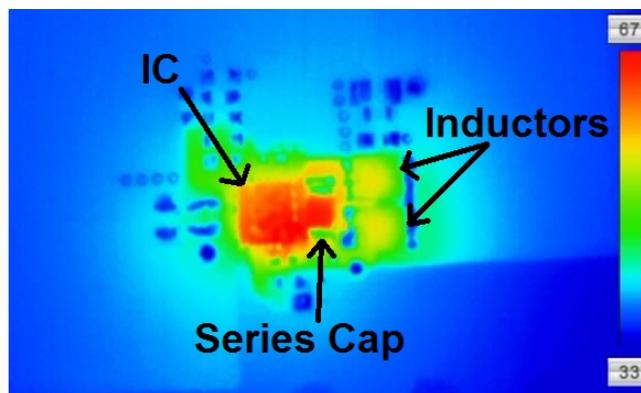
Figure 20. Thermal Image of Converter Prototype Operating at 10 A (Full Load Current)

5 Conclusions

The buck converter has been the workhorse topology for point-of-load dc-dc converter for decades. The buck converter has some fundamental limitations when attempting to operate at high switching frequencies in high conversion ratio applications. The series capacitor buck converter provides an alternate approach that can overcome many of the challenges faced by buck converters. The converter topology has lower switching loss, automatic inductor current balancing, lower peak-to-peak inductor current ripple, and high side switch on-time doubling.

Experimental results demonstrate the benefits of the series capacitor buck converter in a 12-V input, 1.2-V / 10-A output application. Steady-state waveforms show the reduced switch node voltages and inductor current balancing. Efficiency and power loss measurements indicate that the series capacitor buck converter has higher peak efficiency than a conventional buck converter operating at four times lower frequency. Full load transient response with about 50 mV output voltage deviation and excellent dynamic current balancing was observed with only 91 µF of output capacitance. Bode plot measurements reveal high closed loop bandwidth of around 321 kHz with adequate phase margin of 53.6 degrees. Thermal imaging results show that inductor size reduction is possible without being thermally limited.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision **Page**

- Changed Figure 7, L_b To L_a and current direction arrow from left to right ………………………………………………… 5

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