TPS92691/-Q1 Multi-Topology LED Driver With Rail-to-Rail Current Sense Amplifier

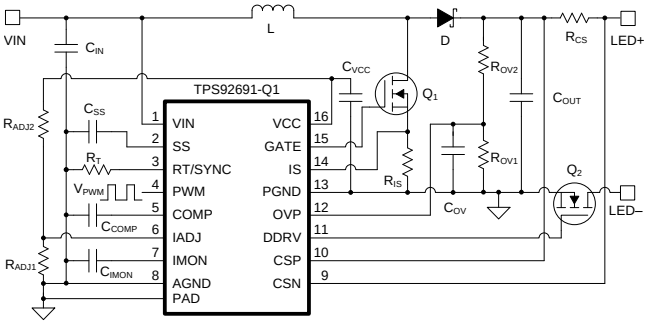
1 Features

- Wide Input Voltage: 4.5 V to 65 V
- Wide Output Voltage Range: 2 V to 65 V
- Low Input Offset Rail-to-Rail Current Sense Amplifier
  - Better than ±3% LED Current Accuracy over 25°C to 140°C Junction Temperature Range
  - Compatible With High-Side and Low-Side Current Sense Implementations
- High-Impedance Analog LED Current Adjust Input (IADJ) With over 15:1 Contrast Ratio
- Over 1000:1 Series FET PWM Dimming Ratio With Integrated Series N-Channel Dim Driver Interface
- Continuous LED Current Monitor Output for System Fault Detection and Diagnoses
- Programmable Switching Frequency With External Clock Synchronization Capability
- Programmable Soft-Start and Slope Compensation
- Comprehensive Fault Protection Circuitry Including VCC Undervoltage Lockout (UVLO), Output Overvoltage Protection (OVP), Cycle-by-Cycle Switch Current Limit, and Thermal Protection
- TPS92691-Q1: Automotive Q100 Grade 1 Qualified

2 Applications

- TPS92691-Q1: Automotive Exterior Lighting Applications
- Architectural and General Lighting Applications

Typical Boost LED Driver Application Schematic



3 Description

The TPS92691/-Q1 is a versatile LED controller that can support a range of step-up or step-down driver topologies. The device implements a fixed-frequency peak current mode control technique with programmable switching frequency, slope compensation, and soft-start timing. It incorporates a high voltage (65-V) rail-to-rail current sense amplifier that can directly measure LED current using either a high-side or a low-side series sense resistor. The amplifier is designed to achieve low input offset voltage and attain better than ±3% LED current accuracy over junction temperature range of 25°C to 140°C and output common-mode voltage range of 0 to 60 V.

LED current can be independently modulated using either analog or PWM dimming techniques. Linear analog dimming response with 15:1 range is obtained by varying the voltage from 140 mV to 2.25 V across the high impedance analog adjust (IADJ) input. PWM dimming of LED current is achieved by modulating the PWM input pin with the desired duty cycle and frequency. Optional DDRV gate driver output can be used to enable series FET dimming functionality to get over 1000:1 contrast ratio.

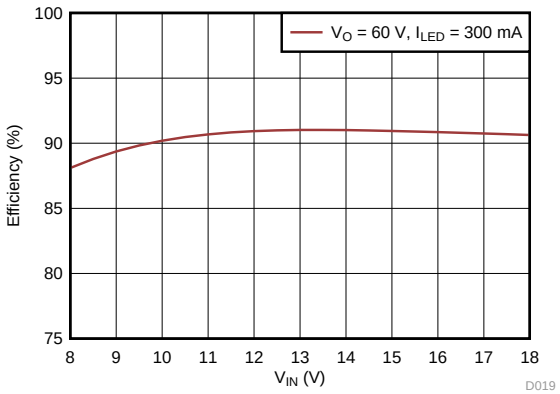
The TPS92691/-Q1 supports continuous LED status check through the current monitor (IMON) output. This allows for LED short circuit or open circuit detection and protection. Additional fault protection features include VCC UVLO, output OVP, switch cycle-by-cycle current limit, and thermal protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92691-Q1 TPS92691	HTSSOP (16)	5.10 mm × 6.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Output Voltage



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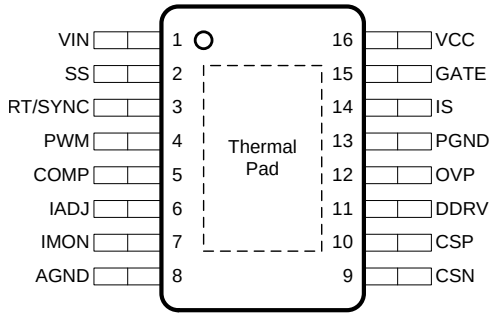
4 Revision History

DATE	REVISION	NOTES
December 2015	*	Initial release.

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP with PowerPAD™
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	—	Input supply for the internal VCC regulator. Bypass with 100-nF capacitor to GND located close to the controller.
2	SS	I/O	Soft-start programming pin. Connect a capacitor to AGND to extend the start-up time. Switching can be disabled by shorting the pin to GND.
3	RT/SYNC	I/O	Oscillator frequency programming pin. Connect a resistor to AGND to set the switching frequency. The internal oscillator can be synchronized by coupling an external clock pulse through 100-nF series capacitor.
4	PWM	I	PWM dimming input. Driving the pin below 2.3 V (typ), turns off switching, idles the oscillator, disconnects the COMP pin, and sets DDRV output to ground. The input signal duty cycle controls the average LED current through PWM dimming operation. Connect to VCC when not used for PWM dimming.
5	COMP	I/O	Transconductance error amplifier output. Connect compensation network to achieve desired closed-loop response.
6	IADJ	I	LED current reference input. Connecting pin to VCC with 100-kΩ series resistor sets internal reference voltage to 2.42 V and the current sense threshold, $V_{(CSP-CSN)}$to 172 mV. The pin can be modulated by external voltage source from 0 V to 2.25 V to implement analog dimming.
7	IMON	O	LED current report pin. The LED current sensed by CSP/CSN input is reported as $V_{IMON} = 14 \times I_{LED} \times R_{cs}$. Bypass with a 1-nF ceramic capacitor to AGND.
8	AGND	—	Analog ground. Return for the internal voltage reference and analog circuit. Connect to circuit ground, GND, to complete return path.
9	CSN	I	Current sense amplifier negative input (–). Connect directly to the negative node of LED current sense resistor R_{CS}).
10	CSP	I	Current sense amplifier positive input (+). Connect directly to the positive node of LED current sense resistor R_{CS}).
11	DDRV	O	Series dimming FET gate driver output. Connect to gate of external N-channel MOSFET or a level-shift circuit with P-channel MOSFET to implement series FET PWM dimming.
12	OVP	I	Hysteretic overvoltage protection input. Connect resistor divider from output voltage to set OVP threshold and hysteresis.
13	PGND	—	Power ground connection pin for internal N-channel MOSFET gate drivers. Connect to circuit ground, GND, to complete return path.
14	IS	I	Switch current sense input. Connected to the switch current sense resistor, R_{IS}, in the source of the N-channel MOSFET.
15	GATE	O	N-channel MOSFET gate driver output. Connect to gate of external switching N-channel MOSFET.
16	VCC	—	VCC bias supply pin. Locally decouple to PGND using a 2.2-µF to 4.7-µF ceramic capacitor located close to the controller.
PowerPAD		—	The AGND and PGND pin must be connected to the exposed PowerPAD for proper operation. This PowerPAD must be connected to PCB ground plane using multiple vias for good thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage	VIN, CSP, CSN	–0.3	65	V
	IADJ, IS, PWM, RT/SYNC	–0.3	8.8	V
	OVP, SS	–0.3	5.5	V
	CSP to CSN(3), PGND	–0.3	0.3	V
Output voltage(4)	VCC, GATE, DDRV	–0.3	8.8	V
	COMP	–0.3	5.0	V
Source current	IMON	—	100	µA
	GATE, DDRV (Pulsed <20 ns)	—	500	mA
Sink current	GATE, DDRV (Pulsed <20 ns)	—	500	mA
Operating junction temperature, T_J		–40	140	°C
Storage temperature, T_{stg}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to AGND unless otherwise noted
(3) Continuous sustaining voltage
(4) All output pins are not specified to have an external voltage applied.

6.2 ESD Ratings

				VALUE	UNIT
TPS92691-Q1 IN PWP (HTSSOP) PACKAGE					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, all pins(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins except 1, 8, 9, and 16	±500	
			Pins 1, 8, 9, and 16	±750	
TPS92691 IN PWP (HTSSOP) PACKAGE					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(3)		±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	6.5	14	65	V
VIN, crank	Supply input, battery crank voltage	4.5			V
V_{CSP}, V_{CSN}	Current sense common mode	0		60	V
f_{SW}	Switching frequency	80		700	kHz
f_{SYNC}	SYNC frequency	0.8 × f_{sw}		1.2 × f_{SW}	kHz
V_{IADJ}	Current reference voltage	0.14		$V_{IADJ(CLAMP)}$	V
T_A	Operating ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS92691/-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 140°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
V_{DO}	LDO dropout voltage	I_{CC} = 20 mA, V_{IN} = 5 V		300		mV
BIAS SUPPLY (VCC)						
$V_{CC(REG)}$	Regulation voltage	No load	7.0	7.5	8.0	V
$V_{CC(UVLO)}$	Supply undervoltage protection	VCC rising threshold, V_{IN} = 8 V		4.1	4.35	V
		VCC falling threshold, V_{IN} = 8 V	3.75	4.0		V
		Hysteresis		100		mV
$I_{CC(LIMIT)}$	Supply current limit	V_{CC} = 0 V	26	38	46	mA
$I_{CC(STBY)}$	Supply stand-by current	V_{PWM} = 0 V		1.8	2.1	mA
$I_{CC(SW)}$	Supply switching current	V_{CC} = 7.5 V, C_{GATE} = 1 nF		5.1	6.6	mA
OSCILLATOR (RT/SYNC)						
f_{SW}	Switching frequency	R_T = 40 kΩ	165	200	230	kHz
		R_T = 20 kΩ	327	390	448	kHz
V_{RT}	RT output voltage			1		V
V_{SYNC}	SYNC rising threshold	$V_{RT/SYNC}$ rising		2.7	3.1	V
	SYNC falling threshold	$V_{RT/SYNC}$ falling	1.8	2		V
$t_{SYNC(MIN)}$	Minimum SYNC clock pulse width			100		ns
GATE DRIVER (GATE)						
R_{GH}	Gate driver high side resistance	I_{GATE} = –10 mA		5.4	11.2	Ω
R_{GL}	Gate driver low side resistance	I_{GATE} = 10 mA		4.3	10.5	Ω
CURRENT SENSE (IS)						
$V_{IS(LIMIT)}$	Current limit threshold		497	525	550	mV
$t_{IS(BLANK)}$	Leading edge blanking time		103	150	188	ns
$t_{IS(FAULT)}$	Current limit fault time			35		µs
$t_{ILMT(DLY)}$	IS to GATE propagation delay	V_{IS} pulsed from 0 to 1 V		100		ns
PWM COMPARATOR AND SLOPE COMPENSATION						
D_{MAX}	Maximum duty cycle		90.4%	93%	94.7%	
V_{LV}	IS to COMP level shift voltage	No slope compensation added	1.17	1.5	1.8	V
V_{SL}	Slope compensation	D = D_{MAX} (with max slope compensation)		200		mV
I_{LV}	IS level shift bias current	No slope compensation added		25		µA

(1) All voltages are with respect to AGND unless otherwise noted

Electrical Characteristics (continued)

T_J = –40°C to 140°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LV} + I_{SL}	IS level shift source current	D = D_{MAX} (with max slope compensation)		115		µA
CURRENT SENSE AMPLIFIER (CSP, CSN)						
$V_{CS(offset)}$	Cumulative offset voltage at V_{CSP} = 60 V and $V_{(CSP-CSN)}$ = 150 mV, referred to current sense input	–40°C ≤ T_J ≤ 140°C	–5.2		5.9	mV
		25°C ≤ T_J ≤ 140°C	–4.4		4.6	mV
	Cumulative offset voltage at V_{CSP} = 60 V and $V_{(CSP-CSN)}$ = 10 mV, referred to current sense input	–40°C ≤ T_J ≤ 140°C	–3.5		5.0	mV
		25°C ≤ T_J ≤ 140°C	-2.8		4.0	mV
	Cumulative offset voltage at V_{CSN} = 0 V and $V_{(CSP-CSN)}$ = 150 mV, referred to current sense input	–40°C ≤ T_J ≤ 140°C	–5.9		6.7	mV
		25°C ≤ T_J ≤ 140°C	-4.7		5.0	mV
	Cumulative offset voltage at V_{CSN} = 0 V and $V_{(CSP-CSN)}$ = 10 mV, referred to current sense input	–40°C ≤ T_J ≤ 140°C	–2.3		3.2	mV
		25°C ≤ T_J ≤ 140°C	–1.7		2.6	mV
$CS_{(BW)}$	Current sense unity gain bandwidth			500		kHz
$I_{CS(BIAS)}$	CSP, CSN bias current	$V_{CSP, CSN}$ = 60 V		4		µA
CURRENT MONITOR (IMON)						
$V_{IMON(CLP)}$	IMON output voltage clamp		3.2	3.7	4.2	V
$V_{IMON(OS)}$	IMON buffer offset voltage		–11.4	–1.6	7.3	mV
ANALOG ADJUST (IADJ)						
$V_{IADJ(CLP)}$	IADJ internal clamp voltage	I_{IADJ} = 1 µA	2.27	2.42	2.55	V
$I_{IADJ(BIAS)}$	IADJ input bias current	V_{IADJ} < 2.2 V			90	nA
$R_{IADJ(LMT)}$	IADJ current limiting series resistor	V_{IADJ} > 2.6 V		12		kΩ
ERROR AMPLIFIER (COMP)						
g_M	Transconductance			121		µA/V
$I_{COMP(SRC)}$	COMP current source capacity	V_{IADJ} = 1.4 V, $V_{(CSP-CSN)}$ = 0 V		130		µA
$I_{COMP(SINK)}$	COMP current sink capacity	V_{IADJ} = 0 V, $V_{(CSP-CSN)}$ = 0.1 V		130		µA
$EA_{(BW)}$	Error amplifier bandwidth	–3 dB		5		MHz
$V_{COMP(RST)}$	COMP pin reset voltage			100		mV
$R_{COMP(DCH)}$	COMP discharge FET resistance			246		Ω
SOFT-START (SS)						
I_{SS}	Soft-start source current		7	10	12.8	µA
$V_{SS(RST)}$	Soft-start pin reset voltage			25		mV
$R_{SS(DCH)}$	SS discharge FET resistance			260		Ω
OVERVOLTAGE PROTECTION (OVP)						
$V_{OVP(THR)}$	OVP detection threshold		1.18	1.24	1.31	V
$I_{OVP(HYS)}$	OVP hysteresis current		12	20	27.5	µA
PWM INPUT (PWM)						
$V_{PWM(HIGH)}$	Schmitt trigger logic level (high threshold)			2.5	2.7	V
$V_{PWM(LOW)}$	Schmitt trigger logic level (low threshold)		2.0	2.3		V
$R_{PWM(PD)}$	PWM pulldown resistance			1		MΩ
$t_{DLY(RISE)}$	PWM to DDRV rising delay			54		ns
$t_{DLY(FALL)}$	PWM to DDRV falling delay			72		ns
PWM GATE DRIVE OUTPUT (DDRV)						
R_{DH}	DDRV high-side resistance			6.1	12.8	Ω
R_{DL}	DDRV low-side resistance			5.2	11.4	Ω

Electrical Characteristics (continued)

T_J = –40°C to 140°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown temperature			175		°C
Thermal shutdown hysteresis			25		°C

6.6 Typical Characteristics

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)

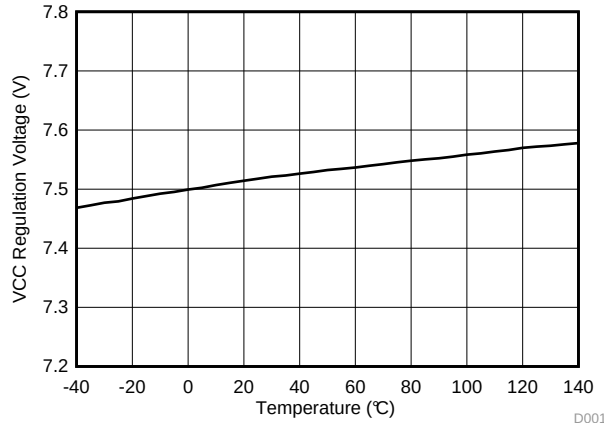


Figure 1. VCC Regulation Voltage vs Temperature

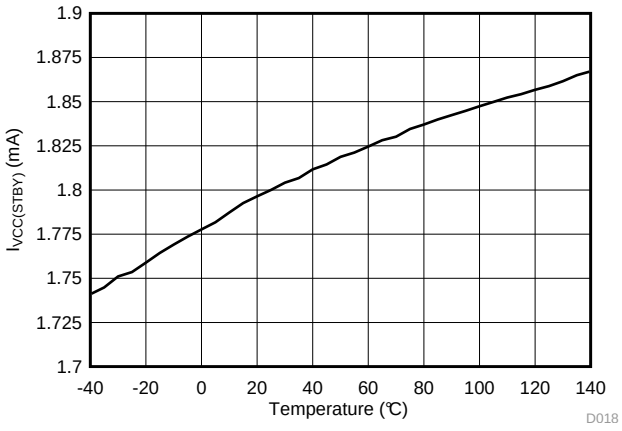


Figure 2. Standby Current vs Temperature

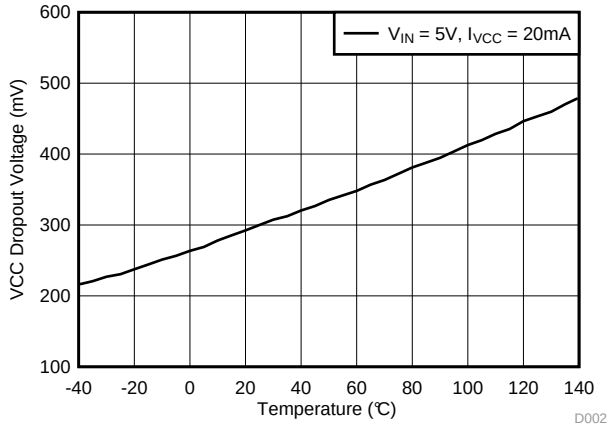


Figure 3. VCC Dropout Voltage vs Temperature

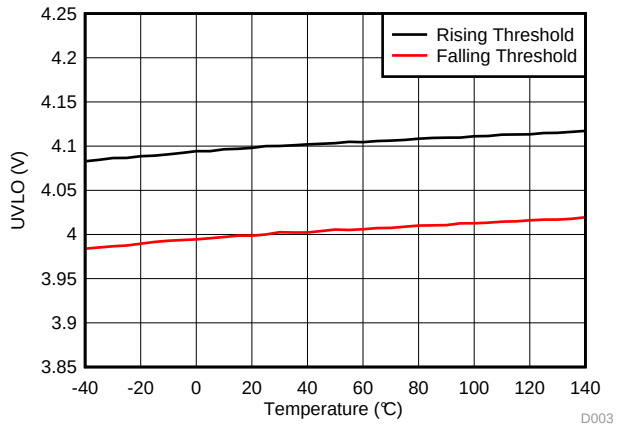


Figure 4. UVLO Threshold vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)

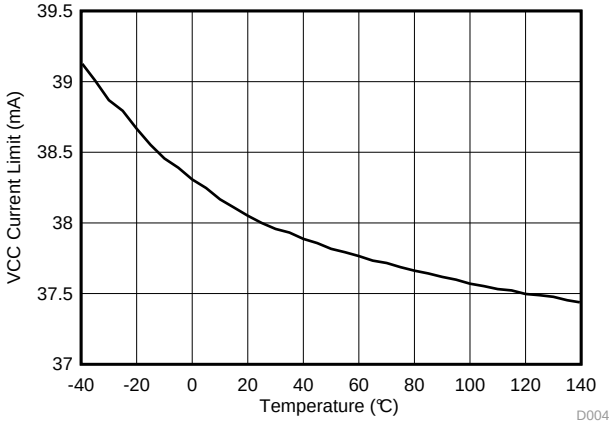


Figure 5. VCC Current Limit vs Temperature

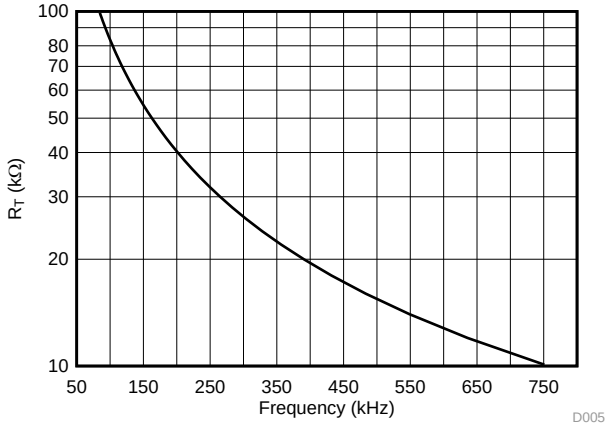


Figure 6. R_T vs Switching Frequency

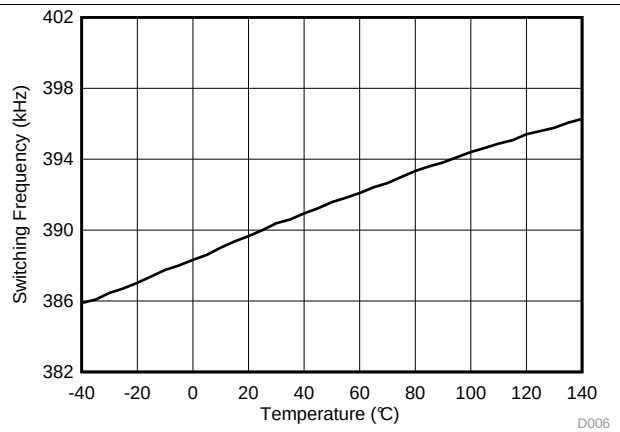


Figure 7. Switching Frequency vs Temperature

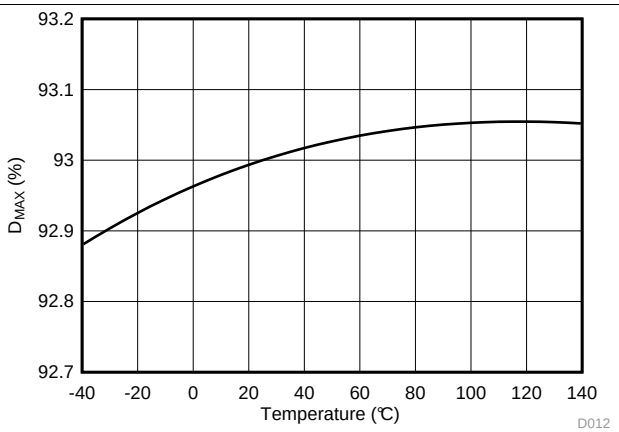


Figure 8. Maximum Duty Cycle vs Temperature

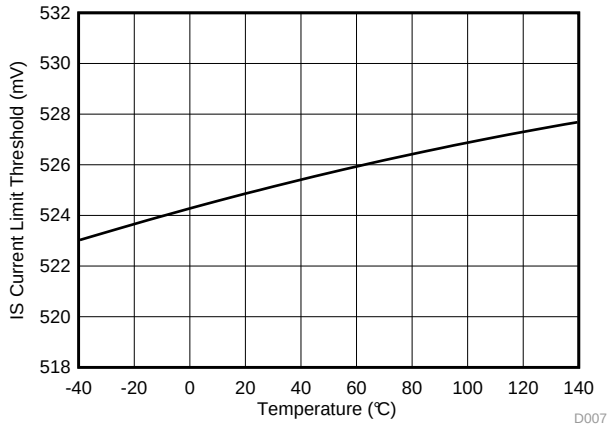


Figure 9. IS Current Limit Threshold vs Temperature

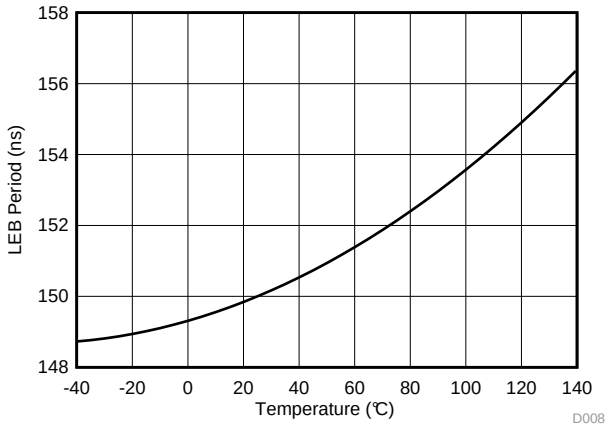
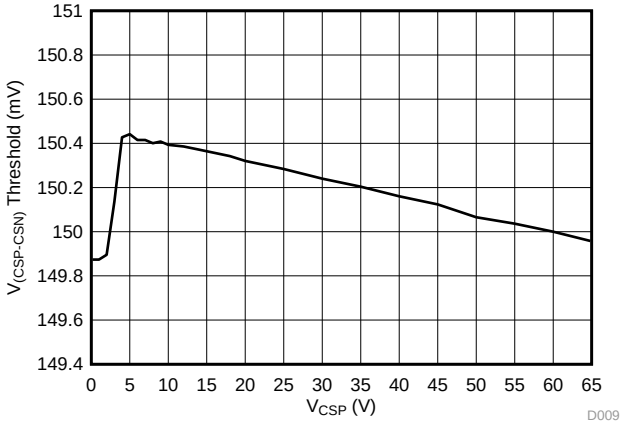


Figure 10. Leading Edge Blanking Period vs Temperature

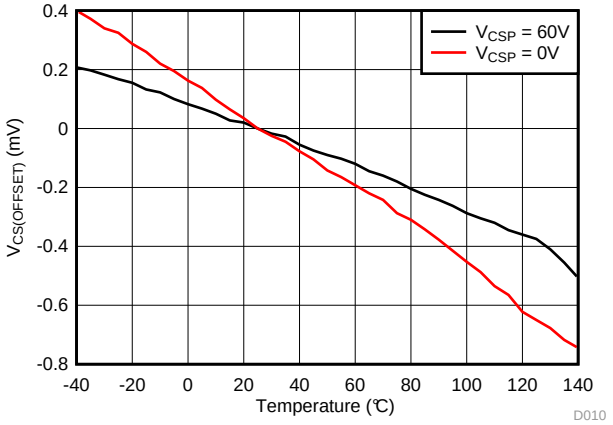
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)



V_{IADJ} = 2.1 V

Figure 11. $V_{(CSP-CSN)}$ Threshold vs V_{CSP}



V_{IADJ} = 2.1 V

Figure 12. Current Sense Amplifier Offset vs Temperature

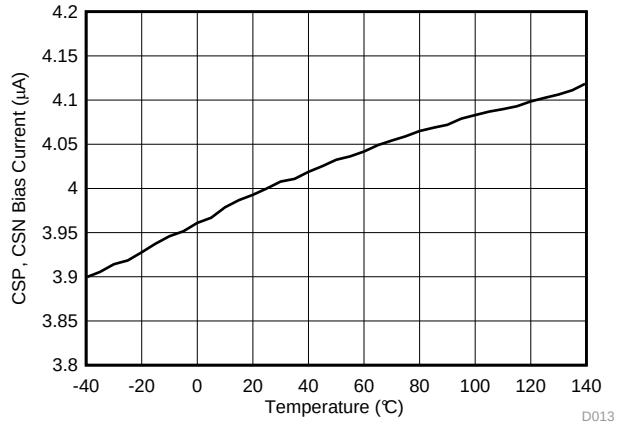


Figure 13. CSP/CSN Input Bias Current vs Temperature

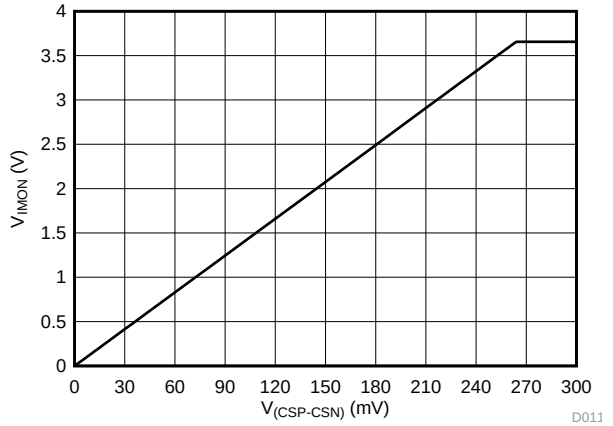


Figure 14. V_{IMON} vs $V_{(CSP-CSN)}$

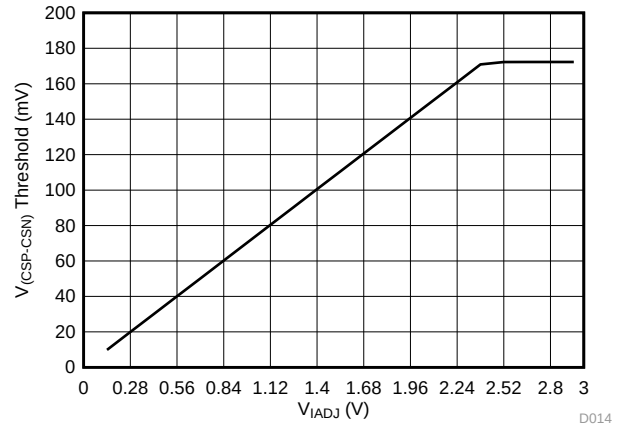


Figure 15. $V_{(CSP-CSN)}$ Threshold vs V_{IADJ}

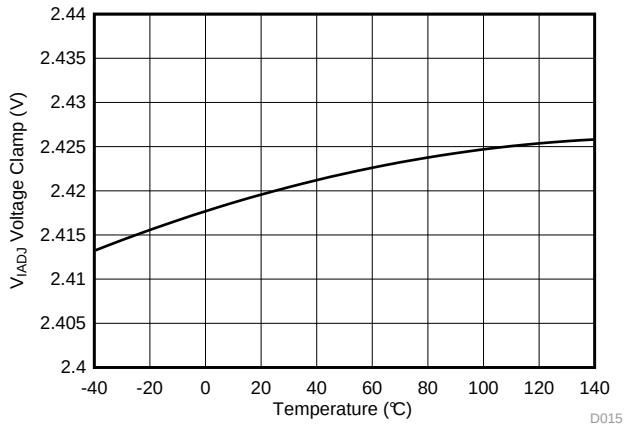


Figure 16. V_{IADJ} Voltage Clamp vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 14 V, V_{IADJ} = 2.2 V, C_{VCC} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, V_{PWM} = 5 V, no load on GATE and DDRV (unless otherwise noted)

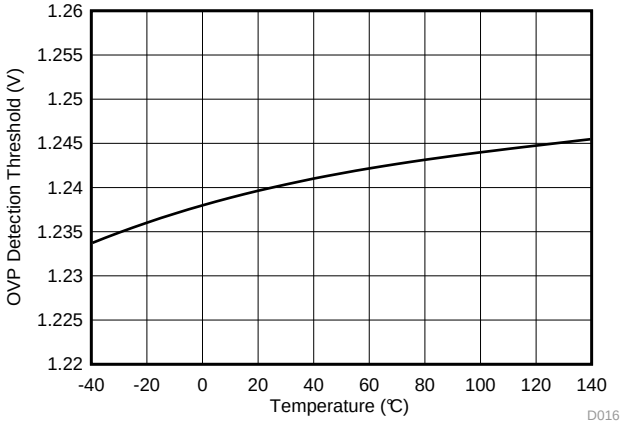


Figure 17. OVP Detection Threshold vs Temperature

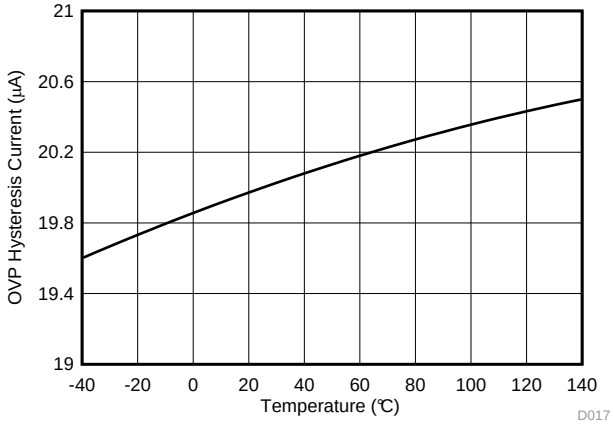


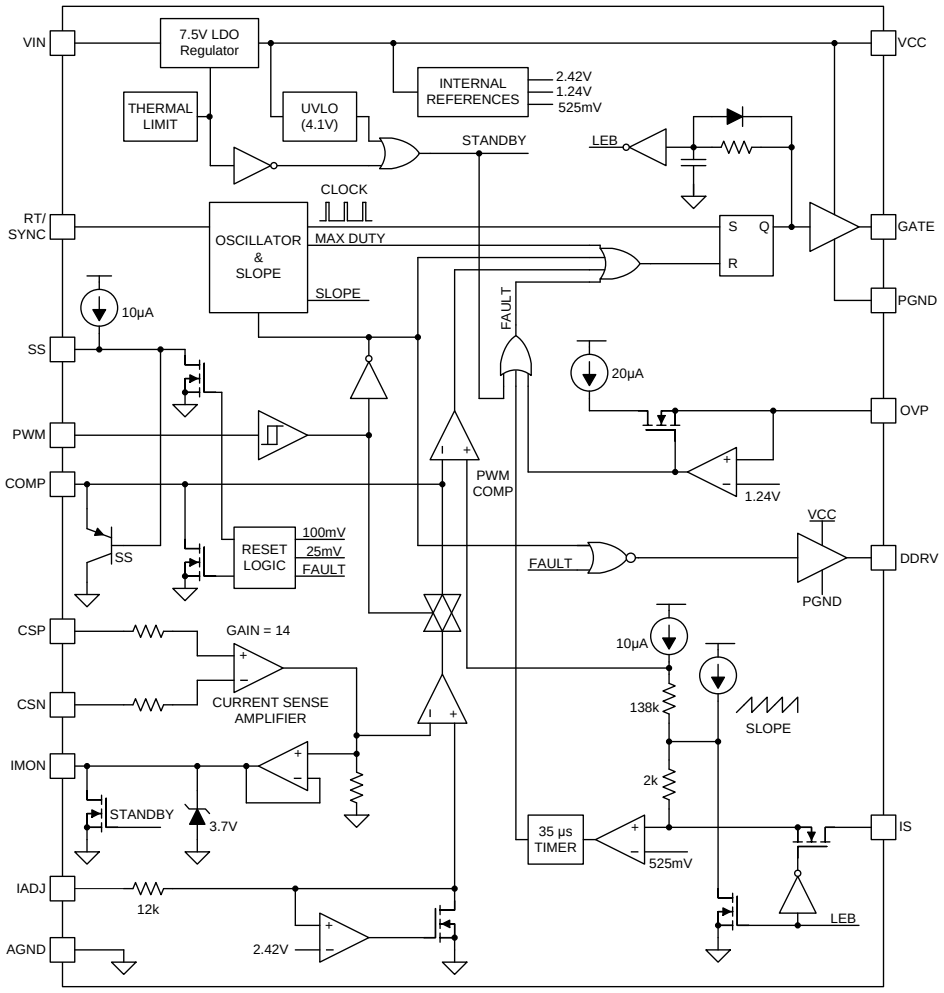
Figure 18. OVP Hysteresis Current vs Temperature

7 Detailed Description

7.1 Overview

The TPS92691/-Q1 wide input range (4.5 V to 65 V) controller features all of the functions necessary to implement a highly efficient and compact LED driver based on step-up or step-down converter topologies. The device implements a fixed-frequency, peak current mode control technique to achieve a constant current output, ideal for driving a single string of series-connected LEDs. The integrated low input offset, rail-to-rail current sense amplifier supports a wide range of output voltages (0 V to 65 V) and is capable of powering an LED string consisting of 1 to more than 20 white LEDs. The controller is compatible with either high- or low-side current shunt sensing technique, based on the LED configuration and driver topology. The LED current sense threshold, set by the analog adjust input, IADJ, provides the capability to analog (amplitude) dim over a linear range of 15:1 by varying the voltage, V_{IADJ}, from 140 mV to 2.25 V. The IADJ input provides the means to externally program LED current and facilitates calibration, brightness correction, and thermal management of the LEDs. High resolution and linear dimming response is achieved by varying the duty cycle of LED current based on the PWM input. The PWM input directly controls the GATE and DDRV drive outputs, controls the internal oscillator, and enables high-speed PWM dimming with over 1000:1 contrast ratio when using an external MOSFET placed in series with the LED load. The current monitor output, IMON, reports the instantaneous status of LED current measured by the rail-to-rail current sense amplifier. This feature is incorporated to indicate LED short and open-circuit failures and enables cable harness fault detection independent of LED driver topology. Other fault protection features include cycle-by-cycle current limiting, hysteresis-based overvoltage protection, VCC undervoltage protection, thermal shutdown, and remote shutdown capability by pulling down the SS pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Regulator and Undervoltage Lockout (UVLO)

The IC incorporates a 65-V input V_{IN} rated linear regulator to generate the 7.5 V (typ) V_{CC} bias supply and other internal reference voltages. The V_{CC} output is monitored to implement UVLO protection. The device is enabled when V_{CC} exceeds the 4.1-V (typ) threshold and is disabled when V_{CC} drops below the 4.0-V (typ) threshold. The UVLO comparator provides 0.1 V of hysteresis to avoid chatter during transitions. The UVLO thresholds are internally fixed and cannot be adjusted. The supply current, I_{CC}, is limited to 26 mA minimum to protect the device under VCC pin short-circuit conditions. The V_{CC} supply powers the internal circuitry and N-channel gate driver outputs, GATE, and DDRV. Place a bypass capacitor in the range of 2.2 µF to 4.7 µF across the V_{CC} output and PGND to ensure proper operation. The regulator operates in dropout when input voltage V_{IN} falls below 7.5 V forcing V_{CC} to be lower than V_{IN} by 300 mV for a 20-mA supply current. The V_{CC} is a regulated output of the internal regulator and is not recommended to be driven from an external power supply.

7.3.2 Oscillator

The TPS92691/-Q1 switching frequency is programmable by a single external resistor connected between the RT/SYNC pin and the AGND pin. To set a desired frequency, f_{SW} (Hz), the resistor value can be calculated from Equation 1.

$$R_T = \frac{1.432 \times 10^{10}}{(f_{SW})^{1.047}} \ (\Omega) \quad (1)$$

Figure 6 shows a graph of switching frequency versus resistance, R_T. TI recommends a switching frequency setting between 80 kHz and 700 kHz for optimal performance over input and output voltage operating range and for best efficiency. Operation at higher switching frequencies requires careful selection of N-channel MOSFET characteristics and should take into consideration additional switching losses and junction temperature rise.

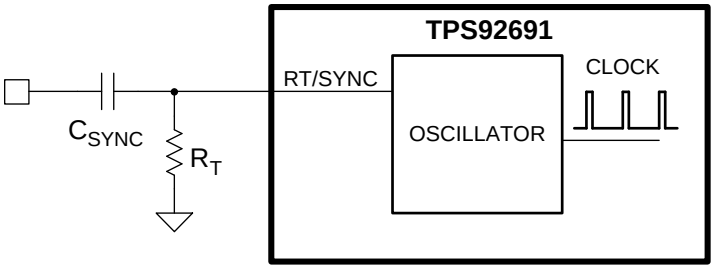


Figure 19. Oscillator Synchronization Through AC Coupling

The internal oscillator can be synchronized by AC coupling an external clock pulse to RT/SYNC pin as shown in Figure 19. The positive going synchronization clock at the RT pin must exceed the RT sync threshold and the negative going synchronization clock at the RT pin must exceed the RT sync falling threshold to trip the internal synchronization pulse detector. TI recommends that the frequency of the external synchronization pulse is within ±20% of the internal oscillator frequency programmed by the R_T resistor. TI recommends a minimum coupling capacitor of 100 nF and typical pulse width of 100 ns for proper synchronization. In the case where external synchronization clock is lost the internal oscillator takes control of the switching rate based on the R_T resistor to maintain output current regulation. The R_T resistor is always required whether the oscillator is free running or externally synchronized.

7.3.3 Gate Driver

The TPS92691/-Q1 contains a N-channel gate driver that switches the output V_{GATE} between V_{CC} and PGND. A peak source and sink current of 500 mA allows controlled slew-rate of the MOSFET gate and drain node voltages, limiting the conducted and radiated EMI generated by switching. The gate driver supply current $I_{CC(GATE)}$ depends on the total gate drive charge (Q_G) of the MOSFET and the operating frequency of the converter, f_{SW}, $I_{CC(GATE)} = Q_G \times f_{SW}$. TI recommends a MOSFET with a low gate charge specification to limit the junction temperature rise and switch transition losses.

Feature Description (continued)

While choosing the N-channel MOSFET device, consider the threshold voltage when operating in the dropout region when V_{IN} is below the V_{CC} regulation level. TI recommends a logic level device with a threshold voltage below 5 V when the device is required to operate at an input voltage less than 7 V.

7.3.4 Rail-to-Rail Current Sense Amplifier

The internal rail-to-rail current sense amplifier measures the average LED current based on the differential voltage drop between the CSP and CSN inputs over a common mode range of 0 V to 65 V. The differential voltage, $V_{(CSP-CSN)}$, is amplified by a voltage-gain factor of 14 and is connected to the negative input of the transconductance error amplifier. Accurate LED current feedback is achieved by limiting the cumulative input offset voltage, (represented by the sum of the voltage-gain error, the intrinsic current sense offset voltage, and the transconductance error amplifier offset voltage) to less than 5 mV over the recommended common-mode voltage, and temperature range.

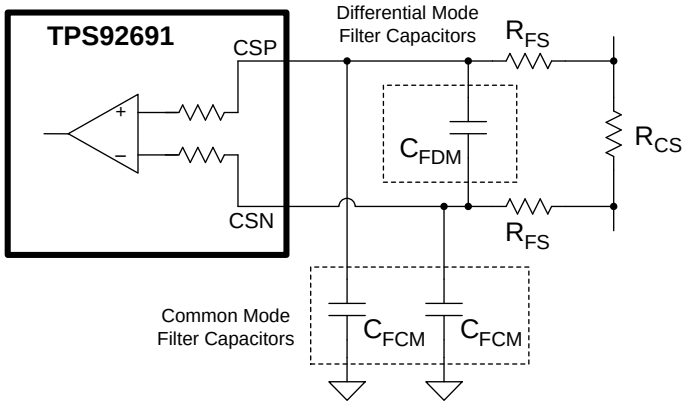


Figure 20. Current Sense Amplifier Input Filter Options

An optional common-mode or differential mode low-pass filter implementation, as shown in Figure 20, can be used to smooth out the effects of large output current ripple and switching current spikes caused by diode reverse recovery. TI recommends a filter resistance in the range of 10 Ω to 100 Ω to limit the additional offset caused by amplifier bias current and achieve best accuracy and line regulation.

7.3.5 Transconductance Error Amplifier

The internal transconductance amplifier generates an error signal proportional to the difference between the LED current sense feedback voltage and the external IADJ input voltage. Closed-loop regulation is achieved by connecting a compensation network to the output of the error amplifier. In most LED driver applications, a stable response can be achieved by connecting a capacitor across the COMP output and ground to implement a simple integral compensator. TI recommends a capacitor value between 10 nF and 100 nF as a good starting point. Higher closed-loop bandwidth can be achieved by implementing a proportional-integral compensator consisting of a series resistor and a capacitor network connected across the COMP output and ground. Based on the converter topology, the compensation network should be tuned to achieve a minimum of 60° of phase margin and 10 dB of gain margin. The *Application and Implementation* section presents detailed equations.

7.3.6 Switch Current Sense and Internal Slope Compensation

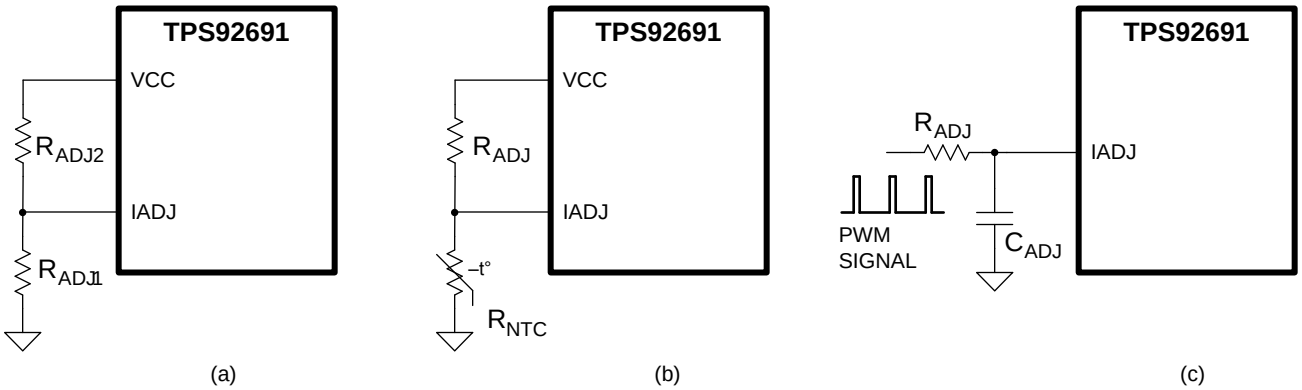
The main MOSFET current is monitored by the IS input pin to implement peak current mode control. The GATE output duty cycle is derived by comparing the peak switch current, measured by the R_{IS} resistor, to the internal COMP voltage threshold. An internal slope signal is added to the measured sense voltage, V_{IS}, to prevent subharmonic oscillations for duty cycles greater than 50%. The linear slope voltage, V_{SL}, of fixed amplitude 200 mV, is derived from a 100-µA sawtooth ramp current synchronized to the internal oscillator frequency. An internal blanking circuit prevents MOSFET switching current spike propagation and premature termination of duty cycle by internally shunting the IS input for 150 ns after the beginning of the new switching period. TI recommends an external low-pass RC filter with resistor values ranging from 100 Ω to 500 Ω for additional noise suppression when operating in the dropout region (V_{IN} less than 7 V).

Feature Description (continued)

Cycle-by-cycle current limit is accomplished by a redundant internal comparator, which immediately terminates the GATE output when the IS input voltage, V_{IS}, exceeds 525-mV (typ) threshold. Upon a current limit event, the SS and COMP pin are internally grounded to reset the state of the controller. The GATE output is enabled after the expiration of the 35-µs internal fault timer and a new start-up sequence is initiated through the SS pin.

7.3.7 Analog Adjust Input

The voltage across the LED current sense resistor, $V_{(CSP–CSN)}$, is regulated to the analog adjust input voltage, V_{IADJ}, scaled by the current sense amplifier voltage gain of 14. The LED current can be linearly adjusted by varying the voltage on IADJ from 140 mV to 2.25 V using either a resistor divider from V_{CC} or a voltage source. The IADJ pin can be connected to V_{CC} through an external resistor to set LED current based on the 2.42-V internal reference voltage. Figure 21 shows different methods to set the IADJ voltage. The IADJ input can be used in conjunction with a NTC resistor to implement thermal foldback protection as shown in Figure 21(b). A PWM signal in conjunction with first- or second-order low-pass filter can be used to program the IADJ voltage as shown in Figure 21(c).



a. Static reference setting resistor divider from VCC
b. Thermal fold-back circuit using external NTC resistor
c. Analog dimming achieved by low-pass filtering external PWM signal

Figure 21. Setting Analog Adjust Input Voltage

7.3.8 PWM Input and Series Dimming FET Gate Driver Output

The TPS92691/-Q1 incorporates a dimming input (PWM) for pulse-width modulating the output LED current. The brightness of the LEDs can be linearly varied by modulating the duty cycle of the pulsating voltage source connected to the PWM input pin. Driving the PWM input below 2.3 V (typ) turns off switching, parks the oscillator, disconnects the COMP pin, and sets the DDRV output to GND in order to maintain the charge on the compensation network and output capacitors. On the rising edge of the PWM input voltage (V_{PWM} > 2.5 V), the GATE and DDRV outputs are enabled to ramp the inductor current to the previous steady-state value. The COMP pin is connected and the error amplifier and oscillator are enabled only when the switch current sense voltage V_{IS} exceeds the COMP voltage, V_{COMP}, thus immediately forcing the converter into steady-state operation with minimum LED current overshoot. The PWM pin should be connected to the V_{CC} if dimming is not required. An internal pulldown resistor sets the input to logic-low and disables the part when the pin is disconnected or left floating.

Feature Description (continued)

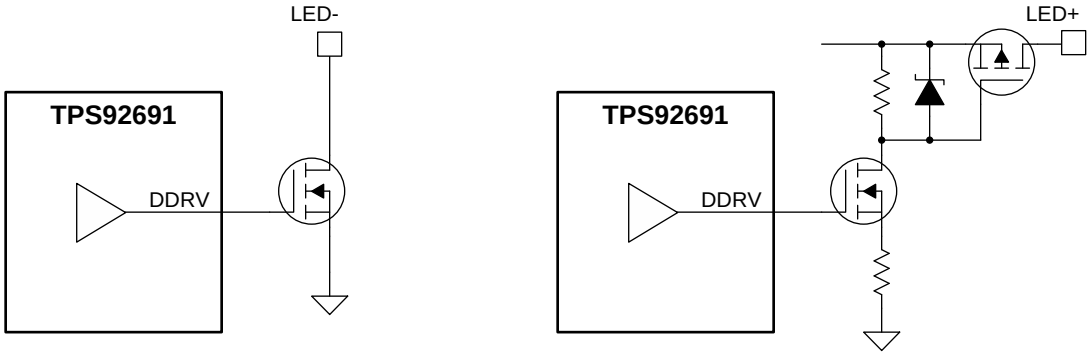


Figure 22. Series Dimming FET Connections

The DDRV output follows the PWM input signal and is capable of sinking and sourcing up to 500 mA of peak current to control a low-side series connected N-channel dimming FET. Alternatively, the DDRV output can be translated with an external level-shift circuit to drive a high-side series P-channel dimming FET as shown in Figure 22. The series dimming FET is required to achieve high contrast ratio as it ensures fast rise and fall times of the LED current in response to the PWM input. Without any dimming FET, the rise and fall times are limited by the inductor slew rate and the closed-loop bandwidth of the system. Leave the DDRV pin unconnected if not used.

7.3.9 Soft-Start

The soft-start feature helps the regulator gradually reach the steady-state operating point, thus reducing startup stresses and surges. The TPS92691/-Q1 clamps the COMP pin to the SS pin, separated by a diode, until LED current nears the regulation threshold. The internal 10-µA soft-start current source gradually increases the voltage on an external soft-start capacitor C_{SS} connected to the SS pin. This results in a gradual rise of the COMP voltage from GND.

The internal 10-µA current source turns on when VCC exceeds the UVLO threshold. At the beginning of the soft-start sequence, the SS pulldown switch is active and is released when the voltage V_{SS} drops below 25 mV. The SS pin can also be pulled down by an external switch to stop switching. When the SS pin is externally driven to enable switching, the slew-rate on the COMP pin should be controlled by choosing a compensation capacitor that avoids large startup transients. The value of C_{SS} should be large enough to charge the output capacitor during the soft-start transition period.

7.3.10 Current Monitor Output

The IMON pin voltage represents the LED current measured by the rail-to-rail current sense amplifier across the external current shunt resistor. The linear relationship between the IMON voltage and LED current includes the amplifier gain-factor of 14 (see Figure 14). The IMON output can be connected to an external microcontroller or comparator to facilitate LED open, short, or cable harness fault detection and mitigation based on programmable threshold V_{OCTH}. The IMON voltage is internally clamped to 3.7 V.

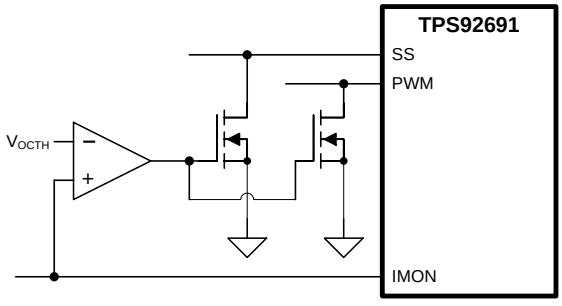


Figure 23. LED Overcurrent Protection using IMON Output

Feature Description (continued)

7.3.11 Overvoltage Protection

The TPS92691/-Q1 device includes a dedicated OVP pin which can be used for either input or output overvoltage protection. This pin features a precision 1.24 V (typ) threshold with 20-µA (typ) of hysteresis current. The overvoltage threshold limit is set by a resistor divider network from the input or output terminal to GND. When the OVP pin voltage exceeds the reference threshold, the GATE and DDRV pins are immediately pulled low and the SS and COMP capacitors are discharged. The GATE is enabled and a new startup sequence is initiated after the voltage drops below the hysteresis threshold set by the 20-µA source current and the external resistor divider.

7.3.12 Thermal Protection

Internal thermal shutdown circuitry is implemented to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 175°C, the controller is forced into a shutdown mode, disabling the internal regulator. This feature is designed to prevent overheating and damage to the device.

7.4 Device Functional Modes

This device has no additional functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS92691/-Q1 controller is suitable for implementing step-up or step-down LED driver topologies including Buck, Boost, Buck-Boost, SEPIC, Cuk, and Flyback. Use the following design procedure to select component values for the TPS92691/-Q1 device. This section presents a simplified discussion of the design process for the Buck, Boost, and Buck-Boost converter. The expressions derived for Buck-Boost can also be altered to select components for a 1:1 coupled-inductor SEPIC converter. The design procedure can be easily adapted for Flyback and Cuk converter topologies.

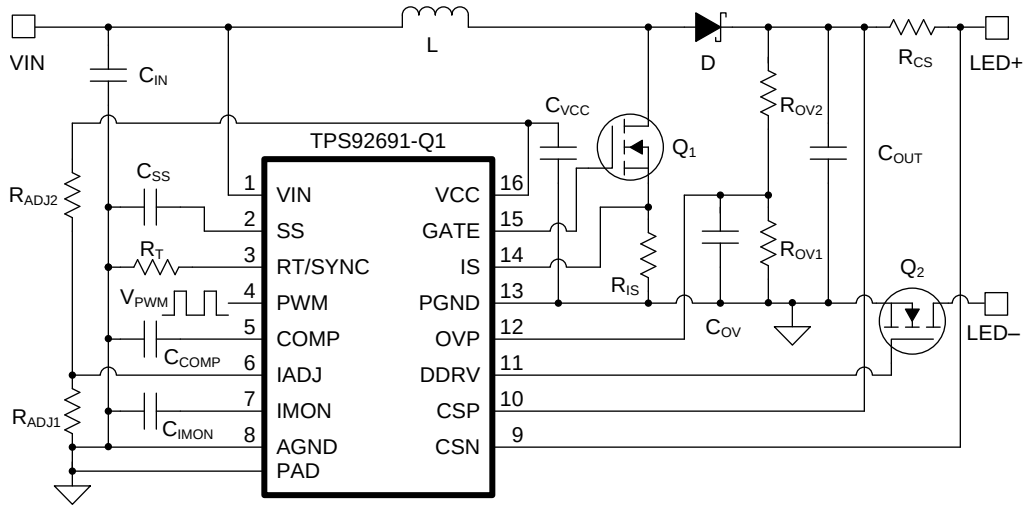


Figure 24. Boost LED Driver

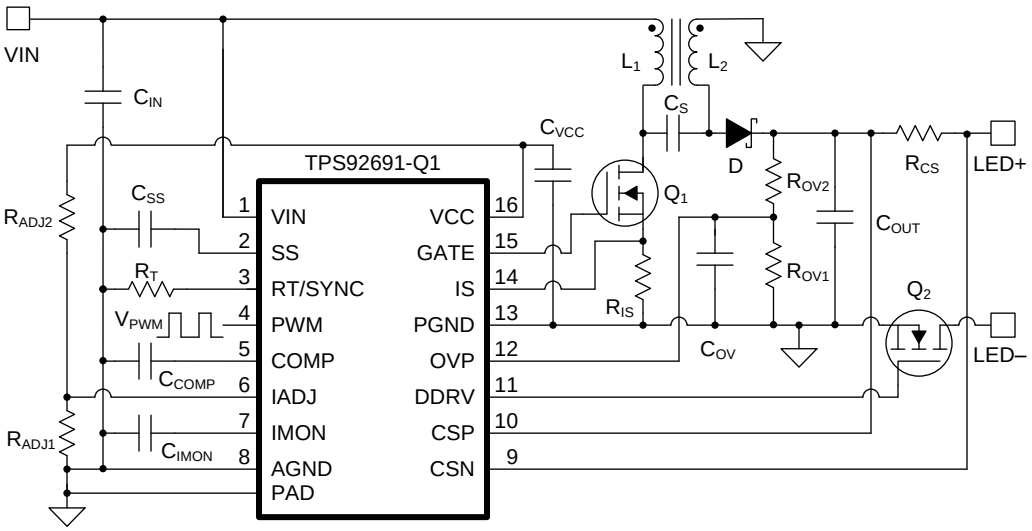


Figure 25. SEPIC LED Driver

Application Information (continued)

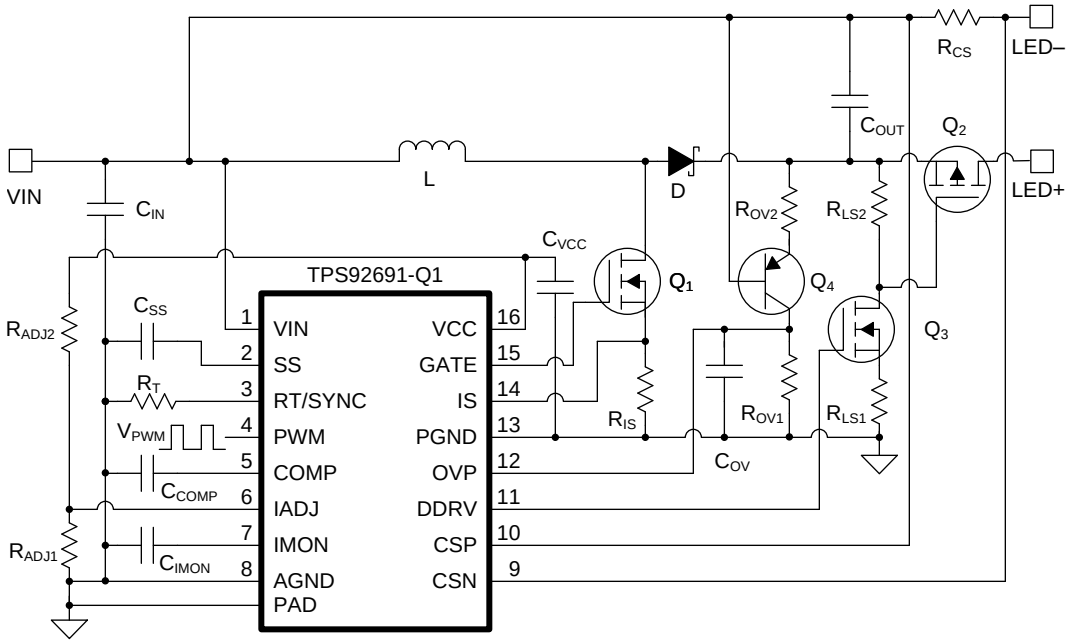


Figure 26. Buck-Boost LED Driver

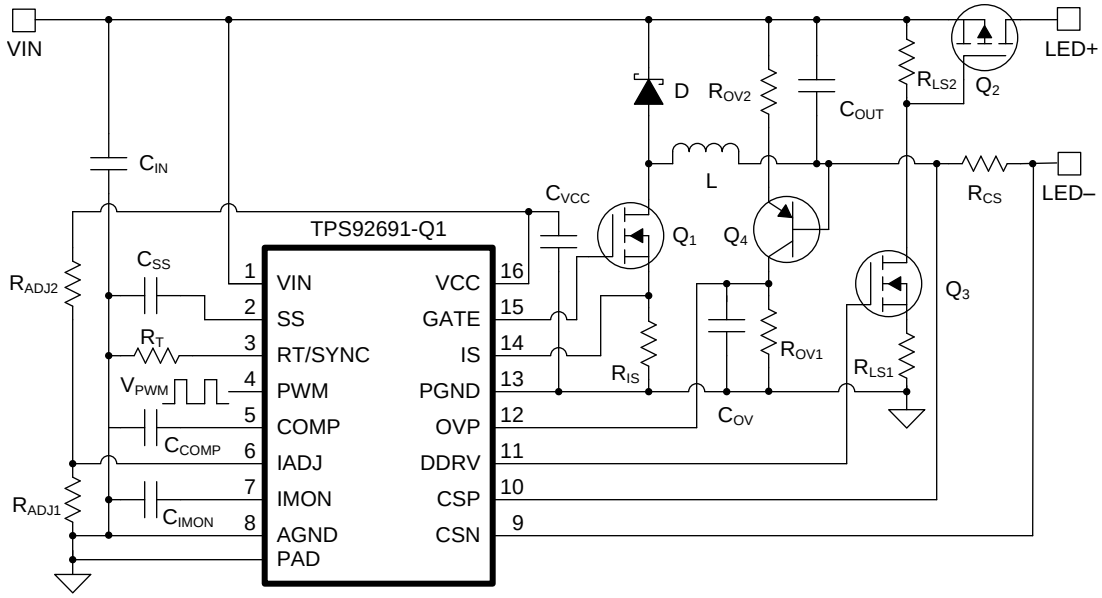


Figure 27. Buck LED Driver

Application Information (continued)

8.1.1 Duty Cycle Considerations

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is derived using expression:

Buck:

$$D = \frac{V_O}{V_{IN}} \quad (2)$$

Boost:

$$D = \frac{V_O - V_{IN}}{V_O} \quad (3)$$

Buck-Boost:

$$D = \frac{V_O}{V_{IN} + V_O} \quad (4)$$

The minimum duty cycle, D_{MIN}, and maximum duty cycle, D_{MAX}, are calculated by substituting maximum input voltage, $V_{IN(MAX)}$, and the minimum input voltage, $V_{IN(MIN)}$, respectively in the previous expressions. The minimum duty cycle achievable by the device is determined by the leading edge blanking period and the switching frequency. The maximum duty cycle is limited by the internal oscillator to 93% (typ) to allow for minimum off-time. It is necessary for the operating duty cycle to be within the operating limits of the device to ensure closed-loop LED current regulation over the specified input and output voltage range.

8.1.2 Inductor Selection

The inductor peak-to-peak ripple current, $\Delta i_{L\text{-}PP}$, is typically set between 10% and 80% of the maximum inductor current, I_L, as a good compromise between core loss and copper loss of the inductor. Higher ripple inductor current allows a smaller inductor size, but places more of a burden on the output capacitor to smooth the LED current ripple. Knowing the desired ripple ratio RR, switching frequency f_{SW}, maximum duty cycle D_{MAX}, and the typical LED current I_{LED}, the inductor value can be calculated as follows:

Buck:

$$\Delta i_{L(PP)} = RR \cdot I_L = RR \cdot I_{LED} \quad (5)$$

$$L = \frac{\left(V_{IN(MIN)} - V_O\right) \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}} \quad (6)$$

Boost and Buck-Boost:

$$\Delta i_{L(PP)} = RR \cdot I_L = RR \cdot \frac{I_{LED}}{1 - D_{MAX}} \quad (7)$$

$$L = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}} \quad (8)$$

As an alternative, the inductor can be selected based on CCM-DCM boundary condition specified based on output power, $P_{O(BDRY)}$. The choice of inductor ensures CCM operation in battery-powered LED driver applications that are designed to support different LED string configurations with a wide range of programmable LED current setpoints. The output power should be calculated based on the lowest LED current and the lowest output voltage requirements for a given application.

$$P_{O(BDRY)} \leq I_{LED(MIN)} \times V_{O(MIN)} \quad (9)$$

Buck:

$$L = \frac{V_{O(MAX)}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times \left(1 - \frac{V_{O(MAX)}}{V_{IN}}\right) \quad (10)$$

Boost:

Application Information (continued)

$$L = \frac{V_{IN}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times \left(1 - \frac{V_{IN}}{V_{O(MAX)}}\right) \quad (11)$$

Buck-Boost:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times \left(\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN}}\right)^2} \quad (12)$$

The saturation current rating of the inductor should be greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

$$I_{L(PK)} = I_L + \frac{V_{IN(MIN)} \times D_{MAX}}{2 \times L \times f_{SW}} \quad (13)$$

8.1.3 Output Capacitor Selection

The output capacitors are required to attenuate the discontinuous or large ripple current generated by switching and achieve the desired peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D, the switching frequency, f_{SW}, and on the converter topology (that is, step-up or step-down). For the Buck and Cuk topology, the inductor is in series with LED load and requires a smaller capacitor than the Boost, Buck-Boost, and SEPIC topologies to achieve the same LED ripple current. The capacitance required for the target LED ripple current can be calculated based on following equations.

Buck:

$$C_{OUT} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED(PP)}} \quad (14)$$

Boost and Buck-Boost:

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}} \quad (15)$$

When choosing the output capacitors, it is important to consider the ESR and the ESL characteristics as they directly impact the LED current ripple. Ceramic capacitors are the best choice due to their low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. TI recommends an X7R dielectric with voltage rating greater than maximum LED stack voltage. An aluminum electrolytic capacitor can be used in parallel with ceramic capacitors to provide bulk energy storage. The aluminum capacitors must have necessary RMS current and temperature ratings to ensure prolonged operating lifetime. The minimum allowable RMS output capacitor current rating, $I_{COUT(RMS)}$, can be approximated:

Buck:

$$I_{COUT(RMS)} = \frac{\Delta i_{LED(PP)}}{\sqrt{12}} \quad (16)$$

Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (17)$$

The expressions (Equation 14 to Equation 17) are best suited for designs driving a fixed LED load, with known output voltage and LED current. For applications that are required to support different LED string configurations with a wide range of programmable LED current setpoints, the previous expressions are rearranged to reflect output capacitance based on the maximum output power, $P_{O(MAX)}$, to ensure that LED current ripple specifications are met over the entire range of operation. *Typical Buck-Boost LED Driver* provides the details for Buck-Boost LED driver.

Application Information (continued)

8.1.4 Input Capacitor Selection

The input capacitors, C_{IN}, smooth the input voltage ripple and store energy to supply input current during input voltage or PWM dimming transients. The series inductor in the Boost, SEPIC, and Cuk topology provides continuous input current and requires a smaller input capacitor to achieve desired input ripple voltage, $\Delta v_{IN(PP)}$. The Buck and Buck-Boost topology have discontinuous input current and require a larger capacitor to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated as follows:

Buck:

$$C_{IN} = \frac{I_{LED} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta v_{IN(PP)}} \quad (18)$$

Boost:

$$C_{IN} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times \Delta v_{IN(PP)}} \quad (19)$$

Buck-Boost:

$$C_{IN} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times \Delta v_{IN(PP)}} \quad (20)$$

X7R dielectric-based ceramic capacitors are the best choice due to their low ESR, high ripple current rating, and good temperature performance. For applications using PWM dimming, TI recommends an aluminum electrolytic capacitor in addition to ceramic capacitors to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

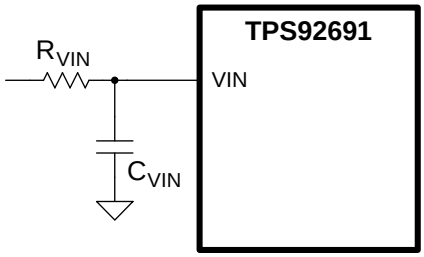


Figure 28. VIN Filter

For most applications, TI highly recommends to bypass the VIN pin with a 0.1-µF ceramic capacitor placed as close as possible to the device and add a series 10-Ω resistor to create a 150-kHz low-pass filter and eliminate undesired high-frequency noise.

8.1.5 Main Power MOSFET Selection

The power MOSFET should be able to sustain the maximum switch node voltage, V_{SW}, and switch RMS current derived based on the converter topology. TI recommends a drain voltage V_{DS} rating of at least 20% greater than the maximum switch node voltage to ensure safe operation. The MOSFET drain-to-source breakdown voltage, V_{DS}, and RMS current ratings are calculated using the following expressions.

Buck:

$$V_{DS} = V_{IN(MAX)} \times 1.2 \quad (21)$$

$$I_{Q(RMS)} = I_{LED} \times \sqrt{D_{MAX}} \quad (22)$$

Boost:

$$V_{DS} = V_{O(OV)} \times 1.2 \quad (23)$$

Application Information (continued)

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}} \quad (24)$$

Buck-Boost:

$$V_{DS} = \left(V_{IN(MAX)} + V_{O(OV)}\right) \times 1.2 \quad (25)$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}} \quad (26)$$

Where the voltage, $V_{O(OV)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions.

Select a MOSFET with low total gate charge, Q_g, to minimize gate drive and switching losses. The MOSFET R_{DS} resistance is usually a less critical parameter because the switch conduction losses are not a significant part of the total converter losses at high operating frequencies. The switching and conduction losses are calculated as follows:

$$P_{COND} = R_{DS} \times I^2_{Q(RMS)} \quad (27)$$

$$P_{SW} = \frac{I_L \times V^2_{SW} \times C_{RSS} \times f_{SW}}{I_{GATE}} \quad (28)$$

C_{RSS} is the MOSFET reverse transfer capacitance. I_L is the average inductor current. I_{GATE} is gate drive output current, typically 500 mA. The MOSFET power rating and package should be selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

8.1.6 Rectifier Diode Selection

A Schottky diode (when used as a rectifier) provides the best efficiency due to low forward voltage drop and near-zero reverse recovery time. TI recommends a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures because it impacts the overall converter operation and efficiency.

The current through the diode, I_D, is given by:

$$I_D = I_L \times (1 - D_{MAX}) \quad (29)$$

The diode should be sized to exceed the current rating, and the package should be able to dissipate power without exceeding the maximum allowable temperature.

8.1.7 LED Current Programming

The LED current is set by the external current sense resistor, R_{CS}, and the analog adjust voltage, V_{IADJ}. The current sense resistor is placed in series with the LED load and can be located either on the high side (connected to the output, V_O), or on the low side (connected to ground, GND). The CSP and CSN inputs of the internal rail-to-rail current sense amplifier are connected to the R_{CS} resistor to enable closed-loop regulation. When V_{IADJ} > 2.5 V, the internal 2.42-V reference sets the $V_{(CSP-CSN)}$ threshold to 172 mV and the LED current is regulated to:

$$I_{LED} = \frac{0.172}{R_{CS}} \quad (30)$$

The LED current can be programmed by varying V_{IADJ} between 140 mV to 2.25 V. The LED current can be calculated using:

$$I_{LED} = \frac{V_{IADJ}}{14 \times R_{CS}} \quad (31)$$

Application Information (continued)

The output voltage ripple should be limited to 50 mV for best performance. TI recommends a low-pass common-mode filter consisting of 10-Ω resistors is series with CSP and CSN inputs and 0.01-µF capacitors to ground to minimize the impact of voltage ripple and noise on LED current accuracy (see Figure 20). A 0.1-µF capacitor across CSP and CSN is included to filter high-frequency differential noise.

8.1.8 Switch Current Sense Resistor and Slope Compensation

The switch current sense resistor, R_{IS}, is used to implement peak current mode control and to set the peak switch current limit. The value of switch current sense R_{IS} is selected to achieve stable inner current loop operation based on the magnitude of slope compensation ramp, V_{SL}, and to protect the main switching MOSFET under fault conditions. The lower of the two values calculated using the following equations should be selected for R_{IS}.

$$R_{IS} = \frac{2 \times V_{SL} \times L \times f_{SW}}{V_{O(MAX)}} \quad (32)$$

$$R_{IS} = \frac{V_{IS(LIMIT)} - V_{SL} \times D_{MAX}}{I_{L(PK)}} \quad (33)$$

The internal slope compensation voltage, V_{SL} is fixed at 200 mV (typ). A resistor can be placed in series with the IS pin to increase slope compensation, if necessary. The peak switch current limit is set based on the internal current limit threshold of 525 mV (typ) and adjusted based on slope compensation to ensure reliable operation while PWM dimming.

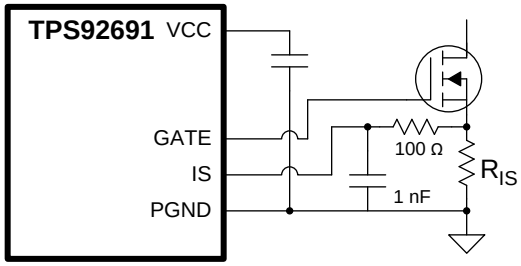


Figure 29. IS Input Filter

The use of a 1-nF and 100-Ω low-pass filter is optional. If used, the resistor value should be less than 500 Ω to limit its influence on the internal slope compensation signal.

8.1.9 Feedback Compensation

The open-loop response is the product of the modulator transfer function (shown in Equation 34) and the feedback transfer function. Using a first-order approximation, the modulator transfer function can be modeled as a single pole created by the output capacitor, and in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance, r_D. Because TI recommends a ceramic capacitor, the ESR of the output capacitor is neglected in the analysis. The small-signal modulator model also includes a DC gain factor that is dependent on the duty cycle, output voltage, and LED current.

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_0 \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \quad (34)$$

Table 1 summarizes the expression for the small-signal model parameters.

Application Information (continued)

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMP to GND (as shown in Figure 30) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in Figure 31, can be used to implement proportional and integral (PI) compensation and to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

Table 1. Small-Signal Model Parameters

	DC GAIN (G_0)	POLE FREQUENCY (ω_P)	ZERO FREQUENCY (ω_Z)
Buck	1	$\frac{1}{r_D \times C_{OUT}}$	—
Boost	$\frac{(1-D)\times V_O}{R_{IS}\times\left(V_O+\left(r_D\times I_{LED}\right)\right)}$	$\frac{V_O+\left(r_D\times I_{LED}\right)}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{L\times I_{LED}}$
Buck-Boost	$\frac{(1-D)\times V_O}{R_{IS}\times\left(V_O+\left(D\times r_D\times I_{LED}\right)\right)}$	$\frac{V_O+\left(D\times r_D\times I_{LED}\right)}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{D\times L\times I_{LED}}$

The feedback transfer function is defined as follows.

Feedback transfer function with integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}}=\frac{14\times g_M\times R_{CS}}{s\times C_{COMP}} \tag{35}$$

Feedback transfer function with proportional integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}}=\frac{14\times g_M\times R_{CS}}{s\times\left(C_{COMP}+C_{HF}\right)}\frac{\left(1+s\times R_{COMP}\times C_{COMP}\right)}{\left(1+s\times R_{COMP}\times\left(\frac{C_{COMP}\times C_{HF}}{C_{COMP}+C_{HF}}\right)\right)} \tag{36}$$

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by placing the low-frequency zero an order of magnitude less than the crossover frequency. Use the following expressions to calculate the compensation network.

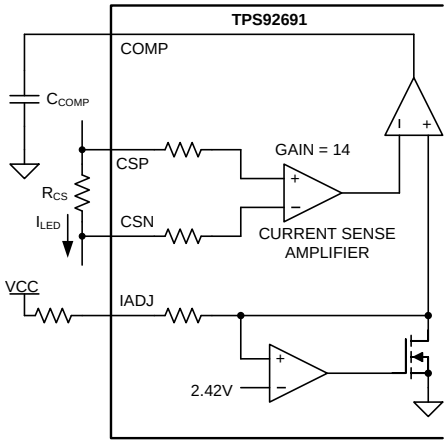


Figure 30. Integral Compensation

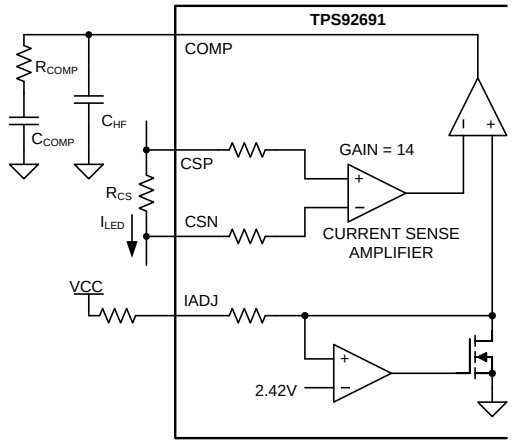


Figure 31. Proportional-Integral Compensation

Buck with integral compensator:

$$C_{COMP}=\frac{8.75\times10^{-3}\times R_{CS}}{\omega_P} \tag{37}$$

Boost and Buck-Boost with proportional integral compensator:

$$C_{COMP} = 8.75 \times 10^{-3} \times \left(\frac{R_{CS} \times G_0}{\omega_Z} \right) \quad (38)$$

$$C_{HF} = \frac{C_{COMP}}{100} \quad (39)$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}} \quad (40)$$

The loop response is verified by applying step input voltage transients. The goal is to minimize LED current overshoot and undershoot with a damped response. Additional tuning of the compensation network may be necessary to optimize PWM dimming performance.

8.1.10 Soft-Start

The soft-start time (t_{SS}) is the time required for the LED current to reach the target setpoint. The required soft-start time, t_{SS}, is programmed using a capacitor, C_{SS}, from SS pin to GND, and is based on the LED current, output capacitor, and output voltage.

$$C_{SS} = 12.5 \times 10^{-6} \left(t_{SS} - \frac{C_{OUT} \times V_{OUT}}{I_{LED}} \right) \quad (41)$$

8.1.11 Overvoltage Protection

The overvoltage threshold is programmed using a resistor divider, R_{OV2} and R_{OV1}, from the output voltage, V_O, to ground for Boost and SEPIC topologies, as shown in Figure 24 and Figure 25. If the LEDs are referenced to a potential other than ground, as in the Buck-Boost or Buck configuration, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors, as shown in Figure 27 and Figure 26. The overvoltage turn-off threshold, $V_{O(OV)}$, is:

Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right) \quad (42)$$

Buck and Buck-Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times \frac{R_{OV2}}{R_{OV1}} + 0.7 \quad (43)$$

The overvoltage hysteresis, $V_{OV(HYS)}$ is:

$$V_{OV(HYS)} = I_{OVP(HYS)} \times R_{OV2} \quad (44)$$

8.1.12 PWM Dimming Considerations

When PWM dimming, the TPS92691/-Q1 requires another MOSFET placed in series with the LED load. This MOSFET should have a voltage rating greater than the output voltage, V_O, and a current rating at least 10% higher than the nominal LED current, I_{LED}.

It is important to control the slew-rate of the external FET to achieve a damped LED current response to PWM rising-edge transitions. For a low-side, N-channel dimming FET, the slew-rate is controlled by placing a resistor in series with the GATE pin. The rise and fall times depend on the value of the resistor and the gate-to-source capacitance of the MOSFET. The series resistor can be bypassed with a diode for fast rise time and slow fall times to achieve 100:1 or higher contrast ratios. If a high-side P-channel dimming FET is used, the rise and fall times can be controlled by selecting appropriate resistors for the level-shift network, R_{LS1} and R_{LS2}, as shown in Figure 26.

8.2 Typical Applications

8.2.1 Typical Boost LED Driver

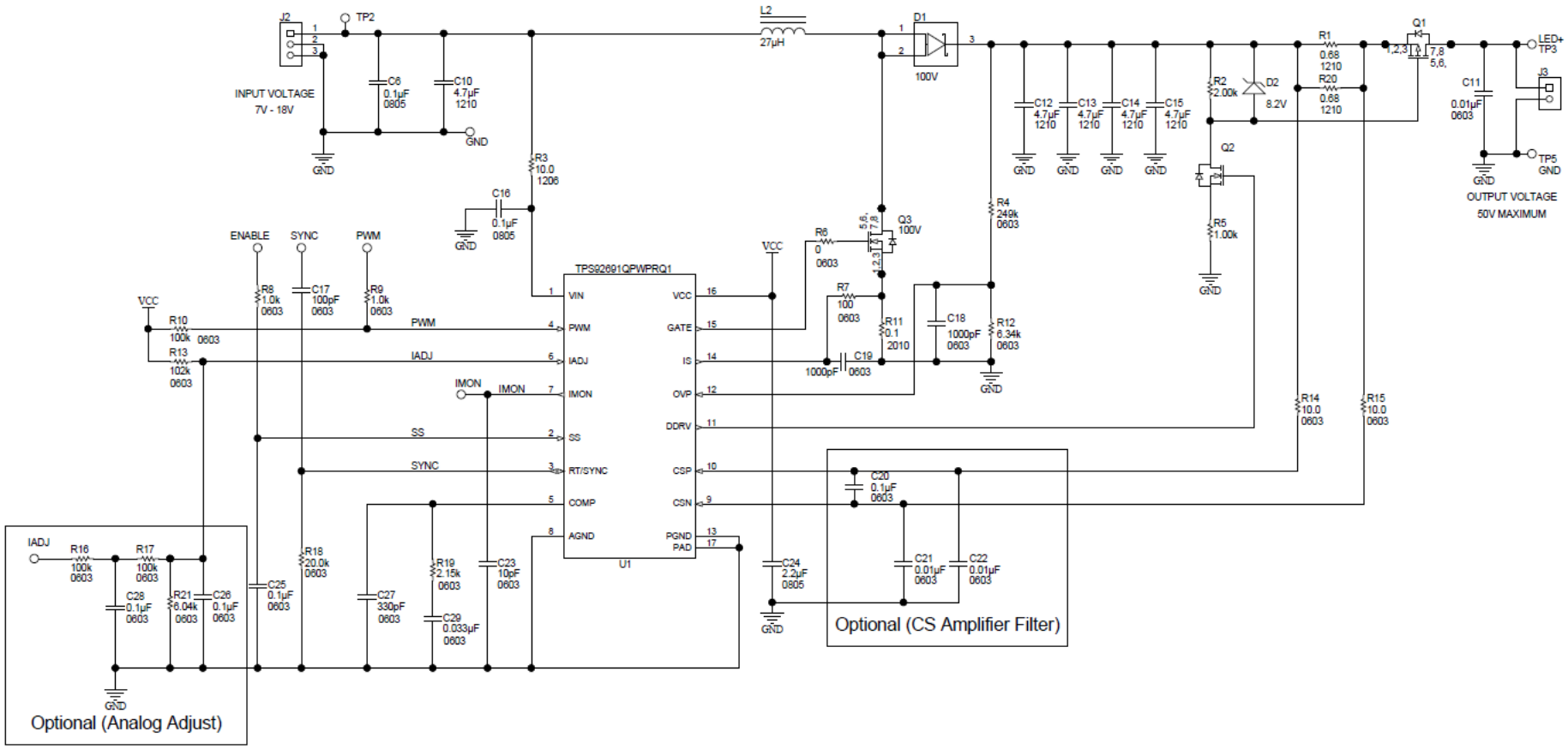


Figure 32. Boost LED Driver With High-Side Current Sense

8.2.1.1 Design Requirements

Table 2 shows the design parameters for the boost LED driver application.

Table 2. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	Input voltage range		7	14	18	V
	Input UVLO setting			4.5		V
OUTPUT CHARACTERISTICS						
	LED forward voltage			3.2		V
	Number of LEDs in series			12		
V_O	Output voltage	LED+ to LED–		38.4		V
I_{LED}	Output current			500		mA
RR	LED current ripple ratio			5%		
r_D	LED string resistance			4		Ω
	Maximum output power			20	25	W
	PWM dimming range	240-Hz PWM frequency	4%		100%	
SYSTEMS CHARACTERISTICS						
$\Delta i_{L(PP)}$	Inductor current ripple			20%		
$\Delta v_{IN(PP)}$	Input voltage ripple			70		mV
$V_{O(OV)}$	Output overvoltage protection threshold			50		V
$V_{OV(HYS)}$	Output overvoltage protection hysteresis			5		V
t_{ss}	Soft-start period			8		ms
	Switching frequency			390		kHz

8.2.1.2 Detailed Design Procedure

This procedure is for the boost LED driver application.

8.2.1.2.1 Calculating Duty Cycle

Solve for D, D_{MAX}, and D_{MIN}:

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{38.4 - 14}{38.4} = 0.6354 \quad (45)$$

$$D_{MAX} = \frac{V_O - V_{IN(MIN)}}{V_O} = \frac{38.4 - 7}{38.4} = 0.8177 \quad (46)$$

$$D_{MIN} = \frac{V_O - V_{IN(MAX)}}{V_O} = \frac{38.4 - 18}{38.4} = 0.5312 \quad (47)$$

8.2.1.2.2 Setting Switching Frequency

Solve for R_T:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{SW})^{1.047}} = \frac{1.432 \times 10^{10}}{\left(390 \times 10^3\right)^{1.047}} = 20.05 \times 10^3 \quad (48)$$

The closest standard resistor of 20 kΩ is selected.

8.2.1.2.3 Inductor Selection

The inductor value should ensure continuous conduction mode (CCM) of operation and should achieve desired ripple specification, $\Delta i_{L(PP)}$.

$$\Delta i_{L(PP)} = RR \times \frac{I_{LED}}{1 - D_{MAX}} = 0.2 \times \frac{0.5}{1 - 0.8177} = 0.5485 \quad (49)$$

Solving for inductor:

$$L = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}} = \frac{7 \times 0.8177}{0.5485 \times 390 \times 10^{3}} = 26.76 \times 10^{-6} \quad (50)$$

The closest standard inductor is 27 µH. The expected inductor ripple based on the chosen inductor is:

$$\Delta i_{L(PP)} = \frac{V_{IN(MIN)} \times D_{MAX}}{L \times f_{SW}} = \frac{7 \times 0.8177}{27 \times 10^{-6} \times 390 \times 10^{3}} = 0.5436 \quad (51)$$

The inductor saturation current rating should be greater than the peak inductor current, $I_{L(PK)}$.

$$I_{L(PK)} = \frac{I_{LED}}{1 - D_{MAX}} + \frac{V_{IN(MIN)} \times D_{MAX}}{2 \times L \times f_{SW}} = \frac{0.5}{1 - 0.8177} + \frac{7 \times 0.8177}{2 \times 27 \times 10^{-6} \times 390 \times 10^{3}} = 3.01 \quad (52)$$

8.2.1.2.4 Output Capacitor Selection

The specified peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$, is:

$$\Delta i_{LED(PP)} = 0.05 \times I_{LED} = 25 \times 10^{-3} \quad (53)$$

The output capacitance required to achieve the target LED current ripple is:

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}} = \frac{0.5 \times 0.8177}{390 \times 10^{3} \times 4 \times 25 \times 10^{-3}} = 10.48 \times 10^{-6} \quad (54)$$

Considering 40% derating factor under DC bias operation, four 4.7-µF, 100-V rated X7R ceramic capacitors are used in parallel to achieve a combined output capacitance of 18.8 µF.

8.2.1.2.5 Input Capacitor Selection

The input capacitor is required to reduce switching noise conducted through the input wires and reduced the input impedance of the LED driver. The capacitor required to limit peak-to-peak input ripple voltage ripple, $\Delta v_{IN(PP)}$, to 70 mV is given by:

$$C_{IN} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times \Delta v_{IN(PP)}} = \frac{0.5436}{8 \times 390 \times 10^{3} \times 70 \times 10^{-3}} = 2.49 \times 10^{-6} \quad (55)$$

A 4.7-µF, 50-V X7R ceramic capacitor is selected.

8.2.1.2.6 Main N-Channel MOSFET Selection

The MOSFET ratings should exceed the maximum output voltage and RMS switch current given by:

$$V_{DS} = V_{O(OV)} \times 1.2 = 50 \times 1.2 = 60 \quad (56)$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}} = 0.5 \times \frac{\sqrt{0.8177}}{1 - 0.8177} = 2.48 \quad (57)$$

A 60-V or a 100-V N-channel MOSFET with current rating exceeding 3 A is required for this design.

8.2.1.2.7 Rectifying Diode Selection

The diode should be selected based on the following voltage and current ratings:

$$V_{D(BR)} = V_{O(OV)} \times 1.2 = 50 \times 1.2 = 60 \quad (58)$$

$$I_D = I_L \times (1 - D_{MAX}) = I_{LED} = 0.5 \quad (59)$$

A 60-V or a 100-V Schottky diode with low reverse leakage current is suitable for this design. The package must be able to handle the power dissipation resulting from continuous forward current, I_D, of 0.5 A.

8.2.1.2.8 Programming LED Current

LED current is based on the current shunt resistor, R_{CS} and the $V_{(CSP-CSN)}$ threshold set by the voltage on the IADJ pin V_{IADJ}. By default, IADJ is tied to VCC via an external resistor to enable the internal reference voltage of 2.42 V that then sets the $V_{(CSP-CSN)}$ threshold to 172 mV. The current shunt resistor value is calculated by:

$$R_{CS} = \frac{0.172}{I_{LED}} = \frac{0.172}{0.5} = 0.344 \tag{60}$$

Two 0.68-Ω resistors are connected in parallel to achieve R_{CS} of 0.34 Ω.

8.2.1.2.9 Setting Switch Current Limit and Slope Compensation

The switch current sense resistor, R_{IS}, is calculated by solving the following equations and choosing the lowest value:

$$R_{IS} = \frac{2 \times V_{SL} \times L \times f_{SW}}{V_{O(MAX)}} = \frac{2 \times 0.2 \times 27 \times 10^{-6} \times 390 \times 10^{3}}{38.4} = 0.11 \tag{61}$$

$$R_{IS} = \frac{V_{IS(LIMIT)} - V_{SL} \times D_{MAX}}{I_{L(PK)}} = \frac{0.525 - 0.2 \times 0.8177}{3.01} = 0.12 \tag{62}$$

A standard value of 0.1 Ω is selected.

8.2.1.2.10 Deriving Compensator Parameters

The modulator transfer function for the Boost converter is derived for nominal V_{IN} voltage and corresponding duty cycle, D, and is given by the following equation. (See Table 1 for more information.)

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_0 \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} = 3.466 \frac{\left(1 - \frac{s}{378.12 \times 10^{3}}\right)}{\left(1 + \frac{s}{14 \times 10^{3}}\right)} \tag{63}$$

The proportional-integral compensator components C_{COMP} and R_{COMP} are obtained by solving the following expressions:

$$C_{COMP} = 8.75 \times 10^{-3} \times \left(\frac{R_{CS} \times G_0}{\omega_Z}\right) = 8.75 \times 10^{-3} \times \left(\frac{0.34 \times 3.466}{378.12 \times 10^{3}}\right) = 27.27 \times 10^{-9} \tag{64}$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}} = \frac{1}{14 \times 10^{3} \times 33 \times 10^{-9}} = 2.165 \times 10^{3} \tag{65}$$

The closet standard capacitor of 33 nF and resistor of 2.15 kΩ is selected. The high frequency pole location is set by a 100 pF C_{HF} capacitor.

8.2.1.2.11 Setting Start-up Duration

The soft-start capacitor required to achieve start-up in 8 ms is given by:

$$C_{SS} = 12.5 \times 10^{-6} \left(t_{SS} - \frac{C_{OUT} \times V_{OUT}}{I_{LED}}\right) = 12.5 \times 10^{-6} \left(8 \times 10^{-3} - \frac{18.8 \times 10^{-6} \times 38.4}{0.5}\right) = 81.9 \times 10^{-9} \tag{66}$$

The closet standard capacitor of 100 nF is selected.

8.2.1.2.12 Setting Overvoltage Protection Threshold

The overvoltage protection threshold of 50 V and hysteresis of 5 V is set by the R_{OV1} and R_{OV2} resistor divider.

$$R_{OV2} = \frac{V_{OV(HYS)}}{20 \times 10^{-6}} = \frac{5}{20 \times 10^{-6}} = 250 \times 10^{3} \tag{67}$$

$$R_{OV1} = \left(\frac{1.24}{V_{O(OV)} - 1.24} \right) R_{OV2} = \left(\frac{1.24}{50 - 1.24} \right) 250 \times 10^3 = 6.36 \times 10^3 \quad (68)$$

The standard resistor values of 249 kΩ and 6.34 kΩ are chosen.

8.2.1.2.13 PWM Dimming Considerations

A series dimming FET is required to meet PWM dimming specification from 100% to 4% duty cycle. A 60-V, 2-A N-channel FET is suitable for this application.

As an alternative, a 60-V, 2-A P-channel FET could be used to achieve PWM dimming. An external level-shift circuit is required to translate the DDRV signal to the gate of the P-channel dimming FET. The drive strength of 5 mA and gate-source voltage of 15 V are set by the 1-kΩ and 2-kΩ level-translator resistors and a small-signal N-channel MOSFET, whose gate is connected to DDRV.

By default, the PWM pin is connected to VCC through a 100-kΩ resistor to enable the part upon start-up.

8.2.1.3 Application Curves

These curves are for the boost LED driver.

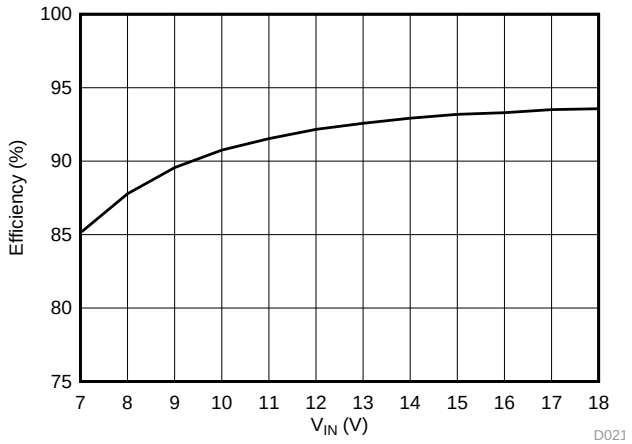
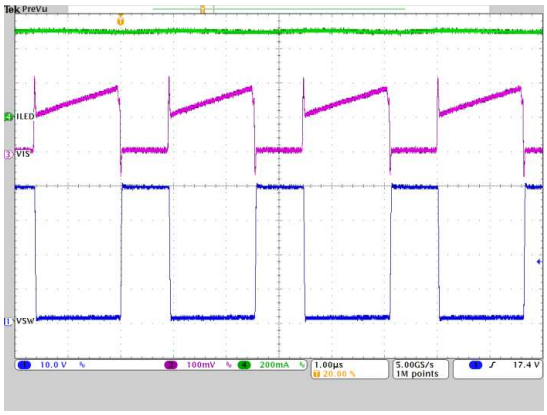
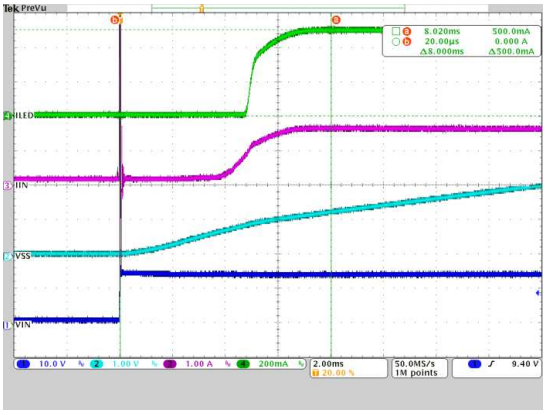


Figure 33. Efficiency vs Input Voltage



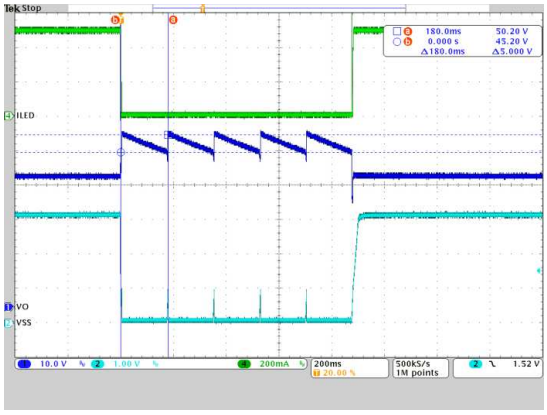
Ch1: Switch node voltage;
Ch3: Switch sense current resistor voltage;
Ch4: LED current; Time: 1 µs/div

Figure 34. Normal Operation



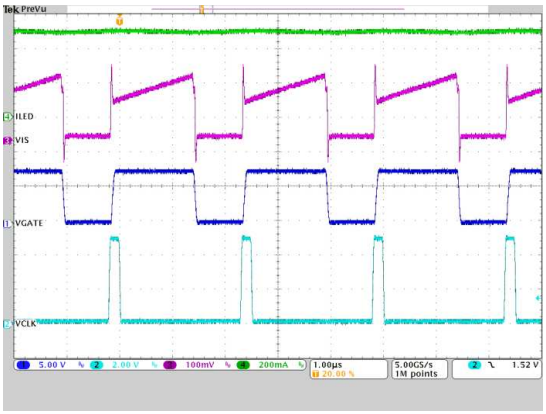
Ch1: Input voltage; Ch2: Soft-start (SS) voltage;
Ch3: Input current;
Ch4: LED current; Time: 2 ms/div

Figure 35. Startup Transient



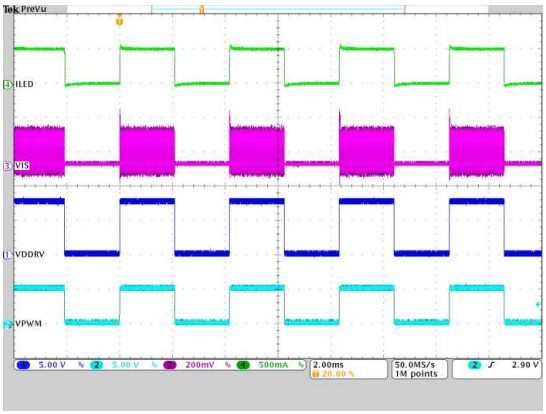
Ch1: Output voltage;
Ch2: Soft-start (SS) voltage;
Ch4: LED current; Time: 200 ms/div

Figure 36. Overvoltage Protection



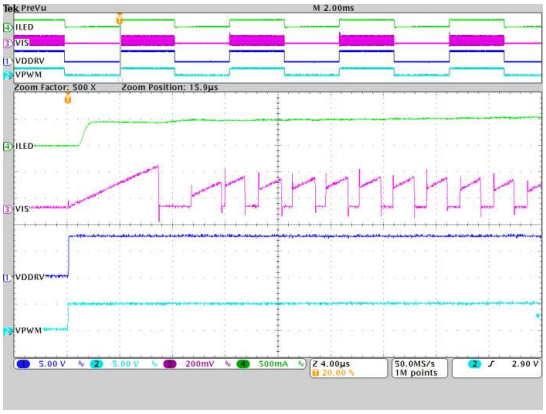
Ch1: GATE voltage; Ch2: External CLK signal;
Ch3: Switch sense current resistor voltage;
Ch4: LED current; Time: 1 µs/div

Figure 37. Clock Synchronization



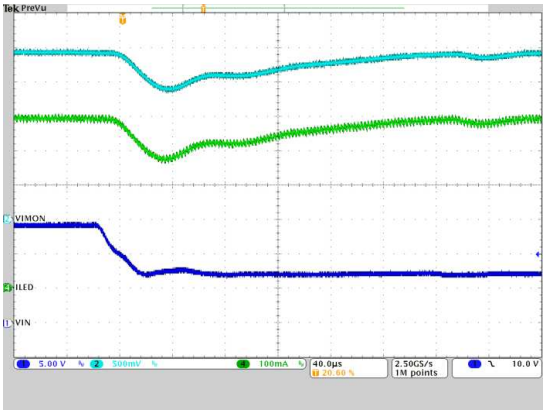
Ch1: DDRV voltage; Ch2: PWM input;
Ch3: Switch sense current resistor voltage;
Ch4: LED current; Time: 2 ms/div

Figure 38. PWM Dimming Transient



Ch1: DDRV voltage; Ch2: PWM input;
Ch3: Switch sense current resistor voltage;
Ch4: LED current; Time: 4 µs/div

Figure 39. PWM Dimming Transient (Zoomed)



Ch1: Input voltage;
Ch2: IMON voltage;
Ch4: LED current; Time: 2 ms/div

Figure 40. Step Input Voltage Transient and IMON Behavior

8.2.2 Typical Buck-Boost LED Driver

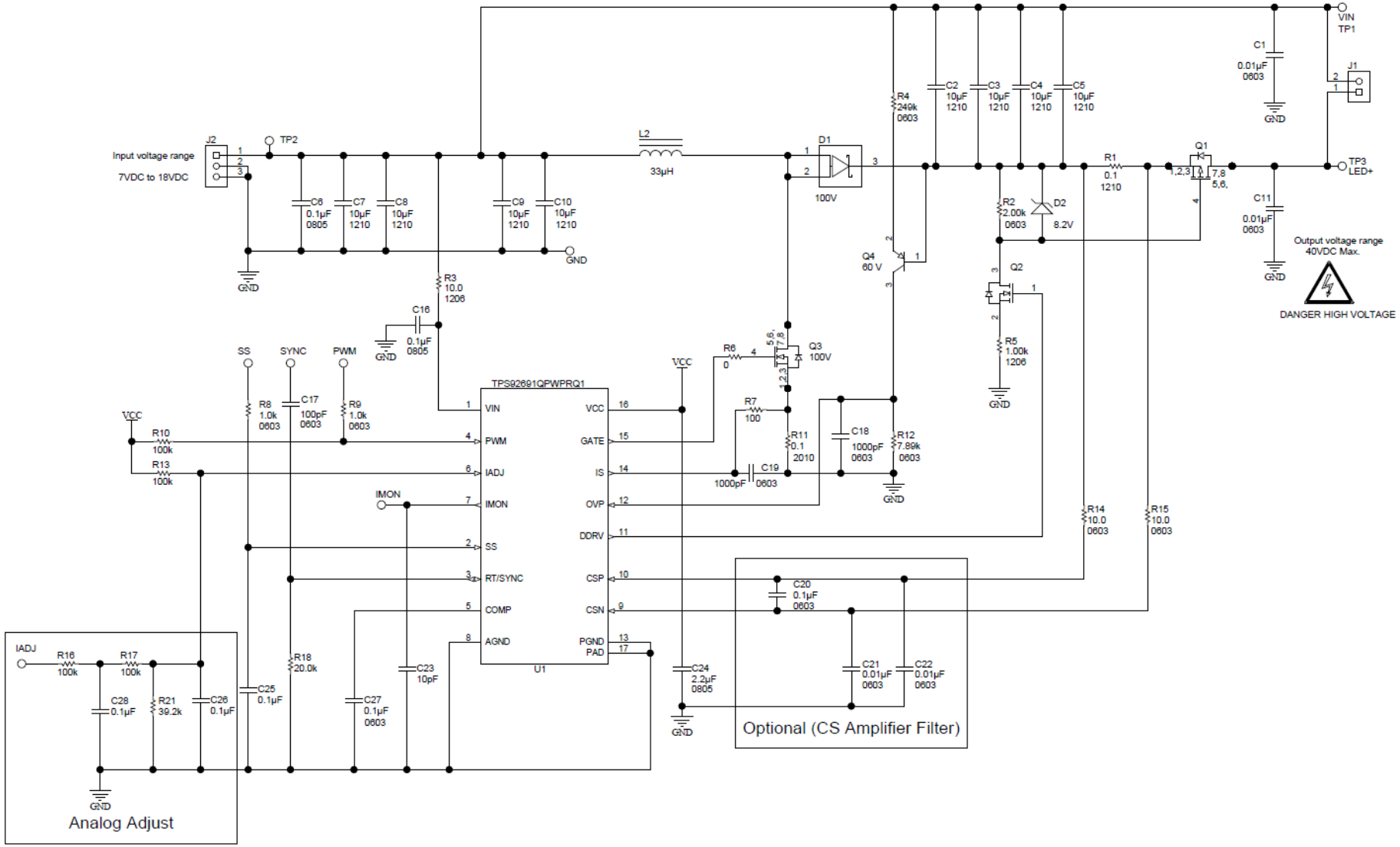


Figure 41. Buck-Boost LED Driver

8.2.2.1 Design Requirements

Buck-Boost LED drivers provide the flexibility needed in applications that support multiple LED load configurations. For such applications, it is necessary to modify the design procedure presented in *Application Information* to account for the wider range of output voltage and LED current specifications. This design is based on the maximum output power $P_{O(MAX)}$, set by the lumen output specified for the lighting application. The design procedure for a battery connected application with 3 to 9 LEDs in series and maximum 15 W output power is outlined in this section.

For applications that have a fixed number of LEDs and a narrow LED current range (for brightness correction), design equations provided in the *Application Information* and simplified design procedure, similar to one outlined in *Typical Boost LED Driver* for Boost LED driver, are recommended for developing an optimized circuit with lower Bill of Material (BOM) cost.

Table 3. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	Input voltage range		7	14	18	V
	Input UVLO setting			4.5		V
OUTPUT CHARACTERISTICS						
	LED forward voltage			3.2		V
	Number of LEDs in series		3	6	9	
V_O	Output voltage	LED+ to LED–	9.6	19.2	28.8	V
I_{LED}	Output current		500	750	1500	mA
$\Delta i_{LED(PP)}$	LED current ripple			5%		
r_D	LED string resistance		1	2	3	Ω
$P_{O(MAX)}$	Maximum output power				15	W
	PWM dimming range	240-Hz PWM frequency	4%		100%	
SYSTEMS CHARACTERISTICS						
$P_{O(BDRY)}$	Output power at CCM-DCM boundary condition			5		W
$\Delta v_{IN(PP)}$	Input voltage ripple			70		mV
$V_{O(OV)}$	Output overvoltage protection threshold			40		V
$V_{OV(HYS)}$	Output overvoltage protection hysteresis			5		V
t_{ss}	Soft-start period			8		ms
	Switching frequency			390		kHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Calculating Duty Cycle

Solving for D, D_{MAX}, and D_{MIN}:

$$D = \frac{V_O}{V_O + V_{IN}} = \frac{19.2}{19.2 + 14} = 0.5783 \quad (69)$$

$$D_{MAX} = \frac{V_{O(MAX)}}{V_{O(MAX)} + V_{IN(MIN)}} = \frac{28.8}{28.8 + 7} = 0.8045 \quad (70)$$

$$D_{MIN} = \frac{V_{O(MIN)}}{V_{O(MIN)} + V_{IN(MAX)}} = \frac{9.6}{9.6 + 18} = 0.3478 \quad (71)$$

8.2.2.2.2 Setting Switching Frequency

Solving for R_T resistor:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{SW})^{1.047}} = \frac{1.432 \times 10^{10}}{(390 \times 10^3)^{1.047}} = 20.05 \times 10^3 \quad (72)$$

8.2.2.2.3 Inductor Selection

The inductor is selected to meet the CCM-DCM boundary power requirement, $P_{O(BDRY)}$. Typically, the boundary condition is set to enable CCM operation at the lowest possible operating power based on minimum LED forward voltage drop and LED current. In most applications, $P_{O(BDRY)}$ is set to be 1/3 of the maximum output power, $P_{O(MAX)}$. The inductor value is calculated for maximum input voltage, $V_{IN(MAX)}$, and output voltage, $V_{O(MAX)}$:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times \left(\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN(MAX)}} \right)^2} = \frac{1}{2 \times 5 \times 390 \times 10^3 \times \left(\frac{1}{28.8} + \frac{1}{18} \right)^2} = 31.46 \times 10^{-6} \quad (73)$$

The closest standard value of 33 µH is selected. The inductor ripple current is given by:

$$\Delta i_{L(PP)} = \frac{V_{IN(MIN)} \times D_{MAX}}{L \times f_{SW}} = \frac{7 \times 0.8045}{33 \times 10^{-6} \times 390 \times 10^3} = 0.4376 \quad (74)$$

The inductor saturation rating should exceed the calculated peak current which is based on the maximum output power using the following expression:

$$I_{L(PK)} = P_{O(MAX)} \times \left(\frac{1}{V_{O(MIN)}} + \frac{1}{V_{IN(MIN)}} \right) + \frac{V_{O(MIN)} \times V_{IN(MIN)}}{2 \times L \times f_{SW} \times \left(V_{O(MIN)} + V_{IN(MIN)} \right)} \quad (75)$$

$$I_{L(PK)} = 15 \times \left(\frac{1}{9.6} + \frac{1}{7} \right) + \frac{9.6 \times 7}{2 \times 33 \times 10^{-6} \times 390 \times 10^3 \times (9.6 + 7)} = 3.863$$

8.2.2.2.4 Output Capacitor Selection

The output capacitor should be selected to achieve the 5% peak-to-peak LED current ripple specification. Based on the maximum power, the capacitor is calculated as follows:

$$C_{OUT} = \frac{P_{O(MAX)}}{f_{SW} \times r_{D(MIN)} \times \Delta i_{LED(PP)} \times \left(V_{O(MIN)} + V_{IN(MIN)} \right)} \quad (76)$$

$$C_{OUT} = \frac{15}{390 \times 10^3 \times 1 \times 0.075 \times (9.6 + 7)} = 30.9 \times 10^{-6}$$

A minimum of four 10-µF, 50-V X7R ceramic capacitors in parallel are needed to meet the LED current ripple specification over the entire range of output power. Additional capacitance may be required based on the derating factor under DC bias operation.

8.2.2.2.5 Input Capacitor Selection

The input capacitor is calculated based on the peak-to-peak input ripple specifications, $\Delta v_{IN(PP)}$. The capacitor required to limit the ripple to 70 mV over range of operation is calculated using:

$$C_{IN} = \frac{P_{O(MAX)}}{f_{SW} \times \Delta v_{IN(PP)} \times \left(V_{O(MIN)} + V_{IN(MIN)} \right)} = \frac{15}{390 \times 10^3 \times 0.07 \times (9.6 + 7)} = 33.1 \times 10^{-6} \quad (77)$$

A parallel combination of four 10-µF, 50-V X7R ceramic capacitors are used for a combined capacitance of 40 µF. Additional capacitance may be required based on the derating factor under DC bias operation.

8.2.2.2.6 Main N-Channel MOSFET Selection

Calculating the minimum transistor voltage and current rating:

$$V_{DS} = 1.2 \times \left(V_{O(OV)} + V_{IN(MAX)} \right) = 1.2 \times (40 + 18) = 69.6 \quad (78)$$

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} \sqrt{\left(1 + \frac{V_{IN(MIN)}}{V_{O(MIN)}}\right)} = \frac{15}{7} \sqrt{\left(1 + \frac{7}{9.6}\right)} = 2.82 \quad (79)$$

This application requires a 60-V or 100-V N-channel MOSFET with a current rating exceeding 3 A.

8.2.2.2.7 Rectifier Diode Selection

Calculating the minimum Schottky diode voltage and current rating:

$$V_{D(BR)} = 1.2 \times \left(V_{O(OV)} + V_{IN(MAX)}\right) = 1.2 \times (40 + 18) = 69.6 \quad (80)$$

$$I_D = I_{LED(MAX)} = 1.5 \quad (81)$$

This application requires a 60-V or 100-V Schottky diode with a current rating exceeding 1.5 A. TI recommends a single high-current diode instead of paralleling multiple lower-current-rated diodes to ensure reliable operation over temperature.

8.2.2.2.8 Setting Switch Current Limit and Slope Compensation

Solving for R_{IS}:

$$R_{IS} = \frac{2 \times V_{SL} \times L \times f_{SW}}{V_{O(MAX)}} = \frac{2 \times 0.2 \times 33 \times 10^{-6} \times 390 \times 10^{3}}{28.8} = 0.179 \quad (82)$$

$$R_{IS} = \frac{V_{IS(LIMIT)} - V_{SL} \times D_{MAX}}{I_{L(PK)}} = \frac{0.525 - 0.2 \times 0.8045}{3.863} = 0.094 \quad (83)$$

A standard resistor of 0.1 Ω is selected based on the lower of the two calculated values. The resistor ensures stable current loop operation with no subharmonic oscillations over the entire input and output voltage ranges.

8.2.2.2.9 Programming LED Current

The LED current can be programmed to match the LED string configuration by using a resistor divider, R_{ADJ1} and R_{ADJ2}, from V_{CC} to GND for a given sense resistor, R_{CS}, as shown in Figure 21. To maximize the accuracy, the IADJ pin voltage is set to 2.1 V for the specified LED current of 1.5 A. The current sense resistor, R_{CS}, is then calculated as:

$$R_{CS} = \frac{V_{IADJ}}{14 \times I_{LED(MAX)}} = \frac{2.1}{14 \times 1.5} = 0.1 \quad (84)$$

A standard resistor of 0.1 Ω is selected. Table 4 summarizes the IADJ pin voltage and the choice of the R_{ADJ1} and R_{ADJ2} resistors for different current settings.

Table 4. Design Requirements

LED CURRENT	IADJ VOLTAGE (V_{IADJ})	R_{ADJ1}	R_{ADJ2}
500 mA	700 mV	10.2 kΩ	100 kΩ
750 mA	1.05 V	16.2 kΩ	100 kΩ
1.5 A	2.1 V	39.2 kΩ	100 kΩ

8.2.2.2.10 Deriving Compensator Parameters

A simple integral compensator provides a good starting point to achieve stable operation across the wide operating range. The modulator transfer function with the lowest frequency pole location is calculated based on maximum output voltage, $V_{O(MAX)}$, duty cycle, D_{MAX}, LED dynamic resistance, $r_{D(MAX)}$, and minimum LED string current, $I_{LED(MIN)}$. (See Table 1 for more information.)

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_0 \frac{\left(1 - \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} = 1.876 \frac{\left(1 - \frac{s}{82.92 \times 10^3}\right)}{\left(1 + \frac{s}{8.68 \times 10^3}\right)} \quad (85)$$

The compensation capacitor needed to achieve stable response is:

$$C_{COMP} = \frac{8.75 \times 10^{-3} \times R_{CS}}{\omega_P} = \frac{8.75 \times 10^{-3} \times 0.1}{8.68 \times 10^{3}} = 100.8 \times 10^{-9} \quad (86)$$

A 100 nF capacitor is selected.

A proportional integral compensator can be used to achieve higher bandwidth and improved transient performance. However, it is necessary to experimentally tune the compensator parameters over the entire operating range to ensure stable operation.

8.2.2.2.11 Setting Startup Duration

Solving for soft-start capacitor, C_{SS}, based on 8-ms startup duration:

$$C_{SS} = 12.5 \times 10^{-6} \left(t_{SS} - \frac{C_{OUT} \times V_{OUT(MAX)}}{I_{LED(MIN)}} \right) = 12.5 \times 10^{-6} \left(8 \times 10^{-3} - \frac{40 \times 10^{-6} \times 28.8}{0.5} \right) = 71.2 \times 10^{-9} \quad (87)$$

A 100-nF soft-start capacitor is selected.

8.2.2.2.12 Setting Overvoltage Protection Threshold

Solving for resistors, R_{OV1} and R_{OV2}:

$$R_{OV2} = \frac{V_{OV(HYS)}}{20 \times 10^{-6}} = \frac{5}{20 \times 10^{-6}} = 250 \times 10^{3} \quad (88)$$

$$R_{OV1} = \frac{1.24 \times R_{OV2}}{V_{O(OV)} - 0.7} = \frac{1.24 \times 250 \times 10^{3}}{40 - 0.7} = 7.89 \times 10^{3} \quad (89)$$

The closest standard values of 249 kΩ and 7.87 kΩ along with a 60-V PNP transistor are used to set the OVP threshold to 40 V with 5 V of hysteresis.

8.2.2.2.13 PWM Dimming Consideration

A 60-V, 2-A P-channel FET is used in conjunction with an external level-shift circuit to achieve PWM dimming. The drive strength of 5 mA and gate-source voltage of 15 V are set by the 1-kΩ and 2-kΩ level-translator resistors and a small-signal N-channel MOSFET, whose gate is connected to DDRV.

8.2.2.3 Application Curves

These curves are for the buck-boost LED driver.

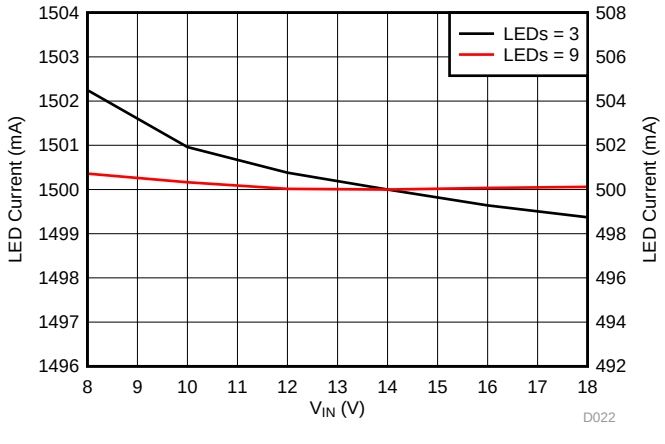
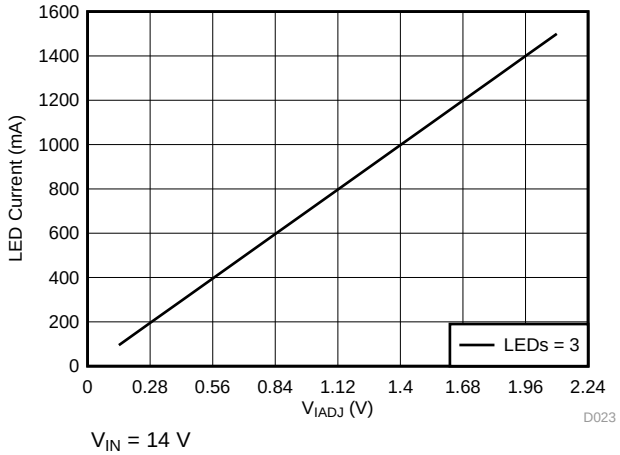


Figure 42. Line Regulation (3 LEDs at 1.5 A and 9 LEDs at 500 mA)



VIN = 14 V

Figure 43. LED Current vs IADJ Voltage

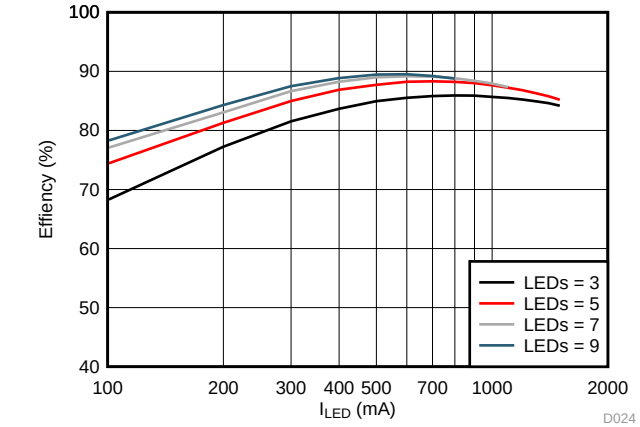


Figure 44. Efficiency from 100 mA to 1.5 A

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 4.5 V and 65 V. The input could be a car battery or another preregulated power supply. If the input supply is located more than a few inches from the TPS92691/-Q1 device, additional bulk capacitance or an input filter may be required in addition to the ceramic bypass capacitors to address noise and EMI concerns.

10 Layout

10.1 Layout Guidelines

- The performance of the switching regulator depends as much on the layout of the PCB as the component selection. Following a few simple guidelines will maximize noise rejection and minimize the generation of EMI within the circuit.
- Discontinuous currents are the most likely to generate EMI. Therefore, take care when routing these paths. The main path for discontinuous current in the TPS92691/-Q1 Buck regulator contains the input capacitor, C_{IN}, the recirculating diode, D, the N-channel MOSFET, Q1, and the sense resistor, R_{IS}. In the TPS92691/-Q1 Boost regulator, the discontinuous current flows through the output capacitor C_{OUT}, diode, D, N-channel MOSFET, Q1, and the current sense resistor, R_{IS}. In Buck-Boost regulator, both loops are discontinuous and should be carefully laid out. These loops should be kept as small as possible and the connection between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L, D, and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.
- CSP and CSN traces should be routed together with Kelvin connections to the current sense resistor as short as possible. If needed, use common mode and differential mode noise filters to attenuate switching and diode reverse recovery noise from affecting the internal current sense amplifier.
- The COMP, IS, OVP, PWM, and IADJ pins are all high-impedance inputs that couple external noise easily; therefore, the loops containing these nodes should be minimized whenever possible.
- In some applications, the LED or LED array can be far away from the TPS92691/-Q1, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
- The TPS92691/-Q1 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction-to-ambient thermal resistance varies with application. The most significant variables are the area of copper in the PCB and the number of vias under the exposed pad. The integrity of the solder connection from the device exposed pad to the PCB is critical. Excessive voids greatly decrease the thermal dissipation capacity.

10.2 Layout Example

VIA TO BOTTOM GROUND PLANE

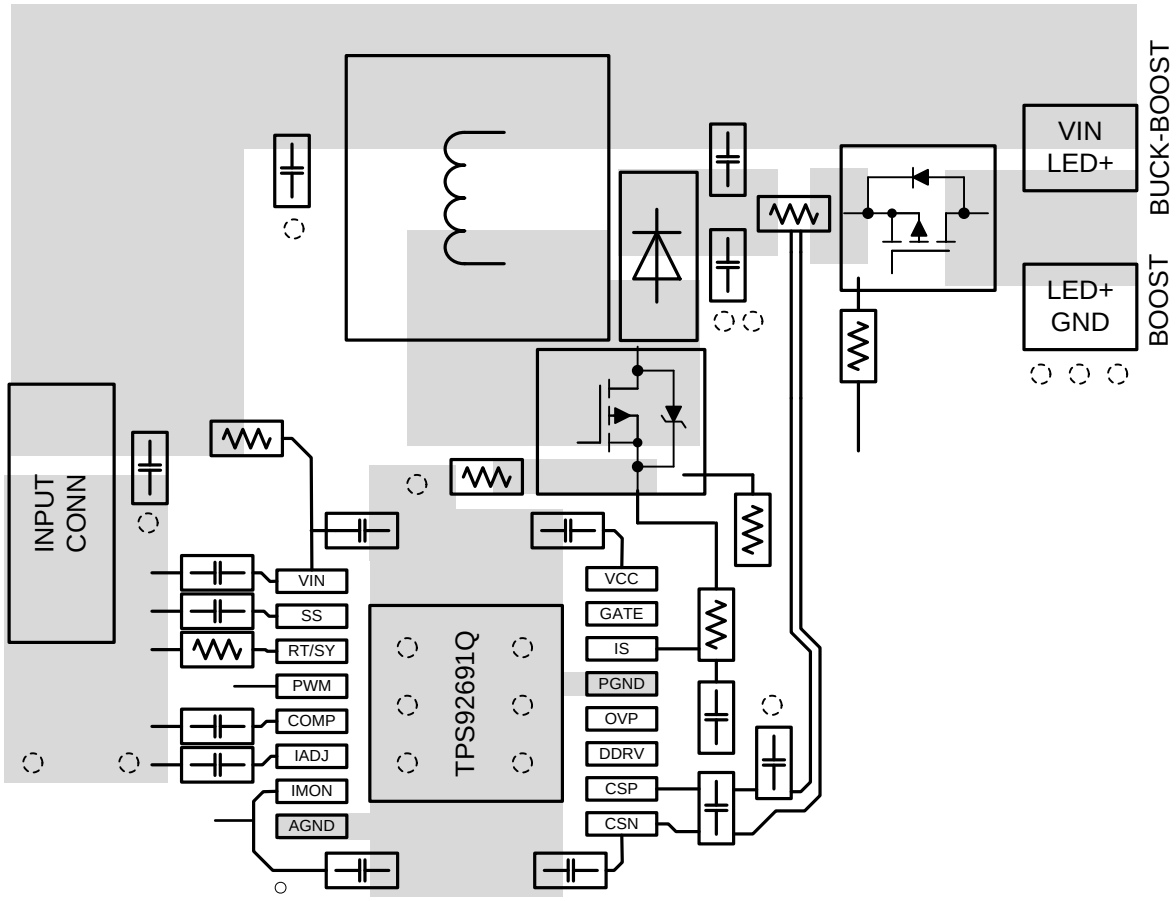


Figure 45. Layout Recommendation

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS92691	Click here	Click here	Click here	Click here	Click here
TPS92691-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92691PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92691	Samples
TPS92691PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92691	Samples
TPS92691QPWPQ1	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92691Q	Samples
TPS92691QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92691Q	Samples
TPS92691QPWPTQ1	ACTIVE	HTSSOP	PWP	16	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92691Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS92691, TPS92691-Q1 :

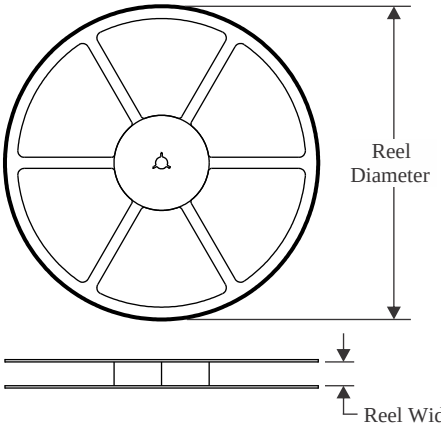
- Catalog: TPS92691
- Automotive: TPS92691-Q1

NOTE: Qualified Version Definitions:

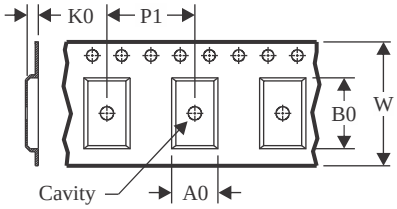
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

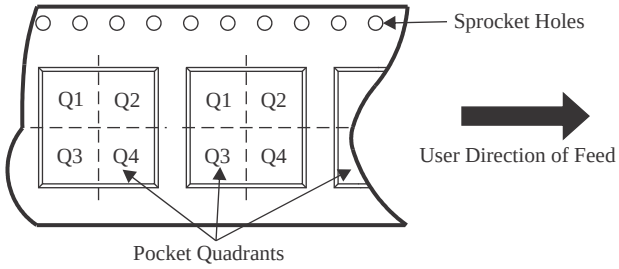


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

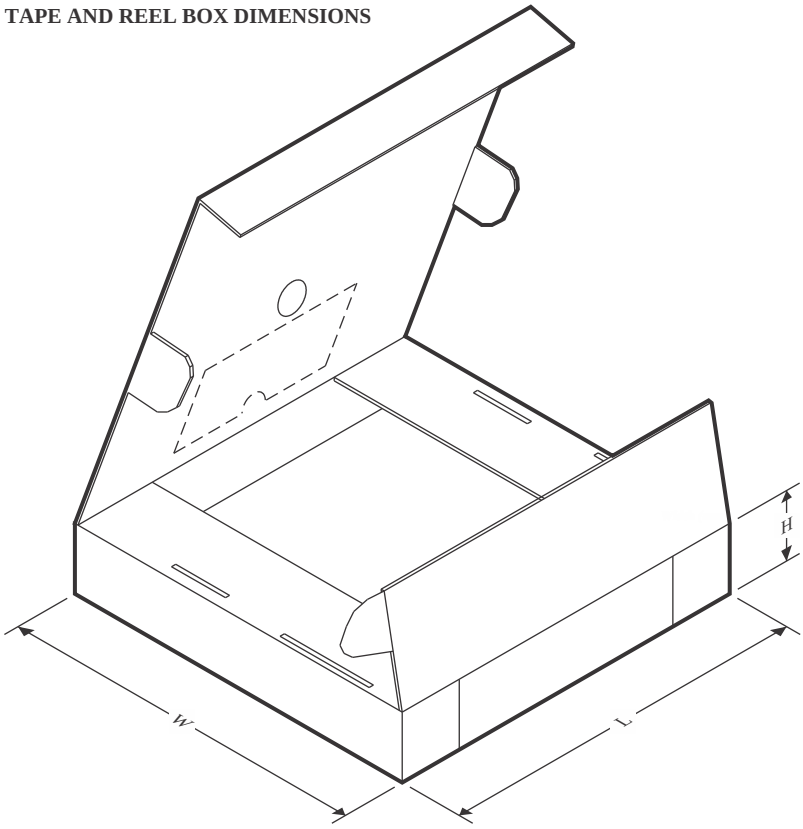
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92691PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS92691QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

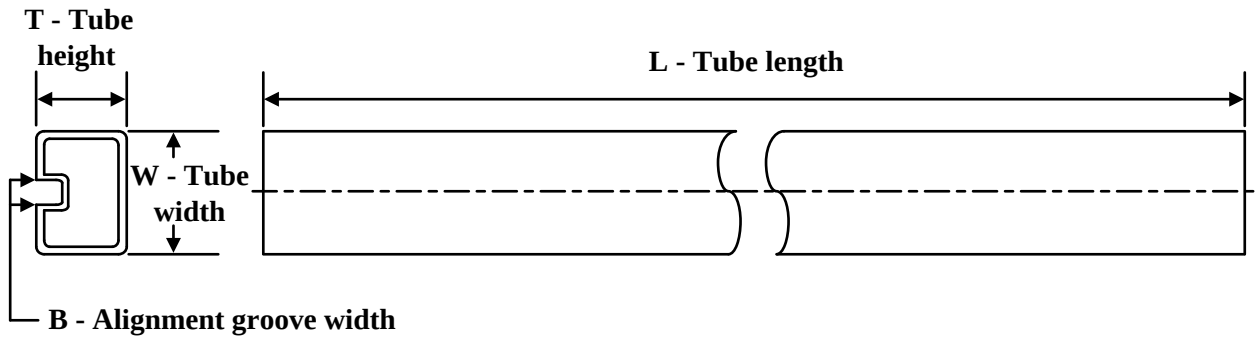
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92691PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS92691QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

TUBE

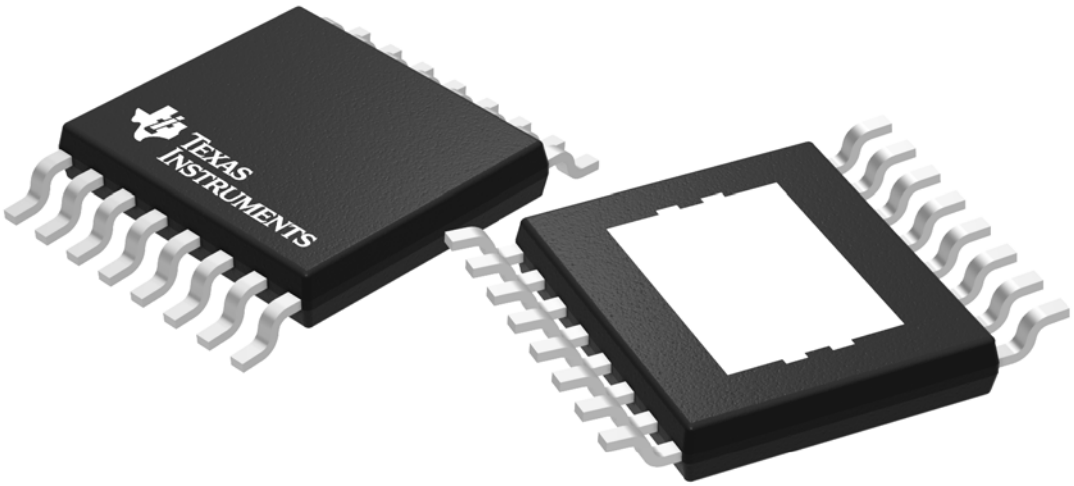


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92691PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
TPS92691QPWPQ1	PWP	HTSSOP	16	90	530	10.2	3600	3.5

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

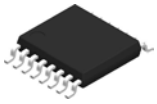
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

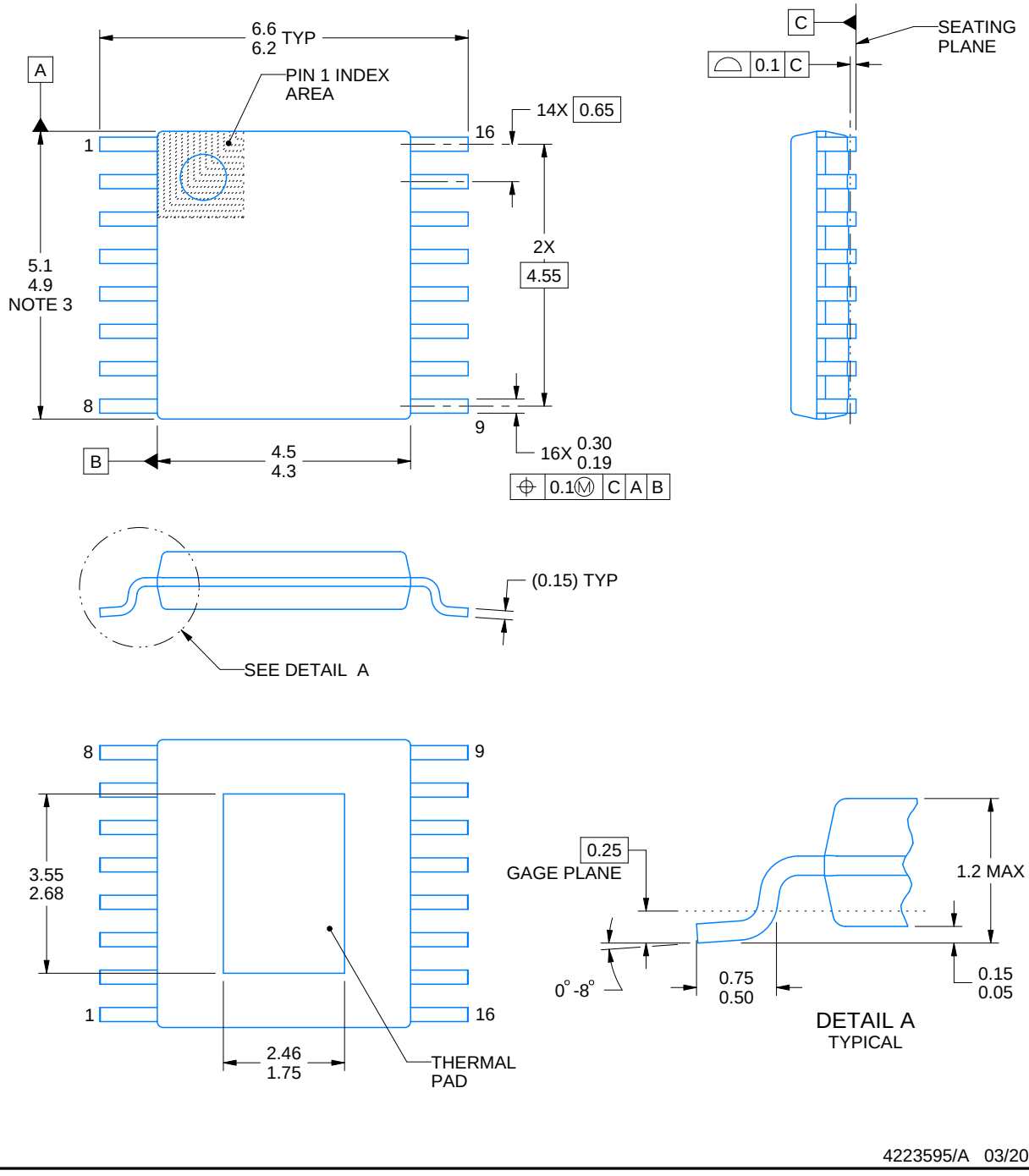
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

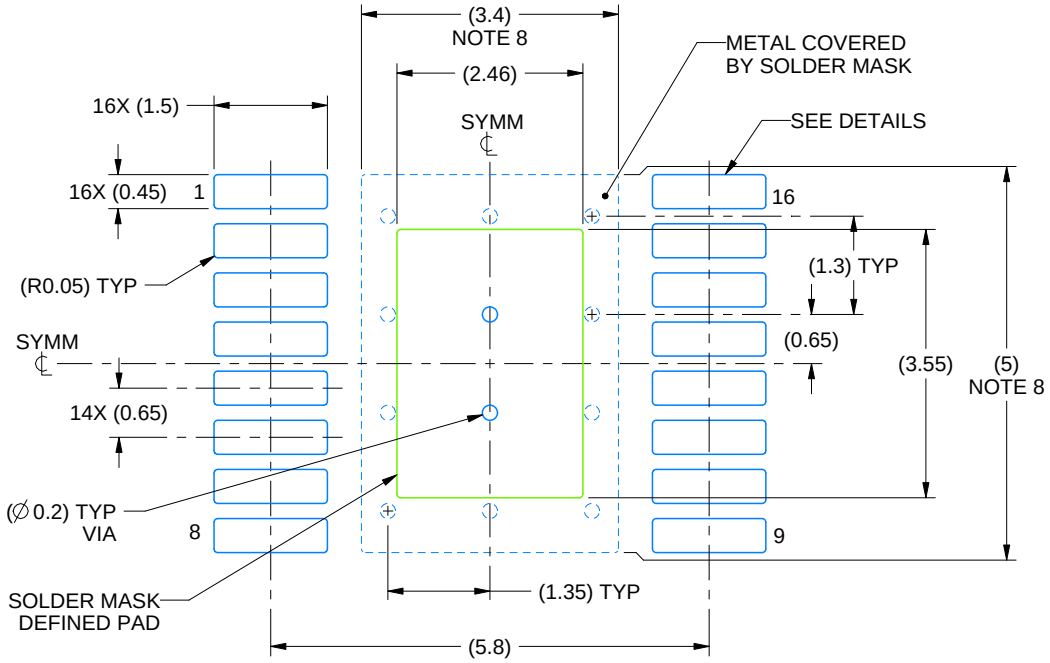
SMALL OUTLINE PACKAGE



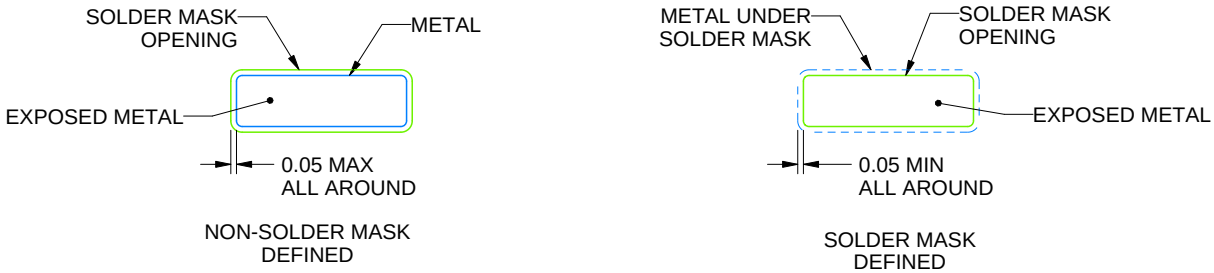
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

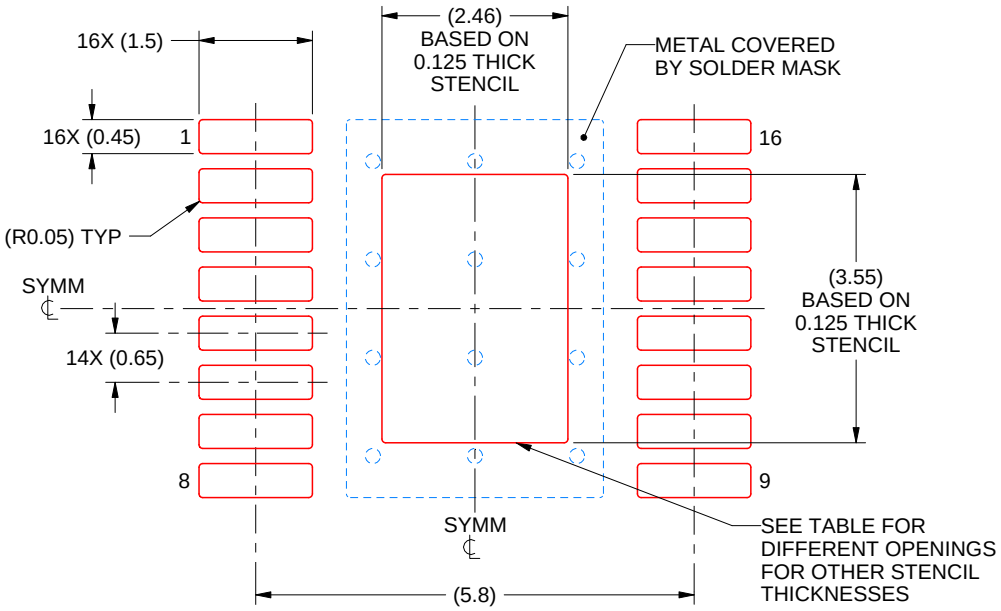


SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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