User's Guide
SLVU459B–May 2011–Revised July 2018

TPS55010EVM-009, Low-Power, Isolated Fly-Buck™ Converter

This user's guide contains information for the TPS55010EVM-009 evaluation module (PWR009). Included are the performance specifications, the schematic, and the bill of materials for the TPS55010EVM-009.

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1 Introduction

This user's guide contains background information for the TPS55010 as well as support documentation for the TPS55010EVM-009 evaluation module (PWR009). Included are the performance specifications, the schematic, and the bill of materials for the TPS55010EVM-009.

1.1 Background

The TPS55010 dc/dc converter is designed to provide up to a 200-mA output from an input voltage source of 4.5 V to 5.5 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board areas that may be achieved when designing with the TPS55010 regulator. The switching frequency is externally set at a nominal 350 kHz. Both high-side and low-side MOSFETs are incorporated inside the TPS55010 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFETs allows the TPS55010 to achieve good efficiency. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS55010 provides adjustable slow-start and undervoltage lockout inputs. The absolute maximum input voltage for the TPS55010EVM-009 is 6 V.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS55010EVM-009	V_{IN} = 4.5 V to 6 V	0 A to 200 mA

1.2 Performance Specification Summary

A summary of the TPS55010EVM-009 performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 5 V and an output voltage of 5 V, unless otherwise specified. The TPS55010EVM-009 is designed and tested for V_{IN} = 4.5 V to 6 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS55010EVM-009 Electrical and Performance Specification

Parameter	Condition		MIN	TYP	MAX	UNIT
Output voltage	4.5 V ≤ V_{IN} ≤ 5.5 V, I_{LOAD} ≤ 200 mA	5 V	4.5	5	6	V
Output current	4.5 V ≤ V_{IN} ≤ 5.5 V				0.2	A
Output ripple voltage, peak-to-peak	I_{LOAD} = 200 mA	V_{IN} = 5 V		20		mV
Switching frequency	I_{LOAD} = 200 mA	V_{IN} = 5 V		350		kHz
Efficiency, end-to-end	I_{LOAD} = 200 mA	V_{IN} = 5 V		85%		
Line regulation	I_{LOAD} = 200 mA	4.5 V ≤ V_{IN} ≤ 5.5 V		±0.06		V
Load regulation	I_{LOAD} = 10 mA to 200 mA	V_{IN} = 5 V		±0.3		V
Control loop crossover frequency	I_{LOAD} = 200 mA			25		kHz
Slow start				40		ms
Operating temperature			–25		85	°C

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS55010. Some modifications can be made to this module.

1.3.1 Input Voltage Range

TPS55010EVM-009 can operate from an input voltage of 5 V or 3.3 V, nominally. For 3.3-V nominal input voltage, remove R3 (allows the EVM to start up from lower input voltages), and change R9 to 511 kΩ (changes switching frequency to 200 kHz).

1.3.2 Operating Frequency, Slow-Start, and UVLO

The operating frequency, slow-start time, and UVLO voltage can be adjusted. R9 sets the operating frequency, C5 sets the slow-start time, and the resistor divider of R2 and R3 sets the UVLO start and stop voltages. See the TPS55010 data sheet (SLVSAV0) for details on adjusting these parameters.

1.3.3 Zener Diode and Output Snubber

Under no-load conditions, VOUT can get as high as 15 V if output voltage limiting is not provided. TPS55010EVM-009 provides a Zener diode (5.6 V nominal) in series with a resistor to limit the output voltage at J2 to 6 V. The Zener diode presents a negligible load to the circuit with external loads above approximately 3 mA at J2.

Placeholders for an R-C snubber are provided across the output rectifier. Although the snubber impacts efficiency, it can be used to dampen the ringing across the rectifier.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS55010EVM-009 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS55010EVM-009 is provided with input/output connectors and test points as shown in Table 3. A power supply capable of supplying 0.5 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. Test-point TP2 provides a place to monitor the V_{IN} input voltages with TP5 providing a convenient ground reference. TP10 is used to monitor the output voltage with TP4 as the ground reference.

Table 3. EVM Connectors and Test Points

Reference Designator	Label	Description
J1	INPUT	VIN connector
J2	OUTPUT	VOUT connector
TP2	VIN	Input VIN circuit point
TP5	GND	Input GND circuit point
TP10	VOUT	Output VOUT circuit point
TP4	AGND	Output AGND circuit point
TP1	FAULT	FAULT pin
TP3	EN	EN pin
TP6	SS	SLOW START pin
TP7	PH	PH pin
TP8	LOOP	Injection point for loop measurements
TP9	VC	Regulated voltage
TP12	GND	Input GND circuit point

2.2 Efficiency

Figure 1 shows the efficiency for the TPS55010EVM-009 at an ambient temperature of 25°C.

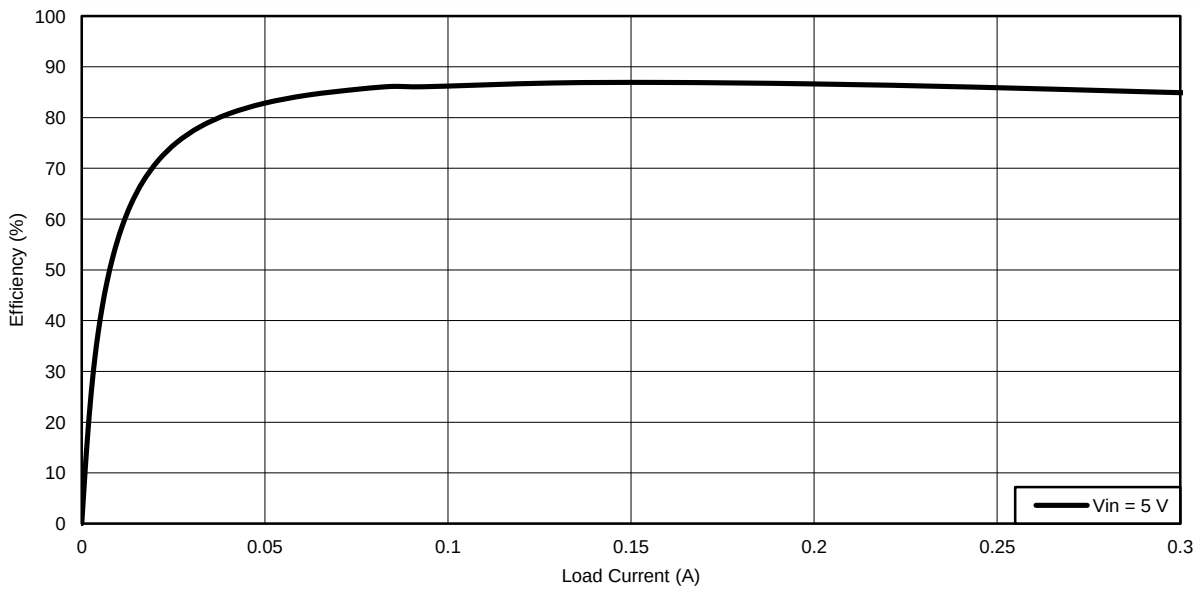

Figure 1. TPS55010EVM-009 Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Load Regulation

Figure 2 shows the load regulation for the TPS55010EVM-009 at an ambient temperature of 25°C.

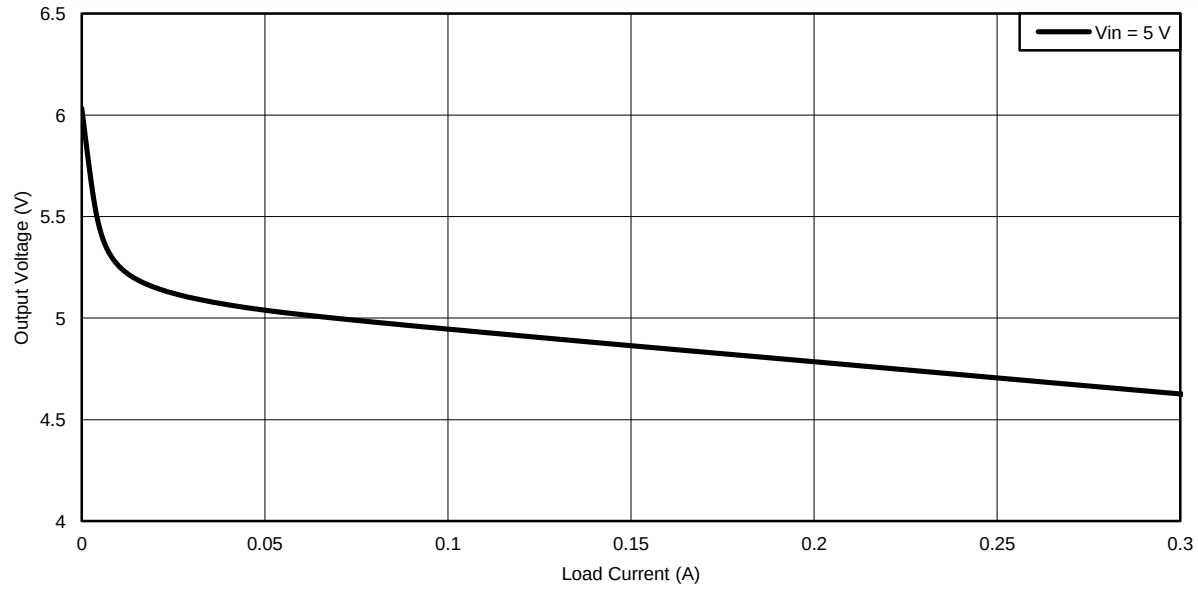

Figure 2. TPS55010EVM-009 Load Regulation

2.4 Line Regulation

Figure 3 shows the line regulation for the TPS55010EVM-009 at an ambient temperature of 25°C.

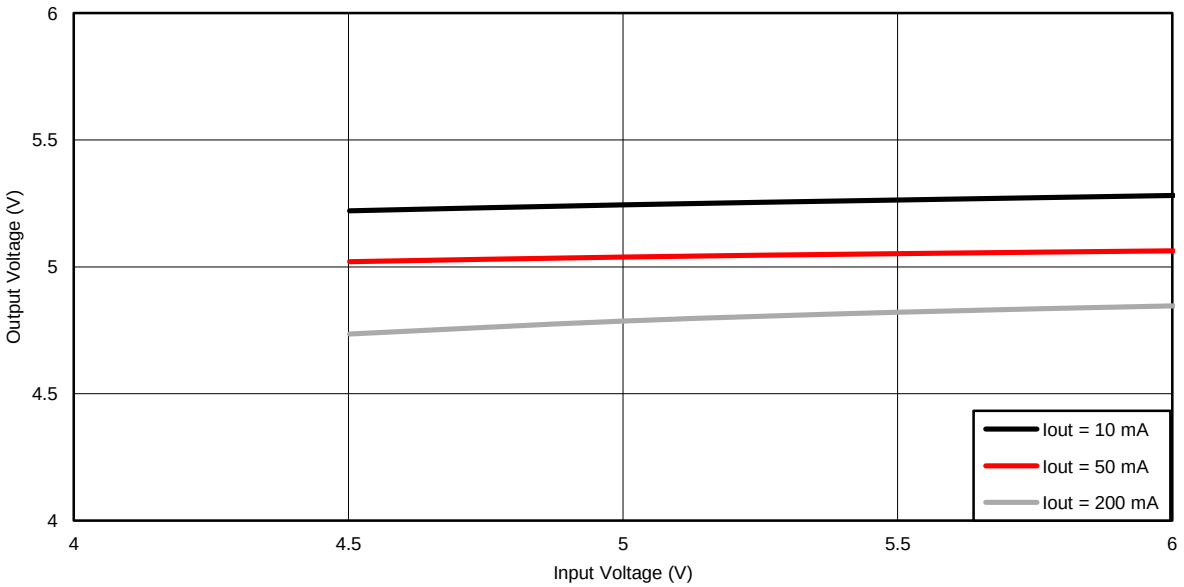

Figure 3. TPS55010EVM-009 Line Regulation, V_{IN} = 5 V

2.5 Loop Characteristics

The TPS55010EVM-009 loop-response characteristics are shown in Figure 4. Gain and phase plots are shown for V_{IN} = 5 V and a load current of both 0 mA and 200 mA. At a 0-mA load, the unity gain bandwidth is 32.5 kHz and phase margin is 53 degrees. At a 200-mA load, the unity gain bandwidth is 25.2 kHz and the phase margin is 82 degrees.

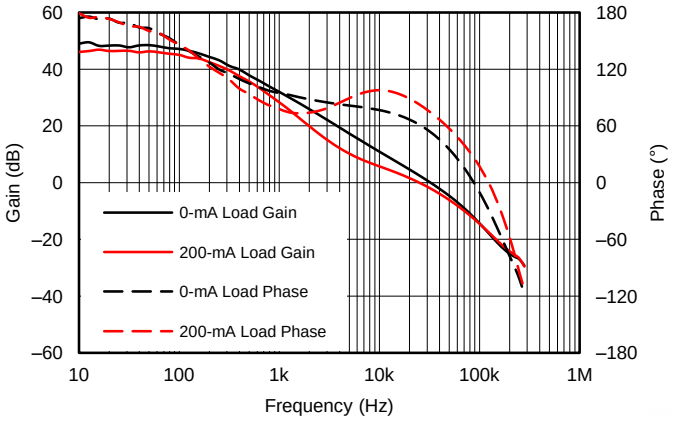

Figure 4. TPS55010EVM-009 Loop Response

2.6 Output Voltage Ripple

The TPS55010EVM-009 output voltage ripple is shown in Figure 5 . The output current is the rated full load of 200 mA and V_{IN} = 5 V. The ripple voltage is measured directly across the output capacitors.

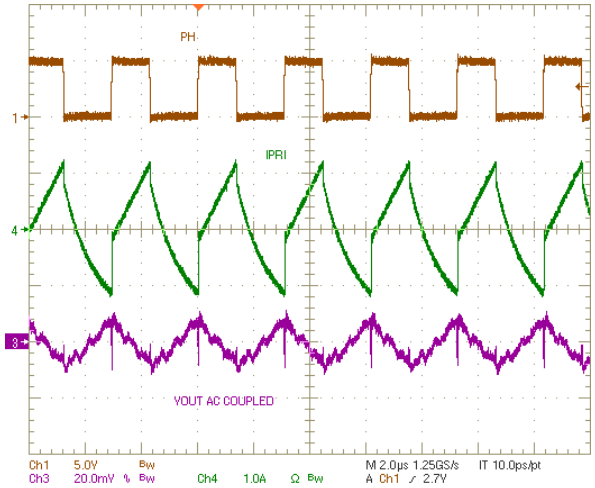

Figure 5. TPS55010EVM-009 Output Voltage Ripple

2.7 Input Voltage Ripple

The TPS55010EVM-009 input voltage ripple is shown in Figure 6 . The output current is the rated full load of 200 mA and V_{IN} = 5 V. The ripple voltage is measured directly across the input capacitors.

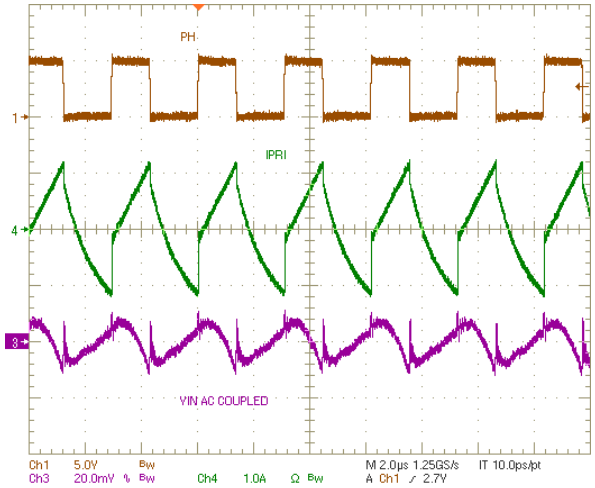

Figure 6. TPS55010EVM-009 Input Voltage Ripple

2.8 Powering Up

Figure 7 shows the start-up waveforms with rising V_{IN} and the output loaded with 22 Ω. In Figure 7, the output starts to rise when V_{IN} reaches the rising UVLO of 4.5 V.

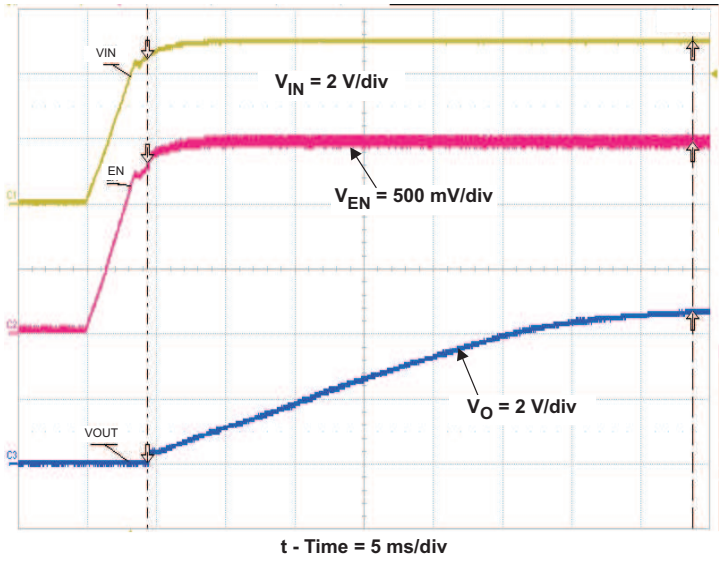

Figure 7. TPS55010EVM-009 Start-Up With Rising V_{IN}

3 Board Layout

This section provides a description of the TPS55010EVM-009, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS55010EVM-009 is shown in Figure 8 through Figure 10. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper. A basic set of layout guidelines include:

- Place the input capacitors close to the TPS55010 VIN and GND terminals.
- Arrange the transformer, input capacitors, and the regulated voltage capacitor in a manner to minimize loop area.
- Connect the GND end of the analog control circuitry (COMP, VSENSE, RT/CLK, and SS pins) together apart from the main power GND. Reference this analog GND trace/shape to the power GND (PowerPAD™ IC package of TPS55010) at a single point.
- The PowerPAD™ package of the TPS55010 provides a means to remove heat from the device and must be connected to the GND plane with multiple vias as shown in the TPS55010 data sheet, SLVSAV0.

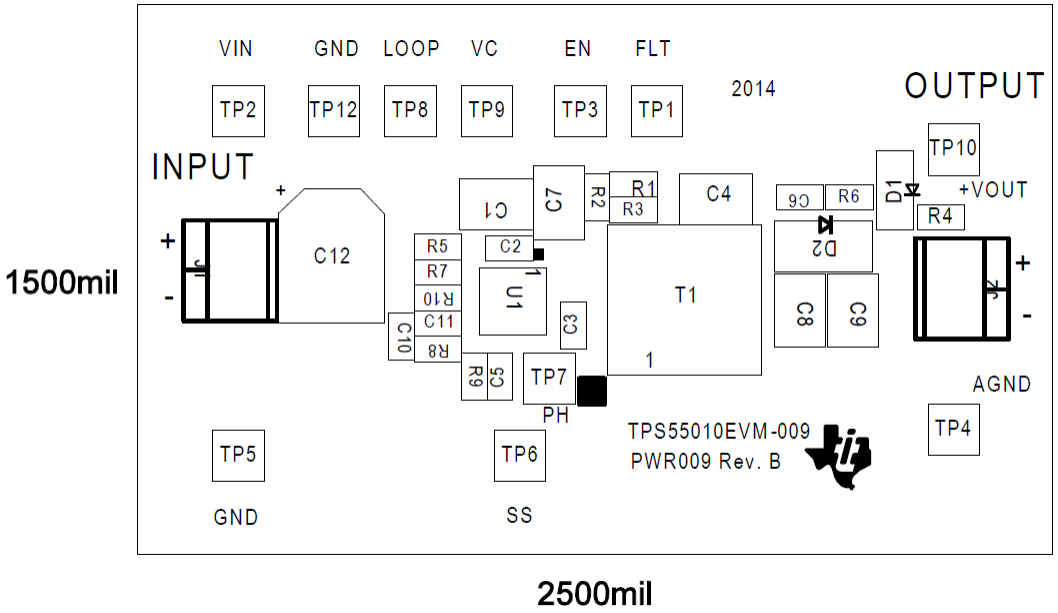

Figure 8. TPS55010EVM-009 Top Assembly

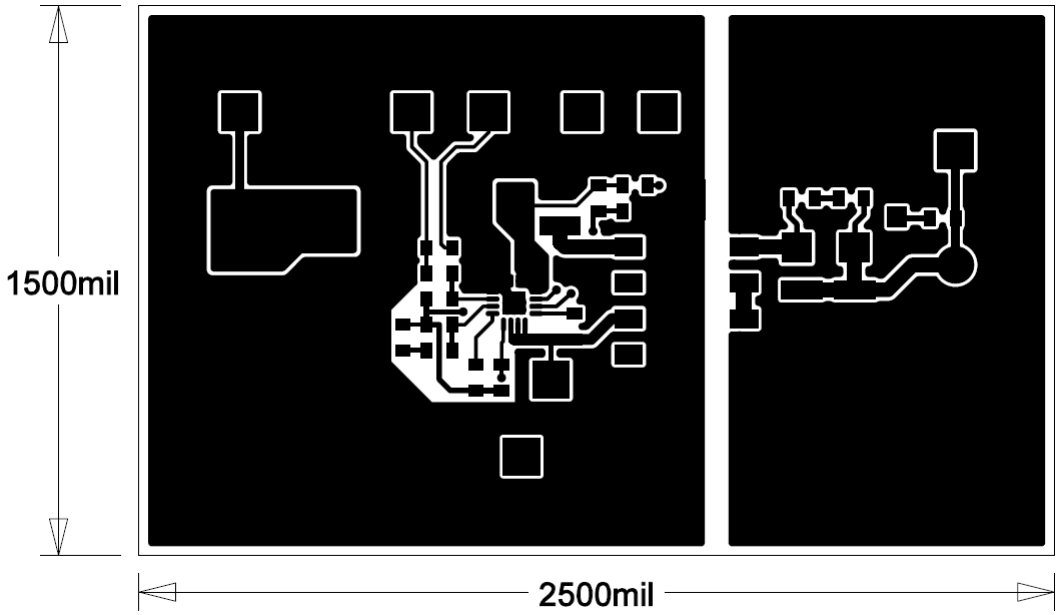

Figure 9. TPS55010EVM-009 Top Copper

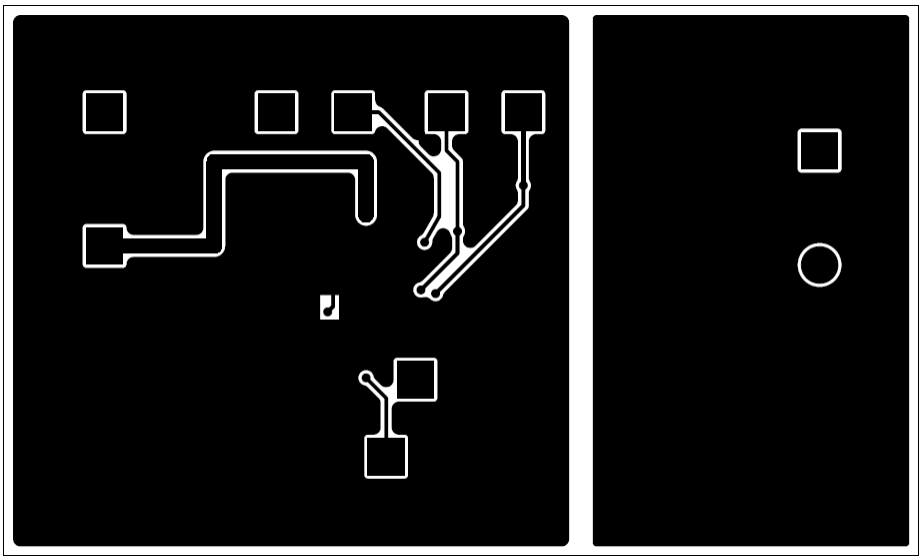

Figure 10. TPS55010EVM-009 Bottom Copper

3.2 Estimated Circuit Area

The estimated printed-circuit board area for the components used in this design is 0.70 in^2. This area does not include test points or connectors.

4 Schematic and Bill of Materials

This section presents the TPS55010EVM-009 schematic and bill of materials.

4.1 Schematic

Figure 11 is the schematic for the TPS55010EVM-009.

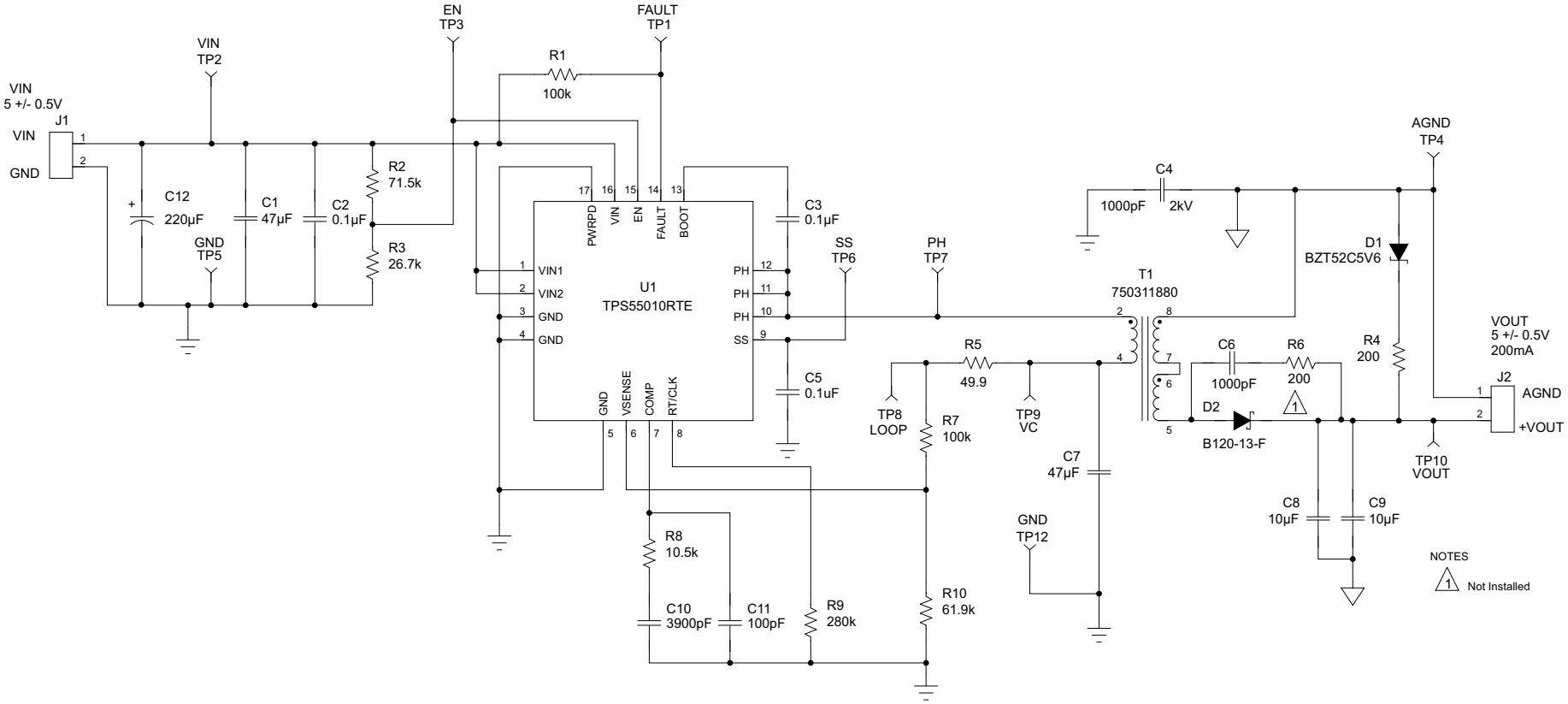

Figure 11. TPS55010EVM-009 Schematic

4.2 Bill of Materials

Table 4 presents the bill of materials for the TPS55010EVM-009.

Table 4. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C7	47µF	Capacitor, Ceramic, 10V, X5R, 10%	1210	Std	Std
3	C2, C3, C5	0.1µF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 10%	0603	Std	Std
1	C4	1000pF	Capacitor, Ceramic, 2kV, X7R, 10%	1210	Std	Std
1	C6	1000pF	Capacitor, Ceramic, Low Inductance, 16V, X7R, 10%	0603	Std	Std
2	C8, C9	10µF	Capacitor, Ceramic, 10V, X5R, 10%	1210	Std	Std
1	C10	3900pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C11	100pF	Capacitor, Ceramic, 50V, NP0, 5%	0603	Std	Std
1	C12	220µF	Capacitor, Aluminum, 6.3V, ±20%	0.260 x 0.276 inch	EEE-FK0J221P	Panasonic
1	D1	BZT52C5V6	Diode, Zener, Planar Power, 500mW, 5.6V	SOD-123	BZT52C5V6-7-F	Diodes, Inc
1	D2	B120-13-F	Diode, Schottky, 1000-mA, 20-V	SMA	B120-13-F	Diodes, Inc
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
2	R1, R7	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	71.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	26.7k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	200	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	200	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R8	DNP	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	280k	Resistor, Chip, 1/16W, 1	0603	Std	Std
1	R10	61.9k	Resistor, Chip, 1/16W, 1	0603	Std	Std
4	TP1, TP3, TP6	5012	Test Point, White, Thru Hole	0.125 x 0.125 inch	5010	Keystone
3	TP2, TP9, TP10	5010	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5010	Keystone
3	TP4, TP5, TP12	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
2	TP7, TP8	5013	Test Point, Orange, Thru Hole	0.125 x 0.125 inch	5013	Keystone
1	T1	2.5µH	Transformer, ±10%	0.410 x 0.510 inch	750311880	Wurth
1	U1	TPS55010RTE	IC, DC-DC Converter	QFN-16	TPS55010RTE	TI
1	--		PCB, 2.5 In x 1.5 In x 0.062 In	2.5" x 2.5" x 0.062"	PWR009	Any

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (June 2014) to B Revision	Page
• Changed schematic values of R7 from 16.5k to 100k and R10 from 10.0 k to 61.9k.	10

Changes from Original (May 2011) to A Revision **Page**

- Changed 7 V to 6 V in background section. 2
- Changed 3 V to 4.5 V in the input voltage and output current summary table and in the first paragraph of the performance specification summary section. 2
- Changed content of the electrical and performance specification table 2
- Changed efficiency graph. 4
- Changed load regulation graph. 4
- Deleted line regulation, VIN = 3.3 V graph. 5
- Changed line regulation graph. 5
- Changed PCB layout images. 8
- Changed schematic diagram. 10
- Changed BOM: moved C7, changed content of C10 and C11 rows. 11

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