Powering the AM335x with the TPS65217x

This User's Guide is a reference for connectivity between the TPS65217 power management IC and the AM335x processor. For detailed information about TPS65217 and AM335x, see the respective data sheets.

1 TPS65217 Overview

The TPS65217 is an optimized and highly integrated power management solution for the AM335x processor. Features of the TPS65217 include:

- Power path management for Lithium-ion battery, USB, and AC inputs
- Linear Battery Charger
- 3 DC/DC Step-Down Converters
- 2 LDOs
- 2 Load Switches (configure as LDOs)
- White LED driver capable of driving up to 20 LEDs

There are four versions of the TPS65217:

TPS65217A is used for the AM335x processor in the ZCE package. In this package, the VDD_MPU and VDD_CORE nodes are shorted together and will only use a single power rail.

TPS65217B is used for the AM335x processor in the ZCZ package. In this package, the VDD_MPU and VDD_CORE rails are separate and can use separate power rails.

TPS65217C is also targeted at the AM335x processor in the ZCZ package, but the DCDC1 output voltage is set to 1.5 V to supply DDR3 memory. This version does not support AM335x RTC-only operation.

TPS65217D is identical to TPS65217C, except DCDC1 is set to 1.35 V to support DDR3L.

PMIC	Processor	Memory
TPS65217A	AM335xZCE	DDR2
TPS65217B	AM335xZCZ	DDR2
TPS65217C	AM335xZCZ	DDR3
TPS65217D	AM335xZCZ	DDR3L

2 Connection Diagram for TPS65217A and AM335x

The block diagram shown in Figure 1 illustrates the connections between TPS65217A and AM335x. Power rails as well as the digital and analog signals are shown. The power rails may be used to power additional parts of the system (DCDC1 powers DDR2 memory).

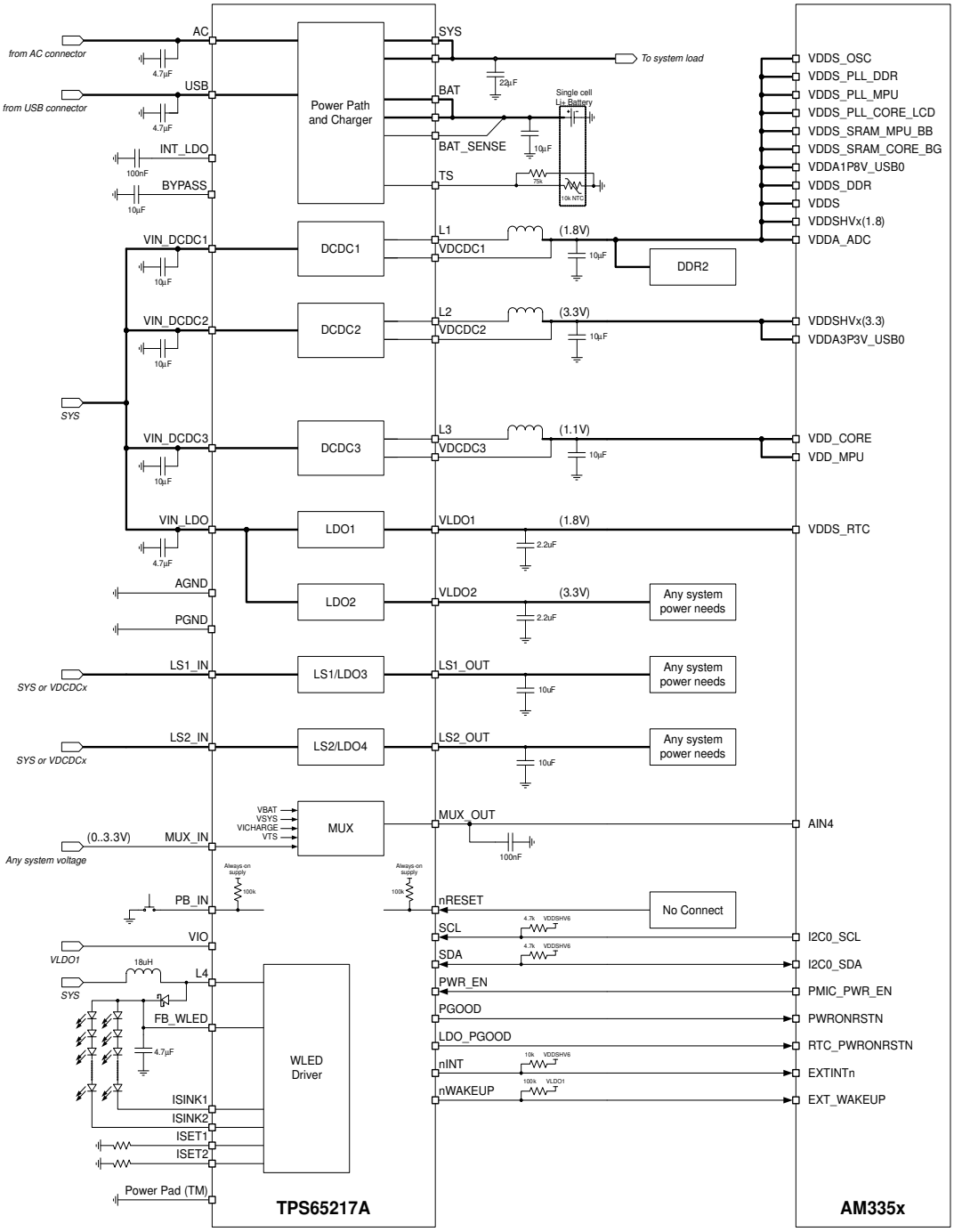


Figure 1. Connection Diagram for TPS65217A and AM335x

3 Power Rails for TPS65217A and AM335x

Table 1 matches the AM335x power terminals with the appropriate power rail from the TPS65217A.

Table 1. Power Rails for TPS65217A and AM335x

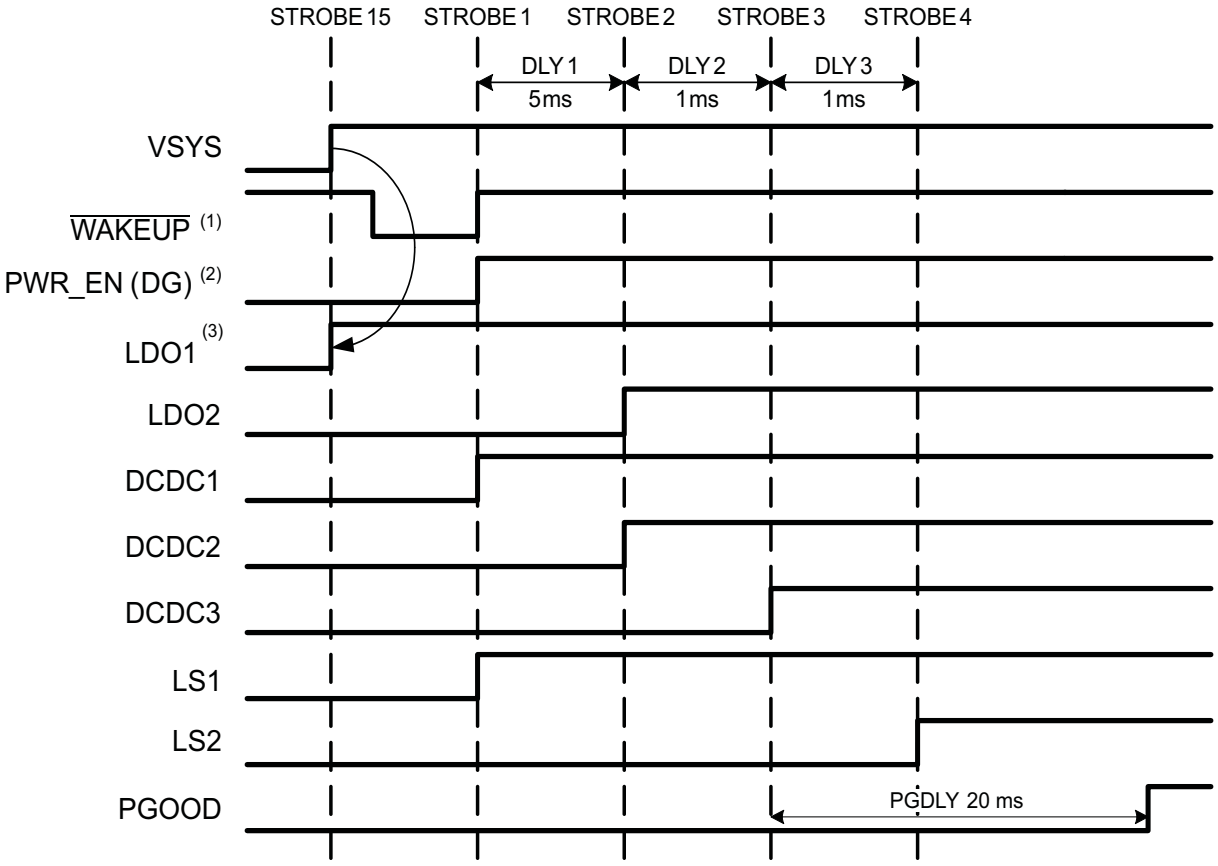
TPS65217A	Voltage (V)	AM335x
DCDC1	1.8	VDDS_DDR
		VDDS
		VDDSHVx(1.8 V)
		VDDS_SRAM_CORE_BG
		VDDS_SRAM_MPU_BB
		VDD_PLL_DDR
		VDDS_PLL_CORE_LCD
		VDDS_PLL_MPU
		VDDS_OSC
		VDDA1P8V_USB0/1
		VDDA_ADC
DCDC2	3.3	VDDSHVx(3.3 V)
		VDDA3P3V_USB0/1
DCDC3	Defaults to 1.1 V. Controlled by I^2C.	VDD_CORE
		VDD_MPU
LDO1	1.8	VDDS_RTC
LDO2	3.3	n/a
LDO3/LS1	Load Switch	n/a
LDO4/LS2	Load Switch	n/a

Each output voltage may be changed dynamically while the TPS65217 is in active mode. This requires use of I^2C commands to the TPS65217.

4 Power-Up Sequence for TPS65217A

Figure 2 and Table 2 describe the power-up sequence of the TPS65217A. This sequence is optimized specifically for the AM335x processor.

NOTE: The power-down sequence follows the reverse of the power-up sequence.



(1) Wakeup↓ events are PB_IN↓ or AC↑ or USB↑

(2) DG = Deglitched

(3) LDO1 turns on as soon as VSYS is present

LDO_PGOOD↑ 20 ms after LDO1↑

Figure 2. Power-Up Sequence Timing Diagram, TPS65217A

Table 2. TPS65217A, Power-Up Sequence

STROBE 15	LDO1
STROBE 1	DCDC1
	LS1
STROBE 2	DCDC2
	LDO2
STROBE 3	DCDC3
STROBE 4	LS2

5 Connections Diagram for TPS65217B and AM335x

The block diagram shown in Figure 3 illustrates the connections between TPS65217B and AM335x. Power rails as well as the digital and analog signals are shown. The power rails may be used to power additional parts of the system (DCDC1 powers DDR2 memory).

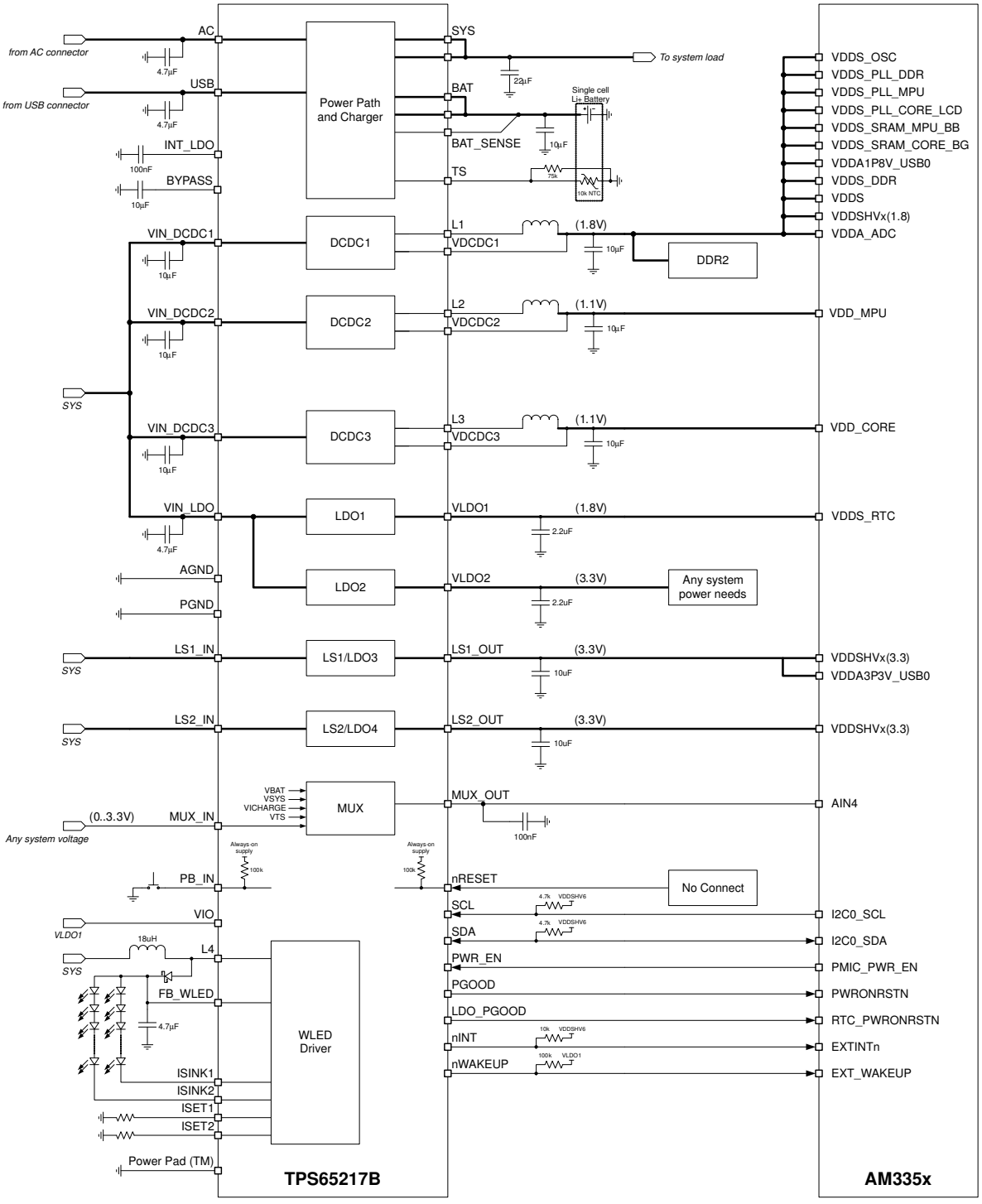


Figure 3. Connection Diagram for TPS65217B and AM335x

6 Power Rails Connections for TPS65217B and AM335x

Table 3 matches the AM335x power terminals with the appropriate power rail from the TPS65217B.

Table 3. Power Rails for TPS65217B and AM335x

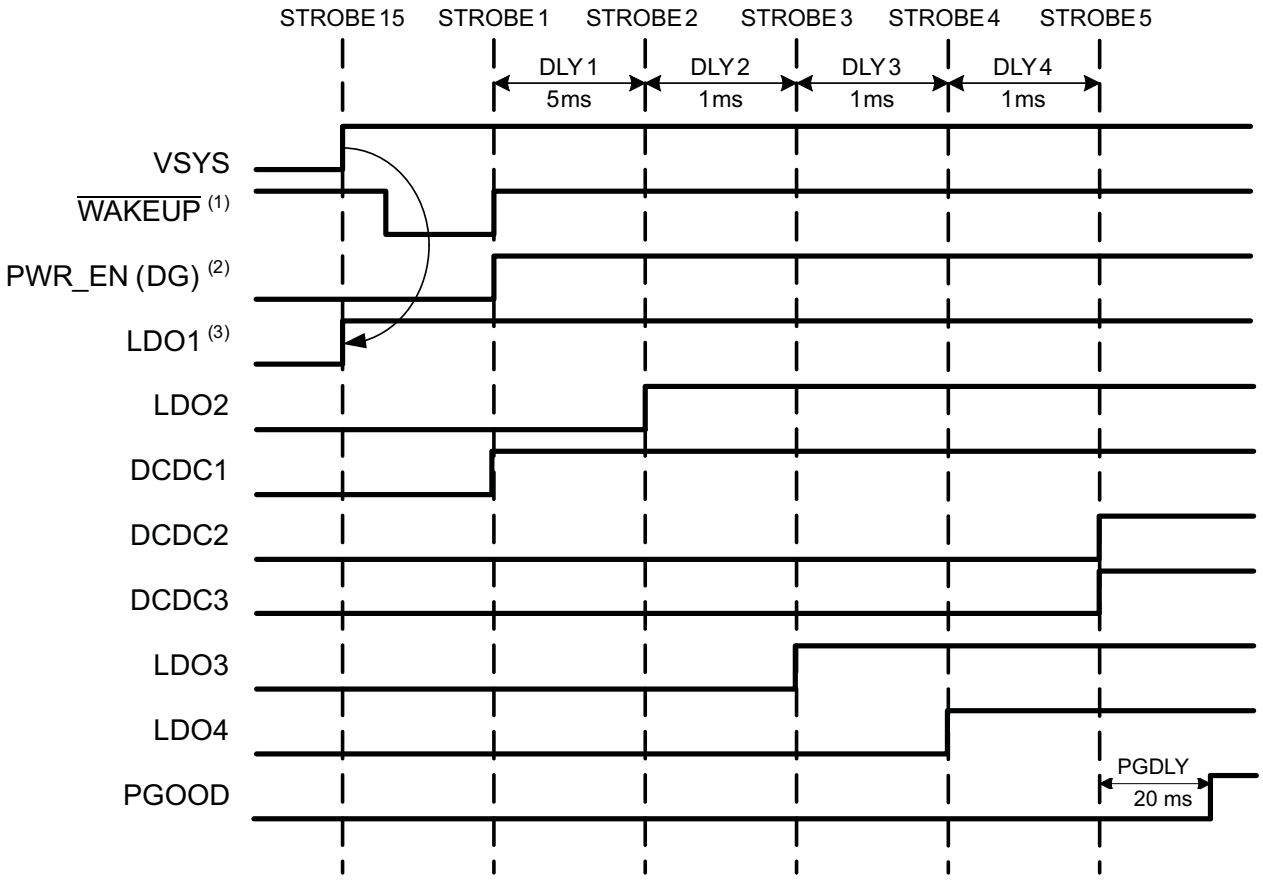
TPS65217B	Voltage (V)	AM335x
DCDC1	1.8	VDDS_DDR
		VDDS
		VDDSHVx(1.8 V)
		VDDS_SRAM_CORE_BG
		VDDS_SRAM_MPU_BB
		VDD_PLL_DDR
		VDDS_PLL_CORE_LCD
		VDDS_PLL_MPU
		VDDS_OSC
		VDDA1P8V_USB0/1
		VDDA_ADC
DCDC2	Defaults to 1.1 V. Controlled by I^2C.	VDD_MPU
DCDC3	Defaults to 1.1 V. Controlled by I^2C.	VDD_CORE
LDO1	1.8	VDDS_RTC
LDO2	3.3	n/a
LDO3/LS1	3.3 (LDO)	VDDSHVx(3.3 V)
		VDDA3P3V_USB0/1
LDO4/LS2	3.3 (LDO)	VDDSHVx(3.3 V)

Each output voltage may be changed dynamically while the TPS65217 is in active mode. This requires use of I^2C commands to the TPS65217.

7 Power-Up Sequence for TPS65217B

Figure 4 and Table 4 describe the power-up sequence of the TPS65217B. This sequence is optimized specifically for the AM335x processor.

NOTE: The power-down sequence follows the reverse of the power-up sequence.



(1) Wakeup↓ events are PB_IN↓ or AC↑ or USB↑

(2) DG = Deglitched

(3) LDO1 turns on as soon as VSYS is present

LDO_PGOOD↑ 20 ms after LDO1↑

Figure 4. Power-Up Sequence Timing Diagram, TPS65217B

Table 4. TPS65217B Power-Up Sequence

STROBE 15	LDO1
STROBE 1	DCDC1
STROBE 2	LDO2
STROBE 3	LDO3
STROBE 4	LDO4
STROBE 5	DCDC2
	DCDC3

8 Connections Diagram for TPS65217C and AM335x

The block diagram shown in Figure 5 illustrates the connections between TPS65217C and AM335x. Power rails as well as the digital and analog signals are shown. The power rails may be used to power additional parts of the system (DCDC1 powers DDR3 memory).

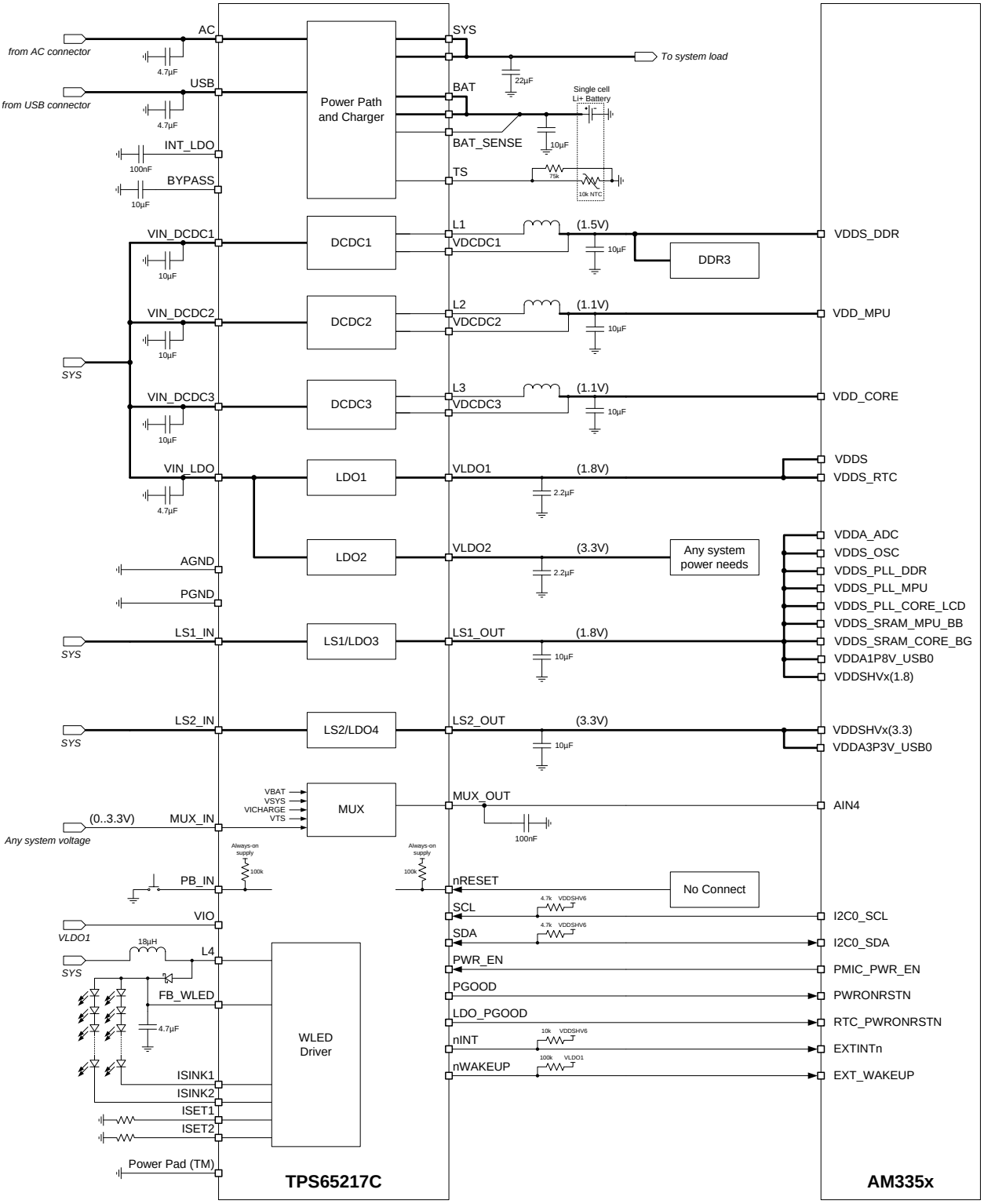


Figure 5. Connection Diagram for TPS65217C and AM335x

9 Power Rails Connections for TPS65217C and AM335x

Table 5 matches the AM335x power terminals with the appropriate power rail from the TPS65217C.

Table 5. Power Rails for TPS65217C and AM335x

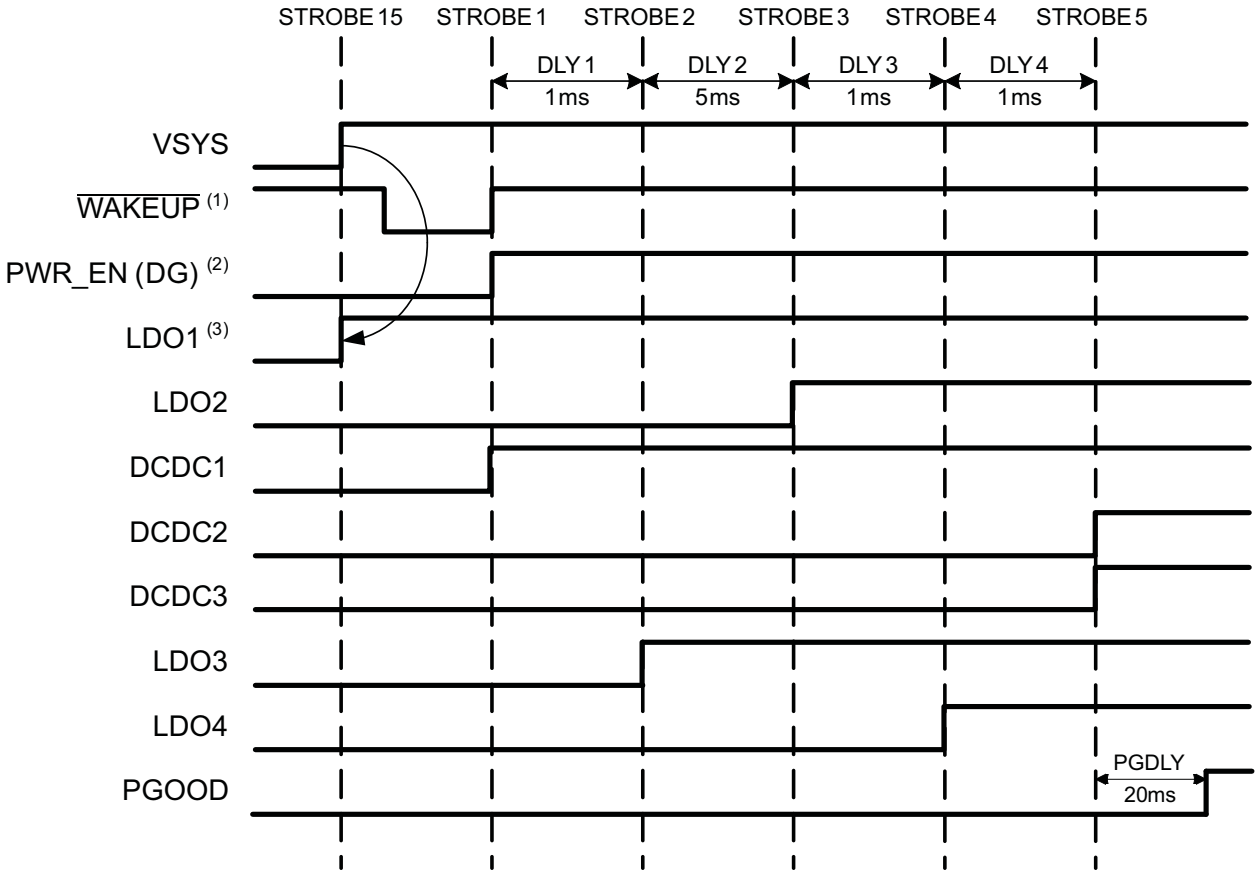
TPS65217C	Voltage (V)	AM335x
DCDC1	1.5	VDDS_DDR
DCDC2	Defaults to 1.1 V. Controlled by I^2C.	VDD_MPU
DCDC3	Defaults to 1.1 V. Controlled by I^2C.	VDD_CORE
LDO1	1.8	VDDS_RTC
		VDDS
LDO2	3.3	n/a
LDO3/LS1	1.8	VDDSHVx(1.8 V)
		VDDS_SRAM_CORE_BG
		VDDS_SRAM_MPU_BB
		VDDS_PLL_DDR
		VDDS_PLL_CORE_LCD
		VDDS_OSC
		VDDA1P8V_USB0/1
		VDDA_ADC
LDO4/LS2	3.3	VDDSHVx(3.3 V)
		VDDA3P3V_USV0/1

Each output voltage may be changed dynamically while the TPS65217 is in active mode. This requires use of I^2C commands to the TPS65217.

10 Power-Up Sequence for TPS65217C

Figure 6 and Table 6 describe the power-up sequence of the TPS65217C. This sequence is optimized specifically for the AM335x processor.

NOTE: The power-down sequence follows the reverse of the power-up sequence.



(1) Wakeup↓ events are PB_IN↓ or AC↑ or USB↑

(2) DG = Deglitched

(3) LDO1 turns on as soon as VSYS is present

LDO_PGOOD↑ 20 ms after LDO1↑

Figure 6. Power-Up Sequence Timing Diagram, TPS65217C

Table 6. TPS65217C Power-Up Sequence

STROBE 15	LDO1
STROBE 1	DCDC1
STROBE 2	LDO3
STROBE 3	LDO2
STROBE 4	LDO4
STROBE 5	DCDC2
	DCDC3

11 PGOOD and LDO_PGOOD Outputs

PGOOD and LDO_PGOOD are push-pull outputs. These outputs are supplied by the VIO pin. During TPS65217 SLEEP mode, all power rails are typically turned off except for LDO1. In order for LDO_PGOOD to remain high during SLEEP mode, connect the VIO pin to LDO1. This allows the LDO_PGOOD signal to be valid even during SLEEP mode. With VIO connected to LDO1, PGOOD and LDO_PGOOD have an output high level of 1.8 V. This level meets the requirements of the PWRONRSTN and RTC_PWRONRSTN input signals of the AM335x processor.

12 MUX_OUT Scaling

The AINx ADC input of the AM335x processor is powered by VDDA_ADC. Therefore the maximum voltage input to the ADC should be 1.8 V. If the output voltage of MUX_OUT will be higher than 1.8 V in your application, then add a resistor divider inbetween MUX_OUT and AINx, such that the voltage at AINx does not exceed 1.8 V. The resistor values must be large enough such that the load on MUX_OUT is low. However, the resistors should not be so large as to impact the performance of the ADC.

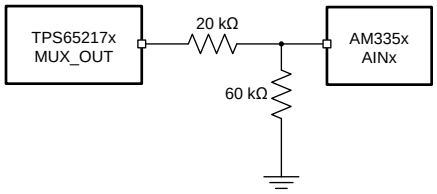


Figure 7. MUX_OUT Scaling Example

13 Pull-Up Resistors

There are four pull-up resistors on the connection diagrams; Figure 1, Figure 3, and Figure 5. nWAKEUP should be pulled up to VLDO1 so that the pull-up source is present even during SLEEP mode. A 100-kΩ pull-up resistor should be used for nWAKEUP to minimize the current load on LDO1. nINT, SCL, and SDA should be pulled up to the same supply that is connected to VDDSHV6. If VDDSHV6 is 1.8 V, then the 1.8-V supply should be used. If VDDSHV6 is 3.3 V, then the 3.3-V supply should be used. SCL and SDA use lower value pull-up resistors in order to decrease rise time of these nodes during I^2C communication.

Revision History

Changes from G Revision (March 2013) to H Revision	Page
• Changed connection diagram for TPS65217C and AM335x.	8
• Changed table contents in Power Rails for TPS65217C and AM335x.	9

Revision History

Changes from H Revision (January 2014) to I Revision	Page
• Changed connection diagram for TPS65217C and AM335x.	8

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