Evaluation Module for the TPS65235 LNB Voltage Regulator With I²C Interface for DiSEqC2.x Application

This document presents the information required to operate the TPS65235 for DiSEqC2.x application as well as the support documentation including schematic, layout, hardware setup, software application, key waveforms, and bill of materials.

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List of Tables

1 Introduction

The TPS65235 device is designed to provide 13-V and 18-V output voltage for satellite receiver, with an operational range of 4.5 V to 16 V.

TPS65235 features I^2C controlled output voltage from 11 V to 20 V with 16 options; output current limit with +/-10% accuracy is set by ISET pin connecting different resistors. The maximum output current limit is up to 1 A.

TPS65235 can also run without I^2C. In non-I^2C mode, the SCL pin and VCTRL pin are used to control 13-V and 18-V output. These two pins can be controlled by GPIO from a processor. A dedicated enable pin EN, is available to turn the LNB output on and off.

The evaluation module is designed to provide access to the features of the TPS65235 for DiSEqC2.x application. While PWR747 is designed for DiSEqC1.x application, some modifications can be made to this module to test performance at different input and output voltages, current, and switching frequency. Contact TI Field Applications Group for advice on these matters.

2 Schematic

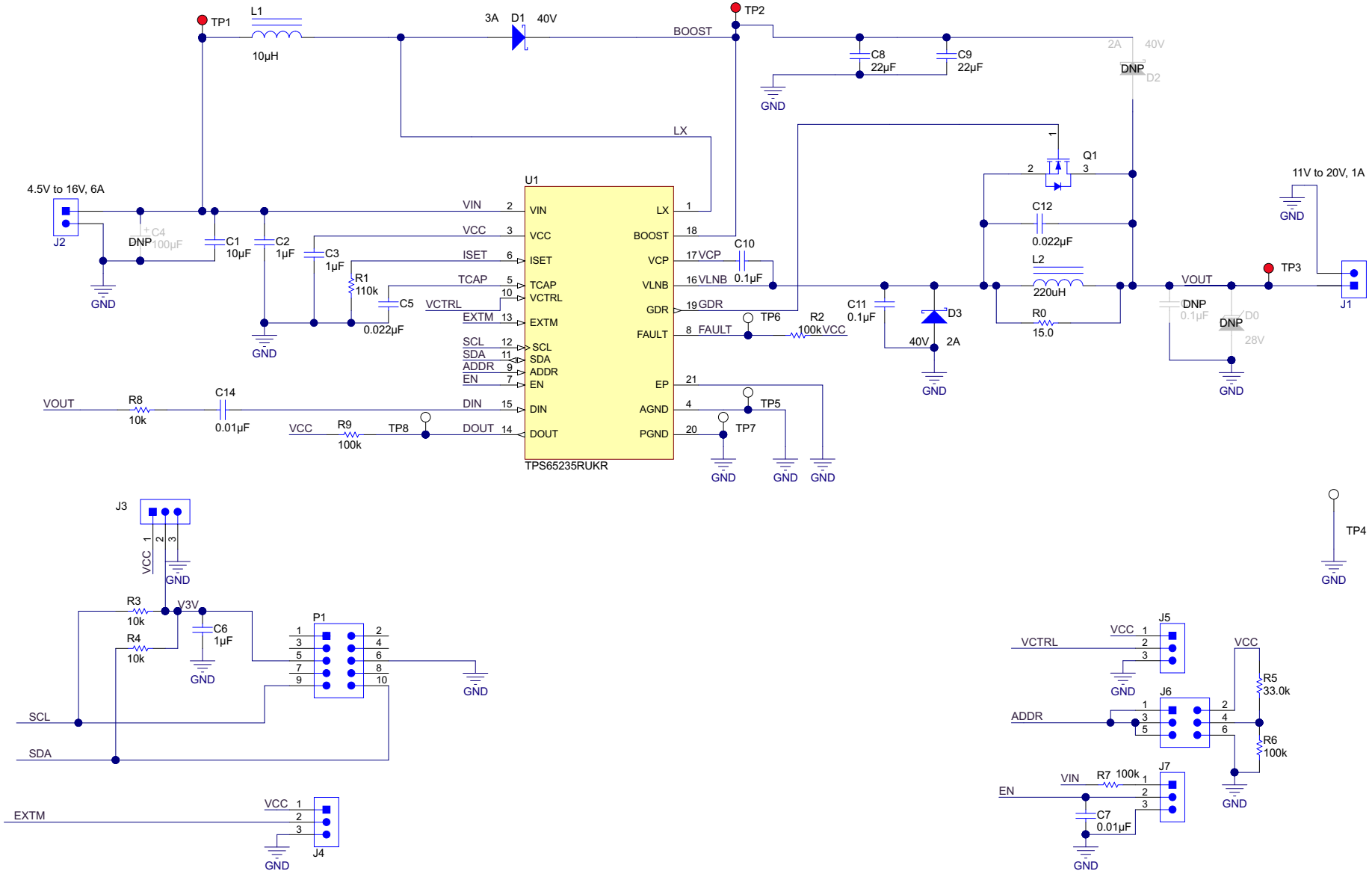

Figure 1. TPS65235 EVM Schematic for DiSEqC 2.x Application

In the TPS65235 application, the recommended ceramic capacitors rated are at least X7R and X5R, 35-V rating and 1206 size for achieving lower LNB output ripple. For this EVM, two 22-µF, 35-V capacitors, C8 and C9, are put at the output of the boost converter. If lower cost is demanded, a 100-µF electrolytic (low ESR) and a 10-µF and 35-V ceramic capacitor also works well.

3 Board Layout

Figure 2 shows the component placement on the EVM. Figure 3 and Figure 4 illustrate the top and bottom layers, respectively.

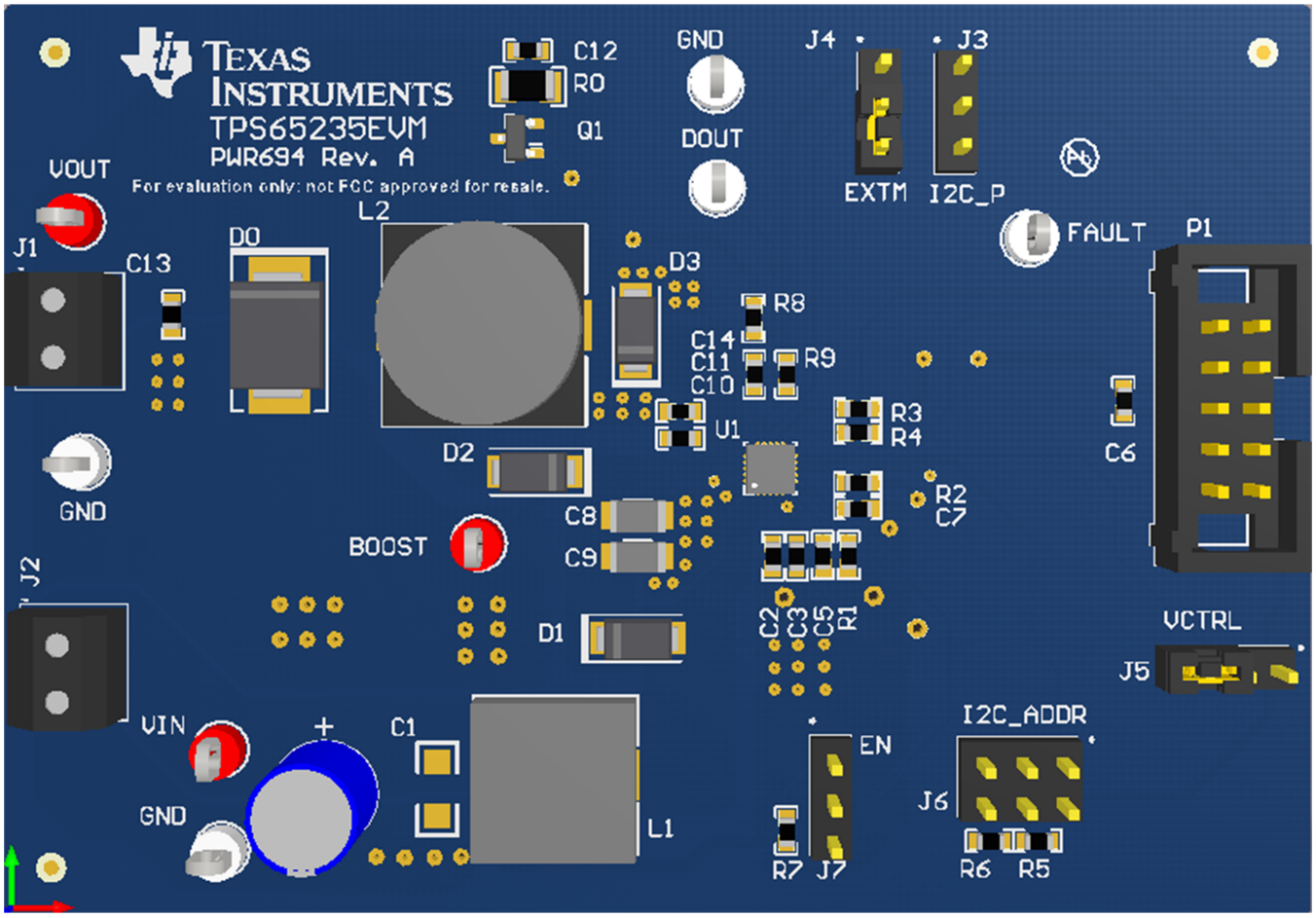

Figure 2. Component Placement (Top Layer)

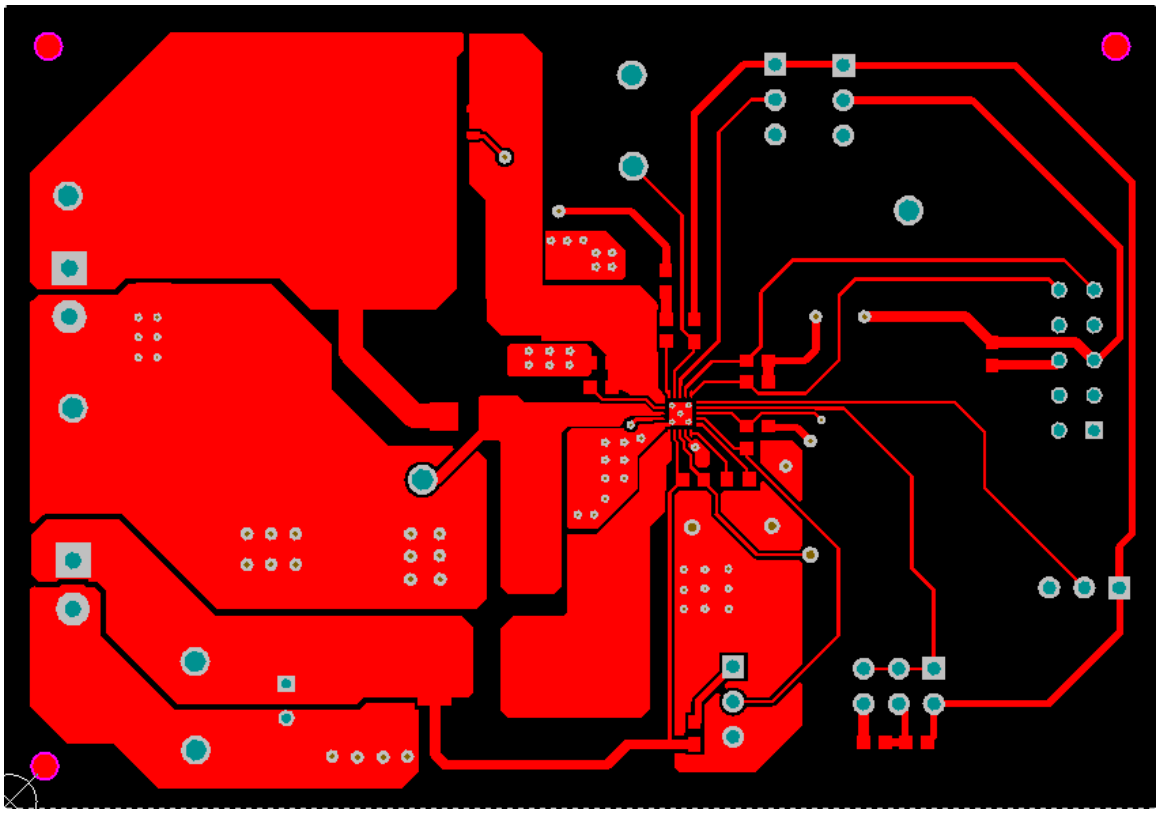

Figure 3. Board Layout (Top Layer)

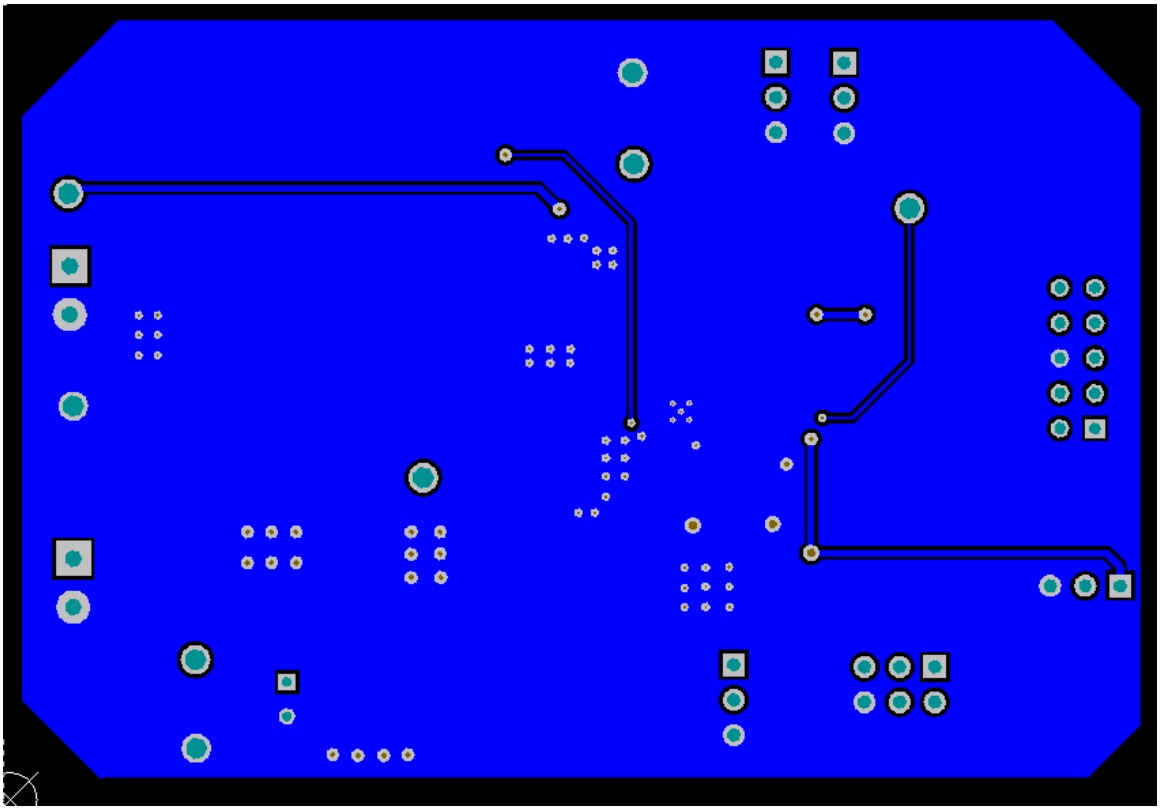

Figure 4. Board Layout (Bottom Layer)

4 Bench Test Setup Conditions

4.1 Headers Description and Jumper Placement

Figure 5 shows the header descriptions and jumper placement.

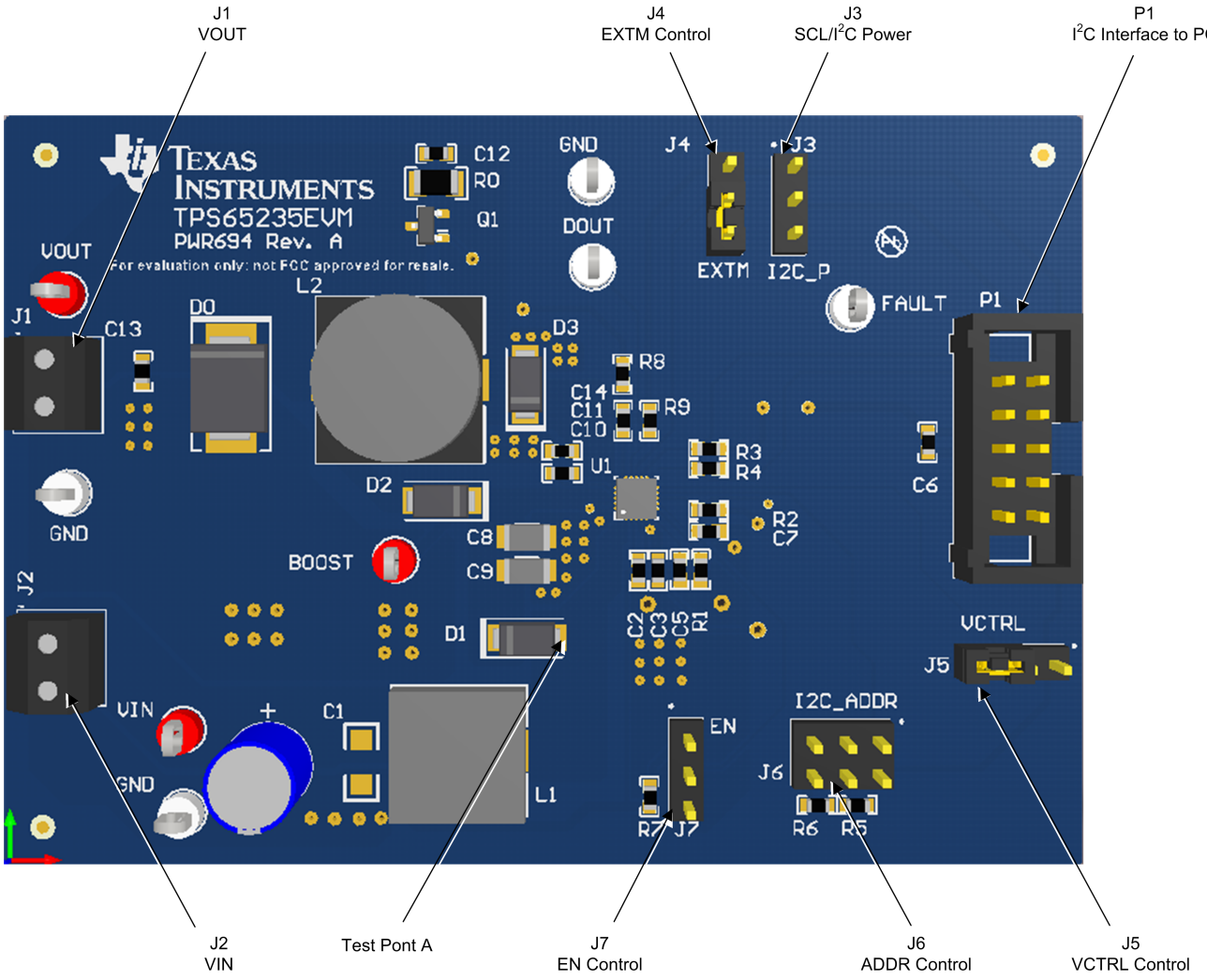

Figure 5. Headers Description and Jumper Placement

Test points:

A: LX for Boost

Notes:

- At non-I²C mode, P1 should be floating, J5 and J3 are used to set the output, refer to Table 3.
- At I²C mode, P1 is connected to the PC through the USB-TO-GPIO box, which makes the SCL signal to be high. J5 can be used to set the default output when powered on, refer to Table 3.
- P1 and J3 cannot be connected at the same time.

Table 1 lists the I/O connections and Table 2 lists the EVM jumpers and switches.

Table 1. Input and Output Connection

#	Function	Description
J1	VOUT Connector	VLNB output
J2	Vin Connector	Apply power supply through this connector

Table 2. Jumpers and Switches

#	Function	Placement	Comment
J3	Output voltage control (SCL)	If the IC is not controlled by I^2C, VCTRL pin and SCL pin are combined to control the VLNB output voltage. Refer to Table 3. Jumper J3-2 and J3-1 makes SCL to VCC connection and gives VLNB with output 14.6 V or 19.4 V. Jumper J3-2 and J3-3 makes SCL to GND connection and gives VLNB with output 13.4 V or 18.2 V.	
	I^2C Power	If the IC is controlled by I^2C, this is used to provide the I^2C power which is connected to the SCL and SDA through pull-up resistors. Leaving non jumper connected sets the power to be 3.3 V from the I^2C interface adapter. Shorting the J3-1 and J3-2 by jumper sets the power to be VCC.	On board VCC is 6.3 V
J4	Tone control (EXTM)	Toggle the EXTM signal (J4-2 to J4-3 and then J4-2 to J4-1), the internal tone signal is superimposed at the VLNB output VOUT. EXTM to GND (J4-2 to J4-3), no internal tone signal is superimposed at the VOUT.	
J5	Output voltage control (VCTRL)	If the IC is not controlled by I^2C, VCTRL pin and SCL pin are combined to control the VLNB output voltage. Refer to Table 3. Jumper J5-2 and J5-1 makes VCTRL to VCC connection and gives VLNB with output 18.2 V or 19.4 V. Jumper J5-2 and J5-3 makes VCTRL to VCC connection and gives VLNB with output 13.4 V or 14.6 V.	
J6	I^2C address set (ADDR)	This pin is the I^2C address set pin: tie to VCC sets I^2C address with 0x08H; floating sets I^2C address with 0x09H; tie to GND sets I^2C address with 0x10H; Resistor divider R9A and R9B make ADDR pin at the voltage to set the I^2C address with 0x11H. Refer to Table 4.	With 3 V-> VCC- 0.8 V will set the I^2C address 0x11H
J7	VLNB output enable (EN)	Jumper EN to GND disables the VLNB output (short J7-2 to J7-3). Jumper EN to Vin through a 100-kΩ resistor enables the VLNB output (short J7-2 to J7-1). Leaving J7 open also enables VLNB output.	

Table 3. VLNB Output Control Without I^2C Interface Connection

EN	SCL	VCRTL	VLNB
H	H	H	19.4 V
H	H	L	14.6 V
H	L	H	18.2 V
H	L	L	13.4 V
L	X	X	0 V

4.2 Hardware Requirement

This EVM requires an external power supply capable of providing 4.5 V to 16 V at 4 A.

The EVM kit includes USB-TO-GPIO interface box which, when installed on a PC and connected to the EVM, allows the user to communicate with the EVM through a GUI interface. The minimum PC requirements are:

- Windows™ 2000, Windows XP or Windows 7 operating system
- USB port
- Minimum of 30 MB of free hard disk space (100 MB recommended)
- Minimum of 256 MB of RAM

4.3 Hardware Setup

After connecting the power supply to J2, floating J7, connect J3, J4, and J5 to GND, J6 and P1 floating, turning on the power supply, the EVM will regulate the output voltages to 13.4 V without tone superimposed.

Perform the following steps to change the output voltage by sending the digital control signal through a PC running the TPS65235 Controller software and USB-TO-GPIO interface box:

- Connect one end of the USB-TO-GPIO box to the PC using the USB cable and the other end to P1 of the TPS65235 using the supplied 10-pin ribbon cable per Figure 6. The connectors on the ribbon cable are keyed to prevent incorrect installation.
- Floating J3.
- Connect the power supply on J2, and turn on the power supply.
- Run the software as explained in Section 5.

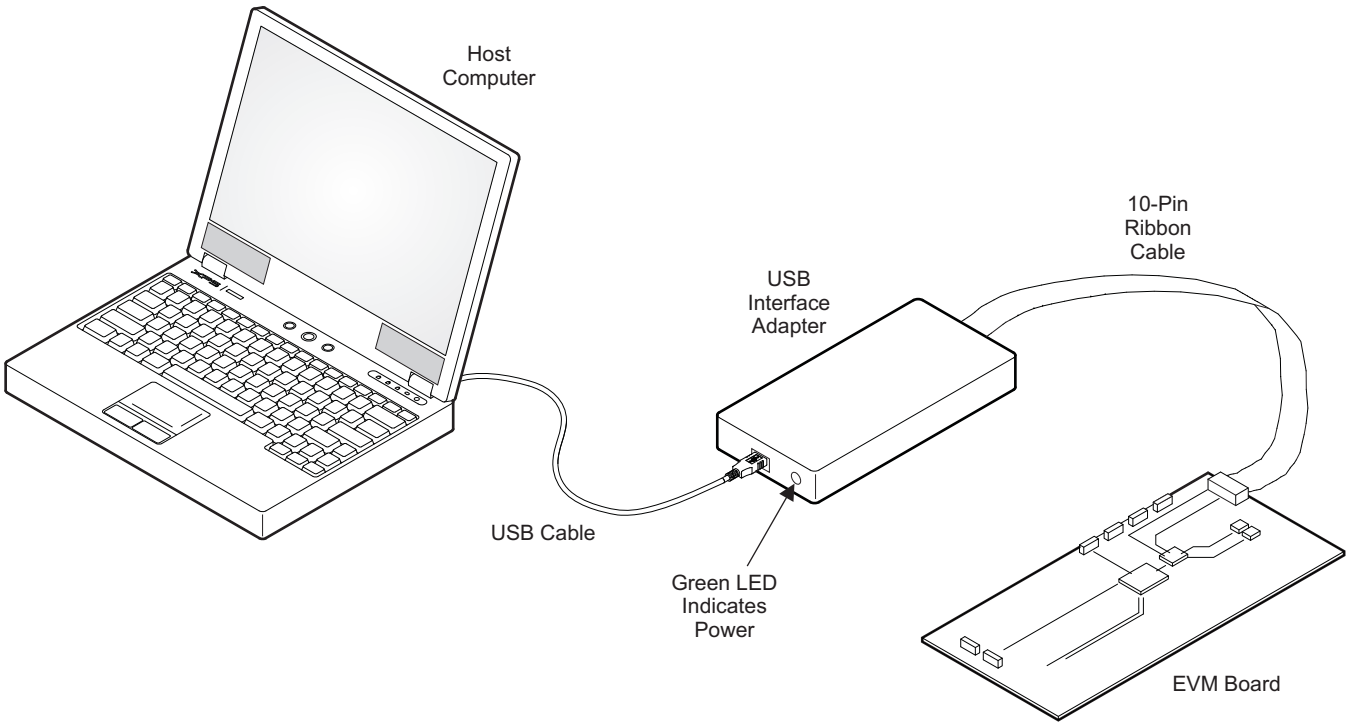

Figure 6. USB Interface Adapter Quick Connection Diagram

5 Software Installation

If installing from the TI Web site, visit SLVC651.

NOTE: This installation page is best viewed with Microsoft Internet Explorer® browser (it may not work correctly with other browsers).

1. Click on the install button; the PC should display a security warning and ask if you want to install this application. Select Install to proceed.
2. To run the software after installation, either use the desktop icon, which is created by the installer if the user agrees to creating a desktop icon, or go to Start → All programs → Texas Instruments → TPS65235.

At start-up, the software first checks the firmware version of the USB-to-GPIO adapter box. If an incorrect firmware version is installed, the software automatically searches the Internet (if connected) for updates. If a new update is available, the software notifies the user of the update then downloads and installs the software. Note that after the firmware is updated, the user must disconnect and then reconnect the USB cable between the adapter and PC, as instructed during the install process. The host PC software also automatically searches on the Internet (if connected) for updates. If a new update is available, the software notifies the user of the update and downloads and installs it. During future use of the software, you are prompted to install a new version if one becomes available on the Web.

NOTE: VERISIGN® Code Signing is used to prevent any malicious code from changing this application. If at any time in the future the binaries are modified, the code will no longer attempt to run.

6 Software Operation

This section provides descriptions of the EVM software.

The supplied software is used to communicate with the TPS65235EVM. Click on the icon on the host computer to start the software. The software first displays the home page for the user interface. Two entrances are available for the expert user or beginner.

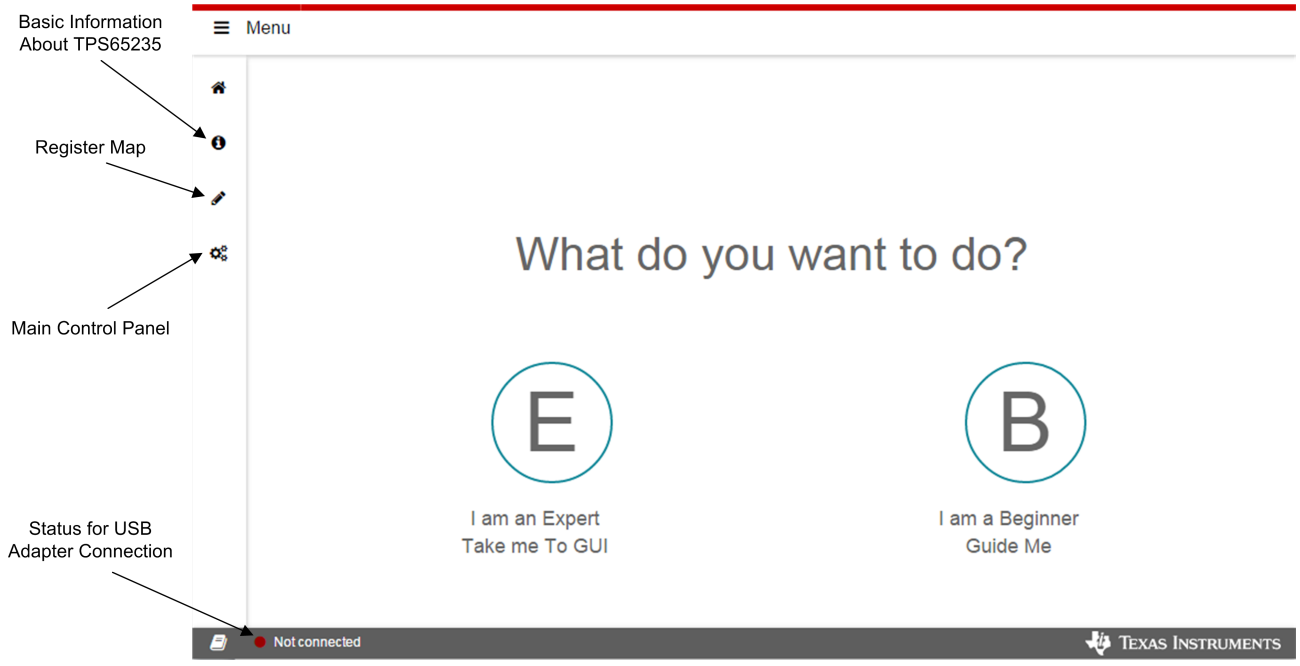

Figure 7. Home Page for GUI Interface

By clicking on the *B* button, the *Basic information about TPS65235* page comes up which lists the features and application information for TPS65235. Follow the steps to do the basic check for the EVM. The GUI will guide the beginner to setup the EVM and GUI.

6.1 Register Map Page

By clicking the *E* button, the Register Map interface comes out. See Figure 8.

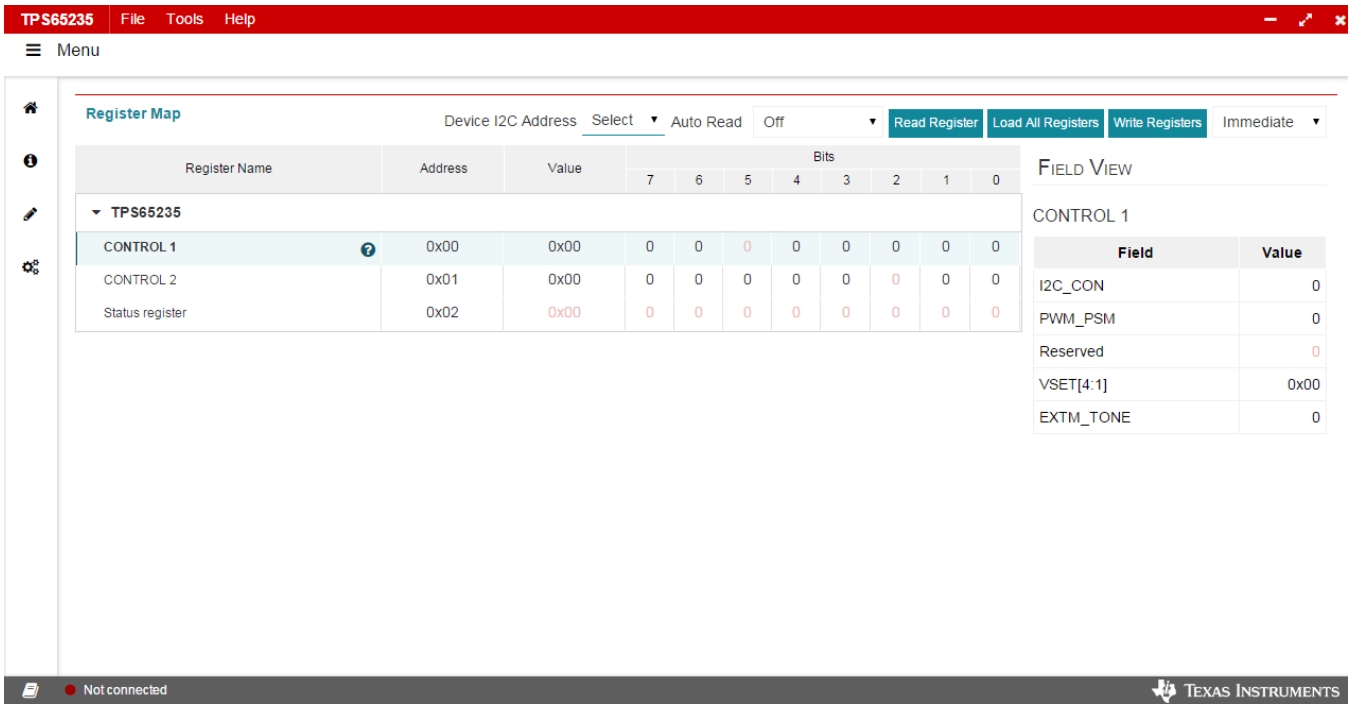

Figure 8. Register Map Page for GUI

Single click on a register name to show *FIELD VIEW*. This shows the detail setting of each bit.

Double click on the bit to change the bit to 0 or 1.

Single click the *?* for the register name to show the detail description page for the register.

For *Write Registers* option, when the *Immediate* option is selected, any change is sent to the EVM immediately; otherwise, *Write Registers* button for each register must be clicked to send the control signal. Register values can be read back from the EVM by clicking *Read Register* for each register or *Load All Registers* or set the *Auto Read* option.

The Status for USB Adapter Connection, only shows the status for the adapter, not the EVM board. The user can select the Write Registers on Register Map page to check whether the board communication is ok or not.

6.2 Basic Settings

Click on the main control panel to show the *Basic Settings* interface. This interface allows the user to set the registers easily. By clicking *Auto Read*, the status is monitored automatically.

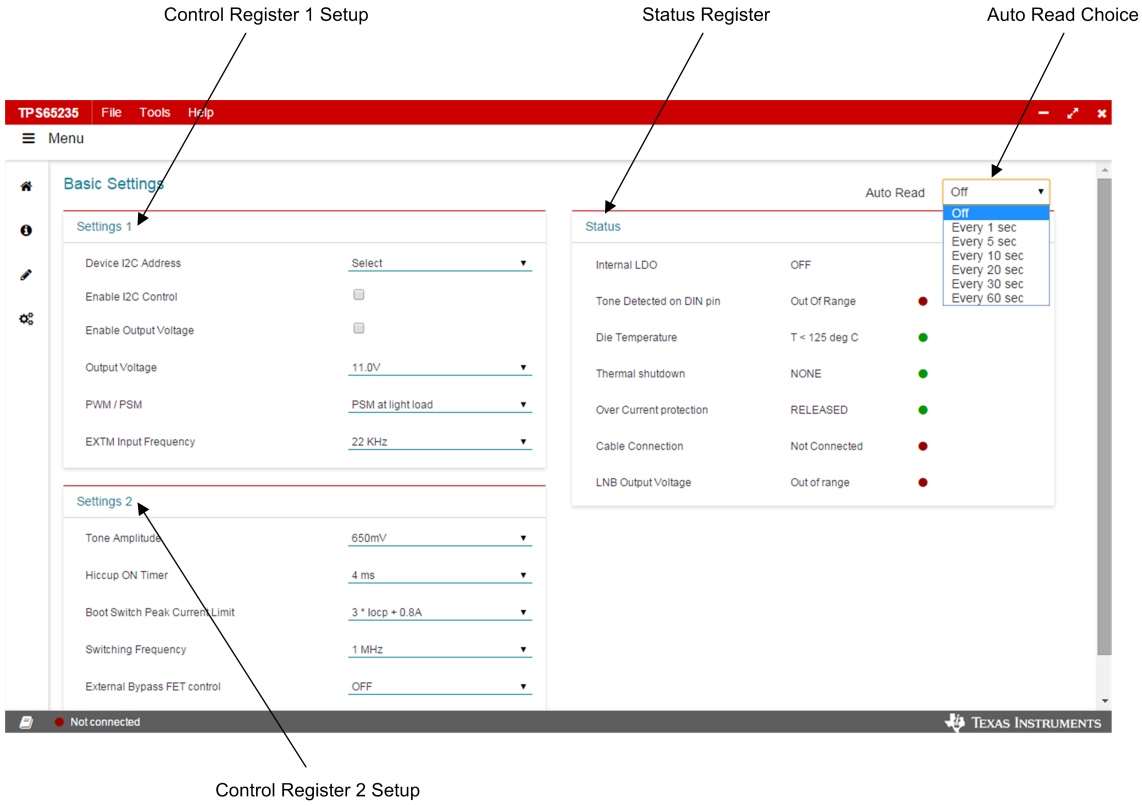

Figure 9. Main Control Panel for GUI

Figure 7 through Figure 9 show the control GUI interface. There are three 8-bit registers embedded in TPS65235, two to control the output voltage characteristics and one for status feedback. Select and check the components on the *Basic Settings* page in the GUI to change the settings, or by also directly clicking the bits of each register on the Register Map page. I²C address is set by J6 for ADDR pin controlling, refer to Table 2 and Table 4.

Table 4. I²C Address Selection

ADDR Pin	I²C Address
Connect to VCC	0x08H
Floating	0x09H
Connected to GND	0x10H
Resistor divider makes voltage in ADDR pin range from 3 V to VCC - 0.8 V	0x11H

7 Test Procedure Example

7.1 Voltage output check

Use the following voltage output checks while testing the EVM:

1. Connect I²C adapter to P1
2. Floating J3, J6, and J7, J4 to GND, J5 to GND
3. Apply 12 V to J2
4. Apply loads or non load to the output connector J1, check the output
5. Set the control register 0x00H and 0x01H to the expected output value and then check the output
6. Monitor the status register 0x02H for the IC status

7.2 Tone Output

Use the following tone output checks while testing the EVM:

1. Connect I²C adaptor to P1
2. Floating J3, J6, and J7, J5 to GND
3. Apply 12 V to J2
4. Toggle the EXTM (J4) from low to high, check the tone output at VOUT
5. Apply loads or non-load to the output connector J1, check the output

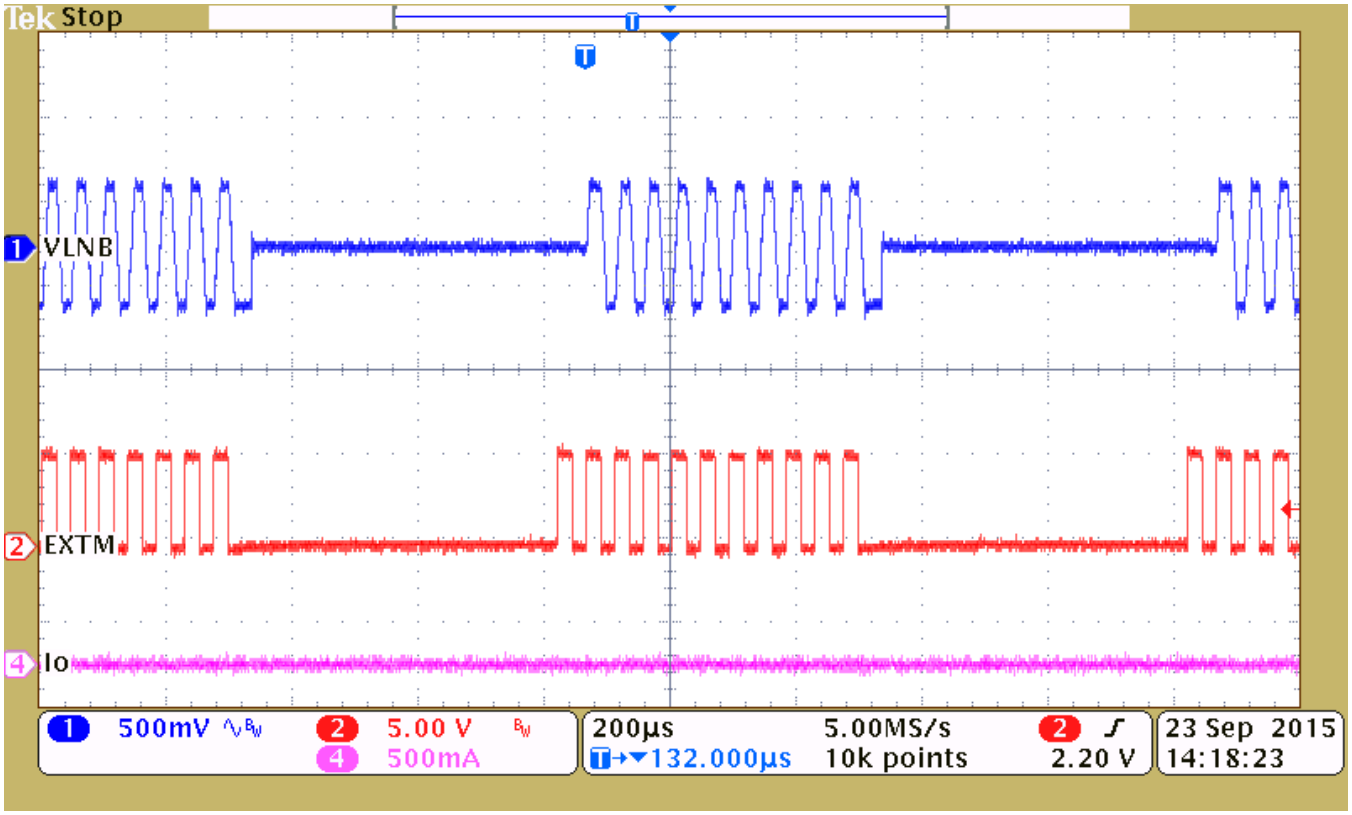

Figure 10. EXTM Has 22-kHz External Tone Input

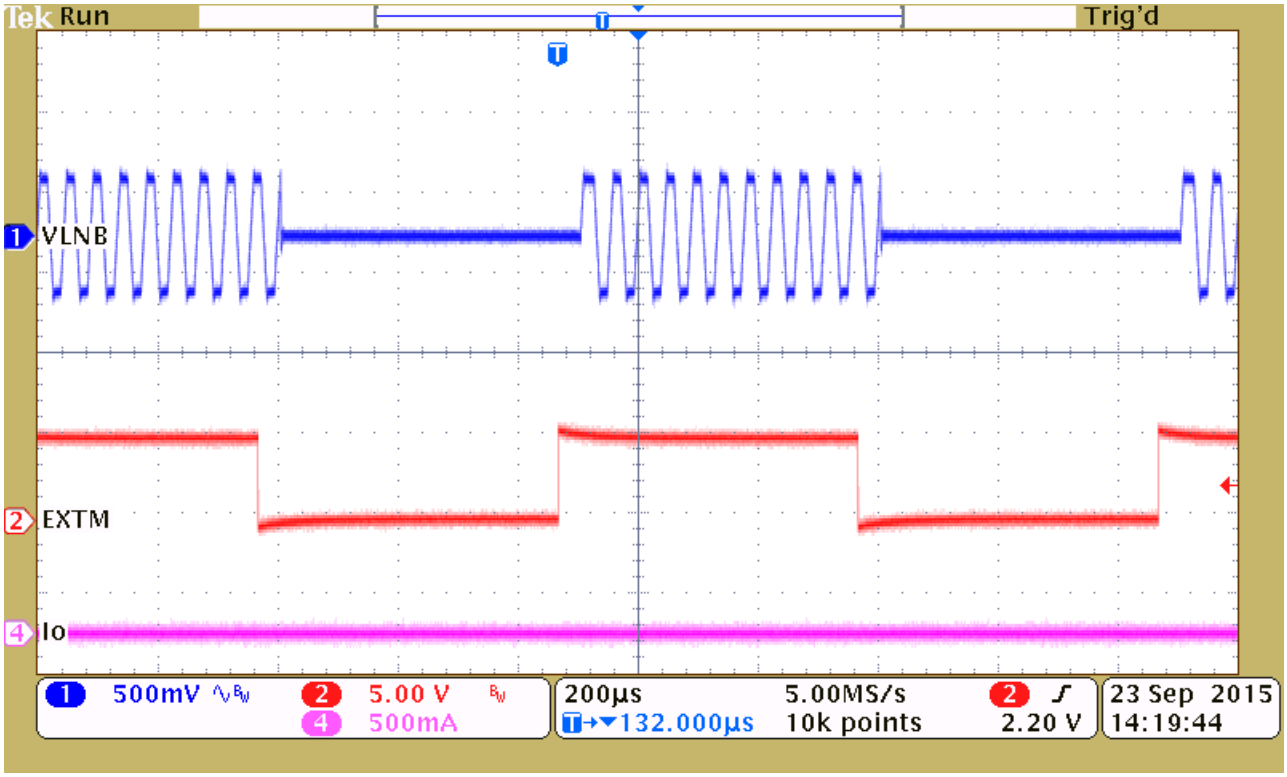

Figure 11. EXTM Has Envelope Input for Tone Output Control

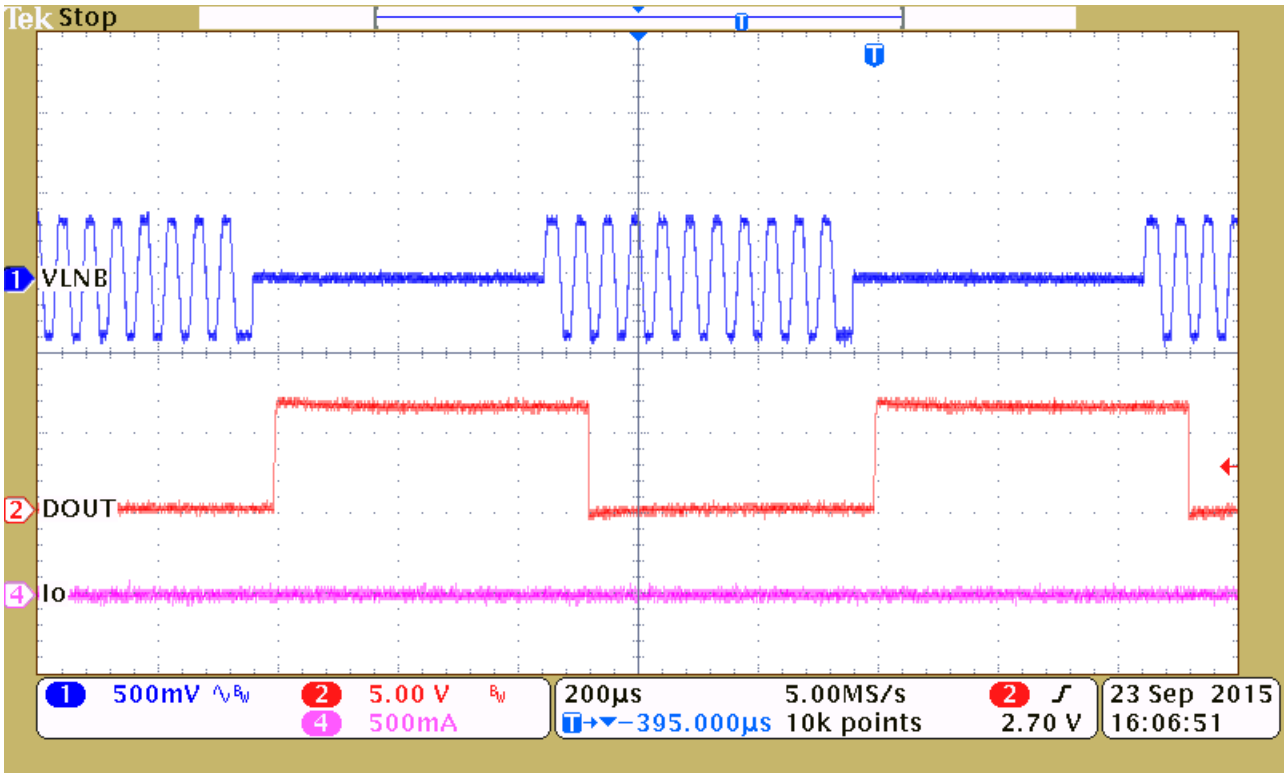

Figure 12. DOUT Output When Tone Received

8 Bill of Materials

Table 5. Bill of Materials

Designator	Description	Manufacturer	Part Number	Qty
PCB	Printed Circuit Board	Any	PWR694	1
C1	CAP, CERM, 10 µF, 25 V, +/- 10%, X5R, 1206	MuRata	GRM31CR61E106KA12L	1
C2, C3, C6	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	MuRata	GRM188R61E105KA12D	3
C5, C12	CAP, CERM, 0.022 µF, 50 V, +/- 10%, X7R, 0603	MuRata	GRM188R71H223KA01D	2
C7, C14	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0603	MuRata	GRM188R71H103KA01D	2
C8, C9	CAP, CERM, 22 µF, 35 V, +/- 20%, X5R, 1206_190	TDK	C3216X5R1V226M	2
C10	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0603	AVX	0603YC104JAT2A	1
C11	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	MuRata	GRM188R71H104KA93D	1
D1	Diode, Schottky, 40 V, 3 A, SMA	Diodes Inc.	B340A-13-F	1
D3	Diode, Schottky, 40 V, 2 A, SMA	Diodes Inc.	B240A-13-F	1
H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
J1, J2	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	2
J3, J4, J5, J7	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	4
J6	Header, 100mil, 3x2, Gold, TH	Samtec	TSW-103-07-G-D	1
L1	Inductor, Shielded, Ferrite, 10 µH, 4 A, 0.0312 Ω, SMD	TDK	CLF10040T-100M	1
L2	Inductor, Shielded, Ferrite, 220 µH, 1.2 A, 0.273 Ω, SMD	TDK	SLF12565T-221M1R0-PF	1
P1	Header (shrouded), 100mil, 5x2, Gold, TH	Omron Electronic Components	XG4C-1031	1
Q1	MOSFET, N-CH, 30 V, 4.5 A, SOT-23	Vishay-Siliconix	SI2316BDS-T1-E3	1
R0	RES, 15.0, 1%, 0.25 W, 1206	Vishay-Dale	CRCW120615R0FKEA	1
R1	RES, 110 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603110KFKEA	1
R2, R6, R7, R9	RES, 100 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	4
R3, R4, R8	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	3
R5	RES, 33.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060333K0FKEA	1
SH-J1, SH-J2	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA	2
TP1, TP2, TP3	Test Point, Multipurpose, Red, TH	Keystone	5010	3
TP4, TP5, TP6, TP7, TP8	Test Point, Multipurpose, White, TH	Keystone	5012	5
U1	LNB VOLTAGE REGULATOR WITH I2C INTERFACE,	Texas Instruments	TPS65235RUKR	1

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