TPS65919-Q1 Register Map

Technical Reference Manual

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Introduction

This document presents a summary of the hardware interface for the TPS65919-Q1 device. Each module instance within the design is shown along with the module register map and bit definitions for each bitfield.

1.1 Register Address Mapping

This document describes the register mapping of the . The operation of the IC is described in the device data sheet, *TPS65919-Q1 Power Management Unit (PMU) for Processor*.

The 3 hex digits of the physical address of the register indicated in this document are mapped as 0xPAA, while P stands for the page number of the register, and AA stands for the register address within the memory page. The page numbers are mapped to the slave device address as following:

Page = 0x0 — Slave Device address 0x12 for DVS registers

Page = 0x1 — Slave Device address 0x48 or 0x58 for Power registers

Page = 0x2 — Slave Device address 0x49 or 0x59 for Interfaces and Auxiliaries registers

Page = 0x3 — Slave Device address 0x4A or 0x5A for Trimming and Test registers

Page = 0x4 —Slave Device address 0x4B or 0x5B for OTP programming registers

For the reset of the registers, the registers are defined by 3 categories:

- POR: Power On Reset registers
- HWRST: Hardware Reset registers
- SWORST: Switch Off Reset registers

These categories of registers (POR, HWRST, SWORST) are described in the device data sheet. When the reset value of a bit register is 0bX, it means the bit value is coming from the OTP memory.

NOTE: All reserved bits are read only (R). Read to an unmapped register returns previous read value.

Register Physical Address

2.1 Register Module Base Address and Size

Table 2-1 lists the base address and address space for the TPS65919-Q1 device functional register modules.

Table 2-1. TPS65919-Q1 Function Register Module Name and Base Address

Module Name	Base Address	Size
FUNC_SMPS_DVS	0x020	32 Bytes
FUNC_BACKUP	0x118	8 Bytes
FUNC_SMPS	0x120	48 Bytes
FUNC_LDO	0x150	47 Bytes
FUNC_SPI	0x17F	1 Byte
FUNC_DVFS	0x180	8 Bytes
FUNC_PMU_CONTROL	0x1A0	32 Bytes
FUNC_RESOURCE	0x1D4	28 Bytes
FUNC_PAD_CONTROL	0x1F0	16 Bytes
FUNC_INTERRUPT	0x210	32 Bytes
FUNC_ID	0x24F	4 Bytes
FUNC_GPIO	0x280	20 Bytes
FUNC_GPADC	0x2C0	32 Bytes
FUNC_DESIGNREV	0x357	1 Byte
FUNC_TRIM_GPADC	0x3CD	18 Bytes

Complex bit access types are encoded to fit into small table cells. Table 2-2 shows the codes that are used for access types in this document.

Table 2-2. FUNC_PAD_CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write

Register Descriptions

3.1 FUNC_SMPS_DVS Registers

Table 3-1 lists the memory-mapped registers for the FUNC_SMPS_DVS. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. FUNC_SMPS_DVS Registers

Address	Acronym	Register Name	Section
22h	SMPS1_FORCE	SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.1.1
23h	SMPS1_VOLTAGE	SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).r. RESET register domain: SWORST	Section 3.1.2
26h	SMPS2_FORCE	SMPS2 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.1.3
27h	SMPS2_VOLTAGE	SMPS2 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.1.4
2Eh	SMPS3_FORCE	SMPS3 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.1.5
2Fh	SMPS3_VOLTAGE	SMPS3 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.1.6

3.1.1 SMPS1_FORCE Register (Address = 22h) [reset = X]

SMPS1_FORCE is shown in Figure 3-1 and described in Table 3-2.

Return to Summary Table.

SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-1. SMPS1_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-2. SMPS1_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS1_FORCE.VSEL voltage is applied When 1: SMPS1_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS1_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register (page1).

3.1.2 SMPS1_VOLTAGE Register (Address = 23h) [reset = X]

SMPS1_VOLTAGE is shown in Figure 3-2 and described in Table 3-3.

Return to Summary Table.

SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).r.
RESET register domain: SWORST

Figure 3-2. SMPS1_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-3. SMPS1_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS1_VOLTAGE.VSEL and SPMS1_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note:RANGE bit is RO when SMPS1 is ON, RANGE bit is RW when SMPS1 is OFF Note: For Dual-phase mode, RANGE=1 (1V to 3.3V) is not supported.
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register (page1).

3.1.3 SMPS2_FORCE Register (Address = 26h) [reset = X]

SMPS2_FORCE is shown in Figure 3-3 and described in Table 3-4.

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SMPS2 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-3. SMPS2_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-4. SMPS2_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS2_FORCE.VSEL voltage is applied When 1: SMPS2_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS2_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.1.4 SMPS2_VOLTAGE Register (Address = 27h) [reset = X]

SMPS2_VOLTAGE is shown in Figure 3-4 and described in Table 3-5.

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SMPS2 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-4. SMPS2_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-5. SMPS2_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS2_VOLTAGE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note:RANGE bit is RO when SMPS2 is ON, RANGE bit is RW when SMPS2 is OFF
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.1.5 SMPS3_FORCE Register (Address = 2Eh) [reset = X]

SMPS3_FORCE is shown in Figure 3-5 and described in Table 3-6.

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SMPS3 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-5. SMPS3_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-6. SMPS3_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS3_FORCE.VSEL voltage is applied When 1: SMPS3_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS3_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register (page1).

3.1.6 SMPS3_VOLTAGE Register (Address = 2Fh) [reset = X]

SMPS3_VOLTAGE is shown in Figure 3-6 and described in Table 3-7.

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SMPS3 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-6. SMPS3_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-7. SMPS3_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS3_VOLTAGE.VSEL and SPMS3_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note:RANGE bit is RO when SMPS3 is ON, RANGE bit is RW when SMPS3 is OFF
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register (page1).

3.2 FUNC_BACKUP Registers

Table 3-8 lists the memory-mapped registers for the FUNC_BACKUP. All register offset addresses not listed in Table 3-8 should be considered as reserved locations and the register contents should not be modified.

Table 3-8. FUNC_BACKUP Registers

Address	Acronym	Register Name	Section
118h	BACKUP0	Backup register #0 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.1
119h	BACKUP1	Backup register #1 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.2
11Ah	BACKUP2	Backup register #2 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.3
11Bh	BACKUP3	Backup register #3 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.4
11Ch	BACKUP4	Backup register #4 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.5
11Dh	BACKUP5	Backup register #5 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.6
11Eh	BACKUP6	Backup register #6 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.7
11Fh	BACKUP7	Backup register #7 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active. RESET register domain: POR	Section 3.2.8

3.2.1 BACKUP0 Register (Address = 118h) [reset = 0h]

BACKUP0 is shown in Figure 3-7 and described in Table 3-9.

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Backup register #0 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-7. BACKUP0 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-9. BACKUP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.2 BACKUP1 Register (Address = 119h) [reset = 0h]

BACKUP1 is shown in Figure 3-8 and described in Table 3-10.

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Backup register #1 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-8. BACKUP1 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-10. BACKUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.3 BACKUP2 Register (Address = 11Ah) [reset = 0h]

BACKUP2 is shown in Figure 3-9 and described in Table 3-11.

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Backup register #2 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-9. BACKUP2 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-11. BACKUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.4 BACKUP3 Register (Address = 11Bh) [reset = 0h]

BACKUP3 is shown in Figure 3-10 and described in Table 3-12.

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Backup register #3 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-10. BACKUP3 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-12. BACKUP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.5 BACKUP4 Register (Address = 11Ch) [reset = 0h]

BACKUP4 is shown in Figure 3-11 and described in Table 3-13.

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Backup register #4 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-11. BACKUP4 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-13. BACKUP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.6 BACKUP5 Register (Address = 11Dh) [reset = 0h]

BACKUP5 is shown in Figure 3-12 and described in Table 3-14.

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Backup register #5 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-12. BACKUP5 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-14. BACKUP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.7 BACKUP6 Register (Address = 11Eh) [reset = 0h]

BACKUP6 is shown in Figure 3-13 and described in Table 3-15.

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Backup register #6 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-13. BACKUP6 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-15. BACKUP6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.2.8 BACKUP7 Register (Address = 11Fh) [reset = 0h]

BACKUP7 is shown in Figure 3-14 and described in Table 3-16.

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Backup register #7 which can be used for storage by the application firmware when the external host is power down. These registers will retain their content as long as VRTC is active.
RESET register domain: POR

Figure 3-14. BACKUP7 Register

7	6	5	4	3	2	1	0
BACKUP							
R/W-0h							

Table 3-16. BACKUP7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BACKUP	R/W	0h	

3.3 FUNC_SMPS Registers

Table 3-17 lists the memory-mapped registers for the FUNC_SMPS. All register offset addresses not listed in Table 3-17 should be considered as reserved locations and the register contents should not be modified.

Table 3-17. FUNC_SMPS Registers

Address	Acronym	Register Name	Section
120h	SMPS1_CTRL	SMPS1 (or SMPS12 in case of dual-phase) control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.3.1
122h	SMPS1_FORCE	SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.3.2
123h	SMPS1_VOLTAGE	SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.3.3
124h	SMPS2_CTRL	SMPS2 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.3.4
126h	SMPS2_FORCE	SMPS2 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.3.5
127h	SMPS2_VOLTAGE	SMPS2 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.3.6
12Ch	SMPS3_CTRL	SMPS3 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.3.7
12Eh	SMPS3_FORCE	SMPS3 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.3.8
12Fh	SMPS3_VOLTAGE	SMPS3 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config). RESET register domain: SWORST	Section 3.3.9

Table 3-17. FUNC_SMPS Registers (continued)

Address	Acronym	Register Name	Section
130h	SMPS4_CTRL	SMPS4 control register. RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.3.10
133h	SMPS4_VOLTAGE	SMPS4 register. Voltage to apply to the resource. RESET register domain: SWORST	Section 3.3.11
144h	SMPS_CTRL	SMPS control register. RESET register domain: HWRST	Section 3.3.12
145h	SMPS_PD_CTRL	SMPS Pull-Down enable register. RESET register domain: HWRST Notes: SMPS pull-down register bits validate the control of the active discharge of each power resource to full-fill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restart correctly at the next power-up sequence.	Section 3.3.13
147h	SMPS_THERMAL_EN	SMPS Thermal feature enable register. RESET register domain: HWRST	Section 3.3.14
148h	SMPS_THERMAL_STATUS	SMPS Thermal status register. RESET register domain: POR	Section 3.3.15
149h	SMPS_SHORT_STATUS	SMPS Short circuit status. RESET register domain: POR	Section 3.3.16
14Ah	SMPS_NEGATIVE_CURRENT_LIMIT_EN	Iload Negative Current Comparator enable register (Negative Current measurement). RESET register domain: HWRST	Section 3.3.17
14Bh	SMPS_POWERGOOD_MASK1	SMPS Power Good (POWERGOOD) mask #1 RESET register domain: POR	Section 3.3.18
14Ch	SMPS_POWERGOOD_MASK2	SMPS Power Good (POWERGOOD) mask #2 RESET register domain: POR (excepted POWERGOOD_TYPE_SELECT which is under HWRST)	Section 3.3.19
14Dh	SMPS_PLL_CTRL	SMPS PLL control register. RESET register domain: HWRST	Section 3.3.20

3.3.1 SMPS1_CTRL Register (Address = 120h) [reset = 0h]

SMPS1_CTRL is shown in Figure 3-15 and described in Table 3-18.

Return to Summary Table.

SMPS1 (or SMPS12 in case of dual-phase) control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-15. SMPS1_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-18. SMPS1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS1_VOLTAGE.VSEL and SMPS1_FORCE.VSEL register and re-load the default value (reset value) in SMPS1_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS1_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).
5-4	STATUS	R	0h	SMPS1 (or SMPS12 in case of dual-phase) status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS1 (or SMPS12 in case of dual-phase) SLEEP Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS1 (or SMPS12 in case of dual-phase) ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.3.2 SMPS1_FORCE Register (Address = 122h) [reset = X]

SMPS1_FORCE is shown in Figure 3-16 and described in Table 3-19.

Return to Summary Table.

SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-16. SMPS1_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-19. SMPS1_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS1_FORCE.VSEL voltage is applied When 1: SMPS1_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS1_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register

3.3.3 SMPS1_VOLTAGE Register (Address = 123h) [reset = X]

SMPS1_VOLTAGE is shown in Figure 3-17 and described in Table 3-20.

Return to Summary Table.

SMPS1 (or SMPS12 in case of dual-phase) DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-17. SMPS1_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-20. SMPS1_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS1_VOLTAGE.VSEL and SMPS1_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note: RANGE bit is RO when SMPS1(or SMPS12 in case of dual-phase) is ON, RANGE bit is RW when SMPS1 (or SMPS12 in case of dual-phase) is OFF Note: For Dual-phase mode, RANGE=1 (1V to 3.3V) is not supported.

Table 3-20. SMPS1_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	VSEL	R/W	X	VSEL[6:0] cross table voltage (OFF,0.5V to 3.3V) RANGE[0]=0 (x1 multiplier)/ 1(x2 multiplier) 0000000 = SMPS OFF/OFF 1000000 = 1.08V/2.16V 0000001 = 0.5V/1V 1000001 = 1.09V/2.18V 0000010 = 0.5V/1V 1000010 = 1.1V/2.2V 0000011 = 0.5V/1V 1000011 = 1.11V/2.22V 0000100 = 0.5V/1V 1000100 = 1.12V/2.24V 0000101 = 0.5V/1V 1000101 = 1.13V/2.26V 0000110 = 0.5V/1V 1000110 = 1.14V/2.28V 0000111 = 0.51V/1.02V 1000111 = 1.15V/2.3V 0001000 = 0.52V/1.04V 1001000 = 1.16V/2.32V 0001001 = 0.53V/1.06V 1001001 = 1.17V/2.34V 0001010 = 0.54V/1.08V 1001010 = 1.18V/2.36V 0001011 = 0.55V/1.1V 1001011 = 1.19V/2.38V 0001100 = 0.56V/1.12V 1001100 = 1.2V/2.4V 0001101 = 0.57V/1.14V 1001101 = 1.21V/2.42V 0001110 = 0.58V/1.16V 1001110 = 1.22V/2.44V 0001111 = 0.59V/1.18V 1001111 = 1.23V/2.46V 0010000 = 0.60V/1.2V 1010000 = 1.24V/2.48V 0010001 = 0.61V/1.22V 1010001 = 1.25V/2.5V 0010010 = 0.62V/1.24V 1010010 = 1.26V/2.52V 0010011 = 0.63V/1.26V 1010011 = 1.27V/2.54V 0010100 = 0.64V/1.28V 1010100 = 1.28V/2.56V 0010101 = 0.65V/1.3V 1010101 = 1.29V/2.58V 0010110 = 0.66V/1.32V 1010110 = 1.3V/2.6V 0010111 = 0.67V/1.34V 1010111 = 1.31V/2.62V 0011000 = 0.68V/1.36V 1011000 = 1.32V/2.64V 0011001 = 0.69V/1.38V 1011001 = 1.33V/2.66V 0011010 = 0.70V/1.4V 1011010 = 1.34V/2.68V 0011011 = 0.71V/1.42V 1011011 = 1.35V/2.7V 0011100 = 0.72V/1.44V 1011100 = 1.36V/2.72V 0011101 = 0.73V/1.46V 1011101 = 1.37V/2.74V 0011110 = 0.74V/1.48V 1011110 = 1.38V/2.76V 0011111 = 0.75V/1.50V 1011111 = 1.39V/2.78V 0100000 = 0.76V/1.52V 1100000 = 1.4V/2.8V 0100001 = 0.77V/1.54V 1100001 = 1.41V/2.82V 0100010 = 0.78V/1.56V 1100010 = 1.42V/2.84V 0100011 = 0.79V/1.58V 1100011 = 1.43V/2.86V 0100100 = 0.8V/1.6V 1100100 = 1.44V/2.88V 0100101 = 0.81V/1.62V 1100101 = 1.45V/2.9V 0100110 = 0.82V/1.64V 1100110 = 1.46V/2.92V 0100111 = 0.83V/1.66V 1100111 = 1.47V/2.94V 0101000 = 0.84V/1.68V 1101000 = 1.48V/2.96V 0101001 = 0.85V/1.7V 1101001= 1.49V/2.98V 0101010 = 0.86V/1.72V 1101010 = 1.5V/3V 0101011 = 0.87V/1.74V 1101011 = 1.51V/3.02V 0101100 = 0.88V/1.76V 1101100 = 1.52V/3.04V 0101101 = 0.89V/1.78V 1101101 = 1.53V/3.06V 0101110 = 0.9V/1.8V 1101110 = 1.54V/3.08V

Table 3-20. SMPS1_VOLTAGE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0101111 = 0.91V/1.82V 1101111 = 1.55V/3.1V
				0110000 = 0.92V/1.84V 1110000 = 1.56V/3.12V
				0110001 = 0.93V/1.86V 1110001 = 1.57V/3.14V
				0110010 = 0.94V/1.88V 1110010 = 1.58V/3.16V
				0110011 = 0.95V/1.90V 1110011 = 1.59V/3.18V
				0110100 = 0.96V/1.92V 1110100 = 1.6V/3.2V
				0110101 = 0.97V/1.94V 1110101 = 1.61V/3.22V
				0110110 = 0.98V/1.96V 1110110 = 1.62V/3.24V
				0110111 = 0.99V/1.98V 1110111 = 1.63V/3.26V
				0111000 = 1.00V/2V 1111000 = 1.64V/3.28V
				0111001 = 1.01V/2.02V 1111001 = 1.65V/3.3V
				0111010 = 1.02V/2.04V 1111010 = 1.65V/3.3V
				0111011 = 1.03V/2.06V 1111011 = 1.65V/3.3V
				0111100 = 1.04V/2.08V 1111100 = 1.65V/3.3V
				0111101 = 1.05V/2.1V 1111101 = 1.65V/3.3V
				0111110 = 1.06V/2.12V 1111110 = 1.65V/3.3V
				0111111 = 1.07V/2.14V 1111111 = 1.65V/3.3V

3.3.4 SMPS2_CTRL Register (Address = 124h) [reset = 0h]

SMPS2_CTRL is shown in Figure 3-18 and described in Table 3-21.

Return to Summary Table.

SMPS2 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-18. SMPS2_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-21. SMPS2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP in SMPS2_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS2_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).
5-4	STATUS	R	0h	SMPS2 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS2 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS2 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.3.5 SMPS2_FORCE Register (Address = 126h) [reset = X]

SMPS2_FORCE is shown in Figure 3-19 and described in Table 3-22.

Return to Summary Table.

SMPS2 DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-19. SMPS2_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-22. SMPS2_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS2_FORCE.VSEL voltage is applied When 1: SMPS2_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS2_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.3.6 SMPS2_VOLTAGE Register (Address = 127h) [reset = X]

SMPS2_VOLTAGE is shown in Figure 3-20 and described in Table 3-23.

Return to Summary Table.

SMPS2 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-20. SMPS2_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-23. SMPS2_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS2_VOLTAGE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note:RANGE bit is RO when SMPS2 is ON, RANGE bit is RW when SMPS2 is OFF
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.3.7 SMPS3_CTRL Register (Address = 12Ch) [reset = 0h]

SMPS3_CTRL is shown in Figure 3-21 and described in Table 3-24.

Return to Summary Table.

SMPS3 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-21. SMPS3_CTRL Register

7	6	5	4	3	2	1	0
WR_S	ROOF_FLOOR_EN	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R/W-0h	R-0h		R/W-0h		R/W-0h	

Table 3-24. SMPS3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS3_VOLTAGE.VSEL and SMPS3_FORCE.VSEL register and re-load the default value (reset value) in SMPS3_FORCE.CMD during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	ROOF_FLOOR_EN	R/W	0h	Roof Floor enable bit (only for DVS) 0: Voltage Selection controlled by SMPS3_FORCE.CMD bit. 1: Voltage Selection controlled by device resource pins (NSLEEP, ENABLE1, ENABLE2).
5-4	STATUS	R	0h	SMPS3 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS3 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS3 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.3.8 SMPS3_FORCE Register (Address = 12Eh) [reset = X]

SMPS3_FORCE is shown in Figure 3-22 and described in Table 3-25.

Return to Summary Table.

SMPS3
DVS register. Voltage to apply to the resource when it is a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-22. SMPS3_FORCE Register

7	6	5	4	3	2	1	0
CMD	VSEL						
R/W-1h	R/W-X						

Table 3-25. SMPS3_FORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CMD	R/W	1h	DVS command register selection: When 0: SMPS3_FORCE.VSEL voltage is applied When 1: SMPS3_VOLTAGE.VSEL voltage is applied (default) CMD is effective if SMPS3_CTRL.ROOF_FLOOR_EN='0'
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.3.9 SMPS3_VOLTAGE Register (Address = 12Fh) [reset = X]

SMPS3_VOLTAGE is shown in Figure 3-23 and described in Table 3-26.

Return to Summary Table.

SMPS3 DVS register. Voltage to apply to the resource when it is not a DVS force command (OTP_Config).
RESET register domain: SWORST

Figure 3-23. SMPS3_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-26. SMPS3_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS3_VOLTAGE.VSEL and SMPS3_FORCE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note:RANGE bit is RO when SMPS3 is ON, RANGE bit is RW when SMPS3 is OFF
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.3.10 SMPS4_CTRL Register (Address = 130h) [reset = 0h]

SMPS4_CTRL is shown in Figure 3-24 and described in Table 3-27.

Return to Summary Table.

SMPS4 control register.
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-24. SMPS4_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED	STATUS		MODE_SLEEP		MODE_ACTIVE	
R/W-0h	R-0h	R-0h		R/W-0h		R/W-0h	

Table 3-27. SMPS4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default value (from OTP) in SMPS4_VOLTAGE.VSEL register during Warm Reset. 1: Maintain current voltage during Warm Reset (Registers remain unchanged - no voltage change).
6	RESERVED	R	0h	
5-4	STATUS	R	0h	SMPS4 Status 00: OFF 01: Forced PWM 10: ECO 11: Forced PWM
3-2	MODE_SLEEP	R/W	0h	SMPS4 SLEEP mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM
1-0	MODE_ACTIVE	R/W	0h	SMPS4 ACTIVE Mode 00: OFF (default) 01: Forced PWM 10: ECO 11: Forced PWM

3.3.11 SMPS4_VOLTAGE Register (Address = 133h) [reset = X]

SMPS4_VOLTAGE is shown in Figure 3-25 and described in Table 3-28.

Return to Summary Table.

SMPS4 register. Voltage to apply to the resource.
RESET register domain: SWORST

Figure 3-25. SMPS4_VOLTAGE Register

7	6	5	4	3	2	1	0
RANGE	VSEL						
R/W-X	R/W-X						

Table 3-28. SMPS4_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RANGE	R/W	X	Range of the VSEL voltage. This bit is applied to SMPS4_VOLTAGE.VSEL 0: 0.5V to 1.65V 1: 1.0 to 3.3V Note:RANGE bit is RO when SMPS4 is ON, RANGE bit is RW when SMPS4 is OFF
6-0	VSEL	R/W	X	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register.

3.3.12 SMPS_CTRL Register (Address = 144h) [reset = X]

SMPS_CTRL is shown in Figure 3-26 and described in Table 3-29.

Return to Summary Table.

SMPS control register.
RESET register domain: HWRST

Figure 3-26. SMPS_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	SMPS1_SMPS12_EN	RESERVED		SMPS12_PHASE_CTRL	
R-0h		R-0h	R-X	R-0h		R/W-0h	

Table 3-29. SMPS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	SMPS1_SMPS12_EN	R	X	Selection of the type of configuration of the SMPS12 0: SMPS1 single phase, SMPS2 single phase 1: SMPS12 dual phase
3-2	RESERVED	R	0h	
1-0	SMPS12_PHASE_CTRL	R/W	0h	Selection of the phase mode of the SMPS12 (SMPS1 Single Phase + SMPS2 Single Phase configuration or SMPS12 Dual Phase configuration) 00: Automatic Phase Selection per SMPS - Multi Phase or Single Phase (default) 11: Automatic Phase Selection per SMPS - Multi Phase or Single Phase 01: Force Single Phase mode (for SMPS1 and SMPS2) 10: Force Multi Phase mode (for SMPS1 and SMPS2) - Prohibited under no-load condition

3.3.13 SMPS_PD_CTRL Register (Address = 145h) [reset = 5Bh]

SMPS_PD_CTRL is shown in Figure 3-27 and described in Table 3-30.

Return to Summary Table.

SMPS Pull-Down enable register.
RESET register domain: HWRST
Notes:
SMPS pull-down register bits validate the control of the active discharge of each power resource to full-fill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restart correctly at the next power-up sequence.

Figure 3-27. SMPS_PD_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R-0h	R-1h	R-0h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-1h

Table 3-30. SMPS_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
5	RESERVED	R	0h	
4	SMPS4	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS4 is in OFF state (default)
3	SMPS3	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS3 is in OFF state (default)
2	RESERVED	R	0h	
1	SMPS2	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS2 is in OFF state (default)
0	SMPS1	R/W	1h	0: Pull-down is disabled 1: Pull-down is enabled when SPMS1 is in OFF state (default)

3.3.14 SMPS_THERMAL_EN Register (Address = 147h) [reset = FFh]

SMPS_THERMAL_EN is shown in Figure 3-28 and described in Table 3-31.

Return to Summary Table.

SMPS Thermal feature enable register.
RESET register domain: HWRST

Figure 3-28. SMPS_THERMAL_EN Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	SMPS3	RESERVED	RESERVED	SMPS12
R-1h	R-1h	R-1h	R-1h	R/W-1h	R-1h	R-1h	R/W-1h

Table 3-31. SMPS_THERMAL_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
5	RESERVED	R	1h	
4	RESERVED	R	1h	
3	SMPS3	R/W	1h	0: SMPS3 Thermal feature is not enabled 1: SMPS3 Thermal feature is enabled (default)
2	RESERVED	R	1h	
1	RESERVED	R	1h	
0	SMPS12	R/W	1h	0: SMPS12 Thermal feature is not enabled 1: SMPS12 Thermal feature is enabled (default) Note: A unique Thermal Sensor is protecting SMPS1 and SMPS2

3.3.15 SMPS_THERMAL_STATUS Register (Address = 148h) [reset = 0h]

SMPS_THERMAL_STATUS is shown in Figure 3-29 and described in Table 3-32.

Return to Summary Table.

SMPS Thermal status register.
RESET register domain: POR

Figure 3-29. SMPS_THERMAL_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	SMPS3	RESERVED	RESERVED	SMPS12
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-32. SMPS_THERMAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	SMPS3	R	0h	0: SMPS3 Thermal measurement is below the limit (SMPS is functional) 1: SMPS3 Thermal measurement is over the limit (see specification)
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	SMPS12	R	0h	0: SMPS12 Thermal measurement is below the limit (SMPS is functional) 1: SMPS12 Thermal measurement is over the limit (see specification)

3.3.16 SMPS_SHORT_STATUS Register (Address = 149h) [reset = 0h]

SMPS_SHORT_STATUS is shown in Figure 3-30 and described in Table 3-33.

Return to Summary Table.

SMPS Short circuit status.
RESET register domain: POR

Figure 3-30. SMPS_SHORT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-33. SMPS_SHORT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
5	RESERVED	R	0h	
4	SMPS4	R	0h	0: SMPS4 is functional . No short detected (default) 1: SMPS4 output is shorted
3	SMPS3	R	0h	0: SMPS3 is functional . No short detected (default) 1: SMPS3 output is shorted
2	RESERVED	R	0h	
1	SMPS2	R	0h	0: SMPS2 is functional . No short detected (default) 1: SMPS2 output is shorted Note: This bit is un-relevant when SMPS12 is in Dual phase mode
0	SMPS1	R	0h	0: SMPS1 (or SMPS12 in Dual phase mode) is functional . No short detected (default) 1: SMPS1 (or SMPS12 in Dual phase mode) output is shorted

3.3.17 SMPS_NEGATIVE_CURRENT_LIMIT_EN Register (Address = 14Ah) [reset = FFh]

SMPS_NEGATIVE_CURRENT_LIMIT_EN is shown in Figure 3-31 and described in Table 3-34.

Return to Summary Table.

Iload Negative Current Comparator enable register (Negative Current measurement).
RESET register domain: HWRST

Figure 3-31. SMPS_NEGATIVE_CURRENT_LIMIT_EN Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R-1h	R-1h	R-1h	R/W-1h	R/W-1h	R-1h	R/W-1h	R/W-1h

Table 3-34. SMPS_NEGATIVE_CURRENT_LIMIT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
5	RESERVED	R	1h	
4	SMPS4	R/W	1h	0: SMPS4 Negative Current comparator for measurement is not enabled 1: SMPS4 Negative Current comparator for measurement is enabled (default)
3	SMPS3	R/W	1h	0: SMPS3 Negative Current comparator for measurement is not enabled 1: SMPS3 Negative Current comparator for measurement is enabled (default)
2	RESERVED	R	1h	
1	SMPS2	R/W	1h	0: SMPS2 Negative Current comparator for measurement is not enabled 1: SMPS2 Negative Current comparator for measurement is enabled (default)
0	SMPS1	R/W	1h	0: SMPS1 Negative Current comparator for measurement is not enabled 1: SMPS1 Negative Current comparator for measurement is enabled (default)

3.3.18 SMPS_POWERGOOD_MASK1 Register (Address = 14Bh) [reset = 5Ah]

SMPS_POWERGOOD_MASK1 is shown in Figure 3-32 and described in Table 3-35.

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SMPS Power Good (POWERGOOD) mask #1
RESET register domain: POR

Figure 3-32. SMPS_POWERGOOD_MASK1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R-0h	R-1h	R-0h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-0h

Table 3-35. SMPS_POWERGOOD_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
5	RESERVED	R	0h	
4	SMPS4	R/W	1h	SMPS4 POWERGOOD Mask bit register 0: SMPS4 line is enabled. The SMPS4 state is generated on POWERGOOD line 1: SMPS4 line is masked. No SMPS4 state is generated on POWERGOOD line (default)
3	SMPS3	R/W	1h	SMPS3 POWERGOOD Mask bit register 0: SMPS3 line is enabled. The SMPS3 state is generated on POWERGOOD line 1: SMPS3 line is masked. No SMPS3 state is generated on POWERGOOD line (default)
2	RESERVED	R	0h	
1	SMPS2	R/W	1h	SMPS2 POWERGOOD Mask bit register 0: SMPS2 line is enabled. The SMPS2 state is generated on POWERGOOD line 1: SMPS2 line is masked. No SMPS2 state is generated on POWERGOOD line (default)
0	SMPS1	R/W	0h	SMPS1 POWERGOOD Mask bit register 0: SMPS1 line is enabled. The SMPS1 state is generated on POWERGOOD line (default) 1: SMPS1 line is masked. No SMPS1 state is generated on POWERGOOD line

3.3.19 SMPS_POWERGOOD_MASK2 Register (Address = 14Ch) [reset = 10h]

SMPS_POWERGOOD_MASK2 is shown in Figure 3-33 and described in Table 3-36.

Return to Summary Table.

SMPS Power Good (POWERGOOD) mask #2
RESET register domain: POR (excepted POWERGOOD_TYPE_SELECT which is under HWRST)

Figure 3-33. SMPS_POWERGOOD_MASK2 Register

7	6	5	4	3	2	1	0
POWERGOOD_TYPE_SELECT	RESERVED		OVC_ALARM	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R-0h		R/W-1h	R-0h	R-0h	R-0h	R-0h

Table 3-36. SMPS_POWERGOOD_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POWERGOOD_TYPE_SELECT	R/W	0h	Selection of the POWERGOOD type of monitoring 0: Voltage monitoring (above threshold)) AND Current monitoring (over current) (default) 1: Current monitoring only (over current)
6-5	RESERVED	R	0h	
4	OVC_ALARM	R/W	1h	OVC_ALARM Mask bit register 0: OVC_ALARM line is enabled. The OVC_ALARM state is generated on POWERGOOD line 1: OVC_ALARM line is masked. No OVC_ALARM state is generated on POWERGOOD line (default)
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.3.20 SMPS_PLL_CTRL Register (Address = 14Dh) [reset = 0h]

SMPS_PLL_CTRL is shown in Figure 3-34 and described in Table 3-37.

Return to Summary Table.

SMPS PLL control register.
RESET register domain: HWRST

Figure 3-34. SMPS_PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				PLL_EN_BYPASS	PLL_BYPASS_CLK	RESERVED	RESERVED
R-0h				R/W-0h	R/W-0h	R-0h	R-0h

Table 3-37. SMPS_PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	PLL_EN_BYPASS	R/W	0h	Enable/disable the bypass mode 0: No Bypass (default) 1: Bypass is enabled
2	PLL_BYPASS_CLK	R/W	0h	Allow to bypass the 6x frequency clock 0: No Bypass (default) 1: Bypass is enabled
1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.4 FUNC_LDO Registers

Table 3-38 lists the memory-mapped registers for the FUNC_LDO. All register offset addresses not listed in Table 3-38 should be considered as reserved locations and the register contents should not be modified.

Table 3-38. FUNC_LDO Registers

Address	Acronym	Register Name	Section
150h	LDO1_CTRL	LDO1 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.4.1
151h	LDO1_VOLTAGE	LDO1 Voltage selection (OTP_Config) RESET register domain: SWORST	Section 3.4.2
152h	LDO2_CTRL	LDO2 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.4.3
153h	LDO2_VOLTAGE	LDO2 Voltage selection (OTP_Config) RESET register domain: SWORST	Section 3.4.4
15Eh	LDO4_CTRL	LDO4 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.4.5
15Fh	LDO4_VOLTAGE	LDO4 Voltage selection (OTP_Config) RESET register domain: SWORST	Section 3.4.6
162h	LDO5_CTRL	LDO5 control register RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain) Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource. MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).	Section 3.4.7
163h	LDO5_VOLTAGE	LDO5 Voltage selection (OTP_Config) RESET register domain: SWORST	Section 3.4.8
16Bh	LDO_PD_CTRL1	LDO Pull-Down enable register #1 RESET register domain: HWRST NOTES: LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.	Section 3.4.9

Table 3-38. FUNC_LDO Registers (continued)

Address	Acronym	Register Name	Section
16Ch	LDO_PD_CTRL2	LDO Pull-Down enable register #2 RESET register domain: HWRST NOTES: LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.	Section 3.4.10
16Dh	LDO_SHORT_STATUS1	LDO Short circuit status register #1 At Power-On, LDO short input informations are masked during 1 ms. This 1 ms masking is activated and re-started each time one LDO is enabled. RESET register domain: POR	Section 3.4.11
16Eh	LDO_SHORT_STATUS2	LDO short circuit status register #2 RESET register domain: POR	Section 3.4.12
17Dh	LDO_PD_CTRL3	LDO Pull-Down enable register #3 RESET register domain: HWRST NOTES: LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements. When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.	Section 3.4.13
17Eh	LDO_SHORT_STATUS3	LDO short circuit status register #3 RESET register domain: POR	Section 3.4.14

3.4.1 LDO1_CTRL Register (Address = 150h) [reset = 0h]

LDO1_CTRL is shown in Figure 3-35 and described in Table 3-39.

Return to Summary Table.

LDO1 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-35. LDO1_CTRL Register

7	6	5	4	3	2	1	0
WR_S	LDO_BYPASS_EN	RESERVED	STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-39. LDO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO1_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6	LDO_BYPASS_EN	R/W	0h	LDO1 bypass enable 0: LDO1 is configured as a standard power resource (default) 1: LDO1 is configured as a bypass LDO (bypass enabled)
5	RESERVED	R	0h	
4	STATUS	R	0h	LDO1 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO1 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO1 ACTIVE Mode 0: OFF 1: ON This bit can be updated by power-up sequencer

3.4.2 LDO1_VOLTAGE Register (Address = 151h) [reset = X]

LDO1_VOLTAGE is shown in Figure 3-36 and described in Table 3-40.

Return to Summary Table.

LDO1 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-36. LDO1_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-40. LDO1_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	VSEL[5:0] cross table voltage (OFF,0.9V to 3.3V) 000000 0V 100000 2,45V 000001 0,9V 100001 2,5V 000010 0,95V 100010 2,55V 000011 1V 100011 2,6V 000100 1,05V 100100 2,65V 000101 1,1V 100101 2,7V 000110 1,15V 100110 2,75V 000111 1,2V 100111 2,8V 001000 1,25V 101000 2,85V 001001 1,3V 101001 2,9V 001010 1,35V 101010 2,95V 001011 1,4V 101011 3V 001100 1,45V 101100 3,05V 001101 1,5V 101101 3,1V 001110 1,55V 101110 3,15V 001111 1,6V 101111 3,2V 010000 1,65V 110000 3,25V 010001 1,7V 110001 3,3V 010010 1,75V 110010 3,3V 010011 1,8V 110011 3,3V 010100 1,85V 110100 3,3V 010101 1,9V 110101 3,3V 010110 1,95V 110110 3,3V 010111 2V 110111 3,3V 011000 2,05V 111000 3,3V 011001 2,1V 111001 3,3V 011010 2,15V 111010 3,3V 011011 2,2V 111011 3,3V 011100 2,25V 111100 3,3V 011101 2,3V 111101 3,3V 011110 2,35V 111110 3,3V 011111 2,4V 111111 3,3V

3.4.3 LDO2_CTRL Register (Address = 152h) [reset = 0h]

LDO2_CTRL is shown in Figure 3-37 and described in Table 3-41.

Return to Summary Table.

LDO2 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-37. LDO2_CTRL Register

7	6	5	4	3	2	1	0
WR_S	LDO_BYPASS_EN	RESERVED	STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-41. LDO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO2_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6	LDO_BYPASS_EN	R/W	0h	LDO2 bypass enable 0: LDO2 is configured as a standard power resource (default) 1: LDO2 is configured as a bypass LDO (bypass enabled)
5	RESERVED	R	0h	
4	STATUS	R	0h	LDO2 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO2 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO2 ACTIVE Mode 0: OFF 1: ON

3.4.4 LDO2_VOLTAGE Register (Address = 153h) [reset = X]

LDO2_VOLTAGE is shown in Figure 3-38 and described in Table 3-42.

Return to Summary Table.

LDO2 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-38. LDO2_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-42. LDO2_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.4.5 LDO4_CTRL Register (Address = 15Eh) [reset = 0h]

LDO4_CTRL is shown in Figure 3-39 and described in Table 3-43.

Return to Summary Table.

LDO4 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-39. LDO4_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED	RESERVED	STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-43. LDO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO8_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6	RESERVED	R/W	0h	
5	RESERVED	R	0h	
4	STATUS	R	0h	LDO4 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO4 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO4 ACTIVE Mode 0: OFF 1: ON

3.4.6 LDO4_VOLTAGE Register (Address = 15Fh) [reset = X]

LDO4_VOLTAGE is shown in Figure 3-40 and described in Table 3-44.

Return to Summary Table.

LDO4 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-40. LDO4_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-44. LDO4_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.4.7 LDO5_CTRL Register (Address = 162h) [reset = 0h]

LDO5_CTRL is shown in Figure 3-41 and described in Table 3-45.

Return to Summary Table.

LDO5 control register
RESET register domain: HWRST (MODE_ACTIVE and MODE_SLEEP are in SWORST domain)
Notes: MODE_SLEEP is used when NSLEEP, ENABLE1, ENABLE2 signals select the resource.
MODE_ACTIVE is used when none of NSLEEP, ENABLE1, ENABLE2 signals select resource (see Resources SLEEP/ACTIVE assignments table in the Data Manual for details).

Figure 3-41. LDO5_CTRL Register

7	6	5	4	3	2	1	0
WR_S	RESERVED		STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R/W-0h	R-0h		R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-45. LDO5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WR_S	R/W	0h	Warm reset sensitivity 0: Re-load the default LDO5_VOLTAGE register value during Warm Reset 1: Maintain current voltage during Warm Reset (no voltage change)
6-5	RESERVED	R	0h	
4	STATUS	R	0h	LDO5 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	LDO5 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	LDO5 ACTIVE Mode 0: OFF 1: ON

3.4.8 LDO5_VOLTAGE Register (Address = 163h) [reset = X]

LDO5_VOLTAGE is shown in Figure 3-42 and described in Table 3-46.

Return to Summary Table.

LDO5 Voltage selection (OTP_Config)
RESET register domain: SWORST

Figure 3-42. LDO5_VOLTAGE Register

7	6	5	4	3	2	1	0
RESERVED		VSEL					
R-0h		R/W-X					

Table 3-46. LDO5_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	VSEL	R/W	X	See VSEL cross table showed in LDO1_VOLTAGE.VSEL register.

3.4.9 LDO_PD_CTRL1 Register (Address = 16Bh) [reset = 83h]

LDO_PD_CTRL1 is shown in Figure 3-43 and described in Table 3-47.

Return to Summary Table.

LDO Pull-Down enable register #1
RESET register domain: HWRST
NOTES:
LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.

Figure 3-43. LDO_PD_CTRL1 Register

7	6	5	4	3	2	1	0
LDO4	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO2	LDO1
R/W-1h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-1h	R/W-1h

Table 3-47. LDO_PD_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO4 is in OFF state
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	LDO2	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO2 is in OFF state
0	LDO1	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDO1 is in OFF state

3.4.10 LDO_PD_CTRL2 Register (Address = 16Ch) [reset = 6h]

LDO_PD_CTRL2 is shown in Figure 3-44 and described in Table 3-48.

Return to Summary Table.

LDO Pull-Down enable register #2
RESET register domain: HWRST
NOTES:
LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.

Figure 3-44. LDO_PD_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO5	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R/W-1h	R-0h

Table 3-48. LDO_PD_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
1	LDO5	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDOLN is in OFF state
0	RESERVED	R	0h	

3.4.11 LDO_SHORT_STATUS1 Register (Address = 16Dh) [reset = 0h]

LDO_SHORT_STATUS1 is shown in Figure 3-45 and described in Table 3-49.

Return to Summary Table.

LDO Short circuit status register #1
At Power-On, LDO short input informations are masked during 1 ms. This 1 ms masking is activated and re-started each time one LDO is enabled.
RESET register domain: POR

Figure 3-45. LDO_SHORT_STATUS1 Register

7	6	5	4	3	2	1	0
LDO4	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO2	LDO1
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-49. LDO_SHORT_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4	R	0h	0: LDO4 is functional. No short detected (default) 1: LDO4 output is short detected
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	LDO2	R	0h	0: LDO2 is functional. No short detected (default) 1: LDO2 output is short detected
0	LDO1	R	0h	0: LDO1 is functional. No short detected (default) 1: LDO1 output is short detected

3.4.12 LDO_SHORT_STATUS2 Register (Address = 16Eh) [reset = 0h]

LDO_SHORT_STATUS2 is shown in Figure 3-46 and described in Table 3-50.

Return to Summary Table.

LDO short circuit status register #2
RESET register domain: POR

Figure 3-46. LDO_SHORT_STATUS2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO5	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-50. LDO_SHORT_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
1	LDO5	R	0h	0: LDOLN is functional. No short detected (default) 1: LDOLN output is short detected
0	RESERVED	R	0h	

3.4.13 LDO_PD_CTRL3 Register (Address = 17Dh) [reset = 80h]

LDO_PD_CTRL3 is shown in Figure 3-47 and described in Table 3-51.

Return to Summary Table.

LDO Pull-Down enable register #3
RESET register domain: HWRST
NOTES:
LDO pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements.
When a pull-down is not enabled, there is always a weak pull-down present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.

Figure 3-47. LDO_PD_CTRL3 Register

7	6	5	4	3	2	1	0
LDOVANA	RESERVED						RESERVED
R/W-1h	R-0h						R-0h

Table 3-51. LDO_PD_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOVANA	R/W	1h	0: Pull-Down is disable 1: Pull-Down is enabled when LDOVANA is in OFF state
6-1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.4.14 LDO_SHORT_STATUS3 Register (Address = 17Eh) [reset = 0h]

LDO_SHORT_STATUS3 is shown in Figure 3-48 and described in Table 3-52.

Return to Summary Table.

LDO short circuit status register #3
RESET register domain: POR

Figure 3-48. LDO_SHORT_STATUS3 Register

7	6	5	4	3	2	1	0
LDOVANA	RESERVED						RESERVED
R-0h	R-0h						R-0h

Table 3-52. LDO_SHORT_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOVANA	R	0h	LDOVANA (internal LDO - reserved) 0: LDOVANA is functional. No short detected (default) 1: LDOVANA output is short detected
6-1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.5 FUNC_SPI Registers

Table 3-53 lists the memory-mapped registers for the FUNC_SPI. All register offset addresses not listed in Table 3-53 should be considered as reserved locations and the register contents should not be modified.

Table 3-53. FUNC_SPI Registers

Address	Acronym	Register Name	Section
17Fh	SPI_PAGE_CTRL	SPI Page Control register (used only when SPI interface is used). RESET register domain: SWORST	Section 3.5.1

3.5.1 SPI_PAGE_CTRL Register (Address = 17Fh) [reset = 0h]

SPI_PAGE_CTRL is shown in Figure 3-49 and described in Table 3-54.

Return to Summary Table.

SPI Page Control register (used only when SPI interface is used).
RESET register domain: SWORST

Figure 3-49. SPI_PAGE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							SPI_PAGE_ACCESS
R-0h							R/W-0h

Table 3-54. SPI_PAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	SPI_PAGE_ACCESS	R/W	0h	Page selection for SPI interface only 0: page1 (ID1=48) and page2 (ID2=49) 1: page1 (ID1=48) and page3 (ID2=4A)

3.6 FUNC_DVFS Registers

Table 3-55 lists the memory-mapped registers for the FUNC_DVFS. All register offset addresses not listed in Table 3-55 should be considered as reserved locations and the register contents should not be modified.

Table 3-55. FUNC_DVFS Registers

Address	Acronym	Register Name	Section
180h	SMPS_DVFS_CTRL	SMPS DVFS control register RESET register domain: SWORST (excepted DVFS_SMPS_SELECT (bit 4) on POR)	Section 3.6.1
181h	SMPS_DVFS_VOLTAGE_MAX	SMPS DVFS maximum voltage register RESET register domain: HWRST	Section 3.6.2
182h	SMPS_DVFS_STATUS	SMPS DVFS status register RESET register domain: HWRST	Section 3.6.3

3.6.1 SMPS_DVFS_CTRL Register (Address = 180h) [reset = 4h]

SMPS_DVFS_CTRL is shown in Figure 3-50 and described in Table 3-56.

Return to Summary Table.

SMPS DVFS control register
RESET register domain: SWORST (excepted DVFS_SMPS_SELECT (bit 4) on POR)

Figure 3-50. SMPS_DVFS_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			DVFS_SMPS_SELECT	DVFS_RESTORE_VALUE	DVFS_ENABLE_RST	DVFS_OFFSET_STEP	DVFS_ENABLE
R-0h			R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 3-56. SMPS_DVFS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	DVFS_SMPS_SELECT	R/W	0h	DVFS (I2C2_SCL, I2C2_SDA) SMPS selection 0: DVFS will control SMPS1(if single phase selected SMPS_CTRL.SMPS12_SMPS1_SMPS2_EN=0) or SMPS12 (dual-phase selected SMPS_CTRL.SMPS12_SMPS1_SMPS2_EN=1) 1: DVFS will control SMPS2(if single phase selected SMPS_CTRL.SMPS12_SMPS1_SMPS2_EN=0) or SMPS12 (dual-phase selected SMPS_CTRL.SMPS12_SMPS1_SMPS2_EN=1) Note: The reset of this bit is on POR
3	DVFS_RESTORE_VALUE	R/W	0h	Control the SMPS12 output voltage upon OFF to ACTIVE transition controlled with ENABLE2 pins 0: upon OFF to ACTIVE transition controlled with ENABLE2 pins, SMPS12 output voltage is set by SMPS12_VOLTAGE.VSEL register 1: upon OFF to ACTIVE transition controlled with ENABLE2 pins, SMPS12 output voltage is set with the latest voltage (sum result of the Offset value computed on PWM_DAT signal plus SMPS12_FORCE.VSEL register) before ACTIVE to OFF. This value is restored only if DVFS feature was already enabled (DVFS_ENABLE=1) before ACTIVE to OFF transition controlled with ENABLE2 pin.
2	DVFS_ENABLE_RST	R/W	1h	Control the DVFS Enable feature upon OFF to ACTIVE transition controlled with ENABLE2 pin. 0: DVFS feature is automatically re-enabled upon OFF to ACTIVE transition controlled with ENABLE2 pin if the feature was already enabled ((DVFS_ENABLE=1) before ACTIVE to OFF transition controlled with ENABLE2 pin 1: DVFS feature is not automatically enable (DVFS_ENABLE=0) upon OFF to ACTIVE transition controlled with ENABLE2 pin. To select the DVFS feature, the DVFS_ENABLE must be written to one by SW
1	DVFS_OFFSET_STEP	R/W	0h	Selection of the offset step for DVFS function: 0: offset step of 10mV (default) 1: offset step of 20mV
0	DVFS_ENABLE	R/W	0h	Selection of the DVFS function: 0: DVFS is not enabled (default) 1: DVFS is enabled (Control of SMPS12) DVFS function in link to I2C2_SCL and I2C2_SDA.

3.6.2 SMPS_DVFS_VOLTAGE_MAX Register (Address = 181h) [reset = 0h]

SMPS_DVFS_VOLTAGE_MAX is shown in Figure 3-51 and described in Table 3-57.

Return to Summary Table.

SMPS DVFS maximum voltage register
RESET register domain: HWRST

Figure 3-51. SMPS_DVFS_VOLTAGE_MAX Register

7	6	5	4	3	2	1	0
LOCK	VOLTAGE_MAX						
R/W-0h	R/W-0h						

Table 3-57. SMPS_DVFS_VOLTAGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOCK	R/W	0h	Access protection of the DVFS1_VOLTAGE_MAX register 0: No protection. R/W access to these register bits 1: Protection of these registers (Read only). This bit will reset (0b0) during HWRST SWITCH-OFF
6-0	VOLTAGE_MAX	R/W	0h	See VSEL cross table showed in SMPS12_VOLTAGE.VSEL register with RANGE[0]=0 (x1 multiplier) and VSEL range from OFF, 0.5 to 1.65V

3.6.3 SMPS_DVFS_STATUS Register (Address = 182h) [reset = 0h]

SMPS_DVFS_STATUS is shown in Figure 3-52 and described in Table 3-58.

Return to Summary Table.

SMPS DVFS status register
RESET register domain: HWRST

Figure 3-52. SMPS_DVFS_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		OFFSET_STATUS					
R-0h		R-0h					

Table 3-58. SMPS_DVFS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5-0	OFFSET_STATUS	R	0h	Offset status register (between 0 and 32 in decimal) SMPS_DVFS_CTRL.DVFS1_OFFSET_STEP=0 (x1 multiplier, 10mv per step)/ 1(x2 multiplier), 20mV per step) 000000: no offset 000001: 10mV/20mV 000010: 20mV/40mV ... 100000: 320mV/640mV 100001: reserved/reserved .. 111111: reserved/reserved

3.7 FUNC_PMU_CONTROL Registers

Table 3-59 lists the memory-mapped registers for the FUNC_PMU_CONTROL. All register offset addresses not listed in Table 3-59 should be considered as reserved locations and the register contents should not be modified.

Table 3-59. FUNC_PMU_CONTROL Registers

Address	Acronym	Register Name	Section
1A0h	DEV_CTRL	Device Control Register RESET register domain: SWORST (excepted OSC_FAILURE on POR)	Section 3.7.1
1A1h	POWER_CTRL	Power control register RESET register domain: SWORST	Section 3.7.2
1A2h	VSYS_LO	VSYS Low threshold register RESET register domain: HWRST	Section 3.7.3
1A3h	VSYS_MON	VSYS Monitoring register. This register is initialized by OTP memory (VSYS_HI - from 2.5V to 3.85V only). The software can overwrite this value by a new value (VSYS_MON - from 2.3V to 4.6V). RESET register domain: SWORST	Section 3.7.4
1A5h	WATCHDOG	Watch dog timer Register RESET register domain: SWORST NOTES: The WATCHDOG.TIMER counter is initialized with the RESET_OUT=0 The WATCHDOG.TIMER counter starts as soon as RESET_OUT is released.	Section 3.7.5
1A8h	VRTC_CTRL	VRTC Control Register RESET register domain: HWRST	Section 3.7.6
1A9h	LONG_PRESS_KEY	Long Press Key (LPK) configuration register RESET register domain: HWRST	Section 3.7.7
1AAh	OSC_THERM_CTRL	Oscillator and Thermal control register RESET register domain: HWRST	Section 3.7.8
1AFh	SWOFF_HWRST	Qualify which switch off events generate a HW RESET (configuration of behavior of the device) RESET register domain: HWRST	Section 3.7.9
1B0h	SWOFF_COLDRST	Qualify which switch off events generate a COLD RESET (configuration of behavior of the device) RESET register domain: HWRST	Section 3.7.10
1B1h	SWOFF_STATUS	Status register: registers switch off event RESET register domain: PORRST	Section 3.7.11
1B2h	PMU_CONFIG	PMU configuration RESET register domain: HWRST	Section 3.7.12
1B3h	PMU_CTRL2	Power Management Unit Control #2 RESET register domain: HWRST	Section 3.7.13
1B5h	PMU_SECONDARY_INT	Configuration and status of the Secondary Interrupt Handler RESET register domain: HWRST	Section 3.7.14
1B7h	SW_REVISION	Software (SW) revision register RESET register domain: HWRST	Section 3.7.15
1B9h	PMU_SECONDARY_INT2	Configuration and status of the Secondary Interrupt Handler (Register2) RESET register domain: HWRST	Section 3.7.16
1C3h	BOOT_STATUS	Boot Status Register RESET register domain: POR	Section 3.7.17

3.7.1 DEV_CTRL Register (Address = 1A0h) [reset = 1h]

DEV_CTRL is shown in Figure 3-53 and described in Table 3-60.

Return to Summary Table.

Device Control Register
RESET register domain: SWORST (excepted OSC_FAILURE on POR)

Figure 3-53. DEV_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				DEV_STATUS		SW_RST	DEV_ON
R-0h				R-0h		R/W-0h	R/W-1h

Table 3-60. DEV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-2	DEV_STATUS	R	0h	Device status 00: OFF 01: ACTIVE 10: Not applicable (ACTIVE) 11: SLEEP
1	SW_RST	R/W	0h	Software Reset (SW_RST) Writing 1 will restart the device (turn-off sequence followed by turn-on sequence) This bit is cleared automatically
0	DEV_ON	R/W	1h	Device ON enable 1: will maintain the device in ACTIVE mode 0: allow the device to go in OFF mode

3.7.2 POWER_CTRL Register (Address = 1A1h) [reset = 7h]

POWER_CTRL is shown in Figure 3-54 and described in Table 3-61.

Return to Summary Table.

Power control register
RESET register domain: SWORST

Figure 3-54. POWER_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					ENABLE2_MASK	ENABLE1_MASK	NSLEEP_MASK
R-0h					R/W-1h	R/W-1h	R/W-1h

Table 3-61. POWER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	ENABLE2_MASK	R/W	1h	Enable of the ENABLE2 line (mask) 0: ENABLE2 is not masked (allow control of the resource with ENABLE2 pin) 1: ENABLE2 is masked (does not affect resource control) (default)
1	ENABLE1_MASK	R/W	1h	Enable of the ENABLE1 line (mask) 0: ENABLE1 is not masked (allow control of the resource with ENABLE1 pin) 1: ENABLE1 is masked (does not affect resource control) (default)
0	NSLEEP_MASK	R/W	1h	Enable of the NSLEEP line (mask) 0: NSLEEP is not masked (allow control of the resource with NSLEEP pin) 1: NSLEEP is masked (does not affect resource control) (default)

3.7.3 VSYS_LO Register (Address = 1A2h) [reset = X]

VSYS_LO is shown in Figure 3-55 and described in Table 3-62.

Return to Summary Table.

VSYS Low threshold register
RESET register domain: HWRST

Figure 3-55. VSYS_LO Register

7	6	5	4	3	2	1	0
RESERVED			THRESHOLD				
R-0h			R-X				

Table 3-62. VSYS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4-0	THRESHOLD	R	X	VSYS_LO - System voltage falling edge threshold. When VCCx input falls below VSYS_LO, device enters OFF mode and is ready for start-up event. Configured by OTP bits. From 2.5V to 3.10V per 50mV step. 00000 = 2.300 V (Reserved) 00001 = 2.050 V (Reserved) 00010 = 2.100 V (Reserved) 00011 = 2.150 V (Reserved) 00100 = 2.200 V (Reserved) 00101 = 2.250 V (Reserved) 00110 = 2.300 V (Reserved) 00111 = 2.350 V (Reserved) 01000 = 2.400 V (Reserved) 01001 = 2.450 V (Reserved) 01010 = 2.500 V 01011 = 2.550 V 01100 = 2.600 V 01101 = 2.650 V 01110 = 2.700 V 01111 = 2.750 V 10000 = 2.800 V 10001 = 2.850 V 10010 = 2.900 V 10011 = 2.950 V 10100 = 3.000 V 10101 = 3.050 V 10110 = 3.100V 10111 = Reserved .. 11111 = Reserved

3.7.4 VSYS_MON Register (Address = 1A3h) [reset = X]

VSYS_MON is shown in Figure 3-56 and described in Table 3-63.

Return to Summary Table.

VSYS Monitoring register. This register is initialized by OTP memory (VSYS_HI - from 2.5V to 3.85V only). The software can overwrite this value by a new value (VSYS_MON - from 2.3V to 4.6V).
RESET register domain: SWORST

Figure 3-56. VSYS_MON Register

7	6	5	4	3	2	1	0
ENABLE	RESERVED	THRESHOLD					
R/W-0h	R-0h	R/W-X					

Table 3-63. VSYS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE	R/W	0h	Enable VSYS monitoring (only in ACTIVE /SLEEP) 0: VSYS monitoring is not enabled 1: VSYS monitoring is enabled
6	RESERVED	R	0h	

Table 3-63. VSYS_MON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESHOLD	R/W	X	VSYS_HI Configured by OTP bits (from 2.5V to 3.85V). By SW, from 2.3V to 4.6V per 50mV step. 000000 = 2.30 V 100000 = 3.60 V 000001 = 2.30 V 100001 = 3.65 V 000010 = 2.30 V 100010 = 3.70 V 000011 = 2.30 V 100011 = 3.75 V 000100 = 2.30 V 100100 = 3.80 V 000101 = 2.30 V 100101 = 3.85 V 000110 = 2.30 V 100110 = 3.90 V 000111 = 2.35 V 100111 = 3.95 V 001000 = 2.40 V 101000 = 4.00 V 001001 = 2.45 V 101001 = 4.05 V 001010 = 2.50 V 101010 = 4.10 V 001011 = 2.55 V 101011 = 4.15 V 001100 = 2.60 V 101100 = 4.20 V 001101 = 2.65 V 101101 = 4.25 V 001110 = 2.70 V 101110 = 4.30 V 001111 = 2.75 V 101111 = 4.35 V 010000 = 2.80 V 110000 = 4.40 V 010001 = 2.85 V 110001 = 4.45 V 010010 = 2.90 V 110010 = 4.50 V 010011 = 2.95 V 110011 = 4.55 V 010100 = 3.00 V 110100 = 4.60 V 010101 = 3.05 V 110101 = 4.60 V 010110 = 3.10 V 110110 = 4.60 V 010111 = 3.15 V 110111 = 4.60 V 011000 = 3.20 V 111000 = 4.60 V 011001 = 3.25 V 111001 = 4.60 V 011010 = 3.30 V 111010 = 4.60 V 011011 = 3.35 V 111011 = 4.60 V 011100 = 3.40 V 111100 = 4.60 V 011101 = 3.45 V 111101 = 4.60 V 011110 = 3.50 V 111110 = 4.60 V 011111 = 3.55 V 111111 = 4.60 V

3.7.5 WATCHDOG Register (Address = 1A5h) [reset = 7h]

WATCHDOG is shown in Figure 3-57 and described in Table 3-64.

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Watch dog timer Register
RESET register domain: SWORST
NOTES:
The WATCHDOG.TIMER counter is initialized with the RESET_OUT=0
The WATCHDOG.TIMER counter starts as soon as RESET_OUT is released.

Figure 3-57. WATCHDOG Register

7	6	5	4	3	2	1	0
RESERVED		LOCK	ENABLE	MODE	TIMER		
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-7h		

Table 3-64. WATCHDOG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	LOCK	R/W	0h	Access protection of the WATCHDOG.ENABLE, WATCHDOC.MODE and WATCHDOG.LOCK bits 0: No protection. R/W access to these register bits 1: Protection of these registers (Read only). This bit will reset (0b0) during SWITCH-OFF
4	ENABLE	R/W	0h	Selection of the Watchdog: 0: Watchdog is not selected (disable) (default) 1: Watchdog is elected (enabled)
3	MODE	R/W	0h	Select type of watchdog behavior: 0: Periodic (default) 1: Interrupt mode
2-0	TIMER	R/W	7h	Timer delay selection: 000: 1s 001: 2s 010: 4s 011: 8s 100: 16s 101: 32s 110: 64s 111: 128s (default)

3.7.6 VRTC_CTRL Register (Address = 1A8h) [reset = X]

VRTC_CTRL is shown in Figure 3-58 and described in Table 3-65.

Return to Summary Table.

VRTC Control Register
RESET register domain: HWRST

Figure 3-58. VRTC_CTRL Register

7	6	5	4	3	2	1	0
VRTC_18_15	VRTC_EN_SLP	VRTC_EN_OFF	VRTC_PWEN	RESERVED			
R-X	R/W-1h	R/W-1h	R/W-1h	R-0h			

Table 3-65. VRTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VRTC_18_15	R	X	VRTC voltage selection. This bit will allow to decrease the power consumption in BACKUP mode by setting the VRTC at 1.5V. 0: 1.8V (default) 1: 1.5V
6	VRTC_EN_SLP	R/W	1h	0: VRTC is configured in the standard power mode configuration when device is in SLEEP state (biasing also in SLEEP state). 1: VRTC is configured in a low-power mode configuration when device is in SLEEP state (biasing also in SLEEP state) (default).
5	VRTC_EN_OFF	R/W	1h	0: VRTC is configured in the standard power mode configuration when device is in OFF state (biasing also in OFF state) 1: VRTC is configured in a low-power mode configuration when device is in OFF state (biasing also in OFF state) (default).
4	VRTC_PWEN	R/W	1h	0: VRTC is configured in a low-power mode configuration. 1: VRTC is configured in the standard power mode configuration (default)
3-0	RESERVED	R	0h	

3.7.7 LONG_PRESS_KEY Register (Address = 1A9h) [reset = 3Ch]

LONG_PRESS_KEY is shown in Figure 3-59 and described in Table 3-66.

Return to Summary Table.

Long Press Key (LPK) configuration register
RESET register domain: HWRST

Figure 3-59. LONG_PRESS_KEY Register

7	6	5	4	3	2	1	0
LPK_LOCK	RESERVED	RESERVED	RESERVED	LPK_TIME		RESERVED	
R/W-0h	R-0h	R-1h	R-1h	R/W-3h		R-0h	

Table 3-66. LONG_PRESS_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LPK_LOCK	R/W	0h	Access protection of the LPK_TIME, LPK_EN and LPK_LOCK registers 0: No protection. R/W access to these register bits (default) 1: Protection of these registers (Read only). This bit will reset (0b0) during SWITCH-OFF
6	RESERVED	R	0h	
5	RESERVED	R	1h	
4	RESERVED	R	1h	
3-2	LPK_TIME	R/W	3h	Long press key duration 00: 6 second 01: 8 second 10: 10 second 11: 4 second (default)
1-0	RESERVED	R	0h	

3.7.8 OSC_THERM_CTRL Register (Address = 1AAh) [reset = Ch]

OSC_THERM_CTRL is shown in Figure 3-60 and described in Table 3-67.

Return to Summary Table.

Oscillator and Thermal control register
RESET register domain: HWRST

Figure 3-60. OSC_THERM_CTRL Register

7	6	5	4	3	2	1	0
VANA_ON_IN_SLEEP	INT_MASK_IN_SLEEP	RC15MHZ_ON_IN_SLEEP	THERM_OFF_IN_SLEEP	THERM_HD_SEL		RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-3h		R-0h	R-0h

Table 3-67. OSC_THERM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VANA_ON_IN_SLEEP	R/W	0h	0: VANA LDO is OFF in SLEEP mode (default) 1: VANA LDO is ON in SLEEP mode (In case some modules are used in SLEEP mode and need VANA (ILMON))
6	INT_MASK_IN_SLEEP	R/W	0h	INT masked selection during SLEEP mode (Released interrupt line only when DEVICE fully wake up) 0: INT is not masked in SLEEP mode (default) 1: INT is asserted when SLEEP2ACTIVE transition is completed (allow to wakeup platform before INT generation)
5	RC15MHZ_ON_IN_SLEEP	R/W	0h	RC15MHZ oscillator selection during SLEEP mode 0: RC15MHZ oscillator is OFF in SLEEP mode. Minimize consumption in SLEEP mode (default) 1: RC15MHZ oscillator is ON in SLEEP mode. It allow to make I2C/SPI access in SLEEP mode.
4	THERM_OFF_IN_SLEEP	R/W	0h	THERM selection during SLEEP mode (Minimization of the power consumption) 0: THERM is ON in SLEEP mode (default) 1: THERM is OFF in SLEEP mode
3-2	THERM_HD_SEL	R/W	3h	Hot die temperature detection selection: 00: 117 / 108 deg. 01: 121 / 112 deg. 10: 125 / 116 deg. 11: 130 / 120 deg. (default)
1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.7.9 SWOFF_HWRST Register (Address = 1AFh) [reset = X]

SWOFF_HWRST is shown in Figure 3-61 and described in Table 3-68.

Return to Summary Table.

Qualify which switch off events generate a HW RESET (configuration of behavior of the device)
RESET register domain: HWRST

Figure 3-61. SWOFF_HWRST Register

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

Table 3-68. SWOFF_HWRST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRON_LPK	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
6	PWRDOWN	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
5	WTD	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
4	TSHUT	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
3	RESET_IN	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
2	SW_RST	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
1	VSYS_LO	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)
0	GPADC_SHUTDOWN	R	X	0: Masked (Switchoff reset) 1: Not masked (Hardware reset)

3.7.10 SWOFF_COLDRST Register (Address = 1B0h) [reset = X]

SWOFF_COLDRST is shown in Figure 3-62 and described in Table 3-69.

Return to Summary Table.

Qualify which switch off events generate a COLD RESET (configuration of behavior of the device)
RESET register domain: HWRST

Figure 3-62. SWOFF_COLDRST Register

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-69. SWOFF_COLDRST Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRON_LPK	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
6	PWRDOWN	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
5	WTD	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
4	TSHUT	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
3	RESET_IN	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
2	SW_RST	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
1	VSYS_LO	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)
0	GPADC_SHUTDOWN	R/W	X	0: Masked (Shutdown) 1: Not masked (Cold restart)

3.7.11 SWOFF_STATUS Register (Address = 1B1h) [reset = 0h]

SWOFF_STATUS is shown in Figure 3-63 and described in Table 3-70.

Return to Summary Table.

Status register: registers switch off event
RESET register domain: PORRST

Figure 3-63. SWOFF_STATUS Register

7	6	5	4	3	2	1	0
PWRON_LPK	PWRDOWN	WTD	TSHUT	RESET_IN	SW_RST	VSYS_LO	GPADC_SHUTDOWN
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

Table 3-70. SWOFF_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWRON_LPK	RC	0h	
6	PWRDOWN	RC	0h	
5	WTD	RC	0h	
4	TSHUT	RC	0h	
3	RESET_IN	RC	0h	
2	SW_RST	RC	0h	
1	VSYS_LO	RC	0h	
0	GPADC_SHUTDOWN	RC	0h	0: no GPADC_SHUTDOWN 1: GPADC_SHUTDOWN occured since last read of this register

3.7.12 PMU_CONFIG Register (Address = 1B2h) [reset = X]

PMU_CONFIG is shown in Figure 3-64 and described in Table 3-71.

Return to Summary Table.

PMU configuration
RESET register domain: HWRST

Figure 3-64. PMU_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	HIGH_VCC_SENSE	PLL_AUTO_CTRL		SWOFF_DLY		RESERVED	AUTODEVON
R-0h	R/W-X	R/W-X		R/W-X		R-0h	R/W-X

Table 3-71. PMU_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	HIGH_VCC_SENSE	R/W	X	Enable input buffer for VCC_SENSE input to reduce input leakage. Rrecommended when VCC_SENSE is >5V 0: VCC_SENSE input buffer is not enabled 1: VCC_SENSE input buffer is enabled
5-4	PLL_AUTO_CTRL	R/W	X	Enable/disable PLL under different device mode: 00 : PLL is not enabled/disabled automatically. PLL enable command should be stored in OTP for power sequence. 01 : Enable PLL in ACTIVE mode at the start point of OFF2ACT transition. Disabled at the end point of ACT2OFF. 10 : Enable PLL in SLEEP mode only. 11 : Enable PLL in both of ACTIVE mode and SLEEP mode at the start point of OFF2ACT transition. Disabled at the end point of ACT2OFF.
3-2	SWOFF_DLY	R/W	X	Delay before to go to SWITCH-OFF to allow host processor to save his context (device will be maintained ACTIVE until delay expiration then SWITCH-OFF) 00: no delay 01: 1 second window (+/- 250ms) 10: 2 second window (+/- 250ms) 11: 4 second window (+/- 250ms)
1	RESERVED	R	0h	
0	AUTODEVON	R/W	X	Selection of the feature Auto Device ON 0: Feature is inactive 1: Feature is active

3.7.13 PMU_CTRL2 Register (Address = 1B3h) [reset = X]

PMU_CTRL2 is shown in Figure 3-65 and described in Table 3-72.

Return to Summary Table.

Power Management Unit Control #2
RESET register domain: HWRST

Figure 3-65. PMU_CTRL2 Register

7	6	5	4	3	2	1	0
SPARE7	SPARE6	SPARE5	SPARE4	INT_LINE_DIS	WDT_HOLD_IN_SLEEP	PWRDOWN_FASTOFF	TSHUT_FASTOFF
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-72. PMU_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPARE7	R/W	X	
6	SPARE6	R/W	X	
5	SPARE5	R/W	X	
4	SPARE4	R/W	X	
3	INT_LINE_DIS	R/W	X	Interrupt line (INT) output buffer configuration 0: Normal operation (standard buffer - OD or PP -) 1: INT output buffer is high-impedance with an internal pull-up to VIO enabled
2	WDT_HOLD_IN_SLEEP	R/W	X	0: primary watchdog timer continues to run in device sleep state 1: primary watchdog timer is hold in device sleep state
1	PWRDOWN_FASTOFF	R/W	X	0: PWRDOWN event triggers normal switch off sequence 1: PWRDOWN event triggers fast switch off sequence (all resources disabeld together)
0	TSHUT_FASTOFF	R/W	X	0: TSHUT event triggers normal switch off sequence 1: TSHUT event triggers fast switch off sequence (all resources disabeld together)

3.7.14 PMU_SECONDARY_INT Register (Address = 1B5h) [reset = X]

PMU_SECONDARY_INT is shown in Figure 3-66 and described in Table 3-73.

Return to Summary Table.

Configuration and status of the Secondary Interrupt Handler
RESET register domain: HWRST

Figure 3-66. PMU_SECONDARY_INT Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	FSD_INT_SRC	RESERVED	RESERVED	RESERVED	FSD_MASK
R-0h	R-0h	R-0h	RC-0h	R-0h	R-0h	R-0h	R/W-X

Table 3-73. PMU_SECONDARY_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	FSD_INT_SRC	RC	0h	First Supply Detection (FSD) interrupt status source 0: First Supply Detection (FSD) is not the source of interrupt line BB_FSD 1: First Supply Detection (FSD) is the source of interrupt line BB_FSD
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	FSD_MASK	R/W	X	Secondary level of mask for FSD_BB interrupt line. First Supply Detection (FSD) Mask. 0: Un-masked 1: Masked

3.7.15 SW_REVISION Register (Address = 1B7h) [reset = X]

SW_REVISION is shown in Figure 3-67 and described in Table 3-74.

Return to Summary Table.

Software (SW) revision register
RESET register domain: HWRST

Figure 3-67. SW_REVISION Register

7	6	5	4	3	2	1	0
SW_REVISION							
R-X							

Table 3-74. SW_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW_REVISION	R	X	Software (SW) revision register - This revision will be representative of the OTP version.

3.7.16 PMU_SECONDARY_INT2 Register (Address = 1B9h) [reset = 0h]

PMU_SECONDARY_INT2 is shown in Figure 3-68 and described in Table 3-75.

Return to Summary Table.

Configuration and status of the Secondary Interrupt Handler (Register2)
RESET register domain: HWRST

Figure 3-68. PMU_SECONDARY_INT2 Register

7	6	5	4	3	2	1	0
RESERVED			DVFS_INT_SRC	RESERVED			DVFS_MASK
RC-0h			RC-0h	R-0h			R/W-0h

Table 3-75. PMU_SECONDARY_INT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	RC	0h	
4	DVFS_INT_SRC	RC	0h	DVFS (Voltage plus offset over voltage max) interrupt status source 0: DVFS (Voltage plus offset over voltage max) is not the source of interrupt line 1: DVFS (Voltage plus offset over voltage max) is the source of interrupt line
3-1	RESERVED	R	0h	
0	DVFS_MASK	R/W	0h	Secondary level of mask for DVFS interrupt line. Voltage plus offset over voltage max mask. 0: Un-masked 1: Masked

3.7.17 BOOT_STATUS Register (Address = 1C3h) [reset = X]

BOOT_STATUS is shown in Figure 3-69 and described in Table 3-76.

Return to Summary Table.

Configuration and status of the Boot Status Register. The boot mode is only latched during POR, and should not be changed while the PMIC is supplied.
RESET register domain: POR

Figure 3-69. BOOT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							BOOT_MODE
R-0h							R-X

Table 3-76. BOOT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	BOOT_MODE	R	X	BOOT mode selection 0: BOOT pin is pulled low 1: BOOT pin is pulled high

3.8 FUNC_RESOURCE Registers

Table 3-77 lists the memory-mapped registers for the FUNC_RESOURCE. All register offset addresses not listed in Table 3-77 should be considered as reserved locations and the register contents should not be modified.

Table 3-77. FUNC_RESOURCE Registers

Address	Acronym	Register Name	Section
1D6h	REGEN1_CTRL	REGEN1 control register RESET register domain: SWORST	Section 3.8.1
1D7h	PLLEN_CTRL	PLLEN control register RESET register domain: SWORST	Section 3.8.2
1DAh	NSLEEP_RES_ASSIGN	NSLEEP resource assignment register RESET register domain: HWRST	Section 3.8.3
1DBh	NSLEEP_SMPS_ASSIGN	NSLEEP input signal SMPS resource assignment register RESET register domain: HWRST	Section 3.8.4
1DCh	NSLEEP_LDO_ASSIGN1	NSLEEP input signal LDO resource assignment register #1 RESET register domain: HWRST	Section 3.8.5
1DDh	NSLEEP_LDO_ASSIGN2	NSLEEP input signal LDO resource assignment register #2 RESET register domain: HWRST	Section 3.8.6
1DEh	ENABLE1_RES_ASSIGN	ENABLE1 resource assignment register RESET register domain: HWRST	Section 3.8.7
1DFh	ENABLE1_SMPS_ASSIGN	ENABLE1 input signal SMPS resource assignment register RESET register domain: HWRST	Section 3.8.8
1E0h	ENABLE1_LDO_ASSIGN1	ENABLE1 input signal LDO resource assignment register #1 RESET register domain: HWRST	Section 3.8.9
1E1h	ENABLE1_LDO_ASSIGN2	ENABLE1 input signal LDO resource assignment register #2 RESET register domain: HWRST	Section 3.8.10
1E2h	ENABLE2_RES_ASSIGN	ENABLE2 resource assignment register RESET register domain: HWRST	Section 3.8.11
1E3h	ENABLE2_SMPS_ASSIGN	ENABLE2 input signal SMPS resource assignment register RESET register domain: HWRST	Section 3.8.12
1E4h	ENABLE2_LDO_ASSIGN1	ENABLE2 input signal LDO resource assignment register #1 RESET register domain: HWRST	Section 3.8.13
1E5h	ENABLE2_LDO_ASSIGN2	ENABLE2 input signal LDO resource assignment register #2 RESET register domain: HWRST	Section 3.8.14
1E6h	REGEN2_CTRL	REGEN2 control register RESET register domain: SWORST	Section 3.8.15
1E7h	REGEN3_CTRL	REGEN3 control register RESET register domain: SWORST	Section 3.8.16

3.8.1 REGEN1_CTRL Register (Address = 1D6h) [reset = X]

REGEN1_CTRL is shown in Figure 3-70 and described in Table 3-78.

Return to Summary Table.

REGEN1 control register
RESET register domain: SWORST

Figure 3-70. REGEN1_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-78. REGEN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	REGEN1 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	REGEN1 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	REGEN1 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.2 PLLEN_CTRL Register (Address = 1D7h) [reset = 0h]

PLLEN_CTRL is shown in Figure 3-71 and described in Table 3-79.

Return to Summary Table.

PLLEN control register
RESET register domain: SWORST

Figure 3-71. PLLEN_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-0h

Table 3-79. PLLEN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	PLLEN Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	PLLEN SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	0h	PLLEN ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.3 NSLEEP_RES_ASSIGN Register (Address = 1DAh) [reset = 0h]

NSLEEP_RES_ASSIGN is shown in Figure 3-72 and described in Table 3-80.

Return to Summary Table.

NSLEEP resource assignment register
RESET register domain: HWRST

Figure 3-72. NSLEEP_RES_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED				PLL_EN	REGEN3	REGEN2	REGEN1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-80. NSLEEP_RES_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	PLL_EN	R/W	0h	0: NSLEEP has no effect on PLL_EN 1: PLL_EN is controlled by NSLEEP
2	REGEN3	R/W	0h	0: NSLEEP has no effect on REGEN3 1: REGEN3 is controlled by NSLEEP
1	REGEN2	R/W	0h	0: NSLEEP has no effect on REGEN2 1: REGEN2 is controlled by NSLEEP
0	REGEN1	R/W	0h	0: NSLEEP has no effect on REGEN1 1: REGEN1 is controlled by NSLEEP

3.8.4 NSLEEP_SMPS_ASSIGN Register (Address = 1DBh) [reset = 0h]

NSLEEP_SMPS_ASSIGN is shown in Figure 3-73 and described in Table 3-81.

Return to Summary Table.

NSLEEP input signal SMPS resource assignment register
RESET register domain: HWRST

Figure 3-73. NSLEEP_SMPS_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-81. NSLEEP_SMPS_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
5	RESERVED	R	0h	
4	SMPS4	R/W	0h	0: NSLEEP has no effect on SMPS4 1: SMPS4 is controlled by NSLEEP
3	SMPS3	R/W	0h	0: NSLEEP has no effect on SMPS3 1: SMPS3 is controlled by NSLEEP
2	RESERVED	R/W	0h	
1	SMPS2	R/W	0h	0: NSLEEP has no effect on SMPS2 1: SMPS2 is controlled by NSLEEP
0	SMPS1	R/W	0h	0: NSLEEP has no effect on SMPS1 (or SMPS12 is dual phase selected) 1: SMPS1 (or SMPS12 is dual phase selected) is controlled by NSLEEP)

3.8.5 NSLEEP_LDO_ASSIGN1 Register (Address = 1DCh) [reset = 0h]

NSLEEP_LDO_ASSIGN1 is shown in Figure 3-74 and described in Table 3-82.

Return to Summary Table.

NSLEEP input signal LDO resource assignment register #1
RESET register domain: HWRST

Figure 3-74. NSLEEP_LDO_ASSIGN1 Register

7	6	5	4	3	2	1	0
LDO4	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO2	LDO1
R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

Table 3-82. NSLEEP_LDO_ASSIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4	R/W	0h	0: NSLEEP has no effect on LDO4 1: LDO4 is controlled by NSLEEP
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R/W	0h	
2	RESERVED	R	0h	
1	LDO2	R/W	0h	0: NSLEEP has no effect on LDO2 1: LDO2 is controlled by NSLEEP
0	LDO1	R/W	0h	0: NSLEEP has no effect on LDO1 1: LDO1 is controlled by NSLEEP

3.8.6 NSLEEP_LDO_ASSIGN2 Register (Address = 1DDh) [reset = 0h]

NSLEEP_LDO_ASSIGN2 is shown in Figure 3-75 and described in Table 3-83.

Return to Summary Table.

NSLEEP input signal LDO resource assignment register #2
RESET register domain: HWRST

Figure 3-75. NSLEEP_LDO_ASSIGN2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO5	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h

Table 3-83. NSLEEP_LDO_ASSIGN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
1	LDO5	R/W	0h	0: NSLEEP has no effect on LDO5 1: LDO5 is controlled by NSLEEP
0	RESERVED	R	0h	

3.8.7 ENABLE1_RES_ASSIGN Register (Address = 1DEh) [reset = 0h]

ENABLE1_RES_ASSIGN is shown in Figure 3-76 and described in Table 3-84.

Return to Summary Table.

ENABLE1 resource assignment register
RESET register domain: HWRST

Figure 3-76. ENABLE1_RES_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED				PLL_EN	REGEN3	REGEN2	REGEN1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-84. ENABLE1_RES_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	PLL_EN	R/W	0h	0: ENABLE1 has no effect on PLL_EN 1: PLL_EN is controlled by ENABLE1
2	REGEN3	R/W	0h	0: ENABLE1 has no effect on REGEN3 1: REGEN3 is controlled by ENABLE1
1	REGEN2	R/W	0h	0: ENABLE1 has no effect on REGEN2 1: REGEN2 is controlled by ENABLE1
0	REGEN1	R/W	0h	0: ENABLE1 has no effect on REGEN1 1: REGEN1 is controlled by ENABLE1

3.8.8 ENABLE1_SMPS_ASSIGN Register (Address = 1DFh) [reset = 0h]

ENABLE1_SMPS_ASSIGN is shown in Figure 3-77 and described in Table 3-85.

Return to Summary Table.

ENABLE1 input signal SMPS resource assignment register
RESET register domain: HWRST

Figure 3-77. ENABLE1_SMPS_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

Table 3-85. ENABLE1_SMPS_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
5	RESERVED	R	0h	
4	SMPS4	R/W	0h	0: ENABLE1 has no effect on SMPS4 1: SMPS4 is controlled by ENABLE1
3	SMPS3	R/W	0h	0: ENABLE1 has no effect on SMPS3 1: SMPS3 is controlled by ENABLE1
2	RESERVED	R	0h	
1	SMPS2	R/W	0h	0: ENABLE1 has no effect on SMPS2 1: SMPS2 is controlled by ENABLE1
0	SMPS1	R/W	0h	0: ENABLE1 has no effect on SMPS1(or SMPS12 is dual phase selected) 1: SMPS1 (or SMPS12 is dual phase selected) is controlled by ENABLE1

3.8.9 ENABLE1_LDO_ASSIGN1 Register (Address = 1E0h) [reset = 0h]

ENABLE1_LDO_ASSIGN1 is shown in Figure 3-78 and described in Table 3-86.

Return to Summary Table.

ENABLE1 input signal LDO resource assignment register #1
RESET register domain: HWRST

Figure 3-78. ENABLE1_LDO_ASSIGN1 Register

7	6	5	4	3	2	1	0
LDO4	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO2	LDO1
R/W-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h

Table 3-86. ENABLE1_LDO_ASSIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4	R/W	0h	0: ENABLE1 has no effect on LDO4 1: LDO4 is controlled by ENABLE1
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	LDO2	R/W	0h	0: ENABLE1 has no effect on LDO2 1: LDO2 is controlled by ENABLE1
0	LDO1	R/W	0h	0: ENABLE1 has no effect on LDO1 1: LDO1 is controlled by ENABLE1

3.8.10 ENABLE1_LDO_ASSIGN2 Register (Address = 1E1h) [reset = 0h]

ENABLE1_LDO_ASSIGN2 is shown in Figure 3-79 and described in Table 3-87.

Return to Summary Table.

ENABLE1 input signal LDO resource assignment register #2
RESET register domain: HWRST

Figure 3-79. ENABLE1_LDO_ASSIGN2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO5	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h

Table 3-87. ENABLE1_LDO_ASSIGN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
1	LDO5	R/W	0h	0: ENABLE1 has no effect on LDO5 1: LDO5 is controlled by ENABLE1
0	RESERVED	R	0h	

3.8.11 ENABLE2_RES_ASSIGN Register (Address = 1E2h) [reset = 0h]

ENABLE2_RES_ASSIGN is shown in Figure 3-80 and described in Table 3-88.

Return to Summary Table.

ENABLE2 resource assignment register
RESET register domain: HWRST

Figure 3-80. ENABLE2_RES_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED				PLL_EN	REGEN3	REGEN2	REGEN1
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-88. ENABLE2_RES_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	PLL_EN	R/W	0h	0: ENABLE2 has no effect on PLL_EN 1: PLL_EN is controlled by ENABLE2
2	REGEN3	R/W	0h	0: ENABLE2 has no effect on REGEN3 1: REGEN3 is controlled by ENABLE2
1	REGEN2	R/W	0h	0: ENABLE2 has no effect on REGEN2 1: REGEN2 is controlled by ENABLE2
0	REGEN1	R/W	0h	0: ENABLE2 has no effect on REGEN1 1: REGEN1 is controlled by ENABLE2

3.8.12 ENABLE2_SMPS_ASSIGN Register (Address = 1E3h) [reset = 0h]

ENABLE2_SMPS_ASSIGN is shown in Figure 3-81 and described in Table 3-89.

Return to Summary Table.

ENABLE2 input signal SMPS resource assignment register
RESET register domain: HWRST

Figure 3-81. ENABLE2_SMPS_ASSIGN Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	SMPS4	SMPS3	RESERVED	SMPS2	SMPS1
R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

Table 3-89. ENABLE2_SMPS_ASSIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
5	RESERVED	R	0h	
4	SMPS4	R/W	0h	0: ENABLE2 has no effect on SMPS4 1: SMPS4 is controlled by ENABLE2
3	SMPS3	R/W	0h	0: ENABLE2 has no effect on SMPS3 1: SMPS3 is controlled by ENABLE2
2	RESERVED	R	0h	
1	SMPS2	R/W	0h	0: ENABLE2 has no effect on SMPS3 1: SMPS3 is controlled by ENABLE2
0	SMPS1	R/W	0h	0: ENABLE2 has no effect on SMPS1 (or SMPS12 is dual phase selected) 1: SMPS1 (or SMPS12 is dual phase selected) is controlled by ENABLE2

3.8.13 ENABLE2_LDO_ASSIGN1 Register (Address = 1E4h) [reset = 0h]

ENABLE2_LDO_ASSIGN1 is shown in Figure 3-82 and described in Table 3-90.

Return to Summary Table.

ENABLE2 input signal LDO resource assignment register #1
RESET register domain: HWRST

Figure 3-82. ENABLE2_LDO_ASSIGN1 Register

7	6	5	4	3	2	1	0
LDO4	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO2	LDO1
R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h

Table 3-90. ENABLE2_LDO_ASSIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO4	R/W	0h	0: ENABLE2 has no effect on LDO4 1: LDO4 is controlled by ENABLE2
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R/W	0h	
2	RESERVED	R	0h	
1	LDO2	R/W	0h	0: ENABLE2 has no effect on LDO2 1: LDO2 is controlled by ENABLE2
0	LDO1	R/W	0h	0: ENABLE2 has no effect on LDO1 1: LDO1 is controlled by ENABLE2

3.8.14 ENABLE2_LDO_ASSIGN2 Register (Address = 1E5h) [reset = 0h]

ENABLE2_LDO_ASSIGN2 is shown in Figure 3-83 and described in Table 3-91.

Return to Summary Table.

ENABLE2 input signal LDO resource assignment register #2
RESET register domain: HWRST

Figure 3-83. ENABLE2_LDO_ASSIGN2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO5	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h

Table 3-91. ENABLE2_LDO_ASSIGN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
1	LDO5	R/W	0h	0: ENABLE2 has no effect on LDO5 1: LDO5 is controlled by ENABLE2
0	RESERVED	R	0h	

3.8.15 REGEN2_CTRL Register (Address = 1E6h) [reset = X]

REGEN2_CTRL is shown in Figure 3-84 and described in Table 3-92.

Return to Summary Table.

REGEN2 control register
RESET register domain: SWORST

Figure 3-84. REGEN2_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-92. REGEN2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	REGEN2 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	REGEN2 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	REGEN2 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.8.16 REGEN3_CTRL Register (Address = 1E7h) [reset = X]

REGEN3_CTRL is shown in Figure 3-85 and described in Table 3-93.

Return to Summary Table.

REGEN3 control register
RESET register domain: SWORST

Figure 3-85. REGEN3_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			STATUS	RESERVED	MODE_SLEEP	RESERVED	MODE_ACTIVE
R-0h			R-0h	R-0h	R/W-0h	R-0h	R/W-X

Table 3-93. REGEN3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STATUS	R	0h	REGEN3 Status 0: OFF 1: ON
3	RESERVED	R	0h	
2	MODE_SLEEP	R/W	0h	REGEN3 SLEEP Mode 0: OFF 1: ON
1	RESERVED	R	0h	
0	MODE_ACTIVE	R/W	X	REGEN3 ACTIVE Mode (OTP-Sequencer) 0: OFF 1: ON

3.9 FUNC_PAD_CONTROL Registers

Table 3-94 lists the memory-mapped registers for the FUNC_PAD_CONTROL. All register offset addresses not listed in Table 3-94 should be considered as reserved locations and the register contents should not be modified.

Table 3-94. FUNC_PAD_CONTROL Registers

Address	Acronym	Register Name	Section
1F2h	OD_OUTPUT_CTRL2	Open Drain control register #2 RESET register domain: HWRST	Section 3.9.1
1F4h	PU_PD_INPUT_CTRL1	Pull-up Pull-down control register #1 RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)	Section 3.9.2
1F5h	PU_PD_INPUT_CTRL2	Pull-up Pull-down control register #2 RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)	Section 3.9.3
1F6h	PU_PD_INPUT_CTRL3	Pull-up Pull-down control register #3 RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)	Section 3.9.4
1F8h	OD_OUTPUT_CTRL	Open Drain control register RESET register domain: HWRST Note: It is user responsibility to take care about the IO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections	Section 3.9.5
1F9h	POLARITY_CTRL	Polarity control register. This register allows to invert the initial polarity of the input or output pin. RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO polarity	Section 3.9.6
1FAh	PRIMARY_SECONDARY_PAD1	PAD/PIN function register (Primary vs. Secondary) #1 RESET register domain: HWRST	Section 3.9.7
1FBh	PRIMARY_SECONDARY_PAD2	PAD/PIN function register (Primary vs. Secondary) #2 RESET register domain: HWRST	Section 3.9.8
1FCh	I2C_SPI	Validity memory RESET register domain: HWRST	Section 3.9.9

3.9.1 OD_OUTPUT_CTRL2 Register (Address = 1F2h) [reset = X]

OD_OUTPUT_CTRL2 is shown in Figure 3-86 and described in Table 3-95.

Return to Summary Table.

Open Drain control register #2
RESET register domain: HWRST

Figure 3-86. OD_OUTPUT_CTRL2 Register

7	6	5	4	3	2	1	0
RESET_OUT_OD	RESERVED				RESERVED	REGEN2_OD	RESERVED
R/W-X	R-0h				R-0h	R/W-X	R-0h

Table 3-95. OD_OUTPUT_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET_OUT_OD	R/W	X	0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)
6-3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	REGEN2_OD	R/W	X	0: open drain not enable (Push-Pull enabled) 1: open drain enable (Push-Pull not enable)
0	RESERVED	R	0h	

3.9.2 PU_PD_INPUT_CTRL1 Register (Address = 1F4h) [reset = X]

PU_PD_INPUT_CTRL1 is shown in Figure 3-87 and described in Table 3-96.

Return to Summary Table.

Pull-up Pull-down control register #1
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)

Figure 3-87. PU_PD_INPUT_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RESET_IN_PD	RESERVED	RESERVED	RESERVED	PWRDOWN_PD	RESERVED	NRESWARM_PD
R-0h	R/W-X	R-0h	R-0h	R-0h	R/W-X	R-0h	R/W-X

Table 3-96. PU_PD_INPUT_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESET_IN_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	PWRDOWN_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled
1	RESERVED	R	0h	
0	NRESWARM_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default for non-reset)

3.9.3 PU_PD_INPUT_CTRL2 Register (Address = 1F5h) [reset = 16h]

PU_PD_INPUT_CTRL2 is shown in Figure 3-88 and described in Table 3-97.

Return to Summary Table.

Pull-up Pull-down control register #2
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)

Figure 3-88. PU_PD_INPUT_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	ENABLE2_PD	ENABLE1_PU	ENABLE1_PD	NSLEEP_PU	NSLEEP_PD
R-0h		R-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-0h

Table 3-97. PU_PD_INPUT_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	ENABLE2_PD	R/W	1h	0: Pull-down not enabled 1: Pull-down enabled (default)
3	ENABLE1_PU	R/W	0h	0: Pull-up not enabled (default) 1: Pull-up enabled
2	ENABLE1_PD	R/W	1h	0: Pull-down not enabled 1: Pull-down enabled (default)
1	NSLEEP_PU	R/W	1h	0: Pull-up not enabled 1: Pull-up enabled (default)
0	NSLEEP_PD	R/W	0h	0: Pull-down not enabled (default) 1: Pull-down enabled

3.9.4 PU_PD_INPUT_CTRL3 Register (Address = 1F6h) [reset = 44h]

PU_PD_INPUT_CTRL3 is shown in Figure 3-89 and described in Table 3-98.

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Pull-up Pull-down control register #3
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO direction and type (Open drain / Push-Pull)

Figure 3-89. PU_PD_INPUT_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED	SYNCDCDC_PD	RESERVED	RESERVED	RESERVED	POWERHOLD_PD	RESERVED	RESERVED
R-0h	R/W-1h	R-0h	R-0h	R-0h	R/W-1h	R-0h	R-0h

Table 3-98. PU_PD_INPUT_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	-
6	SYNCDCDC_PD	R/W	1h	Secondary function of GPIO_3 0: Pull-down not enabled 1: Pull-down enabled
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	POWERHOLD_PD	R/W	1h	Secondary function of GPIO_5 0: Pull-down not enabled 1: Pull-down enabled (default)
1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.9.5 OD_OUTPUT_CTRL Register (Address = 1F8h) [reset = 0h]

OD_OUTPUT_CTRL is shown in Figure 3-90 and described in Table 3-99.

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Open Drain control register
RESET register domain: HWRST
Note: It is user responsibility to take care about the IO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections

Figure 3-90. OD_OUTPUT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	INT_OD	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h

Table 3-99. OD_OUTPUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	INT_OD	R/W	0h	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.9.6 POLARITY_CTRL Register (Address = 1F9h) [reset = X]

POLARITY_CTRL is shown in Figure 3-91 and described in Table 3-100.

Return to Summary Table.

Polarity control register. This register allows to invert the initial polarity of the input or output pin.
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the IO polarity

Figure 3-91. POLARITY_CTRL Register

7	6	5	4	3	2	1	0
INT_POLARITY	GPIO_6_POLARITY	GPIO_5_POLARITY	GPIO_4_POLARITY	GPIO_3_POLARITY	GPIO_2_POLARITY	GPIO_1_POLARITY	GPIO_0_POLARITY
R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-100. POLARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POLARITY	R/W	X	Select the polarity of the INT output line 0: Interrupt line (INT) is low when interrupt is pending (default) 1: Interrupt line (INT) is high when interrupt is pending
6	GPIO_6_POLARITY	R/W	X	Select the polarity of the GPIO_6 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low In case NSLEEP input line is selected as secondary function: 0: Resources will go in SLEEP mode when NSLEEP is low (default) 1: Resources will go in SLEEP mode when NSLEEP is high
5	GPIO_5_POLARITY	R/W	X	Select the polarity of the GPIO_5 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low
4	GPIO_4_POLARITY	R/W	X	Select the polarity of the GPIO_4 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low
3	GPIO_3_POLARITY	R/W	X	Select the polarity of the GPIO_3 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low In case ENABLE1 input line is selected as secondary function: 0: Resources will be enable when ENABLE1 is high (default) 1: Resources will be enable when ENABLE1 is low
2	GPIO_2_POLARITY	R/W	X	Select the polarity of the GPIO_2 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low In case ENABLE1 input line is selected as secondary function: 0: Resources will be enable when ENABLE1 is high (default) 1: Resources will be enable when ENABLE1 is low

Table 3-100. POLARITY_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	GPIO_1_POLARITY	R/W	X	Select the polarity of the GPIO_1 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low In case RESET_IN input line is selected as secondary function: 0: Device is switch-off when RESET_IN is low (default) 1: Device is switch-off when RESET_IN is high In case NRESWARM input line is selected as secondary function: 0: Device is warm reset when NRESWARM is low (default) 1: Device is warm reset when NRESWARM is high
0	GPIO_0_POLARITY	R/W	X	Select the polarity of the GPIO_0 input or output lines and associated secondary functions 0: inversion not enable - active high (default) 1: inversion is enabled - active low In case ENABLE2 input line is selected as secondary function: 0: Resources will be enable when ENABLE2 is high (default) 1: Resources will be enable when ENABLE12is low In case POWERDOWN input line is selected as secondary function: 0: Inversion is not enabled - active high (default) 1: Inversion is enabled - active low

3.9.7 PRIMARY_SECONDARY_PAD1 Register (Address = 1FAh) [reset = X]

PRIMARY_SECONDARY_PAD1 is shown in Figure 3-92 and described in Table 3-101.

Return to Summary Table.

PAD/PIN function register (Primary vs. Secondary) #1
RESET register domain: HWRST

Figure 3-92. PRIMARY_SECONDARY_PAD1 Register

7	6	5	4	3	2	1	0
GPIO_3		GPIO_2		GPIO_1		GPIO_0	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 3-101. PRIMARY_SECONDARY_PAD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	GPIO_3	R/W	X	Selection primary or secondary function associated to GPIO_3 pin/pad 00: Primary function is selected (GPIO_3) 01: Secondary function is selected (ENABLE2) 10: Secondary function is selected (REGEN1) 11: Secondary function is selected (SYNCDCDC)
5-4	GPIO_2	R/W	X	Selection primary or secondary function associated to GPIO_2 pin/pad 00: Primary function is selected (GPIO_2) 01: Reserved 10: Secondary function is selected (ENABLE1) 11: Secondary function is selected (I2C_SDA_SDO)
3-2	GPIO_1	R/W	X	Selection primary or secondary function associated to GPIO_1 pin/pad 00: Primary function is selected (GPIO_1) 01: Secondary function is selected (RESET_IN) 10: Secondary function is selected (NRESWARM) 11: Secondary function is selected (VBUS_SENSE)
1-0	GPIO_0	R/W	X	Selection primary or secondary function associated to GPIO_0 pin/pad 00: Primary function is selected (GPIO_0) 01: Secondary function is selected (PWRDOWN) 10: Secondary function is selected (ENABLE2) 11: Secondary function is selected (REGEN1)

3.9.8 PRIMARY_SECONDARY_PAD2 Register (Address = 1FBh) [reset = X]

PRIMARY_SECONDARY_PAD2 is shown in Figure 3-93 and described in Table 3-102.

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PAD/PIN function register (Primary vs. Secondary) #2
RESET register domain: HWRST

Figure 3-93. PRIMARY_SECONDARY_PAD2 Register

7	6	5	4	3	2	1	0
RESERVED	SYNCCLKOUT	GPIO_6		GPIO_5		GPIO_4	
R-0h	R/W-X	R/W-X		R/W-X		R/W-X	

Table 3-102. PRIMARY_SECONDARY_PAD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SYNCCLKOUT	R/W	X	Selects the primary or secondary function associated to the SYNCCLKOUT pin/pad 0: Primary function is selected (SYNCDCDCCLK) 1: Secondary function is selected (CLK32KGO)
5-4	GPIO_6	R/W	X	Selection primary or secondary function associated to GPIO_6 pin/pad 00: Primary function is selected (GPIO_6) 01: Secondary function is selected (NSLEEP) 10: Secondary function is selected (POWERGOOD) 11: Secondary function is selected (REGEN3)
3-2	GPIO_5	R/W	X	Selection primary or secondary function associated to GPIO_5 pin/pad 00: Primary function is selected (GPIO_5) 01: Secondary function is selected (POWERHOLD) 10: Secondary function is selected (REGEN3) 11: Secondary function is selected (REGEN3)
1-0	GPIO_4	R/W	X	Selection primary or secondary function associated to GPIO_4 pin/pad 00: Primary function is selected (GPIO_4) 01: Reserved 10: Secondary function is selected (REGEN2) 11: Secondary function is selected (I2C2_SCL_SCE)

3.9.9 I2C_SPI Register (Address = 1FCh) [reset = X]

I2C_SPI is shown in Figure 3-94 and described in Table 3-103.

Return to Summary Table.

Validity memory
RESET register domain: HWRST

Figure 3-94. I2C_SPI Register

7	6	5	4	3	2	1	0
I2C2OTP_EN	I2C2OTP_PAGESEL	ID_I2C2	I2C_SPI	ID_I2C1			
R/W-0h	R/W-0h	R/W-X	R/W-X	R/W-X			

Table 3-103. I2C_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C2OTP_EN	R/W	0h	I2C to OTP (I2C2OTP) feature selection (EVM purpose only) 0: I2C2OTP is disable 1: I2C2OTP is enabled
6	I2C2OTP_PAGESEL	R/W	0h	I2C to OTP (I2C2OTP) page selection (EVM purpose only) 0: page0 is selected (OTP-page0 (Test/Trim - reserved), OTP-page1 (Sequencer - LSB), OTP-page2 (Sequencer), OTP-page3 (Sequencer)) 1: page1 is selected (OTP-page4 (Sequencer - MSB), OTP-page5 (Config))
5	ID_I2C2	R/W	X	I2C_2 address for page access versus initial address (0H12) 0: Address 0H12 1: Address 0H22
4	I2C_SPI	R/W	X	Selection of the interface 0: I2C 1: SPI
3-0	ID_I2C1	R/W	X	I2C_1 address for page accesses versus initial address (0H48, 0H49, 0H4A, 0H4B (OTP)) I2C_1[0]=0: 0H48 I2C_1[0]=1: 0H58 I2C_1[1]=0: 0H49 I2C_1[1]=1: 0H59 I2C_1[2]=0: 0H4A I2C_1[2]=1: 0H5A I2C_1[3]=0: 0H4B I2C_1[3]=1: 0H5B

3.10 FUNC_INTERRUPT Registers

Table 3-104 lists the memory-mapped registers for the FUNC_INTERRUPT. All register offset addresses not listed in Table 3-104 should be considered as reserved locations and the register contents should not be modified.

Table 3-104. FUNC_INTERRUPT Registers

Address	Acronym	Register Name	Section
210h	INT1_STATUS	Interrupt Status Register #1 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST	Section 3.10.1
211h	INT1_MASK	Interrupt Line Mask Register #1 RESET register domain: HWRST	Section 3.10.2
212h	INT1_LINE_STATE	Interrupt source line state Register #1 RESET register domain: HWRST	Section 3.10.3
215h	INT2_STATUS	Interrupt Status Register #2 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST	Section 3.10.4
216h	INT2_MASK	Interrupt Line Mask Register #2 RESET register domain: HWRST	Section 3.10.5
217h	INT2_LINE_STATE	Interrupt source line state Register #2 RESET register domain: HWRST	Section 3.10.6
21Ah	INT3_STATUS	Interrupt Status Register #3 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST	Section 3.10.7
21Bh	INT3_MASK	Interrupt Line Mask Register #3 RESET register domain: HWRST	Section 3.10.8
21Ch	INT3_LINE_STATE	Interrupt source line state Register #3 RESET register domain: HWRST	Section 3.10.9
21Fh	INT4_STATUS	Interrupt Status Register #4 The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR) RESET register domain: HWRST	Section 3.10.10
220h	INT4_MASK	Interrupt Line Mask Register #4 RESET register domain: HWRST	Section 3.10.11
221h	INT4_LINE_STATE	Interrupt source line state Register #4 RESET register domain: HWRST	Section 3.10.12
222h	INT4_EDGE_DETECT1	Interrupt Edge Detection Register #4.1 RESET register domain: HWRST	Section 3.10.13
223h	INT4_EDGE_DETECT2	Interrupt Edge Detection Register #4.2 RESET register domain: HWRST	Section 3.10.14
224h	INT_CTRL	Interrupt control register RESET register domain: HWRST	Section 3.10.15
225h	OTP_CRC_RESULTS	OTP CRC Checker reuslt register RESET register domain: HWRST	Section 3.10.16

3.10.1 INT1_STATUS Register (Address = 210h) [reset = 0h]

INT1_STATUS is shown in Figure 3-95 and described in Table 3-105.

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Interrupt Status Register #1
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-95. INT1_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	VSYS_MON	HOTDIE	PWRDOWN	RESERVED	LONG_PRESS_KEY	PWRON	RESERVED
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

Table 3-105. INT1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	RC	0h	
6	VSYS_MON	RC	0h	VSYS_MON status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected
5	HOTDIE	RC	0h	HOTDIE status bit register (internal event) 0: no detection 1: Rising or Falling edge are detected
4	PWRDOWN	RC	0h	PWRDOWN status bit register associated to PWRDOWN pin 0: no detection 1: Rising or Falling edge are detected
3	RESERVED	RC	0h	
2	LONG_PRESS_KEY	RC	0h	LONG_PRESS_KEY (Long Key press duration) status bit register 0: no detection 1: Falling edge is detected
1	PWRON	RC	0h	PWRON status bit register associated to PWRON pin 0: no detection 1: Falling edge is detected
0	RESERVED	RC	0h	

3.10.2 INT1_MASK Register (Address = 211h) [reset = X]

INT1_MASK is shown in Figure 3-96 and described in Table 3-106.

Return to Summary Table.

Interrupt Line Mask Register #1
RESET register domain: HWRST

Figure 3-96. INT1_MASK Register

7	6	5	4	3	2	1	0
RESERVED	VSYS_MON	HOTDIE	PWRDOWN	RESERVED	LONG_PRESS_KEY	PWRON	RESERVED
R/W-0h	R/W-X	R/W-X	R/W-X	R-0h	R/W-X	R/W-X	R-0h

Table 3-106. INT1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	VSYS_MON	R/W	X	VSYS_MON Line Mask bit register 0: VSYS_MON line is enabled. An interrupt is generated on INT line 1: VSYS_MON line is masked. No interrupt is generated on INT line
5	HOTDIE	R/W	X	HOTDIE Line Mask bit register 0: HOTDIE line is enabled. An interrupt is generated on INT line 1: HOTDIE line is masked. No interrupt is generated on INT line
4	PWRDOWN	R/W	X	PWRDOWN Line Mask bit register 0: PWRDOWN line is enabled. An interrupt is generated on INT line 1: PWRDOWN line is masked. No interrupt is generated on INT line
3	RESERVED	R	0h	
2	LONG_PRESS_KEY	R/W	X	LONG_PRESS_KEY Line Mask bit register 0: LONG_PRESS_KEY line is enabled. An interrupt is generated on INT line 1: LONG_PRESS_KEY line is masked. No interrupt is generated on INT line
1	PWRON	R/W	X	PWRON Line Mask bit register 0: PWRON line is enabled. An interrupt is generated on INT line 1: PWRON line is masked. No interrupt is generated on INT line
0	RESERVED	R	0h	

3.10.3 INT1_LINE_STATE Register (Address = 212h) [reset = 0h]

INT1_LINE_STATE is shown in Figure 3-97 and described in Table 3-107.

Return to Summary Table.

Interrupt source line state Register #1
RESET register domain: HWRST

Figure 3-97. INT1_LINE_STATE Register

7	6	5	4	3	2	1	0
RESERVED	VSYS_MON	HOTDIE	PWRDOWN	RESERVED	LONG_PRESS_KEY	PWRON	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-107. INT1_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	VSYS_MON	R	0h	VSYS_MON line state register 0: VSYS_MON line is equal to 0 1: VSYS_MON line is equal to 1
5	HOTDIE	R	0h	HOTDIE line state register 0: HOTDIE line is equal to 0 1: HOTDIE line is equal to 1
4	PWRDOWN	R	0h	PWRDOWN line state register 0: PWRDOWN line is equal to 0 1: PWRDOWN line is equal to 1
3	RESERVED	R	0h	
2	LONG_PRESS_KEY	R	0h	LONG_PRESS_KEY line state register 0: LONG_PRESS_KEY line is equal to 0 1: LONG_PRESS_KEY line is equal to 1
1	PWRON	R	0h	PWRON line state register 0: PWRON line is equal to 0 1: PWRON line is equal to 1
0	RESERVED	R	0h	

3.10.4 INT2_STATUS Register (Address = 215h) [reset = 0h]

INT2_STATUS is shown in Figure 3-98 and described in Table 3-108.

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Interrupt Status Register #2
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-98. INT2_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	SHORT	FSD	RESET_IN	RESERVED	WDT	OTP_ERROR	RESERVED
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

Table 3-108. INT2_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	RC	0h	
6	SHORT	RC	0h	SHORT status bit register associated (internal event) 0: no detection 1: Rising or falling edge are detected
5	FSD	RC	0h	First Supply Detection (FSD) status bit register (internal event) 0: no detection 1: Rising edge is detected To know the interrupt source (FSD First Supply Detection or BB battery bounce), you must read the PMU_SECONDARY_INT.
4	RESET_IN	RC	0h	RESET_IN status bit register associated to RESET_IN pin 0: no detection 1: Rising edge is detected
3	RESERVED	RC	0h	
2	WDT	RC	0h	WDT status bit register (internal event) 0: no detection 1: Rising edge is detected
1	OTP_ERROR	RC	0h	OTP_ERROR status bit register (internal event) 0: no detection 1: Rising edge is detected
0	RESERVED	RC	0h	

3.10.5 INT2_MASK Register (Address = 216h) [reset = X]

INT2_MASK is shown in Figure 3-99 and described in Table 3-109.

Return to Summary Table.

Interrupt Line Mask Register #2
RESET register domain: HWRST

Figure 3-99. INT2_MASK Register

7	6	5	4	3	2	1	0
RESERVED	SHORT	FSD	RESET_IN	RESERVED	WDT	OTP_ERROR	RESERVED
R-0h	R/W-X	R/W-X	R/W-X	R-0h	R/W-X	R/W-X	R/W-0h

Table 3-109. INT2_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SHORT	R/W	X	SHORT Line Mask bit register 0: SHORT line is enabled. An interrupt is generated on INT line 1: SHORT line is masked. No interrupt is generated on INT line
5	FSD	R/W	X	First Supply Detection (FSD) Line Mask bit register 0: FSD line is enabled. An interrupt is generated on INT line 1: FSD line is masked. No interrupt is generated on INT line
4	RESET_IN	R/W	X	RESET_IN Line Mask bit register 0: RESET_IN line is enabled. An interrupt is generated on INT line 1: RESET_IN line is masked. No interrupt is generated on INT line
3	RESERVED	R	0h	
2	WDT	R/W	X	WDT (Watchdog) Line Mask bit register 0: WDT (Watchdog) line is enabled. An interrupt is generated on INT line 1: WDT (Watchdog) line is masked. No interrupt is generated on INT line
1	OTP_ERROR	R/W	X	OTP_ERROR Line Mask bit register 0: OTP_ERROR line is enabled. An interrupt is generated on INT line 1: OTP_ERROR line is masked. No interrupt is generated on INT line
0	RESERVED	R/W	0h	

3.10.6 INT2_LINE_STATE Register (Address = 217h) [reset = 0h]

INT2_LINE_STATE is shown in Figure 3-100 and described in Table 3-110.

Return to Summary Table.

Interrupt source line state Register #2
RESET register domain: HWRST

Figure 3-100. INT2_LINE_STATE Register

7	6	5	4	3	2	1	0
RESERVED	SHORT	FSD	RESET_IN	RESERVED	WDT	OTP_ERROR	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-110. INT2_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SHORT	R	0h	SHORT line state register 0: SHORT line is equal to 0 1: SHORT line is equal to 1
5	FSD	R	0h	First Supply Detection (FSD) line state register 0: FSD line is equal to 0 1: FSD line is equal to 1
4	RESET_IN	R	0h	RESET_IN line state register 0: RESET_IN line is equal to 0 1: RESET_IN line is equal to 1
3	RESERVED	R	0h	BATREMOVAL line state register 0: BATREMOVAL line is equal to 0 1: BATREMOVAL line is equal to 1
2	WDT	R	0h	WDT line state register 0: WDT line is equal to 0 1: WDT line is equal to 1
1	OTP_ERROR	R	0h	OTP_ERROR line state register 0: OTP_ERROR line is equal to 0 1: OTP_ERROR line is equal to 1
0	RESERVED	R	0h	

3.10.7 INT3_STATUS Register (Address = 21Ah) [reset = 0h]

INT3_STATUS is shown in Figure 3-101 and described in Table 3-111.

Return to Summary Table.

Interrupt Status Register #3
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-101. INT3_STATUS Register

7	6	5	4	3	2	1	0
VBUS	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

Table 3-111. INT3_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS	RC	0h	VBUS status bit register (VBUS pin) 0: no detection 1: Rising or falling edge are detected
6	RESERVED	RC	0h	
5	RESERVED	RC	0h	
4	RESERVED	RC	0h	
3	RESERVED	RC	0h	
2	GPADC_EOC_SW	RC	0h	GPADC_EOC_SW status bit register associated (internal event) 0: no detection 1: Rising or falling edge are detected
1	GPADC_AUTO_1	RC	0h	GPADC_AUTO_1 status bit register (internal event) 0: no detection 1: Rising edge is detected
0	GPADC_AUTO_0	RC	0h	GPADC_AUTO_0 status bit register (Internal event) 0: no detection 1: Rising edge is detected

3.10.8 INT3_MASK Register (Address = 21Bh) [reset = X]

INT3_MASK is shown in Figure 3-102 and described in Table 3-112.

Return to Summary Table.

Interrupt Line Mask Register #3
RESET register domain: HWRST

Figure 3-102. INT3_MASK Register

7	6	5	4	3	2	1	0
VBUS	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0
R/W-X	R-0h	R-0h	R-0h	R-0h	R/W-X	R/W-X	R/W-X

Table 3-112. INT3_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS	R/W	X	VBUS Line Mask bit register (VBUS pin) 0: VBUS line is enabled. An interrupt is generated on INT line 1: VBUS line is masked. No interrupt is generated on INT line
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	GPADC_EOC_SW	R/W	X	GPADC_EOC_SW Line Mask bit register (Internal event) 0: GPADC_EOC_SW line is enabled. An interrupt is generated on INT line 1: GPADC_EOC_SW line is masked. No interrupt is generated on INT line
1	GPADC_AUTO_1	R/W	X	GPADC_AUTO_1 Line Mask bit register (Internal event) 0: GPADC_AUTO_1 line is enabled. An interrupt is generated on INT line 1: GPADC_AUTO_1 line is masked. No interrupt is generated on INT line
0	GPADC_AUTO_0	R/W	X	GPADC_AUTO_0 Line Mask bit register (Internal event) 0: GPADC_AUTO_0 line is enabled. An interrupt is generated on INT line 1: GPADC_AUTO_0 line is masked. No interrupt is generated on INT line

3.10.9 INT3_LINE_STATE Register (Address = 21Ch) [reset = 0h]

INT3_LINE_STATE is shown in Figure 3-103 and described in Table 3-113.

Return to Summary Table.

Interrupt source line state Register #3
RESET register domain: HWRST

Figure 3-103. INT3_LINE_STATE Register

7	6	5	4	3	2	1	0
VBUS	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_EOC_SW	GPADC_AUTO_1	GPADC_AUTO_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-113. INT3_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBUS	R	0h	VBUS line state register (VBUS pin) 0: VBUS line is equal to 0 1: VBUS line is equal to 1
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	GPADC_EOC_SW	R	0h	GPADC_EOC_SW line state register (Internal event) 0: GPADC_EOC_SW line is equal to 0 1: GPADC_EOC_SW line is equal to 1
1	GPADC_AUTO_1	R	0h	GPADC_AUTO_1 line state register (internal event) 0: GPADC_AUTO_1 line is equal to 0 1: GPADC_AUTO_1 line is equal to 1
0	GPADC_AUTO_0	R	0h	GPADC_AUTO_0 line state register (Internal event) 0: GPADC_AUTO_0 line is equal to 0 1: GPADC_AUTO_0 line is equal to 1

3.10.10 INT4_STATUS Register (Address = 21Fh) [reset = 0h]

INT4_STATUS is shown in Figure 3-104 and described in Table 3-114.

Return to Summary Table.

Interrupt Status Register #4
The bit can be cleared on read or cleared by writing 1(see INT_CTRL.INT_CLEAR)
RESET register domain: HWRST

Figure 3-104. INT4_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h

Table 3-114. INT4_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	RC	0h	
6	GPIO_6	RC	0h	GPIO_6 status bit register associated to GPIO_6 pin 0: no detection 1: Rising or Falling edge are detected
5	GPIO_5	RC	0h	GPIO_5 status bit register associated to GPIO_5 pin 0: no detection 1: Rising or Falling edge are detected
4	GPIO_4	RC	0h	GPIO_4 status bit register associated to GPIO_4 pin 0: no detection 1: Rising or Falling edge are detected
3	GPIO_3	RC	0h	GPIO_3 status bit register associated to GPIO_3 pin 0: no detection 1: Rising or Falling edge are detected
2	GPIO_2	RC	0h	GPIO_2 status bit register associated to GPIO_2 pin 0: no detection 1: Rising or Falling edge are detected
1	GPIO_1	RC	0h	GPIO_1 status bit register associated to GPIO_1 pin 0: no detection 1: Rising or Falling edge are detected
0	GPIO_0	RC	0h	GPIO_0 status bit register associated to GPIO_0 pin 0: no detection 1: Rising or Falling edge are detected

3.10.11 INT4_MASK Register (Address = 220h) [reset = X]

INT4_MASK is shown in Figure 3-105 and described in Table 3-115.

Return to Summary Table.

Interrupt Line Mask Register #4
RESET register domain: HWRST

Figure 3-105. INT4_MASK Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R-0h	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X

Table 3-115. INT4_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6	R/W	X	GPIO_6 Line Mask bit register 0: GPIO_6 line is enabled. An interrupt is generated on INT line 1: GPIO_6 line is masked. No interrupt is generated on INT line
5	GPIO_5	R/W	X	GPIO_5 Line Mask bit register 0: GPIO_5 line is enabled. An interrupt is generated on INT line 1: GPIO_5 line is masked. No interrupt is generated on INT line
4	GPIO_4	R/W	X	GPIO_4 Line Mask bit register 0: GPIO_4 line is enabled. An interrupt is generated on INT line 1: GPIO_4 line is masked. No interrupt is generated on INT line Note: Cannot be used as wake-up event because buffer needs power supply. So must be masked by default (OTP).
3	GPIO_3	R/W	X	GPIO_3 Line Mask bit register 0: GPIO_3 line is enabled. An interrupt is generated on INT line 1: GPIO_3 line is masked. No interrupt is generated on INT line
2	GPIO_2	R/W	X	GPIO_2 Line Mask bit register 0: GPIO_2 line is enabled. An interrupt is generated on INT line 1: GPIO_2 line is masked. No interrupt is generated on INT line
1	GPIO_1	R/W	X	GPIO_1 Line Mask bit register 0: GPIO_1 line is enabled. An interrupt is generated on INT line 1: GPIO_1 line is masked. No interrupt is generated on INT line
0	GPIO_0	R/W	X	GPIO_0 Line Mask bit register 0: GPIO_0 line is enabled. An interrupt is generated on INT line 1: GPIO_0 line is masked. No interrupt is generated on INT line

3.10.12 INT4_LINE_STATE Register (Address = 221h) [reset = 0h]

INT4_LINE_STATE is shown in Figure 3-106 and described in Table 3-116.

Return to Summary Table.

Interrupt source line state Register #4
RESET register domain: HWRST

Figure 3-106. INT4_LINE_STATE Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-116. INT4_LINE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6	R	0h	GPIO_6 line state register 0: GPIO_6 line is equal to 0 1: GPIO_6 line is equal to 1
5	GPIO_5	R	0h	GPIO_5 line state register 0: GPIO_5 line is equal to 0 1: GPIO_5 line is equal to 1
4	GPIO_4	R	0h	GPIO_4 line state register 0: GPIO_4 line is equal to 0 1: GPIO_4 line is equal to 1
3	GPIO_3	R	0h	GPIO_3 line state register 0: GPIO_3 line is equal to 0 1: GPIO_3 line is equal to 1
2	GPIO_2	R	0h	GPIO_2 line state register 0: GPIO_2 line is equal to 0 1: GPIO_2 line is equal to 1
1	GPIO_1	R	0h	GPIO_1 line state register 0: GPIO_1 line is equal to 0 1: GPIO_1 line is equal to 1
0	GPIO_0	R	0h	GPIO_0 line state register 0: GPIO_0 line is equal to 0 1: GPIO_0 line is equal to 1

3.10.13 INT4_EDGE_DETECT1 Register (Address = 222h) [reset = FFh]

INT4_EDGE_DETECT1 is shown in Figure 3-107 and described in Table 3-117.

Return to Summary Table.

Interrupt Edge Detection Register #4.1
RESET register domain: HWRST

Figure 3-107. INT4_EDGE_DETECT1 Register

7	6	5	4	3	2	1	0
GPIO_3_RISING	GPIO_3_FALLING	GPIO_2_RISING	GPIO_2_FALLING	GPIO_1_RISING	GPIO_1_FALLING	GPIO_0_RISING	GPIO_0_FALLING
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-117. INT4_EDGE_DETECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_3_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
6	GPIO_3_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
5	GPIO_2_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
4	GPIO_2_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
3	GPIO_1_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
2	GPIO_1_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
1	GPIO_0_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
0	GPIO_0_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)

3.10.14 INT4_EDGE_DETECT2 Register (Address = 223h) [reset = 3Fh]

INT4_EDGE_DETECT2 is shown in Figure 3-108 and described in Table 3-118.

Return to Summary Table.

Interrupt Edge Detection Register #4.2
RESET register domain: HWRST

Figure 3-108. INT4_EDGE_DETECT2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO_6_RISING	GPIO_6_FALLING	GPIO_5_RISING	GPIO_5_FALLING	GPIO_4_RISING	GPIO_4_FALLING
R-0h	R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 3-118. INT4_EDGE_DETECT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	GPIO_6_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
4	GPIO_6_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
3	GPIO_5_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
2	GPIO_5_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)
1	GPIO_4_RISING	R/W	1h	0: Rising edge detection not enabled 1: Rising edge detection enable (default)
0	GPIO_4_FALLING	R/W	1h	0: Falling edge detection not enabled 1: Falling edge detection enable (default)

3.10.15 INT_CTRL Register (Address = 224h) [reset = 0h]

INT_CTRL is shown in Figure 3-109 and described in Table 3-119.

Return to Summary Table.

Interrupt control register
RESET register domain: HWRST

Figure 3-109. INT_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					INT_PENDING	RESERVED	INT_CLEAR
R-0h					R/W-0h	R-0h	R/W-0h

Table 3-119. INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2	INT_PENDING	R/W	0h	Pending interrupt latching feature selection (interrupt latched in case of new event before clearing on same line) 0: Enabled (default) 1: Not enabled
1	RESERVED	R	0h	
0	INT_CLEAR	R/W	0h	Select the way to clear the interrupt bits (will be apply to ALL the bits) 0: Clear-on-Write - Interrupts cleared by writing 1. This method is bit based (default) 1: Clear-on-Read - Interrupts cleared on read

3.10.16 OTP_CRC_RESULTS Register (Address = 225h) [reset = 0h]

OTP_CRC_RESULTS is shown in Figure 3-110 and described in Table 3-120.

Return to Summary Table.

OTP CRC Checker reuslt register
RESET register domain: HWRST

Figure 3-110. OTP_CRC_RESULTS Register

7	6	5	4	3	2	1	0
RESERVED				CRC_FORCE_OFF	CRC_RESULTS_CFG	CRC_RESULTS_SEQ	CRC_RESULTS_TRIM
R-0h				R-0h	R-0h	R-0h	R-0h

Table 3-120. OTP_CRC_RESULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	CRC_FORCE_OFF	R	0h	0 : Power Sequence is executed through the end after OTP CRC Check 1 : Power Sequence is forced off after OTP CRC Check
2	CRC_RESULTS_CFG	R	0h	CRC result from Configuration data OTP registers: 0: Good 1: Error
1	CRC_RESULTS_SEQ	R	0h	CRC result from Power Sequence OTP registers: 0: Good 1: Error
0	CRC_RESULTS_TRIM	R	0h	CRC result from Trim data OTP registers: 0: Good 1: Error

3.11 FUNC_ID Registers

Table 3-121 lists the memory-mapped registers for the FUNC_ID. All register offset addresses not listed in Table 3-121 should be considered as reserved locations and the register contents should not be modified.

Table 3-121. FUNC_ID Registers

Address	Acronym	Register Name	Section
24Fh	VENDOR_ID_LSB	Vendor ID Register (LSB) RESET register domain: HWRST	Section 3.11.1
250h	VENDOR_ID_MSB	Vendor ID Register (MSB) RESET register domain: HWRST	Section 3.11.2
251h	PRODUCT_ID_LSB	Product ID Register (LSB) RESET register domain: HWRST	Section 3.11.3
252h	PRODUCT_ID_MSB	Product ID Register (MSB) RESET register domain: HWRST	Section 3.11.4

3.11.1 VENDOR_ID_LSB Register (Address = 24Fh) [reset = 51h]

VENDOR_ID_LSB is shown in Figure 3-111 and described in Table 3-122.

Return to Summary Table.

Vendor ID Register (LSB)
RESET register domain: HWRST

Figure 3-111. VENDOR_ID_LSB Register

7	6	5	4	3	2	1	0
VENDOR_ID							
R-51h							

Table 3-122. VENDOR_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDOR_ID	R	51h	Texas Instruments USB Vendor ID (8 LSBs) - Default value: 0x51

3.11.2 VENDOR_ID_MSB Register (Address = 250h) [reset = 4h]

VENDOR_ID_MSB is shown in Figure 3-112 and described in Table 3-123.

Return to Summary Table.

Vendor ID Register (MSB)
RESET register domain: HWRST

Figure 3-112. VENDOR_ID_MSB Register

7	6	5	4	3	2	1	0
VENDOR_ID							
R-4h							

Table 3-123. VENDOR_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VENDOR_ID	R	4h	Texas Instruments USB Vendor ID (8 MSBs) - Default value: 0x04

3.11.3 PRODUCT_ID_LSB Register (Address = 251h) [reset = 17h]

PRODUCT_ID_LSB is shown in Figure 3-113 and described in Table 3-124.

Return to Summary Table.

Product ID Register (LSB)
RESET register domain: HWRST

Figure 3-113. PRODUCT_ID_LSB Register

7	6	5	4	3	2	1	0
PRODUCT_ID							
R-17h							

Table 3-124. PRODUCT_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODUCT_ID	R	17h	Texas Instruments Product ID (8 LSBs) - Default value: 0x35

3.11.4 PRODUCT_ID_MSB Register (Address = 252h) [reset = 9h]

PRODUCT_ID_MSB is shown in Figure 3-114 and described in Table 3-125.

Return to Summary Table.

Product ID Register (MSB)
RESET register domain: HWRST

Figure 3-114. PRODUCT_ID_MSB Register

7	6	5	4	3	2	1	0
PRODUCT_ID							
R-9h							

Table 3-125. PRODUCT_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODUCT_ID	R	9h	Texas Instruments Product ID (8 MSBs) - Default value: 0xC0

3.12 FUNC_GPIO Registers

Table 3-126 lists the memory-mapped registers for the FUNC_GPIO. All register offset addresses not listed in Table 3-126 should be considered as reserved locations and the register contents should not be modified.

Table 3-126. FUNC_GPIO Registers

Address	Acronym	Register Name	Section
280h	GPIO_DATA_IN	GPIO Data input register #1 RESET register domain: HWRST	Section 3.12.1
281h	GPIO_DATA_DIR	GPIO data direction #1 RESET register domain: HWRST	Section 3.12.2
282h	GPIO_DATA_OUT	GPIO Data output register #1 RESET register domain: HWRST	Section 3.12.3
283h	GPIO_DEBOUNCE_EN	GPIO Debounce enable register #1 RESET register domain: HWRST	Section 3.12.4
284h	GPIO_CLEAR_DATA_OUT	GPIO Clear Data Out Register #1 RESET register domain: HWRST	Section 3.12.5
285h	GPIO_SET_DATA_OUT	GPIO Set Data Out Register #1 RESET register domain: HWRST	Section 3.12.6
286h	PU_PD_GPIO_CTRL1	Pull-up Pull-down control register #1 RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)	Section 3.12.7
287h	PU_PD_GPIO_CTRL2	Pull-up Pull-down control register #2 RESET register domain: HWRST Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)	Section 3.12.8
288h	OD_OUTPUT_GPIO_CTRL	Open Drain control register #1 RESET register domain: HWRST Note: It is user responsibility to take care about the GPIO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections	Section 3.12.9

3.12.1 GPIO_DATA_IN Register (Address = 280h) [reset = 0h]

GPIO_DATA_IN is shown in Figure 3-115 and described in Table 3-127.

Return to Summary Table.

GPIO Data input register #1
RESET register domain: HWRST

Figure 3-115. GPIO_DATA_IN Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6_IN	GPIO_5_IN	GPIO_4_IN	GPIO_3_IN	GPIO_2_IN	GPIO_1_IN	GPIO_0_IN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 3-127. GPIO_DATA_IN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6_IN	R	0h	Data read value (in) of the GPIO_6
5	GPIO_5_IN	R	0h	Data read value (in) of the GPIO_5
4	GPIO_4_IN	R	0h	Data read value (in) of the GPIO_4
3	GPIO_3_IN	R	0h	Data read value (in) of the GPIO_3
2	GPIO_2_IN	R	0h	Data read value (in) of the GPIO_2
1	GPIO_1_IN	R	0h	Data read value (in) of the GPIO_1
0	GPIO_0_IN	R	0h	Data read value (in) of the GPIO_0

3.12.2 GPIO_DATA_DIR Register (Address = 281h) [reset = 0h]

GPIO_DATA_DIR is shown in Figure 3-116 and described in Table 3-128.

Return to Summary Table.

GPIO data direction #1
RESET register domain: HWRST

Figure 3-116. GPIO_DATA_DIR Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6_DIR	GPIO_5_DIR	GPIO_4_DIR	GPIO_3_DIR	GPIO_2_DIR	GPIO_1_DIR	GPIO_0_DIR
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-128. GPIO_DATA_DIR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
5	GPIO_5_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
4	GPIO_4_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
3	GPIO_3_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
2	GPIO_2_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
1	GPIO_1_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration
0	GPIO_0_DIR	R/W	0h	0: buffer in input configuration (default) 1: buffer in output configuration

3.12.3 GPIO_DATA_OUT Register (Address = 282h) [reset = 0h]

GPIO_DATA_OUT is shown in Figure 3-117 and described in Table 3-129.

Return to Summary Table.

GPIO Data output register #1
RESET register domain: HWRST

Figure 3-117. GPIO_DATA_OUT Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6_OUT	GPIO_5_OUT	GPIO_4_OUT	GPIO_3_OUT	GPIO_2_OUT	GPIO_1_OUT	GPIO_0_OUT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-129. GPIO_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6_OUT	R/W	0h	Data write value (out) of the GPIO_6
5	GPIO_5_OUT	R/W	0h	Data write value (out) of the GPIO_5
4	GPIO_4_OUT	R/W	0h	Data write value (out) of the GPIO_4
3	GPIO_3_OUT	R/W	0h	Data write value (out) of the GPIO_3
2	GPIO_2_OUT	R/W	0h	Data write value (out) of the GPIO_2
1	GPIO_1_OUT	R/W	0h	Data write value (out) of the GPIO_1
0	GPIO_0_OUT	R/W	0h	Data write value (out) of the GPIO_0

3.12.4 GPIO_DEBOUNCE_EN Register (Address = 283h) [reset = 0h]

GPIO_DEBOUNCE_EN is shown in Figure 3-118 and described in Table 3-130.

Return to Summary Table.

GPIO Debounce enable register #1
RESET register domain: HWRST

Figure 3-118. GPIO_DEBOUNCE_EN Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6_DEBOUNCE_EN	GPIO_5_DEBOUNCE_EN	GPIO_4_DEBOUNCE_EN	GPIO_3_DEBOUNCE_EN	GPIO_2_DEBOUNCE_EN	GPIO_1_DEBOUNCE_EN	GPIO_0_DEBOUNCE_EN
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 3-130. GPIO_DEBOUNCE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
5	GPIO_5_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
4	GPIO_4_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
3	GPIO_3_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
2	GPIO_2_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
1	GPIO_1_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled
0	GPIO_0_DEBOUNCE_EN	R/W	0h	0: No debounce (default) 1: Debounce enabled

3.12.5 GPIO_CLEAR_DATA_OUT Register (Address = 284h) [reset = 0h]

GPIO_CLEAR_DATA_OUT is shown in Figure 3-119 and described in Table 3-131.

Return to Summary Table.

GPIO Clear Data Out Register #1
RESET register domain: HWRST

Figure 3-119. GPIO_CLEAR_DATA_OUT Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6_CLEAR_DATA_OUT	GPIO_5_CLEAR_DATA_OUT	GPIO_4_CLEAR_DATA_OUT	GPIO_3_CLEAR_DATA_OUT	GPIO_2_CLEAR_DATA_OUT	GPIO_1_CLEAR_DATA_OUT	GPIO_0_CLEAR_DATA_OUT
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-131. GPIO_CLEAR_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_6 bit 1: CLEAR GPIO_6 bit
5	GPIO_5_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_5 bit 1: CLEAR GPIO_5 bit
4	GPIO_4_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_4 bit 1: CLEAR GPIO_4 bit
3	GPIO_3_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_3 bit 1: CLEAR GPIO_3 bit
2	GPIO_2_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_2 bit 1: CLEAR GPIO_2 bit
1	GPIO_1_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_1 bit 1: CLEAR GPIO_1 bit
0	GPIO_0_CLEAR_DATA_OUT	W	0h	0: no action on GPIO_0 bit 1: CLEAR GPIO_0 bit

3.12.6 GPIO_SET_DATA_OUT Register (Address = 285h) [reset = 0h]

GPIO_SET_DATA_OUT is shown in Figure 3-120 and described in Table 3-132.

Return to Summary Table.

GPIO Set Data Out Register #1
RESET register domain: HWRST

Figure 3-120. GPIO_SET_DATA_OUT Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_6_SET_DATA_OUT	GPIO_5_SET_DATA_OUT	GPIO_4_SET_DATA_OUT	GPIO_3_SET_DATA_OUT	GPIO_2_SET_DATA_OUT	GPIO_1_SET_DATA_OUT	GPIO_0_SET_DATA_OUT
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 3-132. GPIO_SET_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_6_SET_DATA_OUT	W	0h	0: no action on GPIO_6 bit 1: SET GPIO_6 bit
5	GPIO_5_SET_DATA_OUT	W	0h	0: no action on GPIO_5 bit 1: SET GPIO_5 bit
4	GPIO_4_SET_DATA_OUT	W	0h	0: no action on GPIO_4 bit 1: SET GPIO_4 bit
3	GPIO_3_SET_DATA_OUT	W	0h	0: no action on GPIO_3 bit 1: SET GPIO_3 bit
2	GPIO_2_SET_DATA_OUT	W	0h	0: no action on GPIO_2 bit 1: SET GPIO_2 bit
1	GPIO_1_SET_DATA_OUT	W	0h	0: no action on GPIO_1 bit 1: SET GPIO_1 bit
0	GPIO_0_SET_DATA_OUT	W	0h	0: no action on GPIO_0 bit 1: SET GPIO_0 bit

3.12.7 PU_PD_GPIO_CTRL1 Register (Address = 286h) [reset = X]

PU_PD_GPIO_CTRL1 is shown in Figure 3-121 and described in Table 3-133.

Return to Summary Table.

Pull-up Pull-down control register #1
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)

Figure 3-121. PU_PD_GPIO_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	GPIO_3_PD	GPIO_2_PU	GPIO_2_PD	RESERVED	GPIO_1_PD	RESERVED	GPIO_0_PD
R-0h	R/W-X	R/W-X	R/W-X	R-0h	R/W-X	R-0h	R/W-X

Table 3-133. PU_PD_GPIO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	GPIO_3_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)
5	GPIO_2_PU	R/W	X	0: Pull-up not enabled (default) 1: Pull-up enabled
4	GPIO_2_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)
3	RESERVED	R	0h	
2	GPIO_1_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)
1	RESERVED	R	0h	
0	GPIO_0_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)

3.12.8 PU_PD_GPIO_CTRL2 Register (Address = 287h) [reset = X]

PU_PD_GPIO_CTRL2 is shown in Figure 3-122 and described in Table 3-134.

Return to Summary Table.

Pull-up Pull-down control register #2
RESET register domain: HWRST
Note: It is user responsibility to take care about the pull-up/pull-down selections versus the GPIO direction and type (Open drain / Push-Pull)

Figure 3-122. PU_PD_GPIO_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPIO_6_PD	RESERVED	GPIO_5_PD	GPIO_4_PU	GPIO_4_PD
R-0h	R-0h	R-0h	R/W-X	R-0h	R/W-X	R/W-X	R/W-X

Table 3-134. PU_PD_GPIO_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	GPIO_6_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)
3	RESERVED	R	0h	
2	GPIO_5_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)
1	GPIO_4_PU	R/W	X	0: Pull-up not enabled (default) 1: Pull-up enabled
0	GPIO_4_PD	R/W	X	0: Pull-down not enabled 1: Pull-down enabled (default)

3.12.9 OD_OUTPUT_GPIO_CTRL Register (Address = 288h) [reset = X]

OD_OUTPUT_GPIO_CTRL is shown in Figure 3-123 and described in Table 3-135.

Return to Summary Table.

Open Drain control register #1
RESET register domain: HWRST
Note: It is user responsibility to take care about the GPIO direction and type (Open drain / Push-Pull) versus the pull-up/pull-down selections

Figure 3-123. OD_OUTPUT_GPIO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPIO_4_OD	RESERVED	GPIO_2_OD	RESERVED	RESERVED
R-0h	R-0h	R-0h	R/W-X	R-0h	R/W-X	R-0h	R-0h

Table 3-135. OD_OUTPUT_GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	GPIO_4_OD	R/W	X	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
3	RESERVED	R	0h	
2	GPIO_2_OD	R/W	X	0: open drain not enable (Push-Pull enabled) (default) 1: open drain enable (Push-Pull not enable)
1	RESERVED	R	0h	
0	RESERVED	R	0h	

3.13 FUNC_GPADC Registers

Table 3-136 lists the memory-mapped registers for the FUNC_GPADC. All register offset addresses not listed in Table 3-136 should be considered as reserved locations and the register contents should not be modified.

Table 3-136. FUNC_GPADC Registers

Address	Acronym	Register Name	Section
2C0h	GPADC_CTRL1	GPADC Control Register RESET register domain: HWRST	Section 3.13.1
2C2h	GPADC_FLUSH	GPADC FLUSH register RESET register domain: HWRST	Section 3.13.2
2C3h	GPADC_AUTO_CTRL	GPADC Automatic Control register (Periodic) RESET register domain: HWRST	Section 3.13.3
2C4h	GPADC_STATUS	GPADC Status Register RESET register domain: HWRST	Section 3.13.4
2C5h	GPADC_FLUSH_EN	GPADC FLSUH Enable register RESET register domain: HWRST	Section 3.13.5
2C7h	GPADC_STUCK	GPADC stuck status RESET register domain: HWRST	Section 3.13.6
2C8h	GPADC_AUTO_SELECT	GPADC Automatic (Periodic) Channel selection for Conversion 0 and Conversion 1 RESET register domain: HWRST Note: All Selected channels are queued and converted from channel 0 to 11 The first (lower) converted channel results is placed in GPADC_AUTO_CONV0 register and the second one is placed in GPADC_AUTO_CONV0 register. It is why it is recommended to put the lower channel to convert in AUTO_CONV0_SEL and the higher channel to convert in AUTO_CONV0_SEL.	Section 3.13.7
2C9h	GPADC_AUTO_CONV0_LSB	GPADC data results of the Automatic (Periodic) conversion 0 (LSB) RESET register domain: HWRST	Section 3.13.8
2CAh	GPADC_AUTO_CONV0_MSB	GPADC data results of the Automatic (Periodic) conversion 0 (MSB) RESET register domain: HWRST	Section 3.13.9
2CBh	GPADC_AUTO_CONV1_LSB	GPADC data results of the Automatic (Periodic) conversion 1 (LSB) RESET register domain: HWRST	Section 3.13.10
2CCh	GPADC_AUTO_CONV1_MSB	GPADC data results of the Automatic (Periodic) conversion 1 (MSB) RESET register domain: HWRST	Section 3.13.11
2CDh	GPADC_SW_SELECT	GPADC Software Channel selection for Conversion 0 RESET register domain: HWRST	Section 3.13.12
2CEh	GPADC_SW_CONV0_LSB	GPADC data results of the Software conversion 0 (LSB) RESET register domain: HWRST	Section 3.13.13
2CFh	GPADC_SW_CONV0_MSB	GPADC data results of the Software conversion 0 (MSB) RESET register domain: HWRST	Section 3.13.14
2D0h	GPADC_THRES_CONV0_LSB	LSB of Threshold reference to be compared to the Conversion 0 results RESET register domain: HWRST	Section 3.13.15
2D1h	GPADC_THRES_CONV0_MSB	MSB of Threshold reference to be compared to the Conversion 0 results RESET register domain: HWRST	Section 3.13.16
2D2h	GPADC_THRES_CONV1_LSB	LSB of Threshold reference to be compared to the Conversion 1 results RESET register domain: HWRST	Section 3.13.17
2D3h	GPADC_THRES_CONV1_MSB	MSB of Threshold reference to be compared to the Conversion 1 results RESET register domain: HWRST	Section 3.13.18

Table 3-136. FUNC_GPADC Registers (continued)

Address	Acronym	Register Name	Section
2D4h	GPADC_SMPS_ILMONITOR_EN	GPADC SMPS selection for current measurement RESET register domain: HWRST	Section 3.13.19
2D5h	GPADC_SMPS_VSEL_MONITORING	GPADC SMPS voltage monitoring related to ILMONITORING measurement RESET register domain: HWRST	Section 3.13.20

3.13.1 GPADC_CTRL1 Register (Address = 2C0h) [reset = 0h]

GPADC_CTRL1 is shown in Figure 3-124 and described in Table 3-137.

Return to Summary Table.

GPADC Control Register
RESET register domain: HWRST

Figure 3-124. GPADC_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED		RESERVED		RESERVED	GPADC_FORCE
R-0h	R-0h	R-0h		R-0h		R-0h	R/W-0h

Table 3-137. GPADC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5-4	RESERVED	R	0h	
3-2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	GPADC_FORCE	R/W	0h	Force GPADC module to active (Always On) 0: GPADC OFF. The GPADC is controlled by conversion request in all modes (default) 1: GPADC ON (Always ON - will allow conversion latency)

3.13.2 GPADC_FLUSH Register (Address = 2C2h) [reset = 0h]

GPADC_FLUSH is shown in Figure 3-125 and described in Table 3-138.

Return to Summary Table.

GPADC FLUSH register
RESET register domain: HWRST

Figure 3-125. GPADC_FLUSH Register

7	6	5	4	3	2	1	0
RESERVED						EXTEND_DELAY	FLUSH
R-0h						R/W-0h	R/W-0h

Table 3-138. GPADC_FLUSH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	EXTEND_DELAY	R/W	0h	Extend delay before SW conversion. 0: 0 µs (default) 1: 450 µs
0	FLUSH	R/W	0h	Flush the conversion result of the GPADC when it is stuck in a busy state. This bit can be toggled to 1 and back to 0 to recover the GPADC operation.

3.13.3 GPADC_AUTO_CTRL Register (Address = 2C3h) [reset = 0h]

GPADC_AUTO_CTRL is shown in Figure 3-126 and described in Table 3-139.

Return to Summary Table.

GPADC Automatic Control register (Periodic)
RESET register domain: HWRST

Figure 3-126. GPADC_AUTO_CTRL Register

7	6	5	4	3	2	1	0
SHUTDOWN_CONV1	SHUTDOWN_CONV0	AUTO_CONV1_EN	AUTO_CONV0_EN	COUNTER_CONV			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 3-139. GPADC_AUTO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SHUTDOWN_CONV1	R/W	0h	Shut down control based on Auto conversions (only for CONV1) 0: shut down not enabled (default) 1: enable shut down of the platform if interrupt is not clear within delay time
6	SHUTDOWN_CONV0	R/W	0h	Shut down control based on Auto conversions (only for CONV0) 0: shut down not enabled (default) 1: enable shut down of the platform if interrupt is not clear within delay time
5	AUTO_CONV1_EN	R/W	0h	Automatic Conversion 1 enabling 0: Automatic Conversion 1 is not enable (defaults) 1: Automatic Conversion 1 is enabled
4	AUTO_CONV0_EN	R/W	0h	Automatic Conversion 0 enabling 0: Automatic Conversion 0 is not enable (defaults) 1: Automatic Conversion 0 is enabled
3-0	COUNTER_CONV	R/W	0h	Time slot between conversions (RT and SW modes) or two consecutive conversions (Auto mode) 0000: 1/32s (default) 0001: 1/16s 0010: 1/8s 1110: 512s 1111: 1024s

3.13.4 GPADC_STATUS Register (Address = 2C4h) [reset = 10h]

GPADC_STATUS is shown in Figure 3-127 and described in Table 3-140.

Return to Summary Table.

GPADC Status Register
RESET register domain: HWRST

Figure 3-127. GPADC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			GPADC_AVAILABLE	RESERVED			
R-0h			R-1h	R-0h			

Table 3-140. GPADC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	GPADC_AVAILABLE	R	1h	GPADC availability status 0: Conversions not completed. GPADC not available (busy) 1: Conversions completed. GPADC available
3-0	RESERVED	R	0h	

3.13.5 GPADC_FLUSH_EN Register (Address = 2C5h) [reset = 0h]

GPADC_FLUSH_EN is shown in Figure 3-128 and described in Table 3-141.

Return to Summary Table.

GPADC FLSUH Enable register
RESET register domain: HWRST

Figure 3-128. GPADC_FLUSH_EN Register

7	6	5	4	3	2	1	0
FLUSH_EN	RESERVED			RESERVED			
R/W-0h	R-0h			R/W-0h			

Table 3-141. GPADC_FLUSH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLUSH_EN	R/W	0h	GPADC Flush Enable 0: The Flush operation of GPADC is locked (default) 1: The Flush operation of GPADC is enabled
6-4	RESERVED	R	0h	
3-0	RESERVED	R/W	0h	

3.13.6 GPADC_STUCK Register (Address = 2C7h) [reset = 0h]

GPADC_STUCK is shown in Figure 3-129 and described in Table 3-142.

Return to Summary Table.

GPADC stuck status
RESET register domain: HWRST

Figure 3-129. GPADC_STUCK Register

7	6	5	4	3	2	1	0
RESERVED			STUCK	RESERVED			
R-0h			R-0h	R-0h			

Table 3-142. GPADC_STUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	STUCK	R	0h	GPADC stuck status 0: GPADC is not stuck in a busy state 1: GPADC is stuck in a busy state. Flushing the GPADC is necessary to return it to normal operation
3-0	RESERVED	R	0h	

3.13.7 GPADC_AUTO_SELECT Register (Address = 2C8h) [reset = 0h]

GPADC_AUTO_SELECT is shown in Figure 3-130 and described in Table 3-143.

Return to Summary Table.

GPADC Automatic (Periodic) Channel selection for Conversion 0 and Conversion 1
RESET register domain: HWRST
Note: All Selected channels are queued and converted from channel 0 to 11
The first (lower) converted channel results is placed in GPADC_AUTO_CONV0 register and the second one is placed in GPADC_AUTO_CONV0 register. It is why it is recommended to put the lower channel to convert in AUTO_CONV0_SEL and the higher channel to convert in AUTO_CONV0_SEL.

Figure 3-130. GPADC_AUTO_SELECT Register

7	6	5	4	3	2	1	0
AUTO_CONV1_SEL				AUTO_CONV0_SEL			
R/W-0h				R/W-0h			

Table 3-143. GPADC_AUTO_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	AUTO_CONV1_SEL	R/W	0h	Channel selection for Conversion 1 in Automatic mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 0110: GPADC Channel 6 0111: GPADC Channel 7 others: Reserved
3-0	AUTO_CONV0_SEL	R/W	0h	Channel selection for Conversion 0 in Automatic mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 0110: GPADC Channel 6 0111: GPADC Channel 7 others: Reserved

3.13.8 GPADC_AUTO_CONV0_LSB Register (Address = 2C9h) [reset = 0h]

GPADC_AUTO_CONV0_LSB is shown in Figure 3-131 and described in Table 3-144.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 0 (LSB)
RESET register domain: HWRST

Figure 3-131. GPADC_AUTO_CONV0_LSB Register

7	6	5	4	3	2	1	0
AUTO_CONV0_LSB							
R-0h							

Table 3-144. GPADC_AUTO_CONV0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_CONV0_LSB	R	0h	AUTO Conversion 0 data result (LSB) <7:0>

3.13.9 GPADC_AUTO_CONV0_MSB Register (Address = 2CAh) [reset = 0h]

GPADC_AUTO_CONV0_MSB is shown in Figure 3-132 and described in Table 3-145.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 0 (MSB)
RESET register domain: HWRST

Figure 3-132. GPADC_AUTO_CONV0_MSB Register

7	6	5	4	3	2	1	0
RESERVED				AUTO_CONV0_MSB			
R-0h				R-0h			

Table 3-145. GPADC_AUTO_CONV0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	AUTO_CONV0_MSB	R	0h	AUTO Conversion 0 data result (MSB) <11:8>

3.13.10 GPADC_AUTO_CONV1_LSB Register (Address = 2CBh) [reset = 0h]

GPADC_AUTO_CONV1_LSB is shown in Figure 3-133 and described in Table 3-146.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 1 (LSB)
RESET register domain: HWRST

Figure 3-133. GPADC_AUTO_CONV1_LSB Register

7	6	5	4	3	2	1	0
AUTO_CONV1_LSB							
R-0h							

Table 3-146. GPADC_AUTO_CONV1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_CONV1_LSB	R	0h	AUTO Conversion 1 data result (LSB) <7:0>

3.13.11 GPADC_AUTO_CONV1_MSB Register (Address = 2CCh) [reset = 0h]

GPADC_AUTO_CONV1_MSB is shown in Figure 3-134 and described in Table 3-147.

Return to Summary Table.

GPADC data results of the Automatic (Periodic) conversion 1 (MSB)
RESET register domain: HWRST

Figure 3-134. GPADC_AUTO_CONV1_MSB Register

7	6	5	4	3	2	1	0
RESERVED				AUTO_CONV1_MSB			
R-0h				R-0h			

Table 3-147. GPADC_AUTO_CONV1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	AUTO_CONV1_MSB	R	0h	AUTO Conversion 1 data result (MSB) <11:8>

3.13.12 GPADC_SW_SELECT Register (Address = 2CDh) [reset = 0h]

GPADC_SW_SELECT is shown in Figure 3-135 and described in Table 3-148.

Return to Summary Table.

GPADC Software Channel selection for Conversion 0
RESET register domain: HWRST

Figure 3-135. GPADC_SW_SELECT Register

7	6	5	4	3	2	1	0
SW_CONV_EN	RESERVED		SW_START_CONV0	SW_CONV0_SEL			
R/W-0h	R-0h		R/W-0h	R/W-0h			

Table 3-148. GPADC_SW_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SW_CONV_EN	R/W	0h	Software Conversion enabling 0: Software Conversion is not enable (defaults) 1: Software Conversion is enabled
6-5	RESERVED	R	0h	
4	SW_START_CONV0	R/W	0h	Toggle bit used by host processor to start a conversion (Conversion0) on selected channel by SW_CONV0_SEL Writing logical 0 in this bit has no effect
3-0	SW_CONV0_SEL	R/W	0h	Channel selection for Conversion 0 in SW mode 0000: GPADC Channel 0 0001: GPADC Channel 1 ..... 0110: GPADC Channel 6 0111: GPADC Channel 7 others: Reserved

3.13.13 GPADC_SW_CONV0_LSB Register (Address = 2CEh) [reset = 0h]

GPADC_SW_CONV0_LSB is shown in Figure 3-136 and described in Table 3-149.

Return to Summary Table.

GPADC data results of the Software conversion 0 (LSB)
RESET register domain: HWRST

Figure 3-136. GPADC_SW_CONV0_LSB Register

7	6	5	4	3	2	1	0
SW_CONV0_LSB							
R-0h							

Table 3-149. GPADC_SW_CONV0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW_CONV0_LSB	R	0h	SW Conversion 0 data result (LSB) <7:0>

3.13.14 GPADC_SW_CONV0_MSB Register (Address = 2CFh) [reset = 0h]

GPADC_SW_CONV0_MSB is shown in Figure 3-137 and described in Table 3-150.

Return to Summary Table.

GPADC data results of the Software conversion 0 (MSB)
RESET register domain: HWRST

Figure 3-137. GPADC_SW_CONV0_MSB Register

7	6	5	4	3	2	1	0
RESERVED				SW_CONV0_MSB			
R-0h				R-0h			

Table 3-150. GPADC_SW_CONV0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	SW_CONV0_MSB	R	0h	SW Conversion 0 data result (MSB) <11:8>

3.13.15 GPADC_THRES_CONV0_LSB Register (Address = 2D0h) [reset = 0h]

GPADC_THRES_CONV0_LSB is shown in Figure 3-138 and described in Table 3-151.

Return to Summary Table.

LSB of Threshold reference to be compared to the Conversion 0 results
RESET register domain: HWRST

Figure 3-138. GPADC_THRES_CONV0_LSB Register

7	6	5	4	3	2	1	0
THRES_CONV0_LSB							
R/W-0h							

Table 3-151. GPADC_THRES_CONV0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRES_CONV0_LSB	R/W	0h	Threshold value for Conversion 0 (LSB) <7:0>

3.13.16 GPADC_THRES_CONV0_MSB Register (Address = 2D1h) [reset = 0h]

GPADC_THRES_CONV0_MSB is shown in Figure 3-139 and described in Table 3-152.

Return to Summary Table.

MSB of Threshold reference to be compared to the Conversion 0 results
RESET register domain: HWRST

Figure 3-139. GPADC_THRES_CONV0_MSB Register

7	6	5	4	3	2	1	0
THRES_CONV0_POL	RESERVED			THRES_CONV0_MSB			
R/W-0h	R-0h			R/W-0h			

Table 3-152. GPADC_THRES_CONV0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THRES_CONV0_POL	R/W	0h	Threshold conversion 0 polarity 0: Interrupt generated if Conversion0 result is above threshold 1: Interrupt generated if Conversion0 result is below threshold
6-4	RESERVED	R	0h	
3-0	THRES_CONV0_MSB	R/W	0h	Threshold value for Conversion 0 (MSB) <11:8>

3.13.17 GPADC_THRES_CONV1_LSB Register (Address = 2D2h) [reset = 0h]

GPADC_THRES_CONV1_LSB is shown in Figure 3-140 and described in Table 3-153.

Return to Summary Table.

LSB of Threshold reference to be compared to the Conversion 1 results
RESET register domain: HWRST

Figure 3-140. GPADC_THRES_CONV1_LSB Register

7	6	5	4	3	2	1	0
THRES_CONV1_LSB							
R/W-0h							

Table 3-153. GPADC_THRES_CONV1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	THRES_CONV1_LSB	R/W	0h	Threshold value for Conversion 1 (LSB) <7:0>

3.13.18 GPADC_THRES_CONV1_MSB Register (Address = 2D3h) [reset = 0h]

GPADC_THRES_CONV1_MSB is shown in Figure 3-141 and described in Table 3-154.

Return to Summary Table.

MSB of Threshold reference to be compared to the Conversion 1 results
RESET register domain: HWRST

Figure 3-141. GPADC_THRES_CONV1_MSB Register

7	6	5	4	3	2	1	0
THRES_CONV1_POL	RESERVED			THRES_CONV1_MSB			
R/W-0h	R-0h			R/W-0h			

Table 3-154. GPADC_THRES_CONV1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	THRES_CONV1_POL	R/W	0h	Threshold conversion 1 polarity 0: Interrupt generated if Conversion0 result is above threshold 1: Interrupt generated if Conversion0 result is below threshold
6-4	RESERVED	R	0h	
3-0	THRES_CONV1_MSB	R/W	0h	Threshold value for Conversion 1 (MSB) <11:8>

3.13.19 GPADC_SMPS_ILMONITOR_EN Register (Address = 2D4h) [reset = 7h]

GPADC_SMPS_ILMONITOR_EN is shown in Figure 3-142 and described in Table 3-155.

Return to Summary Table.

GPADC SMPS selection for current measurement
RESET register domain: HWRST

Figure 3-142. GPADC_SMPS_ILMONITOR_EN Register

7	6	5	4	3	2	1	0
RESERVED	SMPS_COMPMODE	SMPS_ILMON_EN	SMPS_ILMON_VADC_MEAS_EN	SMPS_ILMON_SEL			
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-7h			

Table 3-155. GPADC_SMPS_ILMONITOR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	SMPS_COMPMODE	R/W	0h	ILMON comparator enable. This bit can be written 1 ONLY if SMPS_ILMON_EN bit is already 1. If SMPS_ILMON_EN is written with 0, ILMON_COMPMODE bit will be automatically written with 0 too. 0b = ILMON Comparator is disabled 1b = ILMON Comparator is enabled
5	SMPS_ILMON_EN	R/W	0h	Selection of GPADC ILMONITOR feature 0b = Feature not enabled (default) 1b = Feature is enabled
4	SMPS_ILMON_VADC_MEAS_EN	R/W	0h	SMPS_ILMON_VADC_MEAS_EN Allow monitoring of the SMPS load current profile including 100us peaks, for SW development purposes by using VPROG pin (without external resistor). In this mode also offset and gain compensation by trimming are included. 0b = Feature not enable (default) 1b = Feature is enabled
3-0	SMPS_ILMON_SEL	R/W	7h	SMPS I Load Monitor selection (exclusive) Others: Reserved 0000b = SMPS1 / SMPS12 0001b = SMPS2 0010b = Reserved 0011b = SMPS3 0100b = Reserved

3.13.20 GPADC_SMPS_VSEL_MONITORING Register (Address = 2D5h) [reset = 0h]

GPADC_SMPS_VSEL_MONITORING is shown in Figure 3-143 and described in Table 3-156.

Return to Summary Table.

GPADC SMPS voltage monitoring related to ILMONITORING measurement
RESET register domain: HWRST

Figure 3-143. GPADC_SMPS_VSEL_MONITORING Register

7	6	5	4	3	2	1	0
ACTIVE_PHASE	SMPS_VSEL_MONITORING						
R-0h	R-0h						

Table 3-156. GPADC_SMPS_VSEL_MONITORING Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACTIVE_PHASE	R	0h	Specify the number of active phases during measurements 0: One phase 1: Multi-phases (more than one)
6-0	SMPS_VSEL_MONITORING	R	0h	See VSEL cross table showed in SMPS1_VOLTAGE.VSEL register

3.14 FUNC_DESIGNREV Registers

Table 3-157 lists the memory-mapped registers for the FUNC_DESIGNREV. All register offset addresses not listed in Table 3-157 should be considered as reserved locations and the register contents should not be modified.

Table 3-157. FUNC_DESIGNREV Registers

Address	Acronym	Register Name	Section
357h	DESIGNREV	Silicon version number register RESET register domain: POR	Section 3.14.1

3.14.1 DESIGNREV Register (Address = 357h) [reset = X]

DESIGNREV is shown in Figure 3-144 and described in Table 3-158.

Return to Summary Table.

Silicon version number register
RESET register domain: POR

Figure 3-144. DESIGNREV Register

7	6	5	4	3	2	1	0
RESERVED				DESIGNREV			
R-0h				R-X			

Table 3-158. DESIGNREV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3-0	DESIGNREV	R	X	Value depending on silicon version number (From metal bits) 0000 - CS1.0 Revision 0001 - CS1.1 Revision

3.15 FUNC_TRIM_GPADC Registers

Table 3-159 lists the memory-mapped registers for the FUNC_TRIM_GPADC. All register offset addresses not listed in Table 3-159 should be considered as reserved locations and the register contents should not be modified.

Table 3-159. FUNC_TRIM_GPADC Registers

Address	Acronym	Register Name	Section
3CDh	GPADC_TRIM1	RESET register domain: POR	Section 3.15.1
3CEh	GPADC_TRIM2	RESET register domain: POR	Section 3.15.2
3CFh	GPADC_TRIM3	RESET register domain: POR	Section 3.15.3
3D0h	GPADC_TRIM4	RESET register domain: POR	Section 3.15.4
3E4h	GPADC_TRIM5	RESET register domain: POR	Section 3.15.5
3B8h	GPADC_TRIM6	RESET register domain: POR	Section 3.15.6

3.15.1 GPADC_TRIM1 Register (Address = 3CDh) [reset = 0h]

GPADC_TRIM1 is shown in Figure 3-145 and described in Table 3-160.

Return to Summary Table.

RESET register domain: POR

Figure 3-145. GPADC_TRIM1 Register

7	6	5	4	3	2	1	0
GPADC_IN0_IN1_D1							GPADC_IN0_IN1_D1_SIGN
R/W-0h							R/W-0h

Table 3-160. GPADC_TRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	GPADC_IN0_IN1_D1	R/W	0h	GPADC Input Channels 0 and 1 Calibration Value D1
0	GPADC_IN0_IN1_D1_SIGN	R/W	0h	Sign bit of the GPADC Input Channels 0 and 1 Calibration Value D1 0: Positive 1: Negative

3.15.2 GPADC_TRIM2 Register (Address = 3CEh) [reset = 0h]

GPADC_TRIM2 is shown in Figure 3-146 and described in Table 3-161.

Return to Summary Table.

RESET register domain: POR

Figure 3-146. GPADC_TRIM2 Register

7	6	5	4	3	2	1	0
GPADC_IN0_IN1_D2							GPADC_IN0_IN1_D2_SIGN
R/W-0h							R/W-0h

Table 3-161. GPADC_TRIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	GPADC_IN0_IN1_D2	R/W	0h	GPADC Input Channels 0 and 1 Calibration Value D2
0	GPADC_IN0_IN1_D2_SIGN	R/W	0h	Sign bit of the GPADC Input Channels 0 and 1 Calibration Value D2 0: Positive 1: Negative

3.15.3 GPADC_TRIM3 Register (Address = 3CFh) [reset = 0h]

GPADC_TRIM3 is shown in Figure 3-147 and described in Table 3-162.

Return to Summary Table.

RESET register domain: POR

Figure 3-147. GPADC_TRIM3 Register

7	6	5	4	3	2	1	0
VCC_D1							VCC_D1_SIGN
R/W-0h							R/W-0h

Table 3-162. GPADC_TRIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	VCC_D1	R/W	0h	GPADC Input Channel 3 Calibration Value D1 when HIGH_VCC_SENSE=0
0	VCC_D1_SIGN	R/W	0h	Sign bit of the GPADC Input Channel 3 Calibration Value D1 when HIGH_VCC_SENSE=0 0: Positive 1: Negative

3.15.4 GPADC_TRIM4 Register (Address = 3D0h) [reset = 0h]

GPADC_TRIM4 is shown in Figure 3-148 and described in Table 3-163.

Return to Summary Table.

RESET register domain: POR

Figure 3-148. GPADC_TRIM4 Register

7	6	5	4	3	2	1	0
VCC_D2							VCC_D2_SIGN
R/W-0h							R/W-0h

Table 3-163. GPADC_TRIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	VCC_D2	R/W	0h	GPADC Input Channel 3 Calibration Value D2 when HIGH_VCC_SENSE=0
0	VCC_D2_SIGN	R/W	0h	Sign bit of the GPADC Input Channel 3 Calibration Value D2 when HIGH_VCC_SENSE=0 0: Positive 1: Negative

3.15.5 GPADC_TRIM5 Register (Address = 3E4h) [reset = 0h]

GPADC_TRIM5 is shown in Figure 3-149 and described in Table 3-164.

Return to Summary Table.

RESET register domain: POR

Figure 3-149. GPADC_TRIM5 Register

7	6	5	4	3	2	1	0
VCC_D1							VCC_D1_SIGN
R/W-0h							R/W-0h

Table 3-164. GPADC_TRIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	VCC_D1	R/W	0h	GPADC Input Channel 3 Calibration Value D1 when HIGH_VCC_SENSE=1
0	VCC_D1_SIGN	R/W	0h	Sign bit of the GPADC Input Channel 3 Calibration Value D1 when HIGH_VCC_SENSE=1 0: Positive 1: Negative

3.15.6 GPADC_TRIM6 Register (Address = 3B8h) [reset = 0h]

GPADC_TRIM6 is shown in Figure 3-150 and described in Table 3-165.

Return to Summary Table.

RESET register domain: POR

Figure 3-150. GPADC_TRIM6 Register

7	6	5	4	3	2	1	0
VCC_D2							VCC_D2_SIGN
R/W-0h							R/W-0h

Table 3-165. GPADC_TRIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	VCC_D2	R/W	0h	GPADC Input Channel 3 Calibration Value D2 when HIGH_VCC_SENSE=1
0	VCC_D2_SIGN	R/W	0h	Sign bit of the GPADC Input Channel 3 Calibration Value D2 when HIGH_VCC_SENSE=1 0: Positive 1: Negative

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