Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices

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ABSTRACT

Texas Instruments has introduced a family of devices suited to meet the demand for high-speed, high-IF sampling ADC devices like the ADS5500 ADC, capable of sampling at 125 MSPS. To realize the full potential of these high performance devices, it is imperative to provide an extremely low phase noise clock source. The CDC7005 clock distribution chip offers a real-world clocking solution to meet the stringent requirements for high-speed ADCs. This report highlights the limiting agents associated with the clock source that adversely affect the ADC's signal-to-noise performance. The performance of the ADS5500 ADC clocked with the CDC7005 is shown and compared to ideal baseline performance. Further improvement topologies are presented along with measured results that show the CDC7005 can meet or exceed the specifications at high sampling rates, even at the more demanding high input frequencies.

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1 Introduction

New transceiver architectures and PA linearization techniques are being investigated with the introduction of high sampling rate and high IF capability analog-to-digital converters (ADCs). For example, digital predistortion requires high sampling rate ADCs to convert the output spectrum of the PA, including the desired signal and the third and fifth order intermodulation products, for linearization processing. The bandwidth requirements for a multi-carrier WCDMA PA can be as high as 100 MHz. This requires high sampling rate ADCs to suitably capture the signal.

For new receiver designs with multi-carrier signals incorporating cost-savings topologies, there is a need for high IF sampling ADCs. This effectively eliminates the need for a second analog mixer or analog demodulator which simplifies the receiver architecture. A high IF ADC is required to sample the signal at these frequencies with sufficient purity for the advanced telecommunication standards.

Texas Instruments offers a series of high IF, high sampling rate ADCs suitable for the wireless infrastructure market. The ADS5500 is the industry leading 14-bit, 125-MSPS ADC that is capable of achieving good SNR performance with high input frequency signals. In order to realize the devices' full potential, it is important that the clock source have low phase noise. This requirement is often overlooked when evaluating and designing with high-end ADCs. Further, though a suitable source may be used for evaluating purposes, finding a board level solution often proves difficult.

Texas Instruments introduces a board level, low phase noise clocking solution for the ADS5500 and other high speed ADC devices using the CDC7005 clock distribution chip. With proper configuration, the CDC7005 can be used with Texas Instruments high-speed ADCs to achieve ideal performance that is suitable for direct implementation into PCB designs. In addition, the CDC7005 has the capability to drive five independent outputs that can be independently divided down by 2^n (n = 0 to 4). This allows one clock circuitry to provide a clock source for not only the high performance ADCs, but also the other devices on the board requiring an independent clock such as DACs (digital-to-analog converters), DDCs (digital down-converters), and DUCs (digital up-converters). Figure 1 illustrates how the CDC7005 is utilized with the ADC and other devices in a typical transceiver block diagram.

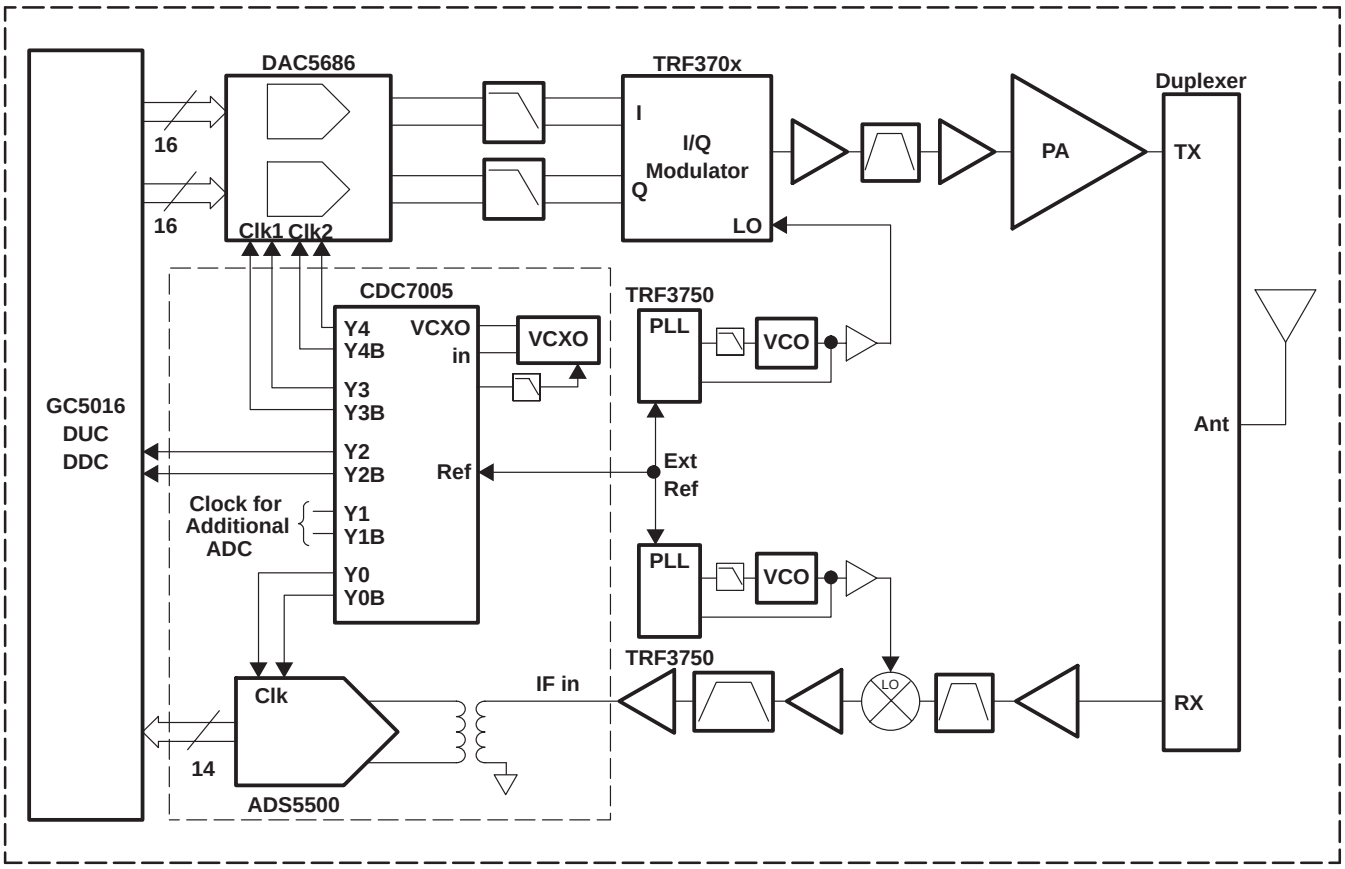

Figure 1. ADS5500 ADC With CDC7005 Clocking Solution Within A Typical Base Station Architecture

2 High IF Sampling Challenges

Clock jitter is defined as the random variation of the clock position compared to its ideal position with respect to time. When the position of the clock varies slightly, it alters the position of the sampling point which in turn samples the input waveform at an imprecise location. This error manifests itself as a signal-to-noise (SNR) degradation.

The SNR degradation attributed to the jitter of the clock is defined as:

$$SNR_j = -20 \times \log\left[\frac{\frac{V_{fs}}{2} \times \left(2 \times \pi \times f_{in}\right) \times 10^{\frac{Vin}{20}} \times \tau_j}{\sqrt{2}}\right]$$

Where:

V_{fs} = Full-scale voltage of the ADC
V_{in} = Relative input amplitude of the signal compared to Vfs expressed in dBFS
f_{in} = Input frequency
t_j = Clock jitter expressed in seconds

Note that the SNR degradation due to clock jitter is independent of the sampling rate; however, it is dependent on the input frequency. If it is noted that the expression inside the brackets is less than unity, then by increasing the input frequency the SNR contribution from the clock jitter becomes more significant. In other words, for a given amount of clock jitter, a higher input IF signal will be more susceptible to SNR degradation. This phenomenon is illustrated in Figure 2. Figure 2 depicts two IF input signals at different frequencies. An ideal clock source with a given amount of jitter samples each signal. The ideal sampling point is shown at the dot, but the jitter will alter the exact point where the signal is sampled. The potential points that could be sampled are depicted by the bold red line between the dashes. The error line on the lower frequency signal is smaller than that on the higher frequency signal. As a result, the higher IF signal will have higher SNR degradation due to clock jitter.

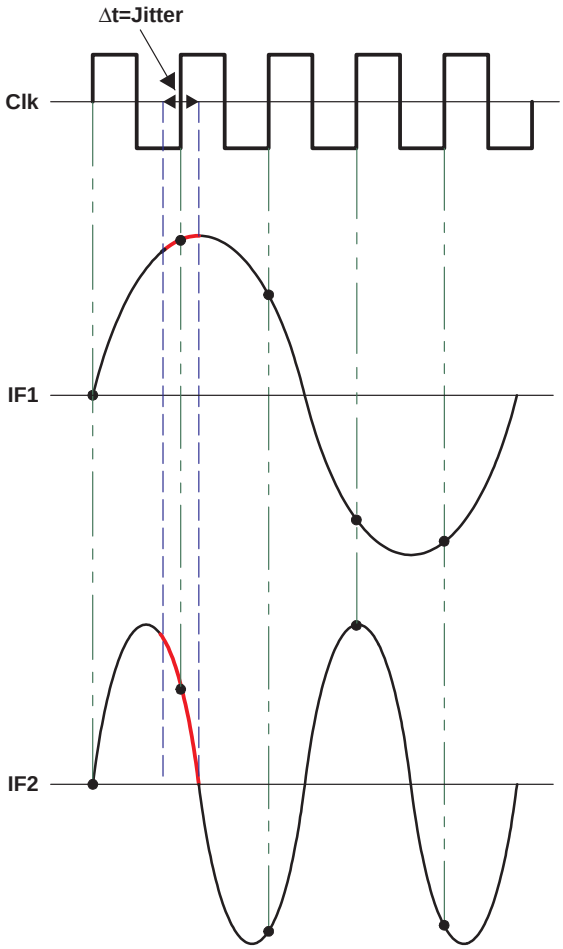

Figure 2. SNR Degradation Due to Jitter for Different IF Input Signals

The total ADC SNR becomes the combination of the SNR contribution from clock jitter and the contribution inherent to the device. The total SNR is given by:

$$SNR_T = -20 \times \log \left[\sqrt{10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_j}{10}\right)}} \right]$$

Where:

SNR_j = SNR contribution due to clock jitter

SNR_{ADC} = SNR contribution inherent in the ADC

In the case of the ADS5500, the baseline performance measured with a low jitter HP8644B signal generator and narrow band-pass filter yields an SNR value around 71.5 dBFS at 100 MHz with the input signal at −1 dBFS. The clock source was measured independently and shown to have approximately 0.25-ps RMS jitter over 1 kHz to 40 MHz. Using the full-scale value of the ADS5500 which is 2.3 Vpp at 100-MHz input frequency and driving the ADC to −1 dBFS, the SNR contribution from the near-ideal clock source is 78.9 dBFS. Given this information and the measured total SNR measurements, the inherent SNR of the ADC is estimated using the equation above to be 72.4 dBFS.

Using the estimated inherent ADC SNR of 72.4 dBFS and the measured jitter of the near-ideal clock source, the performance over input frequency can be calculated. Though ideally the performance is independent of the sampling rate, practically each device is optimized for a specific rate to achieve the best performance. The ADS5500 is optimized around 125-MHz sampling rate. The SNR measurements were taken at 122.88 MHz. Figure 3 shows the measured performance versus predicted performance over input frequency.

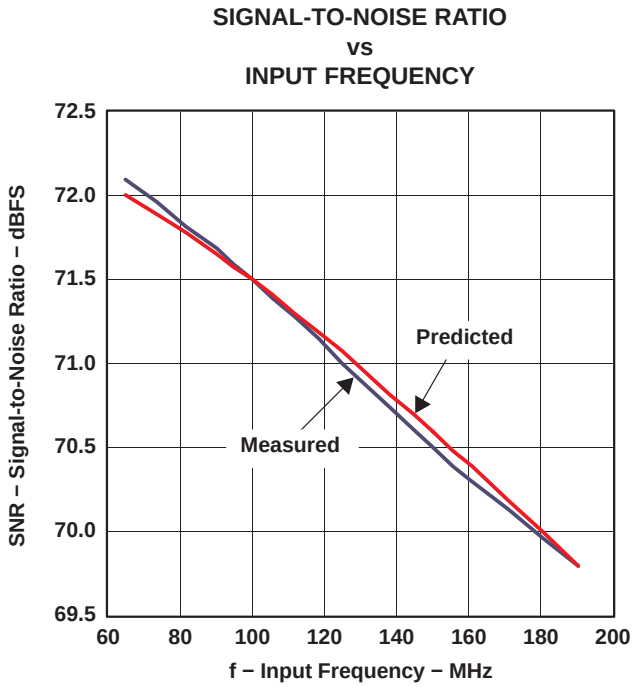

Figure 3. Measured vs Predicted SNR Performance Over Input Frequency

The predicted values match closely to the measured data for the device. As such, these equations can be used to predict performance at any desired input frequency.

3 Effect of Clock Amplitude

With an ideal square-wave clock the sampling is completed at the zero-crossings of the waveform. Further, in some ADC components, like the ADS5500, the data is sampled and latched using the up and down cycles of the clock; hence, it is important for the clock to maintain a 50% duty cycle. Previously, it was shown that jitter effects the sampling position of the input waveform which degrades SNR performance. Thermal noise from a non-ideal clock also contributes to SNR degradation.

Thermal noise contributes a random amplitude vector to the clock source. With an ideal square-wave clock, the signal would slam instantaneously from one state to the other. In this scenario, slight amplitude variations due to noise would have no effect in the transition sampling point. Practically, even with a good square-wave clock, the transition from one state to the other is not instantaneous. There is a finite time in which the transition occurs. Noise on the waveform alters the signal such that the cross-over points occurs slightly off the ideal position. This causes a small error in the sampling point which degrades SNR. Figure 4 illustrates a zoomed in portion of the transition slope of the clock around the crossover point with added random noise. The noise component, Δn, raises the signal to the crossover point which yields a small error Δt.

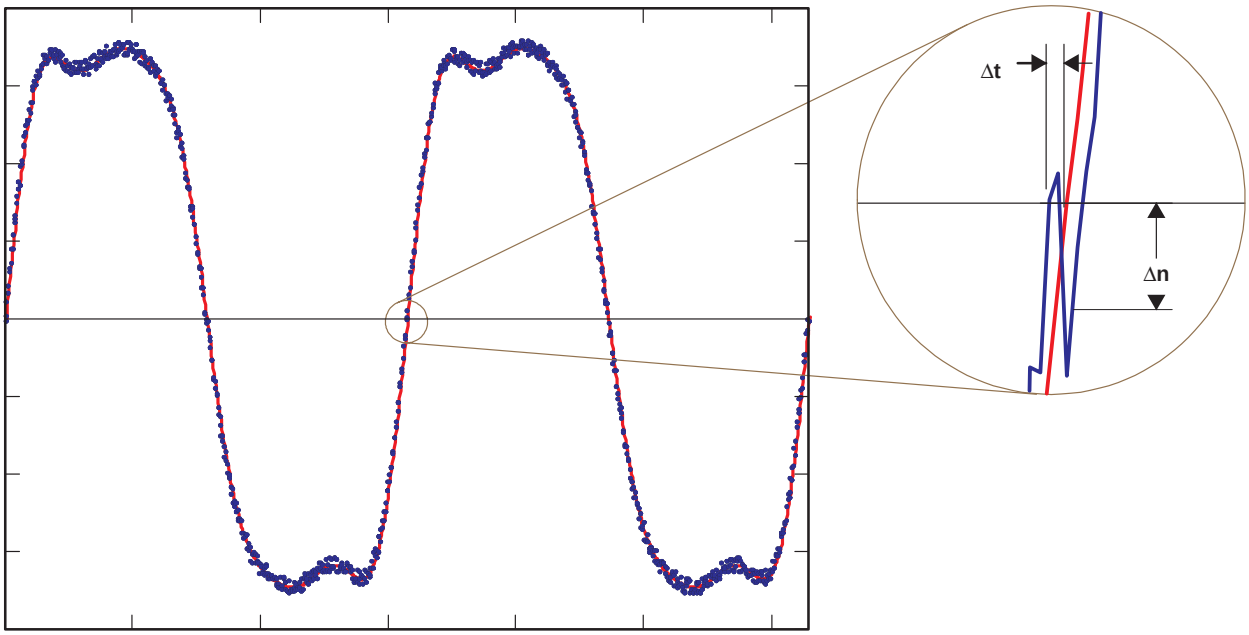

Figure 4. Thermal Noise Component Causing Sampling Error

One method to minimize the impact of thermal noise degradation is to make the transition slope steeper. In other words, by increasing the transition slope of the clock signal, the signal more closely approximates the ideal square wave clock. Conversely, a less steep transition slope is more susceptible to SNR degradation due to thermal noise. Figure 5 illustrates two clock signal transition slopes each subjected with the same thermal noise profile. The noise component is equal for both transition slopes, but the resultant timing error, Δt, is larger for the shallower slope. For this reason, it is desirable to keep the transition slopes as steep as possible in order to minimize the effect of thermal noise.

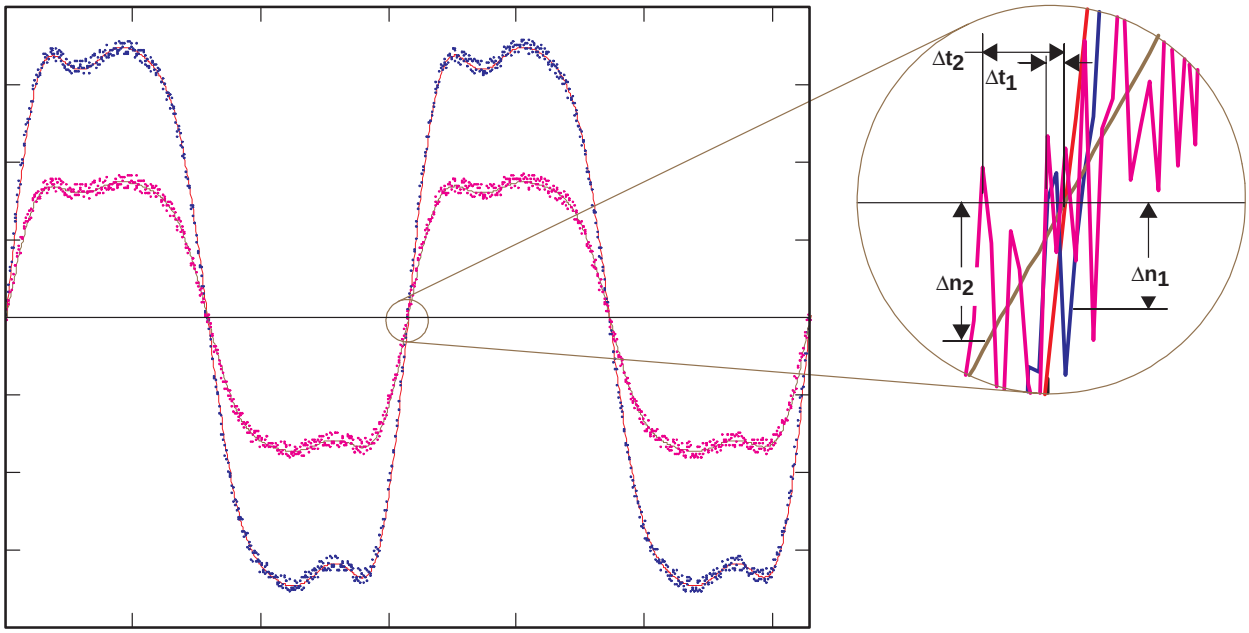

Figure 5. Thermal Noise Effect for Different Slope Clock Signals

The thermal noise component of the clock can be minimized by including a band-pass filter at the clock input centered at the clock frequency of choice [1]. Any suitable band-pass filter topology will suffice, such as an L−C filter, a SAW filter, or a crystal filter. Since the clock frequency is only a single tone, the most narrow bandwidth filter produces the best results. Given the clocking frequencies are around 60 MHz to 125 MHz, a narrow band crystal band-pass filter is the most suitable filter choice and is commonly used with ultra-low phase noise oscillators [2].

The inclusion of a band-pass filter around the clock minimizes noise outside the filter bandwidth, but it also affects the transition slope of the clock signal. A square-wave clock signal is comprised of a fundamental tone and a series of higher order harmonics. By inserting the narrow band-pass filter, the higher harmonics of the clock signal are eliminated. The result is a pure fundamental tone in the frequency domain or a pure sine wave in the time domain. Though the filter has effectively minimized the noise components, it has also inadvertently reduced the transition slope of the clock signal since the transition of a sine wave is shallower than that of a square wave. As shown previously, this shallower transition becomes more susceptible to noise contributions. The band-pass filter not only removes the harmonics of the clock signal resulting in a sine-wave output signal, it also introduces 2 dB to 6 dB of insertion loss. This insertion loss further reduces the amplitude of the clock signal and reduces the transition slope of the signal. In order to keep the transitions sharp, the amplitude of the sine wave signal needs to be increased.

Figure 6 illustrates the way the error from thermal noise is minimized due to a higher amplitude sine-wave signal, because it affectively increases the transition slope of the signal. A low noise amplifier can be inserted prior to the band-pass filter to amplify the signal in order to keep the transition slope as sharp as possible.

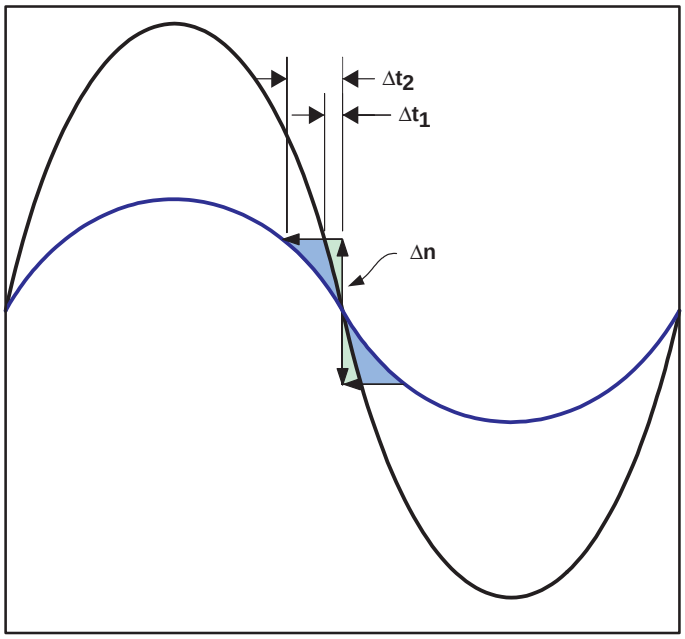

Figure 6. Thermal Noise Effect for Different Amplitude Sinusoids

4 CDC7005 Clocking Solution

The CDC7005 is a high performance, low jitter differential clock driver and clock distribution chip. It has five independently controlled outputs, which can be suitably used to clock high performance ADCs like the ADS5500, as well as satisfy other clocking requirements on the board. The CDC7005 offers a real-world clocking solution for these applications, which can synchronize the clock output to a supplied board reference frequency.

The CDC7005 device's key features are:

1. The reference clock can be synchronized to virtually any VCXO frequency.
2. Reference clock jitter is cleaned
3. Low jitter output
4. Five independent frequency outputs selectable by $/2^n$
5. Differential LVPECL interface

5 CDC7005 Design Considerations

5.1 VCXO Requirement

The CDC7005 utilizes a VCXO (voltage controlled crystal oscillator) as the primary oscillator source that is synchronized to the reference clock. For the best SNR performance of the ADC, it is imperative that the oscillator have low phase noise. The output phase noise performance, or jitter performance, of the CDC7005 is limited by this component.

The VCXO interface to the CDC7005 is shown in Figure 7. It is necessary to provide a PECL interface between the VCXO and the CDC7005 for proper operation. The load resistors are important for ensuring the proper source current while providing a 50-Ω load. It has been shown specifically for the ADS5500 the differential lines should be swapped at this interface for best SNR performance. In other words, the VCXO “A” output is connected to the CDC7005 “B” input. Similarly, the “B” VCXO output is connected to the “A” CDC7005 input.

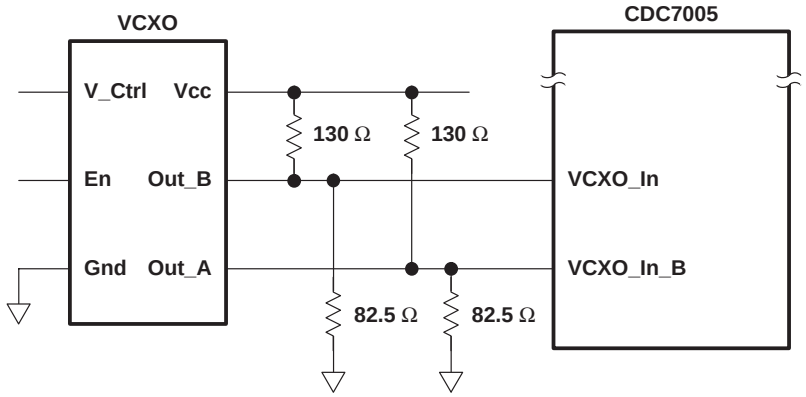

Figure 7. VCXO to CDC7005 Interface

As previously mentioned, the phase noise of the VCXO gates the overall performance of the CDC7005 output. For the experiments in this document, a Toyocom TCO−2111T 122.88-MHz PECL VCXO was used. The phase noise of this device was measured compared to a known good source, the Agilent HP8644B signal generator. The results are shown in Figure 8. The phase noise out of the CDC7005 when coupled with the designated VCXO yields about −145-dBc/Hz phase noise at 10-kHz offset and beyond. This performance is deemed good for an on-board solution. The phase noise of the near-ideal source is about 5 dB better at 10 kHz and improves with the roll-off of the band-pass filter; hence, it is expected that using the VCXO source provides a slight degradation compared to using the near-ideal source.

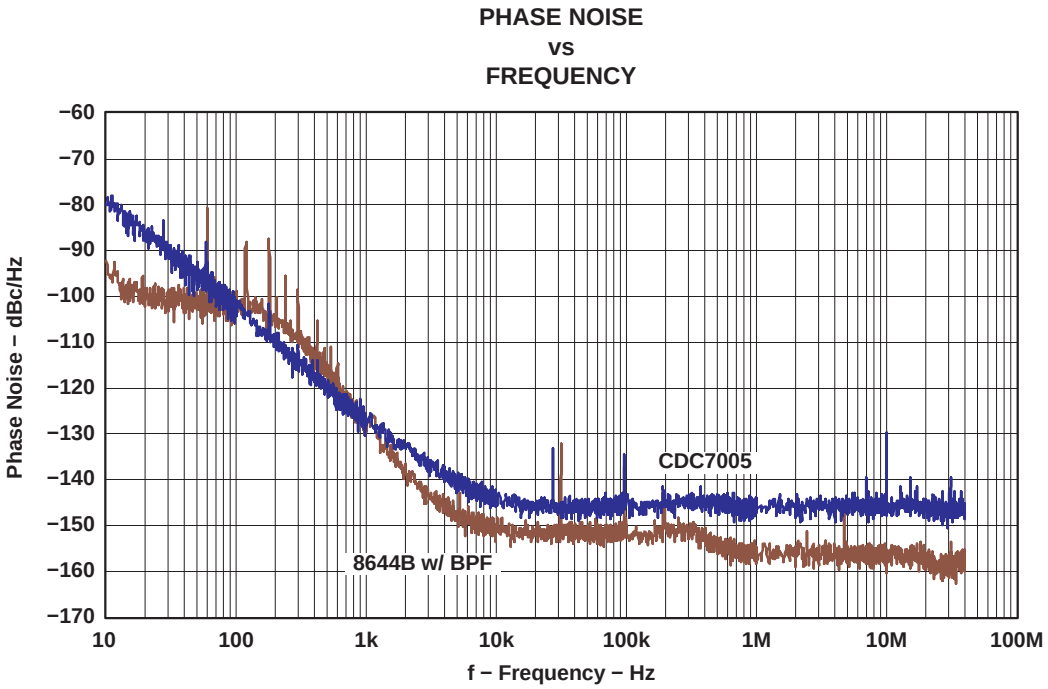

Figure 8. Phase Noise Measurement of the CDC−VCXO Compared With HP8644B

5.2 Proper Terminations

For proper operation, the CDC7005 PECL outputs must be properly terminated. Further, for the best clock signal, it is important to properly terminate the clock input lines close to the ADC device to minimize reflections. Using the differential output is ideal, because it minimizes the susceptibility of outside noise coupling on the line; however, the CDC7005 output ports can also be operated single ended. It is recommended that a transformer be used to convert the signal to differential prior to the ADC interface to gain the benefit described above at the ADC input interface.

Figure 9 shows the CDC7005 terminations suitable for proper operation. The PECL outputs should be terminated in 150 Ω. Alternatively, a pullup resistor value of 130 Ω and a pulldown of 82.5 Ω could be used, which would also provide a 50-Ω load. The pullup and pulldown resistors on the reference clock provide a 50-Ω termination for the clock source while biasing the node at mid-scale. A 100-Ω resistor is placed between the differential pair close to the ADC clock input pins to provide a good 50-Ω termination for the clock. If operating with a single-ended output, then the unused port should still be terminated. The single-ended output is run through a transformer to convert to differential prior to the ADC clock interface. A 4:1 transformer is recommended to provide a voltage increase, so that the resulting signal swing is equivalent to the original differential output. The loop filter components are contingent on the frequency of the VCXO. Proper loop filter design is discussed in detail in the SCAA063 application note.

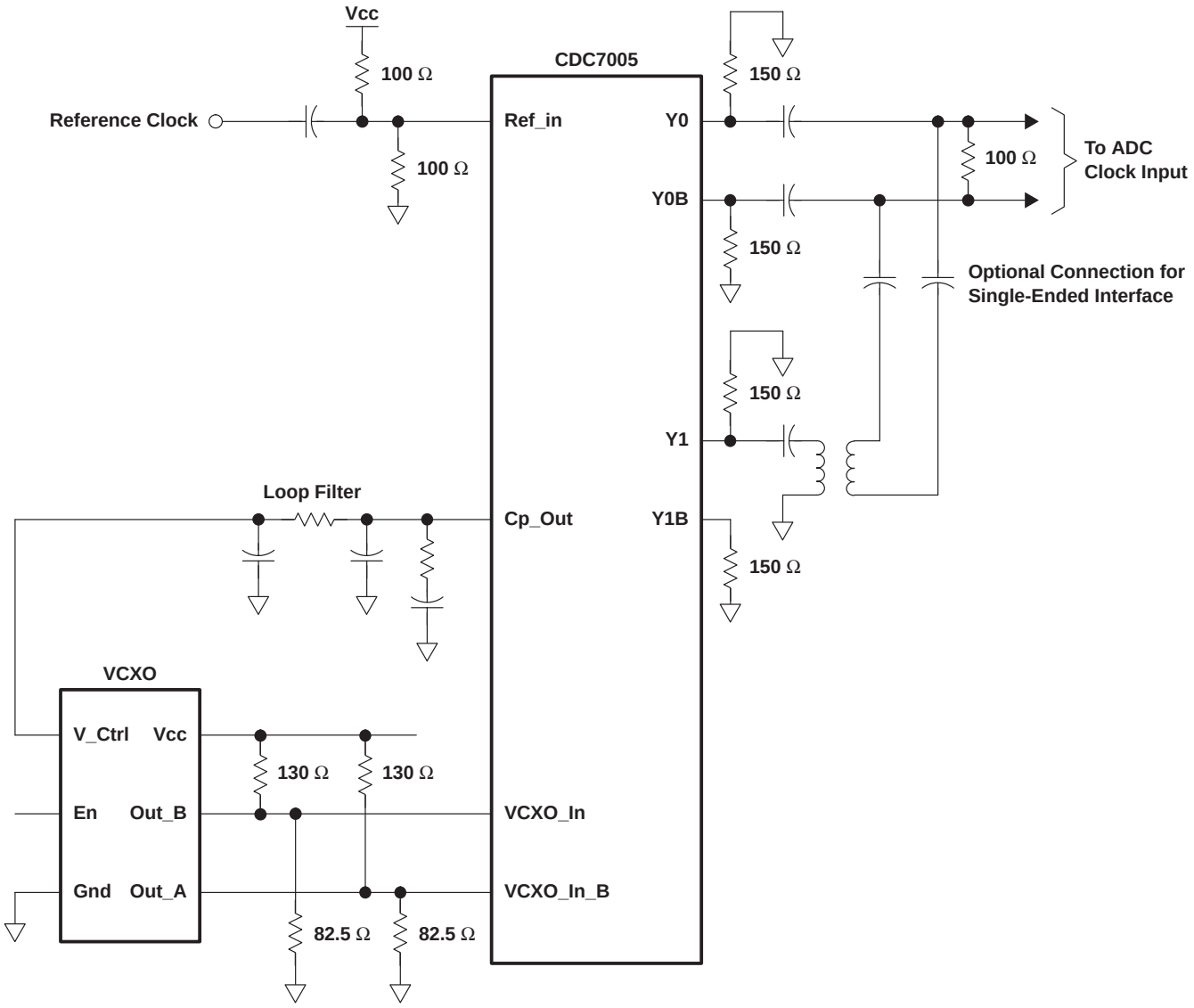

Figure 9. CDC7005 Terminations

5.3 Layout Considerations

A good layout design is required to provide a clean clock signal to the ADC and to ensure the device maintains proper lock with the reference signal. The CDC7005 is a BGA device that has its internal pads connected to either power or ground. Good grounding techniques must be applied to minimize ground loops and spurious output. To achieve this, it is recommended that an 8 mil ground via be buried within each ground pad to provide a low inductance path to the common ground plane. Alternatively, a *dog bone* technique can be employed which provides a ground via just outside the ground pad and is connected with a short trace. Figure 10 shows the suggested layout pattern.

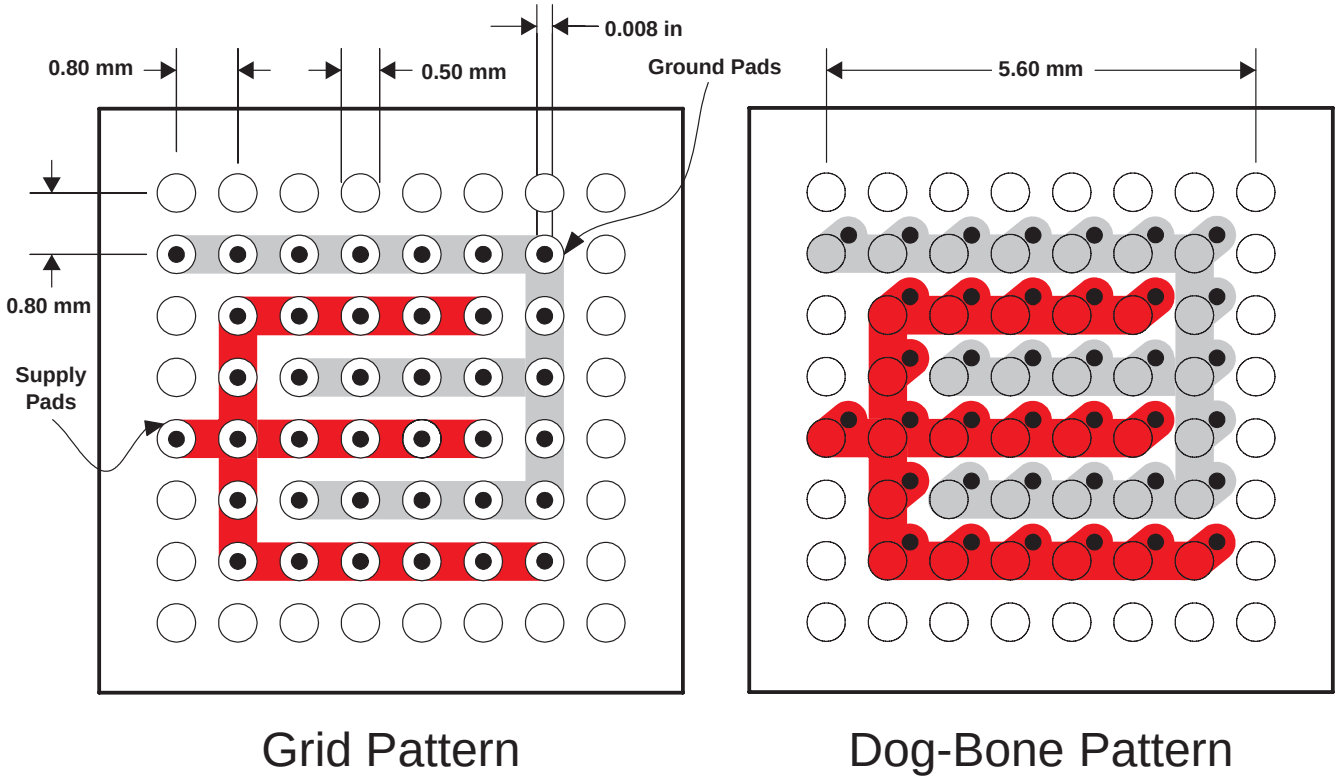

Figure 10. Grounding and Supply Connection Schemes for the CDC7005

It is also important to provide good bypassing of the supplies close to the supply pins of the CDC7005 device. This ensures a good low impedance path to the ground plane for any noise or spurious signals on the supply, which helps provide a cleaner clock for the ADC. Small vias are placed in or close to the supply pads, similar to the ground vias, to provide a direct path to an internal power plane layer. Small 0402 size 0.1-µF capacitors are placed on the opposite side of the board from the device and connect to the existing supply and ground vias to provide supply bypassing.

Figure 11 shows the bypassing pattern that is recommended for the components placed inside the grid pattern. Additional supply bypassing, including larger value capacitors for lower frequency bypassing, is recommended and should be placed close to the device but outside the grid pattern as is conducive for the layout; these bypassing components are not shown in the figures.

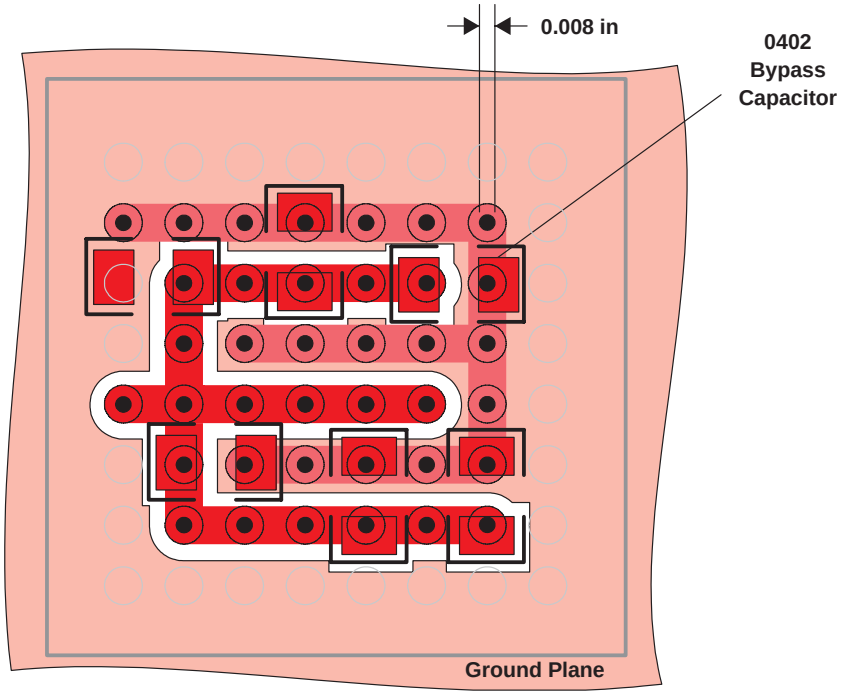

Figure 11. Supply Bypassing for the CDC7005

6 CDC7005 Clock Source for the ADS5500

To illustrate the performance of the CDC7005 clocking solution, the device is coupled with the Toyocom 122.88-MHz VCXO and used to supply the clock signal to the ADS5500. The data is compared to the baseline performance using an extremely good phase-noise generator with a crystal band-pass filter. The test setup is shown in Figure 12.

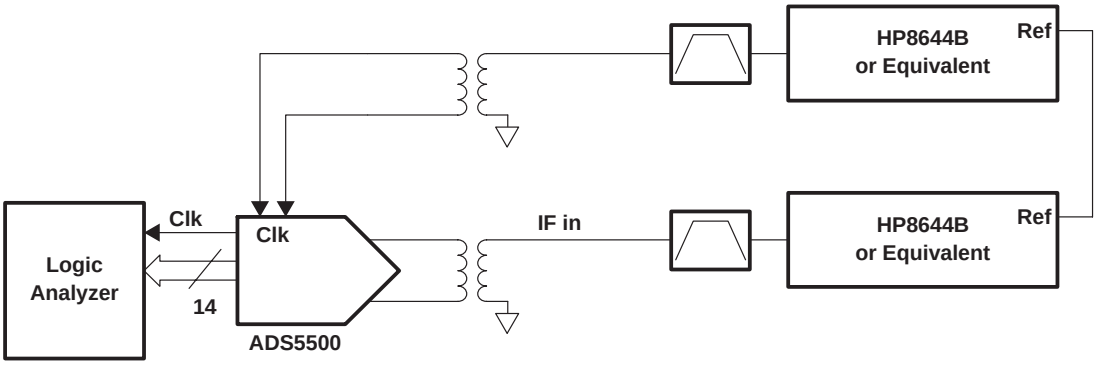

Figure 12. ADC Evaluation Test Set Up (Baseline)

The measured performance of the device over frequency with near-ideal clock source is compared to the performance utilizing the CDC7005 as a clock source. The block diagram of the ADC test set up incorporating the CDC7005 is shown in Figure 13.

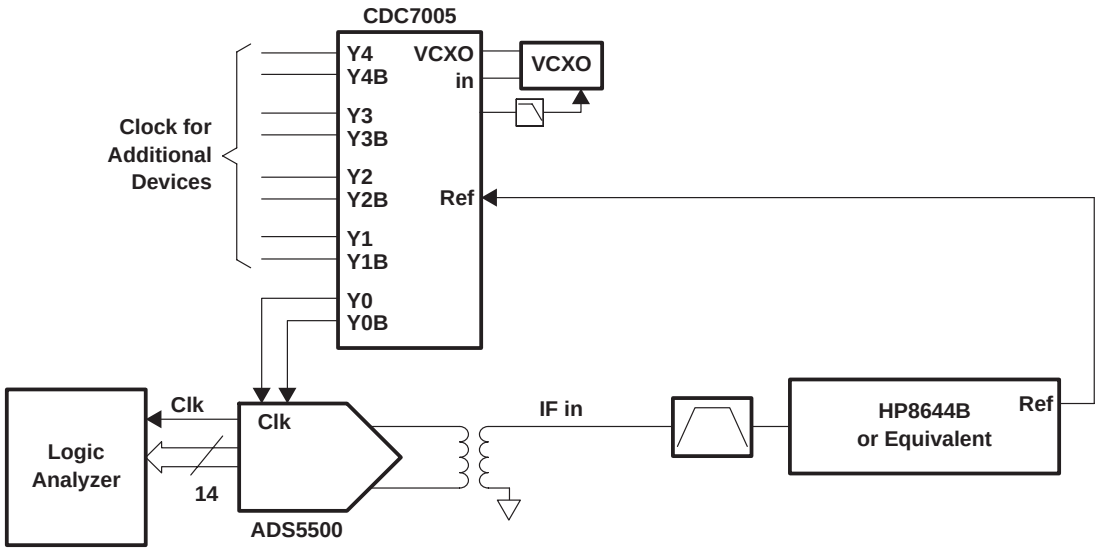

Figure 13. ADC Evaluation Test Setup With the CDC7005 Clocking Source

The measured results for the ADC SNR and SFDR (spurious free dynamic range) are shown in Table 1.

Table 1. SNR and SFDR Measurements With the CDC7005 Clock

	SNR [dBFS]		SFDR [dBc]	
Freq. [MHz]	**Baseline**	**CDC7005**	**Baseline**	**CDC7005**
2	72.9	72.8	85.2	85.2
15.5	73.0	72.8	87.4	87.0
30	72.9	72.4	84.0	86.3
65	72.6	70.9	77.9	80.4
100	72.2	68.8	84.0	84.1
150	70.8	66.3	76.7	79.8
190	70.1	64.9	74.1	74.0

The SNR results are shown versus frequency in Figure 14 and the spectral plot of the performance at 15.5 MHz is displayed in Figure 15.

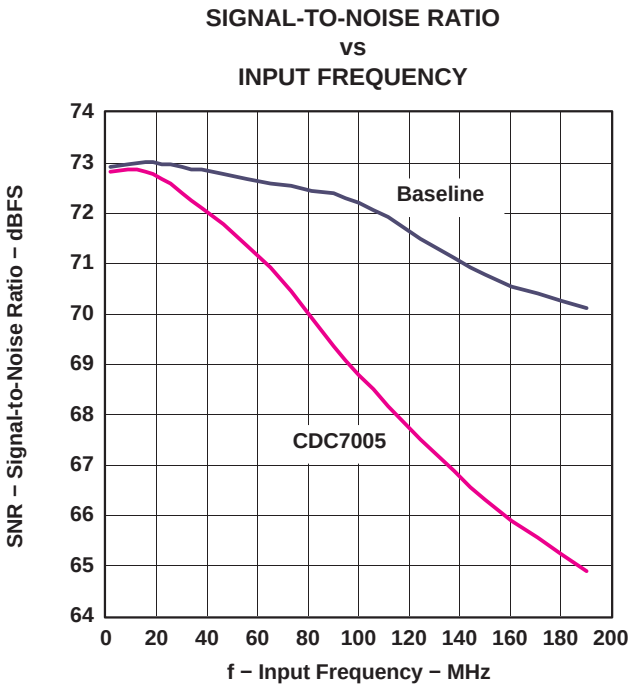

Figure 14. SNR Performance vs IF Input Frequency

If the IF input frequency is at or below the first Nyquist zone, around 60 MHz for this sampling rate, the CDC7005 provides a suitable clock source to achieve SNR values close to the baseline performance. As is expected from the analysis in section 2, the desired performance degrades at higher IF frequencies. Because the jitter associated with the CDC7005 is not quite as good, the SNR degradation is more severe when operating at higher IF frequencies. The SFDR performance is similar to the baseline case and does not degrade over higher IF frequencies; in fact, at some frequencies the performance is superior.

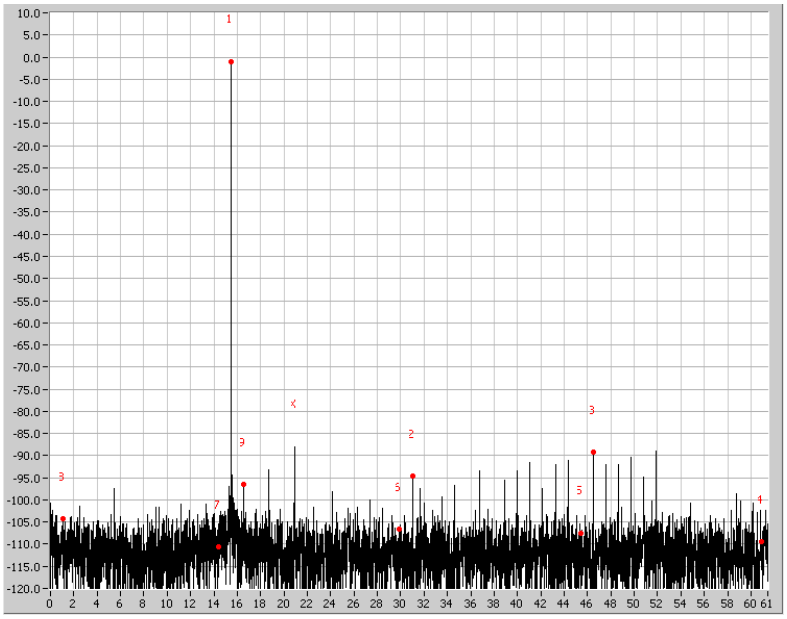

Figure 15. Spectral Performance With the CDC7005 Clock Source at 15.5-MHz IF Input

7 Performance Improvements

7.1 Improved Jitter

One method to achieve performance improvements is to utilize a lower phase noise (or lower jitter) oscillator source. This can be achieved by using a lower jitter VCXO device or by using a lower phase noise VCSO (voltage controlled SAW oscillator). Note that the CDC7005 is capable of dividing down any output, so that the oscillator frequency could be a higher multiple of the desired clock. This is useful for SAW oscillators, which generally operate at 500 MHz and above.

The ADC performance was measured with a lower phase noise LVDS VCXO. The LVDS interface IC in the VCXO has a slightly better noise figure compared to the PECL interface IC. Though the LVDS interface provides a lower signal swing to the CDC7005, there is still sufficient drive for the device to maintain frequency lock. The phase noise of the CDC7005 output using the LVDS VCXO is compared with the measurement using the PECL VCXO in Figure 16. The phase noise measurements show that the noise floor is about 5 dB lower when using the LVDS VCXO rather than the PECL VCXO at 100 kHz and above. The SNR measurement comparison between the two VCXO sources is shown in Figure 17.

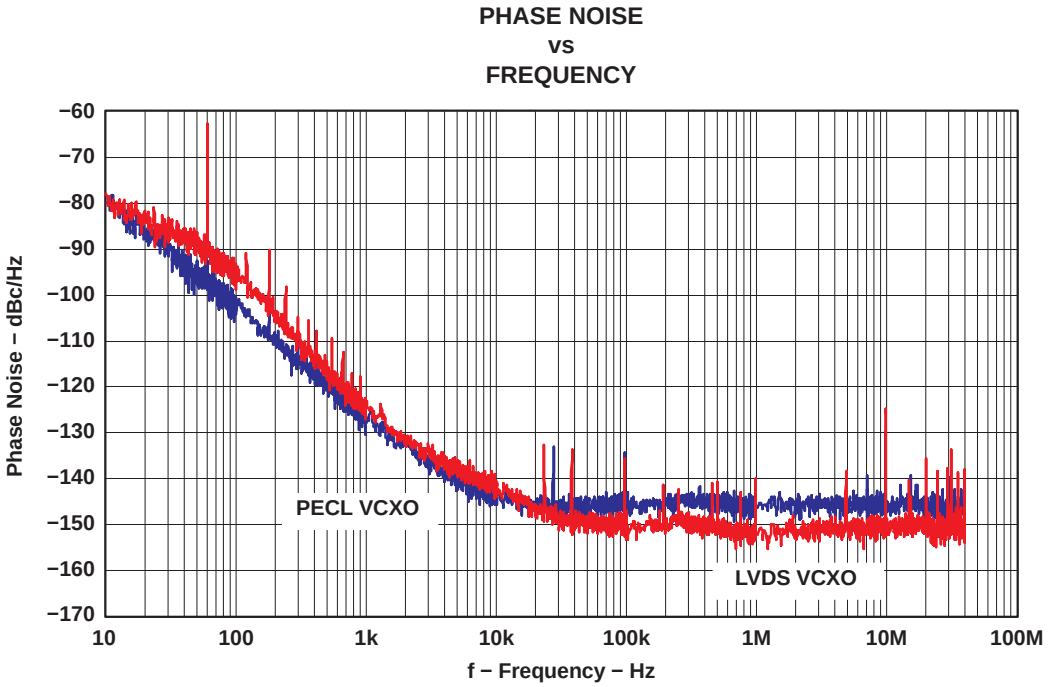

Figure 16. Phase Noise Comparisons of CDC7005 Output With PECL and LVDS VCXOs

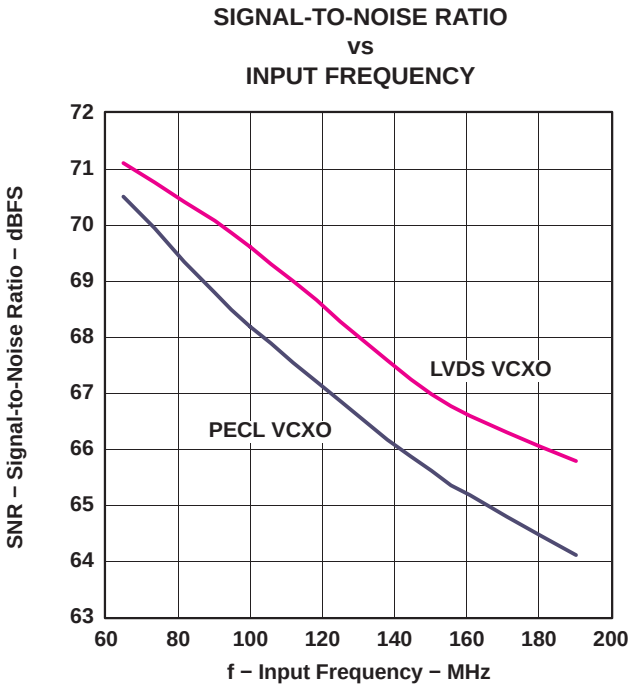

Figure 17. SNR Improvement With Lower Phase Noise VCXO Source

The improved phase noise oscillator yielded as much as 1.5-dB SNR improvement at the high IF input signals. The results show that any phase noise improvement from the oscillator source generally transfers to better SNR performance from the ADC. Though the SNR performance has improved at the high IF inputs, it is still not on par with the baseline measurements; further improvements are required.

7.2 Lower Thermal Noise

As seen in section 3, minimizing thermal noise on the clock improves the phase noise and improves the SNR performance. This is achieved by placing a narrow band crystal filter after the CDC7005 output. The filter used is a Toyocom TF2−C2EC1 122.88-MHz crystal filter with approximately 20 kHz of total bandwidth. The crystal filter is matched to 50 Ω to provide a suitable interface to the other circuitry. The crystal filter introduces about 3 dB of insertion loss. As previously discussed, the combination of the filter's insertion loss and conversion from a square wave output to a sine wave output reduces the transition slope of the clock waveform. The benefit of the added filter is negated by the insertion loss and the loss of square wave. Adding a small broadband amplifier stage just prior to the filter compensates for the loss of the filter and provides steep clock transitions. Though the filter attenuates much of the broadband noise from the amplifier, noise within the filter's pass band still gets through. It is a good design practice to keep the noise figure of the booster amplifier to less than 3 dB.

The phase noise of the CDC7005 (with PECL VCXO) coupled with the amplifier and filter is shown in Figure 18. Below the corner frequency of the band-pass filter, the performance between the two cases is nearly identical. Once the corner frequency is reached, the phase noise improves. After 100-kHz offset, the phase noise performance of the CDC7005−Amp−BPF combination rivals that of the near-ideal source.

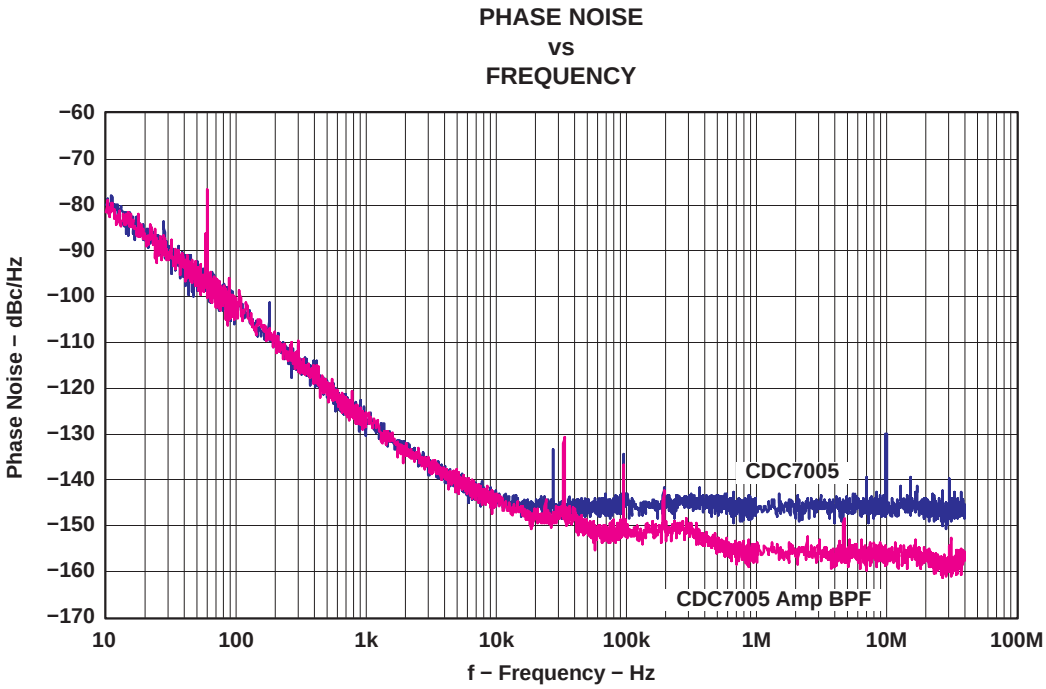

Figure 18. Phase Noise of the CDC7005 With the Amp and BPF Compared to the Unmodified Output

When utilizing an amplifier and crystal filter, it is desirable to operate the CDC7005 in single-ended mode so that only one amplifier and filter is required. It is conceivable to use an identical amplifier and filter in each differential path; however, maintaining matched amplitude and phase over each path over temperature and lot variations may prove difficult. The block diagram of the setup is shown in Figure 19.

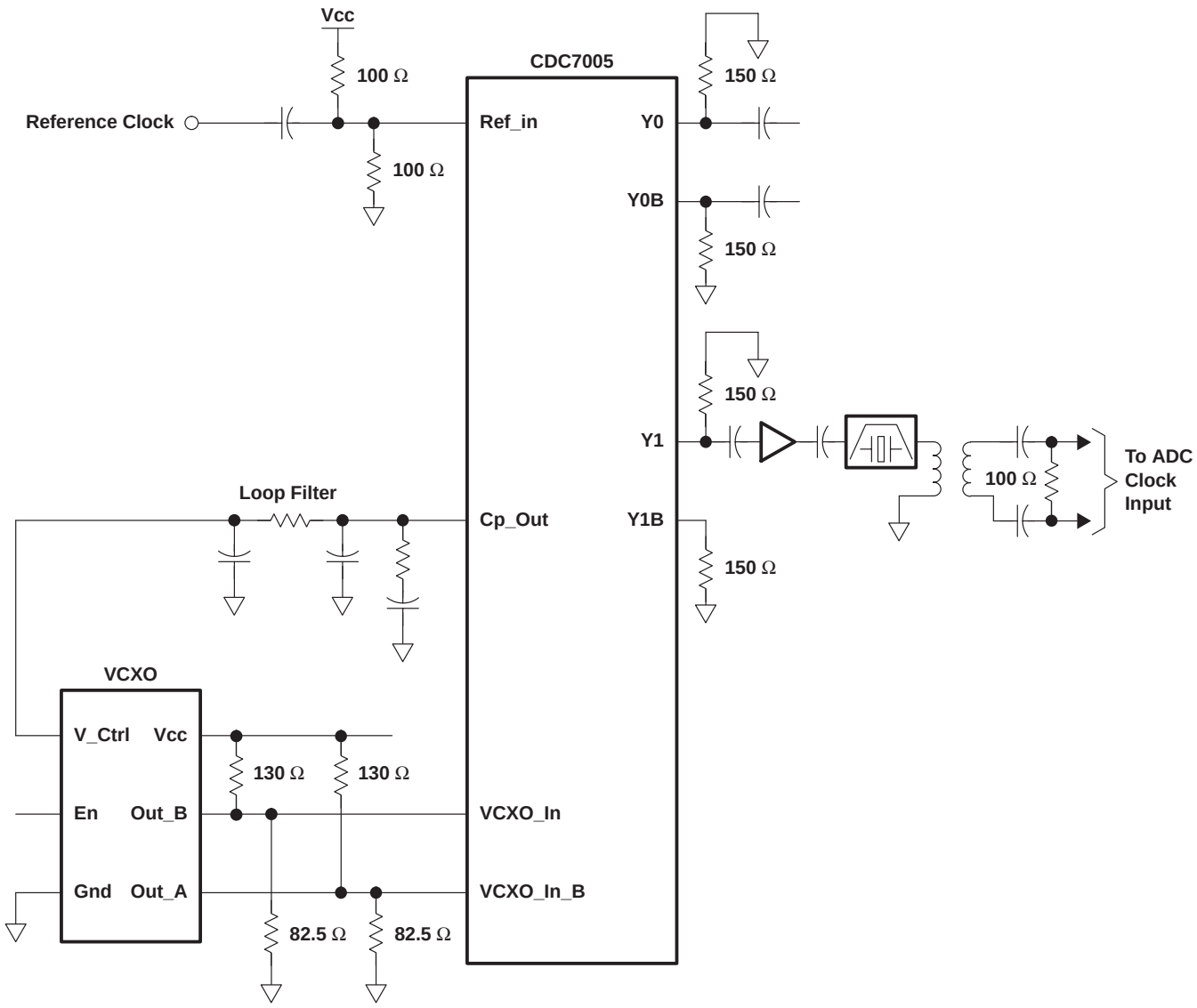

Figure 19. CDC7005 Clocking Topology With An Amplifier and Filter

The ADS5500 device is measured using the CDC7005 with PECL VCXO and the amplifier-filter output network. The performance is measured over higher IF input signals and the results are shown in Table 2.

Table 2. SNR and SFDR Comparisons With A Modified Clock Solution

	SNR [dBFS]			SFDR [dBc]		
Freq. [MHz]	**Baseline**	**CDC7005**	**CDC7005−Amp−BPF**	**Baseline**	**CDC7005**	**CDC7005−Amp BPF**
65	72.6	70.9	72.5	77.9	80.4	80.6
100	72.2	68.8	71.9	84.0	84.1	86.1
150	70.8	66.3	71.0	76.7	79.8	77.1
190	70.1	64.9	70.2	74.1	74.0	74.9

Figure 20 compares the result of the device measured with the near-ideal clock, the CDC7005 clock, and the CDC7005 clock incorporating the amplifier-filter modification.

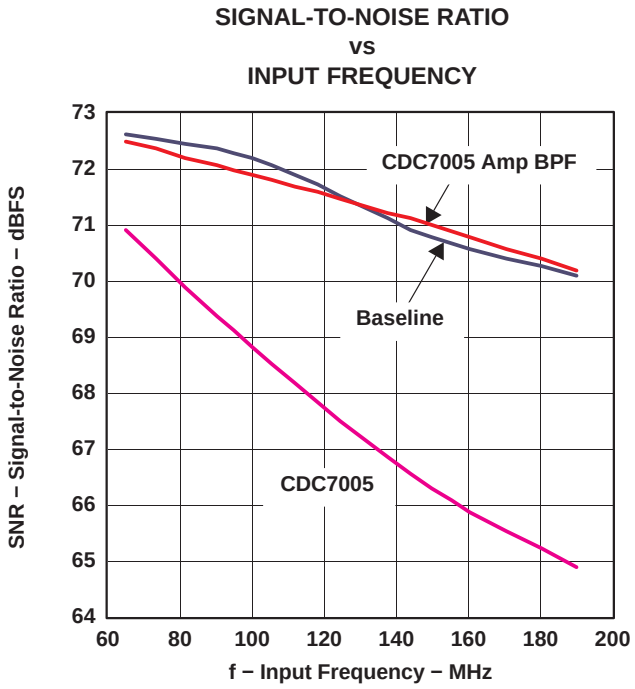

Figure 20. SNR Response With Improved Clocking Topology

Utilizing the amplifier-filter combination improves SNR performance up to 5 dB at high IF frequencies and closely matches the baseline performance. SNR performance around 70 dBFS or greater is achievable up to 190-MHz IF. The spectral plot of the performance at 190-MHz IF is shown in Figure 21.

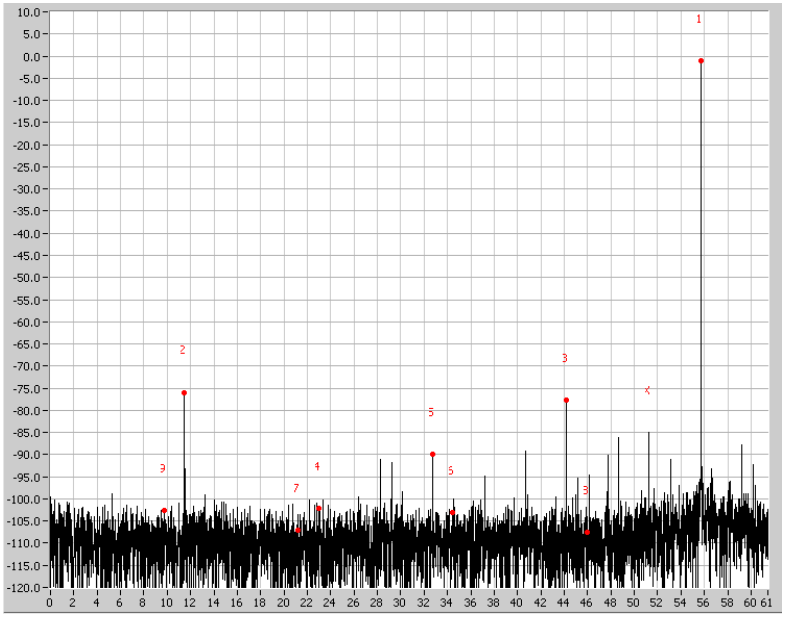

Figure 21. Spectral Plot With CDC7005 Clock Plus Amplifier−BPF at 190-MHz IF Input

Additional measurements were taken on a different ADC series component to verify the clocking performance of the CDC7005 coupled with an amplifier and a filter. The ADS5553, a dual 14-bit, 80-MSPS device was testing using a CDC7005 outfitted with a 122.88-MHz VCXO. The output frequency was divided by two to 61.44 MHz. The baseline measurement and the CDC7005 solution are shown in Figure 22.

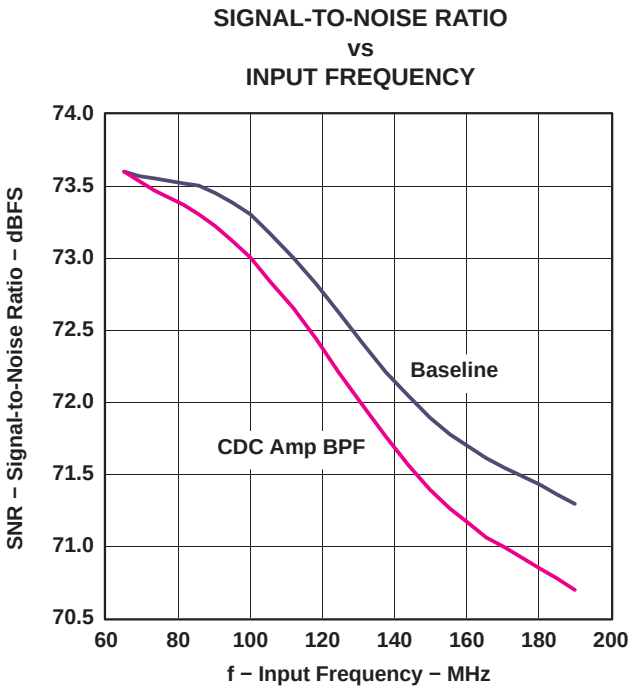

Figure 22. ADS5553 SNR Performance Over Input Frequency With New CDC7005 Clock Topology

The results show that for this device the improved topology yields SNR results that are within 0.5 dB of anticipated baseline values.

8 Conclusion

The CDC7005 device is a clock distribution chip that satisfies the most stringent clocking requirements for high-end ADCs such as the ADS5500. For applications with the input frequency at or below the first Nyquist zone, the CDC7005 is a suitable clock for the ADC device to achieve excellent performance. For applications requiring a high IF input frequency, the performance degrades in a linear fashion with respect to frequency. This degradation can be eliminated by including a narrow band filter, such as a crystal band-pass filter, on the output of the CDC7005 along with an amplifier to ensure sufficient clock amplitude. With this technique, near-ideal ADC performance is achievable with any desired IF frequency. Further, this technique provides an inexpensive real-world solution for clocking high speed ADCs at high IF frequencies. Additionally, the CDC7005 can supply the clock signal, not only to the ADCs, but also all the other clocking devices within the design.

9 References

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