Application Report
SNAA002E–September 1999–Revised May 2013

AN-1125 Laminate CSP/FBGA

ABSTRACT

Laminate substrate based CSPs at TI have been in production for over three years. Texas Instruments has shipped over 300 millions units of the CSP to the wireless industry and has offered both the land grid array (LGA) as well as the fine pitch ball grid array (FBGA) for the CSP. This is the package choice for portable and wireless applications.

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1 Introduction

1.1 Chip Scale Packages

The laminate CSP has passed the reliability test requirements for the wireless application. The solder joint reliability for both laminate LGA and FBGA have passed over 1000 temperature cycles (−40° C to 125° C) without any solder joint failures.

1.2 Applications

Applications include portable applications, including cellular phone, wireless, lap top computers, DSPs, and others.

1.3 CSP Features

The CSP strategy is to leverage the map area array process (MAP) to deliver the smallest, thinnest, cheapest and reliable package solutions. The CSP features are as follows

- Light weight
- Wide range of pin counts (16 to 192 Leads)
- Moisture Resistance JEDEC Level 1, 2 & 3 mostly
- Enhanced Electrical Performance > 2.4 GHz
- JEDEC: MO-208 for P-TFQFN, MO-209 for P-TSSON, MO-205 for LFBGA

1.4 Thermal Characteristics

Thermal performance is measured using a low, effective thermal conductivity test board fabricated per EIA/JESD51-3. Results are shown in Table 1.

Table 1. Thermal Performance of CSP/FBGA

Package	Body Size (mm)	Die Size (mm)	θ j-a (°C/Watt)
Laminate CSP-16 (TFQFN)	3.5 x 3.5 x 1.0	0.84 x 1.49	130
Laminate CSP-24 (TFQFN)	4.5 x 3.5 x 1.0	1.82 x 1.33	112
Laminate CSP-28 (TFQFN)	4.5 x 5.5 x 1.0	3.03 x 1.82	72
Laminate CSP-48 (TSSON)	12.5 x 8.1 x 1.0	5.23 x 3.71	39 (1)
Laminate CSP-128 (TFQFN)	10 x 10 x 1.0	3.68 x 3.45	72 (2)
FBGA-48	7 x 7 x 1.4	2.54 x 2.54	85
FBGA-64	8 x 8x 1.4	3.00 x 1.80	61
FBGA-100	10 x 10 x 1.4	10 x 10	35

(1) with thermal pads
(2) Simulated data

1.5 Reliability

The realiability features are as follows:

- Moisture Sensitivity
  - 16/20/24 (0.6mm ultra thin) CSP: MSL 1 (85° C/85%RH - 168hrs)
    - Floor life: 30° C/60%RH for unlimited
  - 16/20/24/28 CSP: MSL2 (85° C/60%RH - 168hrs)
    - Floor life: 30° C/60%RH for 1 year
  - 40/48/176L CSP & 81/100/192L FBGA: MSL3 (30° C/60%RH - 336hrs)
    - Floor life: 30° C/60%RH for 168hrs
- Characterization: 30°C/60% RH, 336 Hours Soak
- Autoclave: 121°C, 100% RH, 15 psi, 96 Hours

- Temperature Cycle: - 40°C to 125°C, 1000 Cycles
- Dynamic OP Life: 125°C, 1000 Hours
- Temp. Humidity Bias Test: 85°C/85% RH, 1000 Hours

2 CSP/FBGA Offering List

The package offering for CSP and FBGA are shown in Table 2 and Table 3.

Table 2. Package Offering - Laminate CSP

Pin Count	Body Size (mm)	Pitch (mm)	Max. Die Size (mm)	Marketing Drawing	MBS AD#	235°C Reflow	260°C Reflow
16	3.5 x 3.5 x 1.0	0.5	1.73 x 1.73	SLB16A	SLB016AA	MSL2	MSL3
20	3.5 x 3.5 x 1.0	0.5	1.73 x 1.73	SLB20B	SLB020AA	MSL2	MSL3
20	3.5 x 3.5 x 0.8	0.5	1.73 x 1.73	SLD20A	SLD020AA	MSL1	MSL2, MSL1(1)
20	3.5 x 3.5 x 0.6	0.5	1.73 x 1.73	SLE20A	SLE020AA	MSL1	MSL2, MSL1(1)
24	3.5 x 4.5 x 1.0	0.5	1.68 x 2.69	SLB24A	SLB024AA	MSL2	MSL3
24	3.5 x 4.5 x 0.8	0.5	1.68 x 2.69	SLD24A	SLD024AA	MSL1	MSL2, MSL1(1)
24	3.5 x 4.5 x 0.6	0.5	1.68 x 2.69	SLE24A	SLE024AA	MSL1	MSL2, MSL1(1)
24	3.5 x 4.5 x 0.6 (Ldap)	0.5	1.79 x 2.79	SLE24A	SLE024AB	MSL1	MSL2, MSL1(1)
28	4.5 x 5.5 x 1.0	0.5	2.69 x 3.68	SLB28A	SLB028AA	MSL2	MSL3
32	4.5 x 5.5 x 0.8	0.5	2.69 x 3.68	SLD32A	SLD032AA	MSL2	MSL3
40	5.5 x 6.5 x 1.0	0.5	3.63 x 4.65	SLB40B	SLB040AB	MSL3	N/A
40	5.5 x 6.5 x 1.0 custom	0.5	3.63 x 3.84	SLB40A	SLB040AA	MSL3	N/A
48	7.0 x 7.0 x 1.0	0.5	4.93 x 4.93	SLB48B	SLB048AB	MSL3	N/A
48	8.1 x 12.5 x 1.0	0.5	5.89 x 6.17	SLB48A	SLB048AA	MSL4	N/A
128	10.0 x 10.0 x 1.0, DR	0.5	6.13 x 6.13	SLB128A	SLB128AA	MSL4	N/A
128	10.0 x 10.0 x 1.0, TV	0.5	7.88 x 7.88	SLB128B	SLB128AB	MSL4	N/A
128	10.0 x 10.0 x 1.0, Inline	0.5	7.88 x 7.88	SLB128A	SLB128AA	MSL4	N/A
176	13.0 x 13.0 x 1.0	0.5	9.09 x 9.09	SLB176A	SLB176AA	MSL3	N/A

(1) JEDEC standard.

Table 3. Package Offering - FBGA

Pin Count	Body Size (mm)	Pitch (mm)	Max. Die Size (mm)	Marketing Drawing	MBS AD#	235°C Reflow	260°C Reflow
49	7.0 x 7.0 x 1.4	0.8	5.49 x 5.59	SLC49A	SLC049AC	MSL3	MSL4
64	8.0 x 8.0 x 1.4	0.8	5.40 x 5.40	SLC64A	SLC064AC	MSL3	MSL4
81	9.0 x 9.0 x 1.4	0.8	5.13 x 5.13	SLC81A	SLC081AA	MSL3	MSL4
100	10.0 x 10.0 x 1.4	0.8	6.88 x 6.88	SLC100A	SLC100AA	MSL3	MSL4
176	13.0 x 13.0 x 1.4	0.8	9.87 x 9.87	SLC176A	SLC176AA	MSL3	N/A
192	14.0 x 14.0 x 1.4	0.8	10.87 x 10.87	SLC192A	SLC196AA	MSL3	N/A

3 CSP Cross Section

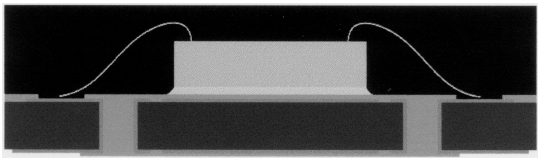


Figure 1. Cross Section View for 24-Lead Laminate CSP

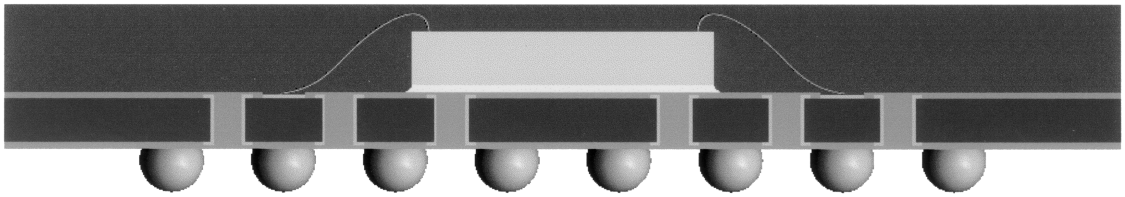
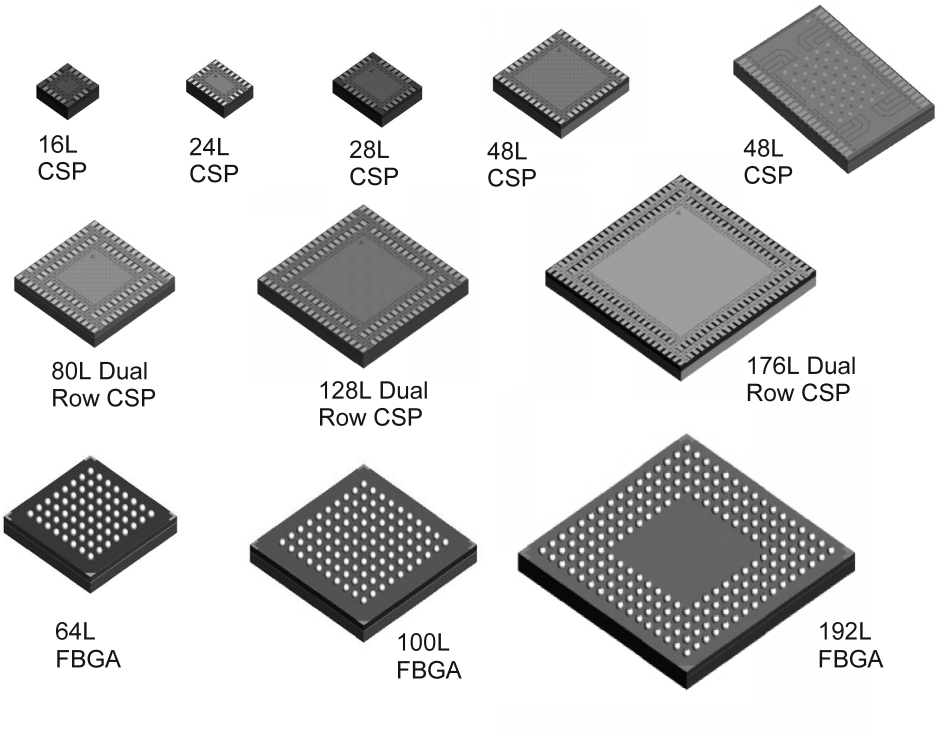
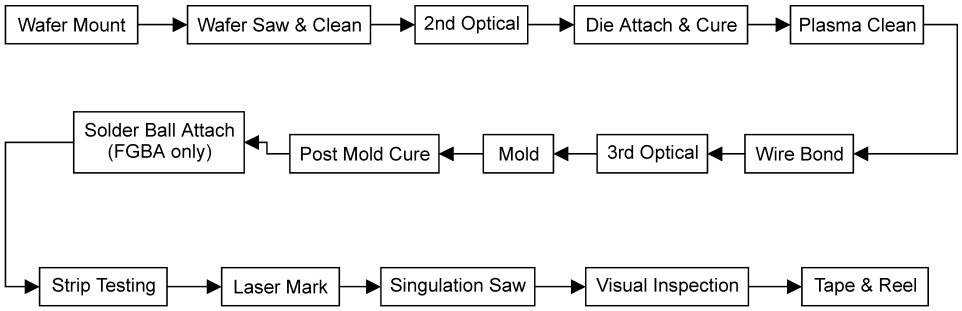


Figure 2. Cross Section View for 64-Lead CSP (FBGA)

4 CSP & FBGA Packages



5 Standard Process Flow



6 Material Properties

Table 4. Laminate CSP/FBGA

Item	Solder Resist	Mold Compound	Die Attach	Substrate	Solder Ball (FBGA)
	Taiyo PSR4000-AUS5	Nitto HC-100-X2 & HC-100 XJA	QMI506	MGC CCL-HC832 & CCL-HC832HS	63Sn/ 37Pb
Glass Transition Temperature Tg (°C)	104	160/165	-19	190/215	183 melting temp
Coefficient thermal expansion (ppm/°C)	16 (< Tg) 210 (> Tg)	7 (> Tg) 30 (>Tg)	57 (< Tg) 139 (> Tg)	X: 14/15 Y: 14/15 Z: 58/45	24.7 (15 -110 °C)
Elastic modulus (Kg/mm2)	N/A	2540/2700	6300	2140-2550/ 2500-2600	N/A
Thermal Conductivity (W/m-K)	0.26	0.97	0.9	0.34/0.50	50

7 Design Guidelines

Over the last few years, design guidelines for laminate CSP have in response to the high demand for smaller packages with larger die. Figure 3 shows the most recent update to laminate CSP design.

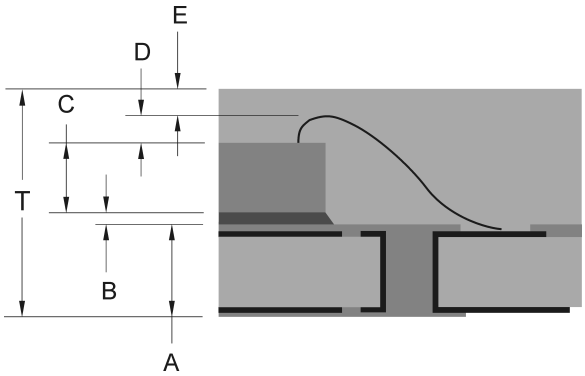


Figure 3. General design specification for laminate CSP.

		Current CSP		Thin CSP			
		(mm)	(mils)	(mm)	(mils)	(mm)	(mils)
T	Package Thickness	1.0	40.0	0.8	31.5	0.6	23.6

		Current CSP		Thin CSP			
		(mm)	(mils)	(mm)	(mils)	(mm)	(mils)
A	Substrate	0.36	14.2	0.20	7.9	0.20	7.9
B	Bondline	0.02	0.5	0.02	0.5	0.02	0.5
C	Die	0.25	10.0	0.25	10.0	0.20	8.0
D	Loop Height	0.18	7.0	0.18	7.0	0.10	4.0
E	Clearance	0.25	10.2	0.15	6.1	0.08	3.2
F	Mold Cap	0.70	27.6	0.60	23.6	0.40	15.7

8 Package Reliability Data

8.1 Precondition

Preconditioning testing is carried out to simulate product shipping, storag,e and surface mount assembly operations. Packages are subjected to the following preconditioning sequence per J-STD-020.

1. C-SAM
2. Temperature cycle: 5 cycles at −40°C to 60°C
3. Bake: 16 hours at 125°C
4. Soaking (specific condition is listed in the Section 1.5 section of the Introduction.)
5. IR reflow
   - 4X - 240° C peak (≤ 28L CSP)
   - 3X - 240°C peak (> 28L CSP)
6. Flux immersion and clean.
7. C-SAM

8.2 Reliability Test Conditions - Three Lots Each

- TMCL: −40° to 125° C for 1000 cycles
- DOPL: 125° C for 1000 hrs
- THBT: 85° C/85% RH for 1000 hrs
- ACLV: 121° C, 100% RH, 15 psi for 96 hrs

9 Application Notes

9.1 Printed Circuit Board (PCB) Layout Guidelines

Two types of land patterns are used for surface mount packages: (1) solder mask defined (SMD) pads that have the solder mask opening smaller than metal pad and (2) non-solder mask defined (NSMD) pads that have the metal pad smaller than the solder mask opening. Figure 4 and Figure 5 illustrate the two types of pad geometry.

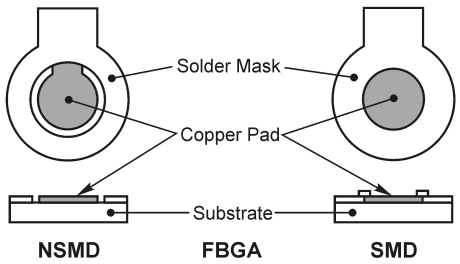


Figure 4. Comparison of NSMD and SMD pads (FBGA)

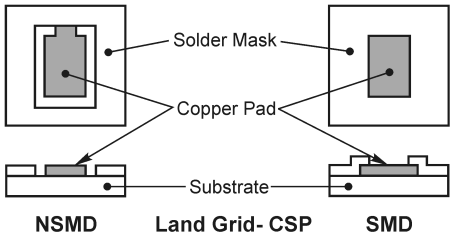


Figure 5. Comparison of NSMD and SMD pads (Laminate CSP)

NSMD definition is preferred due to tighter control of the copper artwork registration compared to that of the solder masking process. Moreover, SMD pad definition can introduce stress concentration points near the solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions. The smaller size of copper pad in the case of the NSMD definition facilitates escape routing on the PCB.

For optimal CSP board reliability, it is recommended to have a 1:1 ratio between the package pad and the PCB pad size. For example, the pad on the peripheral land packages is 0.45mm x 0.30mm, this translates to a 0.45mm x 0.30mm copper pad on the PCB. For package with thermal pads, the PCB board design should match with the package footprint and the thermal pad footprint. Thermal pads are designed to dissipate heat through the GND plane in the PCB board. The vias location for the thermal pads is depending on the via size used for the PCB. For most cell phone application, the build up via (~100 to150 um) is used for via in pad design. For lap top application, larger via (~200 to 250 um) is used between the thermal pads. Via plugging using solder mask is necessary to prevent shorting of pads to the via. The number of vias for the PCB board should be maximized to facilitate the heat dissipation.

A 1: 0.8 ratio is recommended for the FBGA between the package pad and the PCB pad size (to facilitate routing between pads in the area array package). For NSMD pads it is necessary to have a clearance around the copper pad and the solder mask to account for mask registration tolerances (typically ±0.075 mm or 3 mils) and to void any overlap between solder joint and the solder mask. The PCB layout assumes a 0.100 mm (4 mil) wide trace and a 0.5 oz. Copper foil. The recommended ball pad on the PCB is 0.33 mm and solder mask opening is 0.48 mm.

Although, a majority of board level characterization is performed using a PCB with organic solderability preservative coating (OSP) finish, no significant impact of PCB pad finish is observed with the assembly and reliability of either the Laminate CSP or the FBGA. A uniform coating thickness is key for high assembly yield. For an electroplated nickel-immersion gold finish, the gold thickness must be less than 0.5µm to avoid solder joint embrittlement.

9.2 Package to Board Assembly

9.2.1 Surface Mount Considerations

Th lLaminate CSP and FBGA surface mount assembly operations include screen printing solder paste on the PCB, package placement using standard SMT placement equipment, reflow and cleaning (depending on flux type), and packaging handling during assembly.

9.2.2 Stencil Printing Solder Paste

The solder paste is stencil printed onto the board, which involves transferring the solder paste through pre-defined apertures by the application of pressure. Stencil parameters such as aperture area ratio or aspect ratio and fabrication process have significant impact on volume of paste deposited onto the pad. The aperture area ratio is defined as the ratio of stencil aperture cross-section to the aperture wall area. The aspect ratio is defined as the ratio of stencil aperture diameter to the height of the aperture. To obtain the desired solder paste transfer, an area ratio of ≥ 0.66 or an aspect ratio of ≥ 1.5 are recommended. Inspection of the stencil prior to placement of the packages is highly recommended as part of a quality program to improve board assembly yields.

Two typical stencil fabrication methods include laser cut and metal additive processes. Nickel-plated, electropolished laser cut stencils with 5° tapered of aperture walls to facilitate paste release is recommended. For peripheral packages with 0.45 mm x 0.30mm pad size, the following optimized stencil is recommended by TI, as shown in Figure 6.

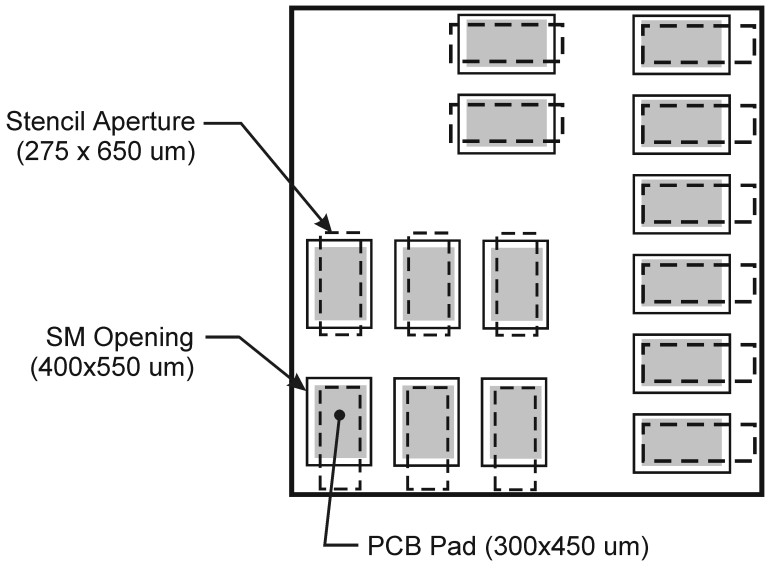


Figure 6. Stencil Design Guidlines

Method of Manufacture	Surface Finish	Stencil Thickness	Aperture Size	Wall Taper
Laser Cut	Electro Polished	125 micron	275 x 650 micron	5°

One of the most critical processes is the consistent solder paste printing. Overprinting is required to obtain maximum solder joint height and volume. Uneven printing volume or tailing of solder paste could result in shorting after reflow. Insufficient solder paste causes insufficient solder joint after reflow. On the other hand, too much solder causes bridging and solder beading after reflow.

For FBGAs the recommended aperture size is 0.1mm larger than the pad size to allow 2 mils or 50 micron overprinting on each side. Example: PCB pad is 0.33 for FBGA package. This will translate to a 0.43 mm aperture on a 0.125mm thick stencil.

Type 3 mesh solder paste is acceptable for applying the solder paste. To avoid drying out the paste follow the handling guidelines recommended by the paste supplier.

9.2.3 Part Placement

Laminate CSP and FBGA packages are placed using standard pick & place equipment with ±0.050mm (± 2 mil) placement accuracy, shown in Figure 7. Package pick and place systems comprise of a vision system to recognize and position the component and a mechanical system to physically perform the pick and place operation. Two commonly used types of vision systems for area array packages are (1) a vision system that locates package outline, and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type often renders more accurate placement but tends to be more expensive and time consuming. A misalignment of 50% of the ball size is tolerable for the FBGA. The Laminate CSP has a ±0.250mm (±10 mil) pad spacing, so the ±0.050mm (± 2 mil) placement accuracy of pick & place equipment is more than acceptable.

Placement in Z direction is 1 to 2 mil into the solder paste with a force of 150 gf or 3N maximum.

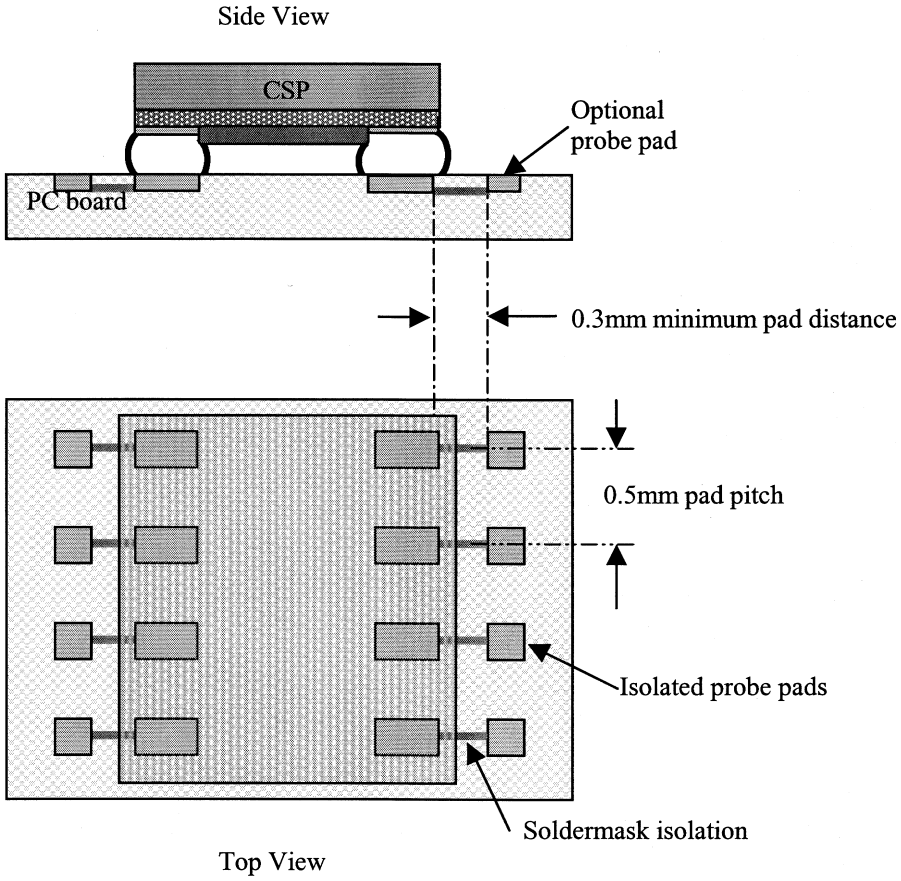


Figure 7. Recommended part placement for Laminate CSP

9.2.4 Solder Paste Reflow & Cleaning

The Laminate CSP and FBGA are assembled using standard SMT reflow processes without any special considerations. Both packages are qualified up to three reflow operations (J-STD-020), excepting for low pin count (≤ 24L) CSP which are qualified up to four reflow passes. Recommended peak reflow temperature is 235° C for the Laminate CSP (< 6mm x 6mm) and 220° C for the FBGA. A typical reflow profile is shown in Figure 8. The actual temperature of the CSP is a function of component density, component location on the board, and size of surrounding components. If necessary, it is recommended that the temperature profile be checked at various locations on the board.

In some applications, a subcontractor reflows the CSPs on a module. The module is reflowed by an OEM to the systems board. In such cases, the component will experience up to five solder reflow operations. The SMT subcontractor is in control of handling and is responsible for guaranteeing the integrity of the CSP. If MSL3 FBGA are out of the dry bag and exposed to 30° C/60% RH environment exceeding 168 hours, baking is required. The recommended baking condition is 125° C for 12 hours minimum.

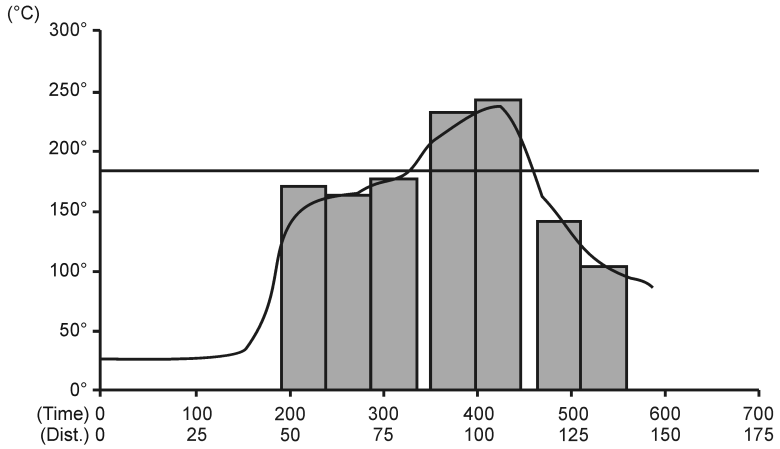


Figure 8. Typical Reflow Profile for Laminate CSP

Zone	1	2	3	4	5	6	7
Top	170° C	165° C	180° C	223° C	256° C	140° C	105° C
Bottom	170° C	165° C	180° C	223° C	256° C	140° C	105° C
Conveyor Speed: 15 in/min, Peak Temp: 235° C, Dwell >183° C: 45-75 sec.							

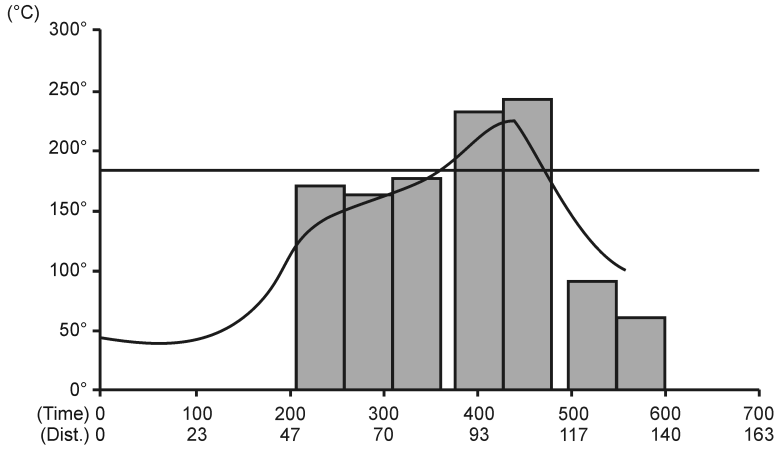


Figure 9. Typical Reflow Profile for FBGA

Zone	1	2	3	4	5	6	7
Top	170° C	160° C	183° C	240° C	255° C	90° C	60° C
Bottom	170° C	160° C	183° C	240° C	255° C	90° C	60° C
Conveyor Speed: 14 in/min, Peak Temp: 220° C, Dwell >183° C: 45-75 sec.							

9.2.5 Double-Sided Process

The double-sided process follows the same procedure as the single-sided process: mount and reflow the packages on one side and simply turn over the board and repeat the process.

9.2.6 Packaging Handling

Standard tape and reel or tray shipping media facilitates package handling during assembly. Handling during board level assembly requires the typical precautions associated with BGA packages (Reference J-STD-013). The Laminate CSP and FBGA packages are compatible with automated pick and place systems. Manual handling of the packages using a vacuum wand or a non-metallic tweezers requires the appropriate ESD protection.

10 Component Rework Procedures

10.1 CSP and FBGA Rework Overview

Removing the Laminate CSP and FBGA from PCB involves heating solder joints above liquidus temperature of eutectic solder using a vacuum gas nozzle. Bake PC board with CSP/FBGA at 125°C for 12 hours minimum prior to any rework. This will remove any residue moisture within the part preventing moisture induced cracking during the demount process. A 1.27 mm (50 mil) keep out zone for adjacent components, including discretes, is recommended for standard rework processing. If adjacent components are closer than 1.27 mm, custom tools will be required for package rework and removal. The rework area can be preheated to 100°C and the custom tool can hold the CSP and FBGA to achieve a 0.5 mm (20 mils) keep out zone.

Ramp rates and thermal profiles must be controlled to minimize damage to surrounding the components. A± 5° C gradient across the heating zone is recommended. Preheating the PCB to a certain temperature (a uniform and reliable board temperature of 100° C is suggested) before heating the CSP will insure a controlled process. Above the liquidus temperature, the nozzle vacuum is automatically activated and the component is picked up. After removing the CSP, the pads may be heated using the same vacuum gas nozzle to reflow any residual solder, which is removed using a Teflon tipped vacuum wand. For component replacement, no-clean flux is applied to the reworked site, and the component is placed, reflowed, inspected, and electrically tested.

10.2 Rework SYstems

The rework systems are available from many suppliers. The following suppliers have produced the BGA/CSP rework stations: METCAL, Austin American Technology (AAT), Air-Vac, Conceptronic, Manix Manufacturing, PACE, Semiconductor Equipment Corp. (SEC), and Sierra Research and Technology (SRT). The heat source for the rework station is based on hot gas, focus IR or thermode. The component removal and attachment method is done with vacuum pick-up tool.

The quality of the rework can be controlled by:

1. Direct the thermal energy through the component body to solder without over heating the adjacent components.
2. Heating should ideally take place in an encapsulated , inert, gas-purged environment, where temperature gradients do not exceed ±5° C across the heating zone.
3. Use of a convective bottom side pre-heater will maximize temperature uniformity for the top and bottom side of the temperature gradients.
4. Use the interchangeable nozzles designed with different geometries to accommodate different applications to direct the airflow path.

10.3 Temperature Calibration

Due to the tight space constraint and minimum stand off height for most CSP and FBGA, it is difficult to mount the thermal couple between the space of the CSP and PCB. If possible, a small hole (just a little lager than the thermal couple), can be drilled into the PCB and the thermal couple can be mounted at the interface between the CSP and PCB for calibration.

A rework solder screen process for Texas Instruments' 176L CSP with METCAL rework station is illustrated in Figure 10 and Figure 11.

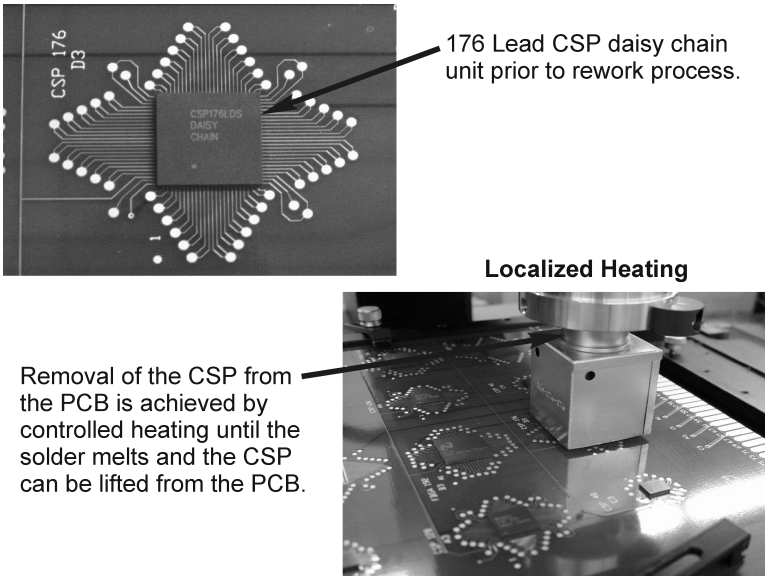


Figure 10. Removing Component from the PCB.

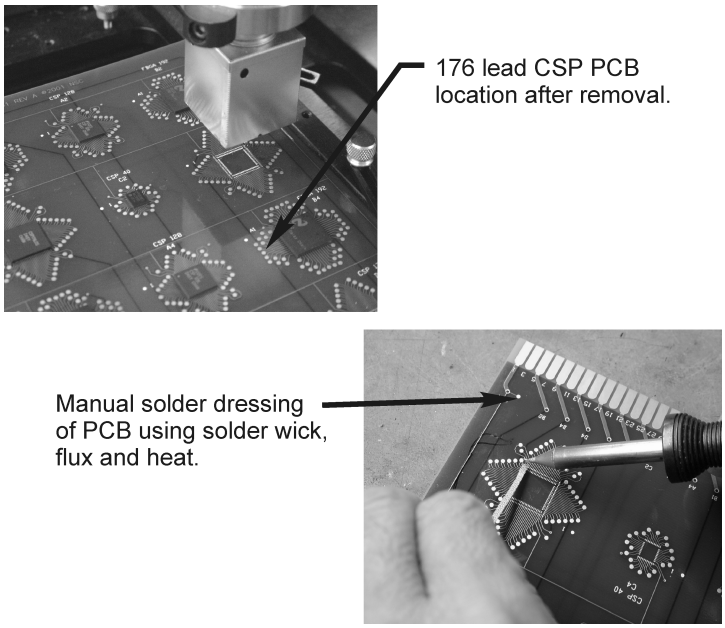


Figure 11. Dressing PCB Footprint for New CSP

10.4 Site Preparation

Once the CSP/FBGA is removed from the PCB board, the site must be cleaned to prepare for package attachment. Care must be taken to avoid burn, lift-off or damaging the attachment area. The best results will be achieved with a low-temperature, blade-style conductive tool matching the foot print area of the CSP, in conjunction with a de-soldering braid. No clean flux is recommended throughout the entire rework process.

10.5 Solder Bump Screen Printing Deposition

The FBGA has solder balls at the bottom, and no additional solder bumping is needed. The TI CSP is a land grid array package. Solder bumping or solder paste screen printing on the package is needed prior to fluxing and component placement. The solder bump on the CSP package can be created by manual solder ball attachment with a 0.45mm diameter solder ball as shown in Figure 12. Prior to CSP ball attachment, bake CSP at 125°C for 12 hours minimum to remove any residual moisture, if not kept in a sealed dry bag. A water-soluble flux is preferred for the solder bumping process.

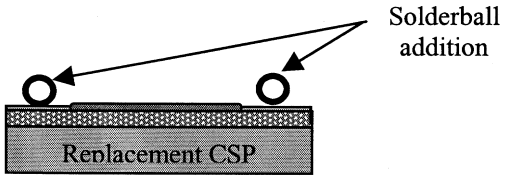


Figure 12. Ball Attachment to Replacement CSP Prior to PCB Mounting

After the solder bumping process, the CSP should be cleaned with DI water to remove the flux residuals. Baking is needed after flux cleaning. The recommended baking condition is 125°C for 12 hours minimum.

Figure 13 shows the pretinned replacement CSP and PCB prior to reattachment. It is important to remove any residual moisture prior to reattachment (bake at 125°C for 12 hours if necessary).

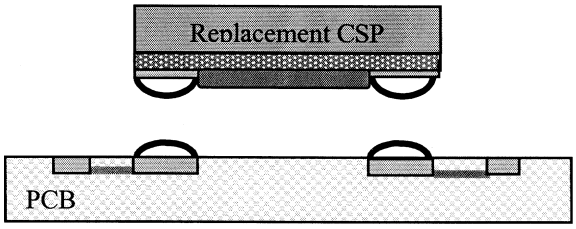


Figure 13. CSP Replacement Part with Solder Ball Addition Prior to Reattachment on PCB

Solder paste screen printing is another rework method to attach the CSP component onto the PCB by using a specialized rework fixture and solder paste template (stencil), shown in Figure 14 and Figure 15. The recommended stencil aperture is shown in Figure 6 above. The solder paste is applied to the fixture. Then, the CSP package is aligned to the fixture to provide accurate paste placement.

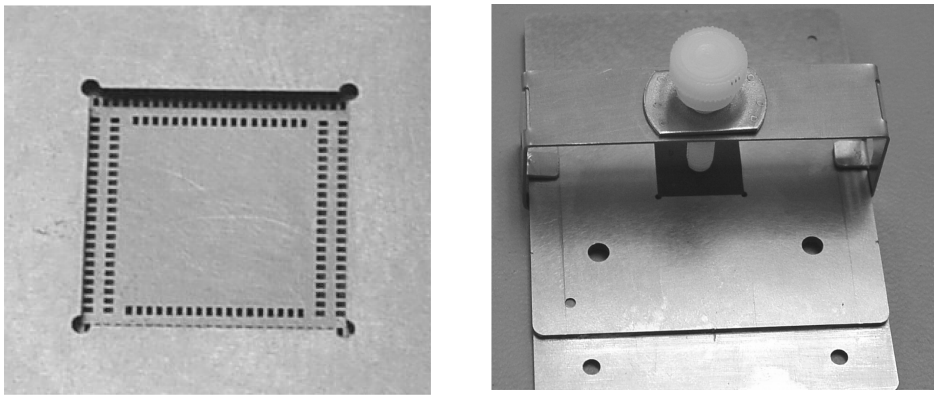


Figure 14. Rework Fixture and Rework Stencil for 176L CSP

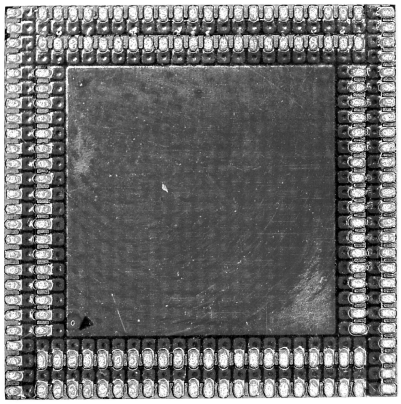


Figure 15. Solder Paste Deposition on 176L CSP

The water-soluble flux is preferred for solder bumping and screen printing processes. After the solder bumping or screen printing process, the CSP should be cleaned with DI water to remove the flux residuals. Baking is needed after the flux cleaning. The recommended baking condition is 125° C for 12 hours minimum.

10.6 Component Placement

Most CSP rework stations will have a pick and place feature for accurate placement alignment. Manual pick and place with eye-ball alignment will be difficult or impossible to achieve consistent placement accuracy. The self-alignment feature for the TI CSP and FBGA will correct the placement error.

Prior to placing the component, the site must be clean with solvent to remove any surface contamination and oxide. A split-beam optical system with 50 -100X magnification for component alignment should be used, illustrated in Figure 16. For CSP, the mini stencil with a squeegee of the same width as stencil should be used, and the aperture should be aligned with pads under 50-100X magnification before paste printing. The placement machine, shown in Figure 17, should allow fine adjustments in X, Y, and θ, and the profiles developed during initial placement can be used for rework.

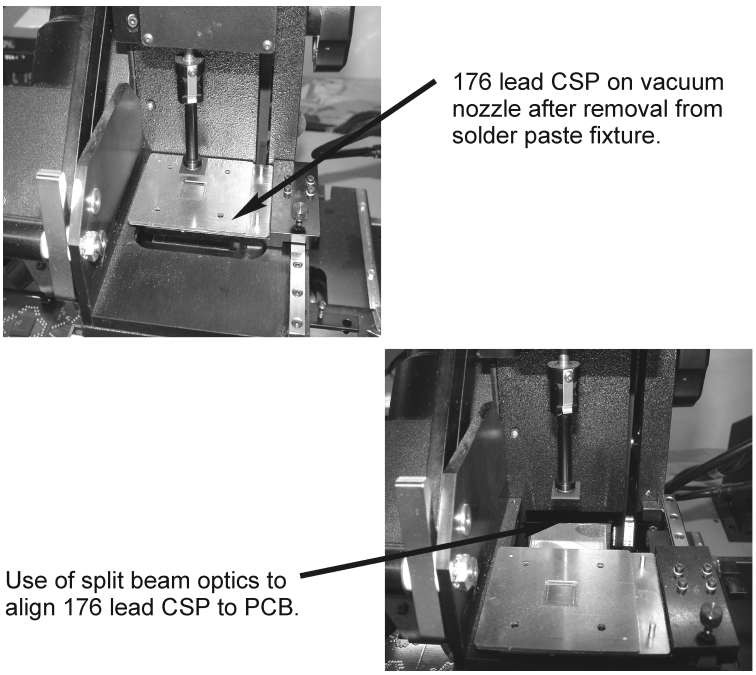


Figure 16. Component Alignment.

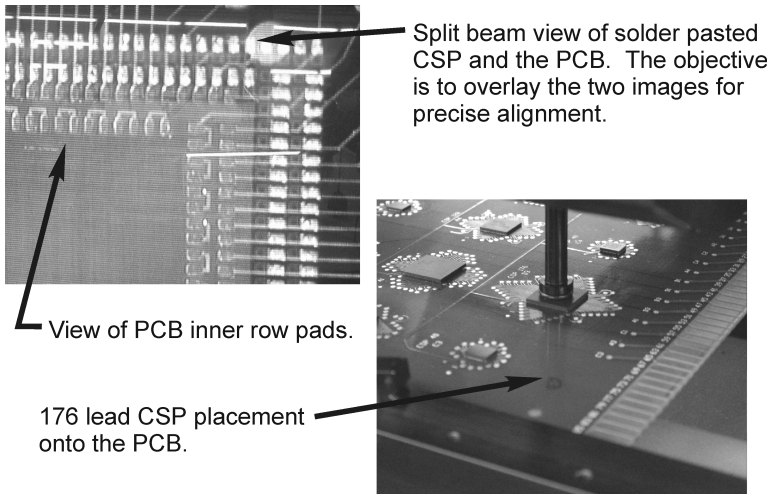


Figure 17. Component Placement.

10.7 Reflow Profile

After placing component on the board, reflow using the standard reflow profile as recommended, shown in Figure 18.

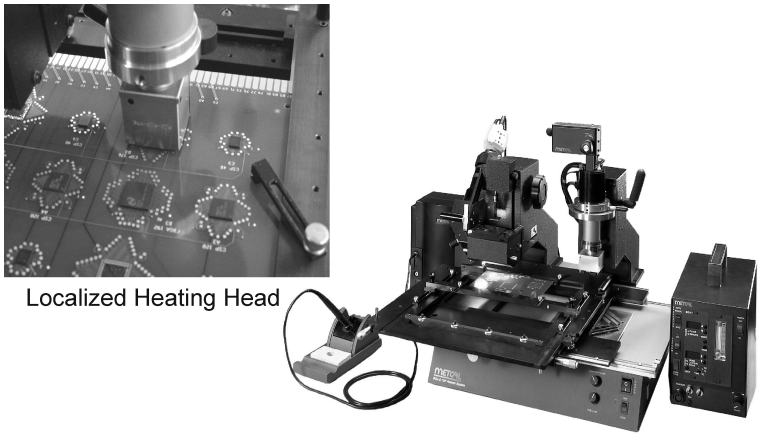


Figure 18. Localized Solder Reflow

10.8 Inspection

After surface mount assembly, solder joints can be inspected using transmission X-ray to identify defects such as bridging, shorts, opens, and voids. A typical X-ray photograph after assembly is shown in Figure 19.

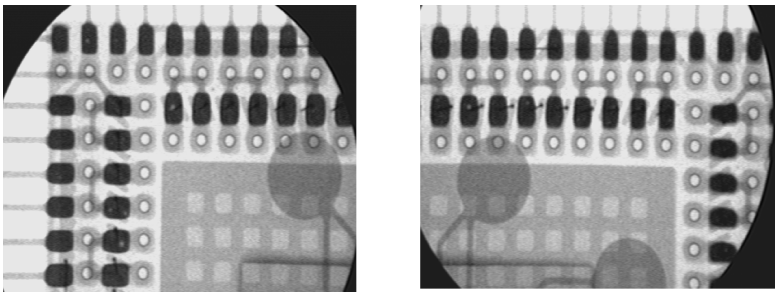


Figure 19. X-ray Inspection of 176L CSP

11 Solder Joint Reliability

11.1 Temperature Cycling Tests

Solder joint reliability is available for the 16/24/28/40/128/176L laminate CSP and the 64/100/192/256L FBGA.

- 4 Layer, FR-4, Tg > 130° C, OSP Surface Finish
- Thickness: 20 & 62 mils

The board level reliability is evaluated using the following temperature cycle conditions:

- TC: −40 to 125° C, single zone, one hour temperature cycling with 15 minutes each for ramps and dwells (IPC-SM-785), shown in Figure 20.

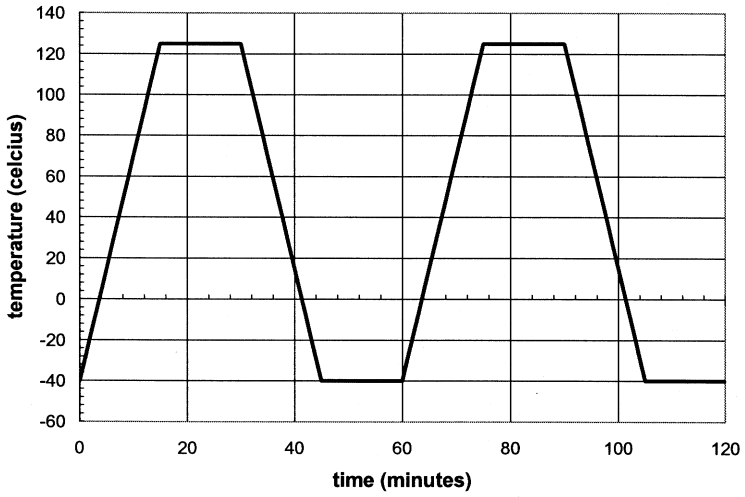


Figure 20. Temperature Cycle Test Condition Profile

Table 5. Solder Joint Reliability Results of CSP and FBGA Package:

PKG	Sample Size	Die Size (mm)	Board Thickness (mm)	Pad Size (mm)	First Fail (Cycle)	50% Failure Rate (Cycles)
16L CSP	39	1.47 x 1.47	1.6	0.25 x 0.45	1600	1942
24L CSP	43	1.43 x 2.43	1.6	0.25 x 0.45	1576	1768
28L CSP	39	2.43 x 3.43	1.6	0.25 x 0.45	1664	N/A
28L CSP	48	2.43 x 3.43	1.6	0.3 x 0.45	>2100	N/A
40L CSP	32	3.38 x 4.39	1.6	0.3 x 0.45	>3500	N/A
48L CSP	48	5.05 x 5.05	1.6	0.3 x 0.45	>2100	N/A

Table 5. Solder Joint Reliability Results of CSP and FBGA Package: (continued)

PKG	Sample Size	Die Size (mm)	Board Thickness (mm)	Pad Size (mm)	First Fail (Cycle)	50% Failure Rate (Cycles)
128L CSP	32	6.2 x 5.8	1.6	0.3 x 0.45	1412	1757
176L CSP	32	6.0 x 6.0	1.6	0.3 x 0.45	1507	1831
64L FBGA	32	3.2 x 3.2	0.8	0.33 Dia.	1823	N/A
100L FBGA	32	8.2 x 8.2	0.8	0.33 Dia.	1143	N/A
192L FBGA	32	10.0 x 10.0	1.6	.04 Dia.	1050	1278
256L FBGA	48	12.0 x 12.0	1.6	0.40 Dia.	805	1207

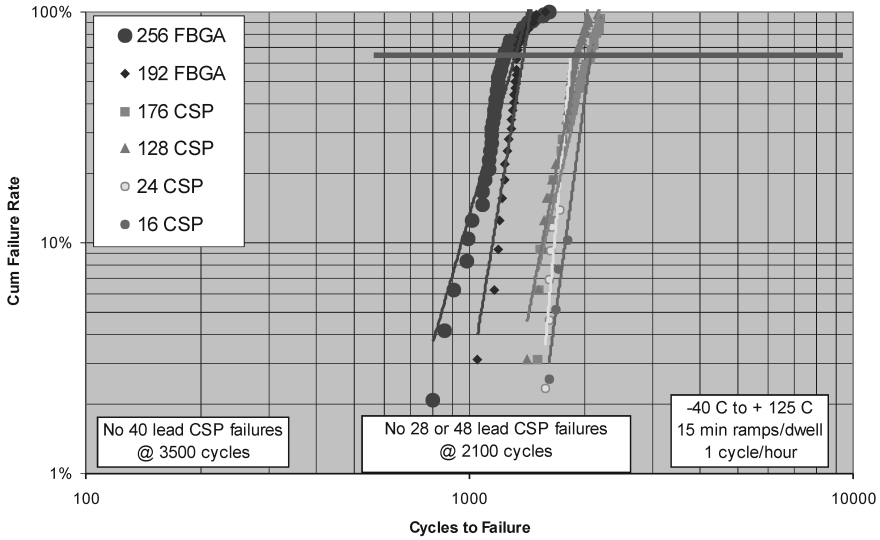


Figure 21. Solder Joint Reliability Weibul Plot

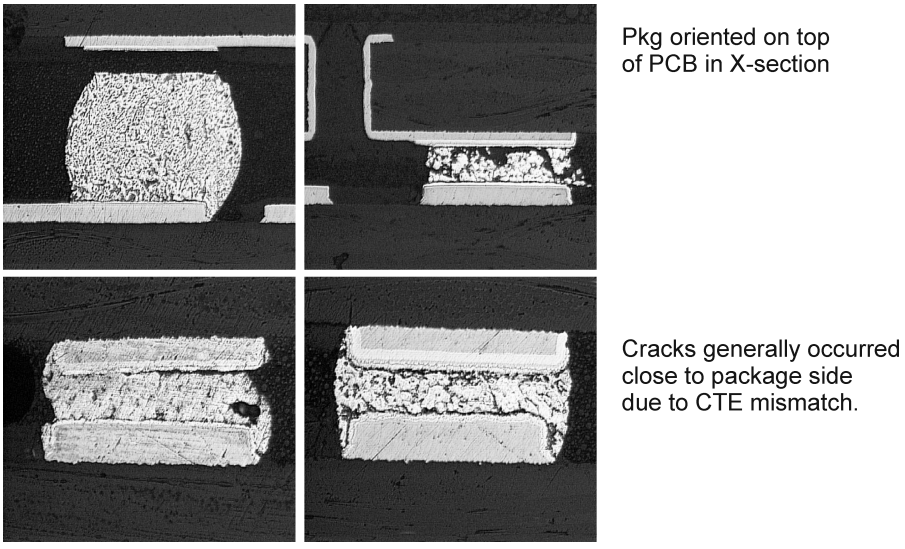
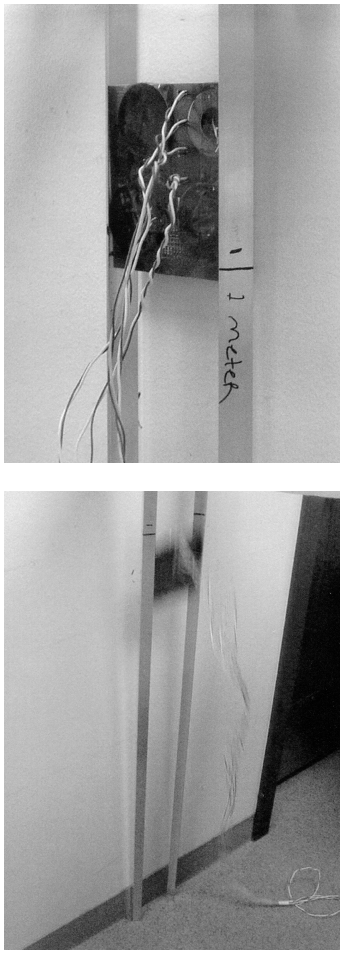


Figure 22. Laminate CSP Solder Joint Failure Mode in TMCL

11.2 Solder Joint Reliability: Drop Testing

Testing was performed on the 24L CSP focusing on solder joint integrity, reliability, and performance when dropped from a 1-meter height. These test conditions were selected based on the most probable customer use. Specifically, applications involving use in cell phones, laptop computers, and handheld wireless products where consumer reliability demands are the highest. Texas Instruments' CSP technology benefits the end user by providing a low profile part that mounts close to the board. This low profile promotes better solder joint reliability due to an extremely low the standoff height.

The 24L CSP was mounted on five individual 1.6mm thick FR-4 printed circuit boards. Each board consisted of four individual 24L CSP units configured for continuous monitoring of each solder joint. Each board was weighted to 150g and dropped from a height of 1-meter. The failure criterion was defined as twice the initial resistance ($2xR_o$). Within each drop test, the resistance was continuously monitored for changes in solder joint resistance. Each of the five boards was dropped a total of 15 times, 5 times on each respective axis (x, y, z).



Results: All of the 24L CSP parts passed with one exception was found to have insufficient solder paste during SMT and therefore considered an invalid failure.

11.3 Solder Joint Reliability: Three Point Bend Test (Bend to Fail)

In this test, the 24L CSP was surface mounted using standard SMT procedures as previously recommended.

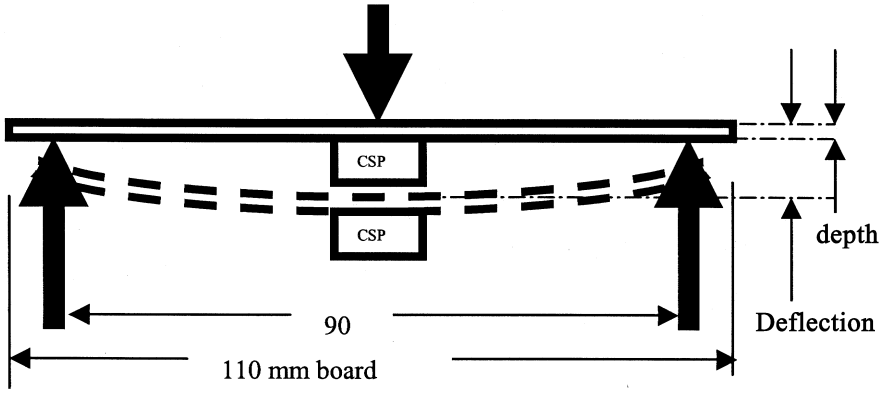


Figure 23. PCB Bend Test for the 24L CSP as Mounted to 1.6mm thick FR-4 Board

In Figure 23, the 24L CSP is shown mounted to a 1.6mm thick FR-4 board in the neutral position (solid line). A force is applied as shown by the heavy arrows along the board. The resulting force causes the board to deflect as shown by the dashed line. The board is placed with the test part centered across a 90mm span. The downward force is applied to the backside of the board causing the soldered joints to deflect. The board was bent until complete solder joint failure occurred as demonstrated in Figure 24.

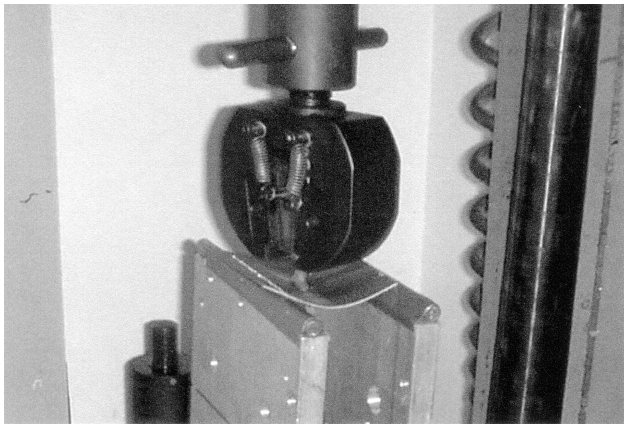


Figure 24. Actual part under flex test conditions.

Results: In all test cases, CSP solder joint part failure was achieved only after board failure. The FR-4 board fractured in all cases causing FR-4 traces to fail.

11.4 SOLDER JOINT PULL & SHEAR TESTING

CSP solder joint connections were tested under pull and shear conditions with the following results as shown in Table 6 and Table 7. A 0.2 in/sec pull and shear rate was used for this test.

Table 6. Pull Test for laminate CSP & FBGA

Lead Count	Sample Size	High Pull Strength per Joint (mN)	Low Pull Strength per Joint (mN)	Average Pull Strength per Joint (mN)	Standard Deviation per Joint
16 CSP	11	337	70	180	90
24 CSP	5	356	65	157	112
28 CSP	4	112	81 (1)	90 (1)	22
48 - 8.1x12.5 CSP	1	126	126	135	-

(1) Large variances in pull and shear test values are due to statistical nature of pull/shear tests and inherent problems in accurate setup.

Table 6. Pull Test for laminate CSP & FBGA (continued)

Lead Count	Sample Size	High Pull Strength per Joint (mN)	Low Pull Strength per Joint (mN)	Average Pull Strength per Joint (mN)	Standard Deviation per Joint
64 FBGA	6	164	31	90	45
100 FBGA	10	146	34	90	45

Table 7. Shear Test for laminate CSP & FBGA

Lead Count	Sample Size	High Shear Strength per Joint (mN)	Low Shear Strength per Joint (mN)	Average Shear Strength per Joint (mN)	Standard Deviation per Joint
16 CSP	17	337	155	210	51
24 CSP	16	506	178	246	85
28 CSP	8	313	104	178	70
48 - 8.1x12.5 CSP	11	389	206	322	60
64 FBGA	16	200	98	161	27
100 FBGA	11	209	101	173	34

12 Tray, Tape & Reel and Test Socket Info

The Laminate CSP is shipped in standard polycarbonate conductive carrier tape with pressure-sensitive adhesive (PSA) cover tape. The FBGA is available in JEDEC trays and will be available in tape and reel for high volume production. Handling damage is minimal due to robust package and interconnect design.

Package	Reel S/N	Tape Carrier S/N	Tape Cover S/N	Tray S/N
16L CSP	017983	068030	025360	071835
20L CSP(1)	017983	068030	025360	071836
20L CSP(2)	017983	076734	025360	071836
24L CSP(1)	017983	066768	025360	071836
24L CSP(2)	017983	076735	025360	071836
28L CSP	017983	068031	025360	071837
40L CSP	017982	073563	900572	N/A
48L CSP	017982	073815	900572	073318
128L CSP	017981	072801	030138	073321
176L CSP	017981	074635	030138	073321
49L FBGA	023815	074066	025361	078086
64L FBGA	023815	069683	030137	073319
100L FBGA	017981	072870	030138	073851
192L FBGA	017981	073544	030138	073324

(1) Use for both 0.8mm and 1.00mm thick package.
(2) Use for only 0.6mm thick package.

Table 8. Supplier Information

Tray Suppliers	KOSTAT Santa Clara, CA (888)390-0885
	Peak International, Inc. Milipitas, CA (408)934-2480
Tape & Reel Suppliers	Advantek Tapping Systems (510)623-1877
	ePak (408)978-3725
Test Suppliers	Johnstech International Corp. Minneapolis, MN (612)378-2020

Table 8. Supplier Information (continued)

Burn in Socket Suppliers	Loranger International Corp. Warren, PA (814)723-2250
	3M Textool™ Austin, TX (800)328-0411
	Yamaichi (408)456-0797

13 Laminated CSP/FBGA DOs and DON'Ts

	DOs	**DON'Ts**
PCB	1:1 ratio between the land grid array CSP pad and the PCB pad. 1:0.8 ratio for the ball grid array FBGA Ball pad on the PCB is 0.33 mm	
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD)	Solder mask defined (SMD)
	Organic Solderability Presevative (OSP) or Ni-Au surface finish range from 0.05 µm to 0.2 µm.	Gold plating thickness > 0.2 µm
	Require surface flatness within 28 µm for Hot Air Solder Leveling (HASL) for land grid array CSP	HASL surface flatness > 28 µm
Stencil	Recommend laser cut + electro polished or additive build up with 5° tapering	
	Stencil thickness is 125 µm	Thickness > 125 µm or < 100 µm
	Aperture opening: 275 µm x 650 µm	
Solder Paste	Type 3 (25 to 45 µm particle size range) or finer.	Type 1 or Type 2

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