User's Guide

SNOA559B–October 2011–Revised May 2013

AN-2127 LM3448 A19 Edison Retrofit Evaluation Board

1 Introduction

This demonstration board highlights the performance of a LM3448 non-isolated LED driver solution that can be used to power a single LED string consisting of eight to twelve series connected LEDs from a 85 V_{RMS} to 135 V_{RMS}, 60 Hz input power supply.

This is a two-layer board using the bottom and top layer for component placement. The demonstration board can be modified to adjust the LED forward current, the number of series connected LEDs that are driven and the switching frequency. The topology used for this evaluation board eliminates the need for passive power factor correction and results in high power factor with minimal component count which results in a size that can fit in a standard A19 Edison socket. This board will also operate correctly and dim smoothly using most standard TRIAC dimmers.

Refer to the *LM3448 Phase Dimmable Offline LED Driver with Integrated FET* (SNOSB51) data sheet for detailed information regarding the LM3448 device. A schematic and layout have also been included along with measured performance characteristics. A bill of materials is also included that describes the parts used on this demonstration board.

2 Key Features

- Drop-in compatibility with TRIAC dimmers
- Line injection circuitry enables PFC values greater than 0.85
- Adjustable LED current and switching frequency
- Flicker free operation

3 Applications

- Retrofit TRIAC Dimming
- Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

4 Performance Specifications

Based on an LED V_f = 3V

Symbol	Parameter	Min	Typ	Max
V_{IN}	Input voltage	85V_{RMS}	120V_{RMS}	135V_{RMS}
V_{OUT}	LED string voltage	-	36V	-
I_{LED}	LED string average current	-	181mA	-
P_{OUT}	Output power	-	6.5W	-

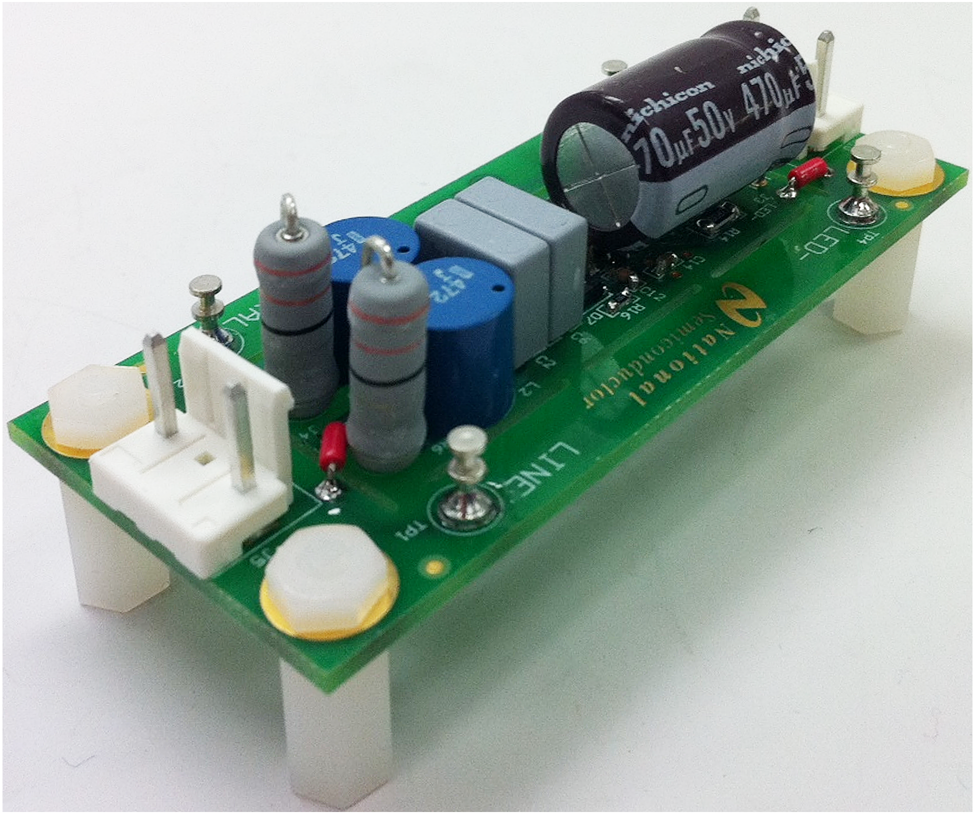


Figure 1. Demo Board

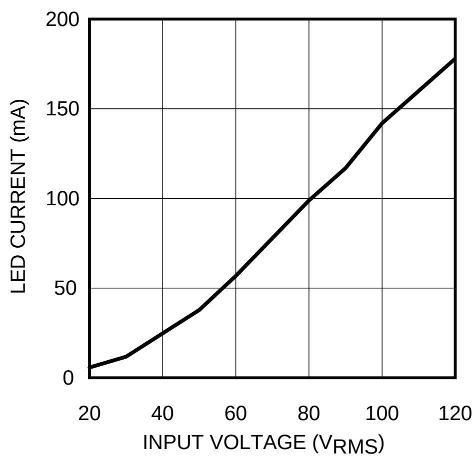


Figure 2. LED Current vs. Line Voltage (using TRIAC Dimmer)

5 Typical Performance Characteristics

T_J=25°C and V_{CC}=12V, unless otherwise specified.

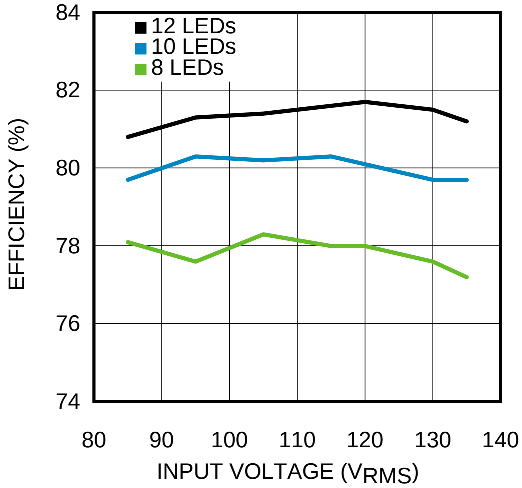


Figure 3. Efficiency vs. Line Voltage

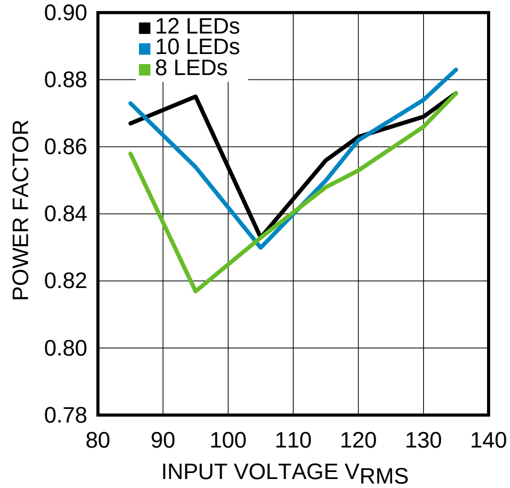


Figure 4. Power Factor vs. Line Voltage

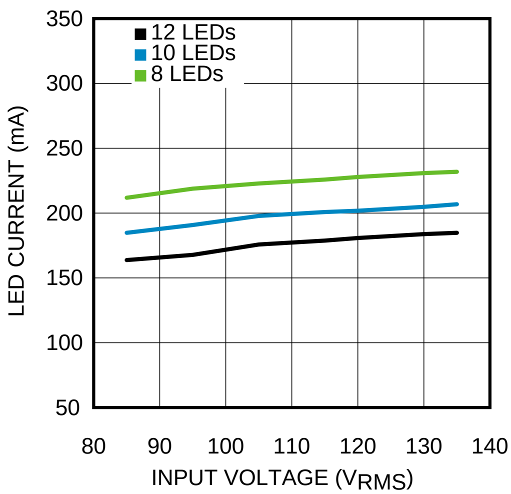


Figure 5. LED Current vs. Line Voltage

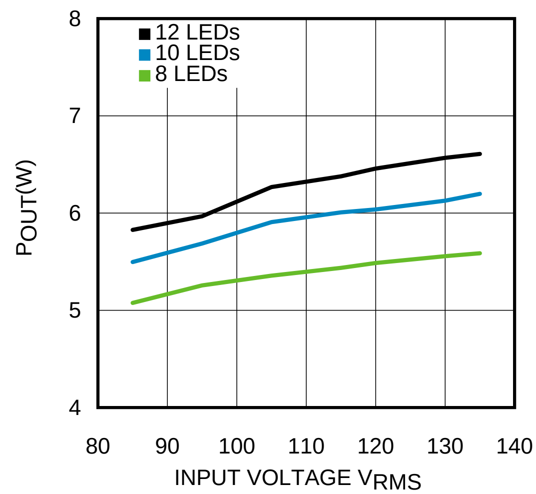


Figure 6. Output Power vs. Line Voltage

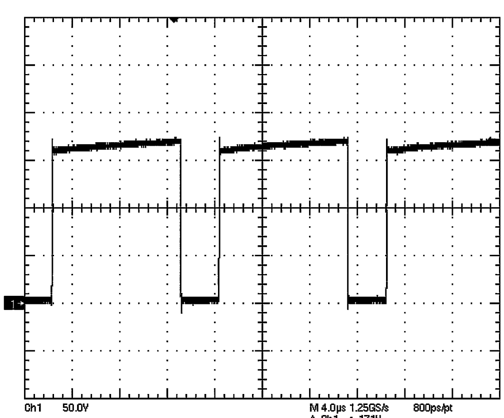


Figure 7. SW FET Drain Voltage Waveform (V_{IN}=120V_{RMS}, 12 LEDs, I_{LED}=181mA)

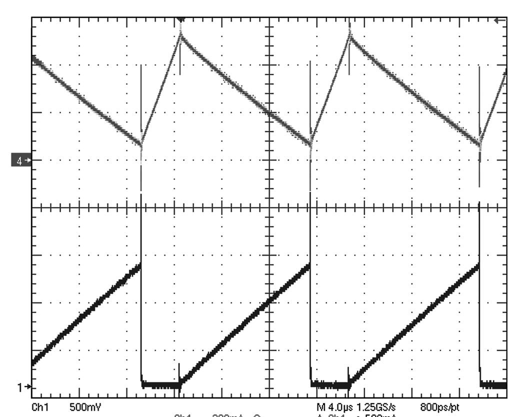


Figure 8. COFF Voltage (CH1), Inductor Current (CH4) (V_{IN}=120V_{RMS}, 12 LEDs, I_{LED}=181mA)

6 EMI Performance

120V, 6.5W Conducted EMI Scans

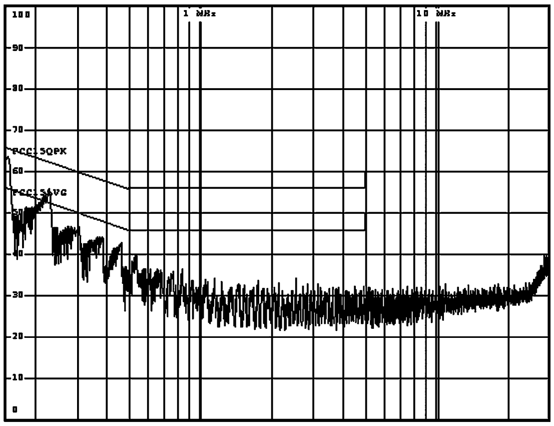


Figure 9. LINE – CISPR/FCC Class B Peak Scan

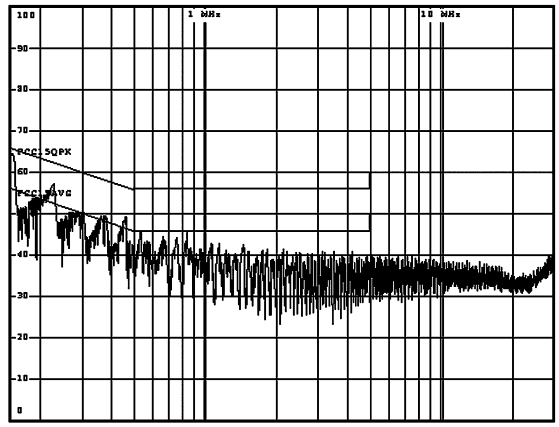


Figure 10. NEUTRAL – CISPR/FCC Class B Peak Scan

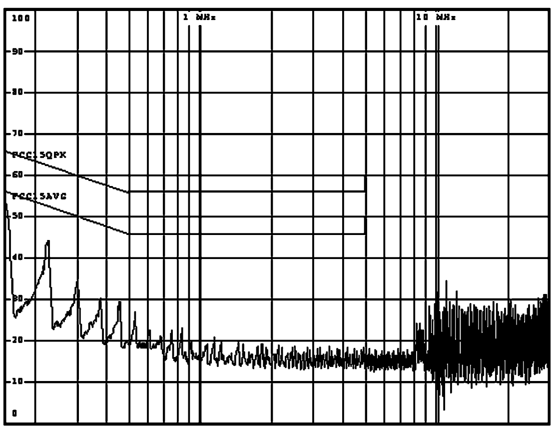


Figure 11. LINE – CISPR/FCC Class B Average Scan

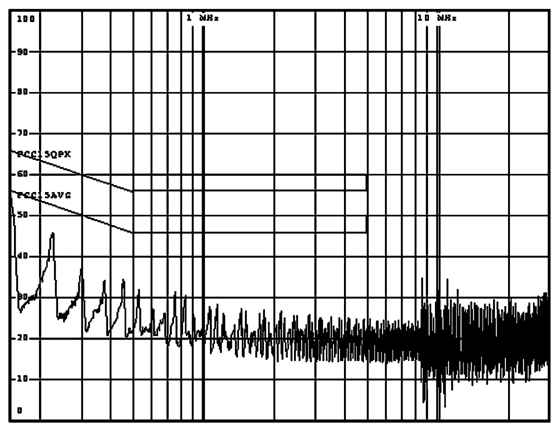


Figure 12. NEUTRAL – CISPR/FCC Class B Average Scan

7 Circuit Operation With Forward Phase TRIAC Dimmer

The dimming operation of the circuit was verified using a forward phase TRIAC dimmer. Waveforms captured at different dimmer settings are shown below:

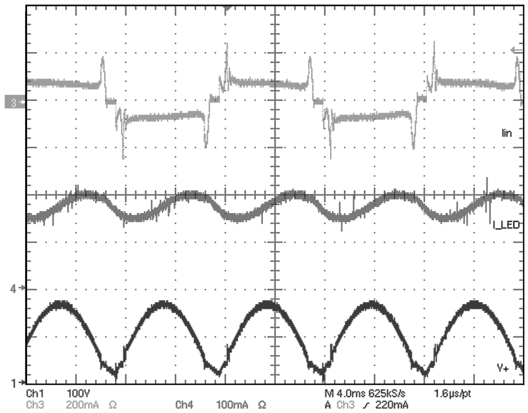


Figure 13. Forward phase circuit at full brightness

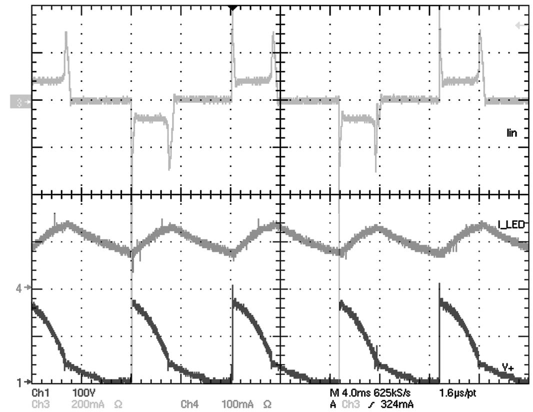


Figure 14. Forward phase circuit at 90° firing angle

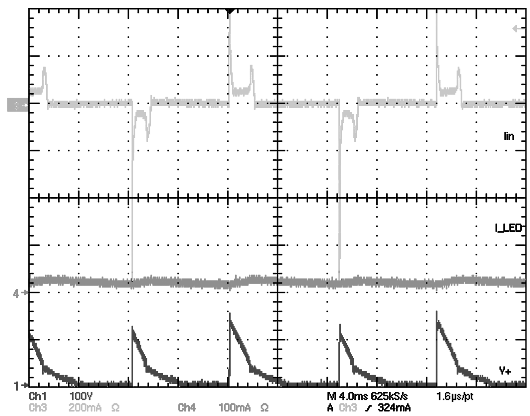


Figure 15. Forward phase circuit at 135° firing angle

8 Circuit Operation With Reverse Phase Dimmer

The circuit operation was also verified using a reverse phase dimmer and waveforms captured at different dimmer settings are shown below:

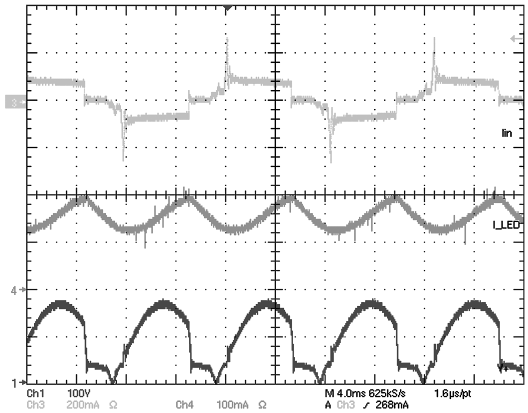


Figure 16. Reverse phase circuit at full brightness

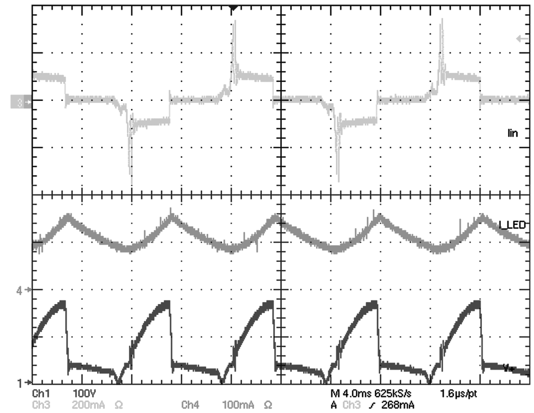


Figure 17. Reverse phase circuit at 90° firing angle

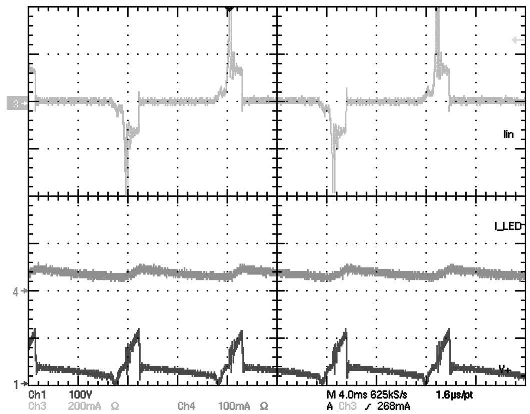
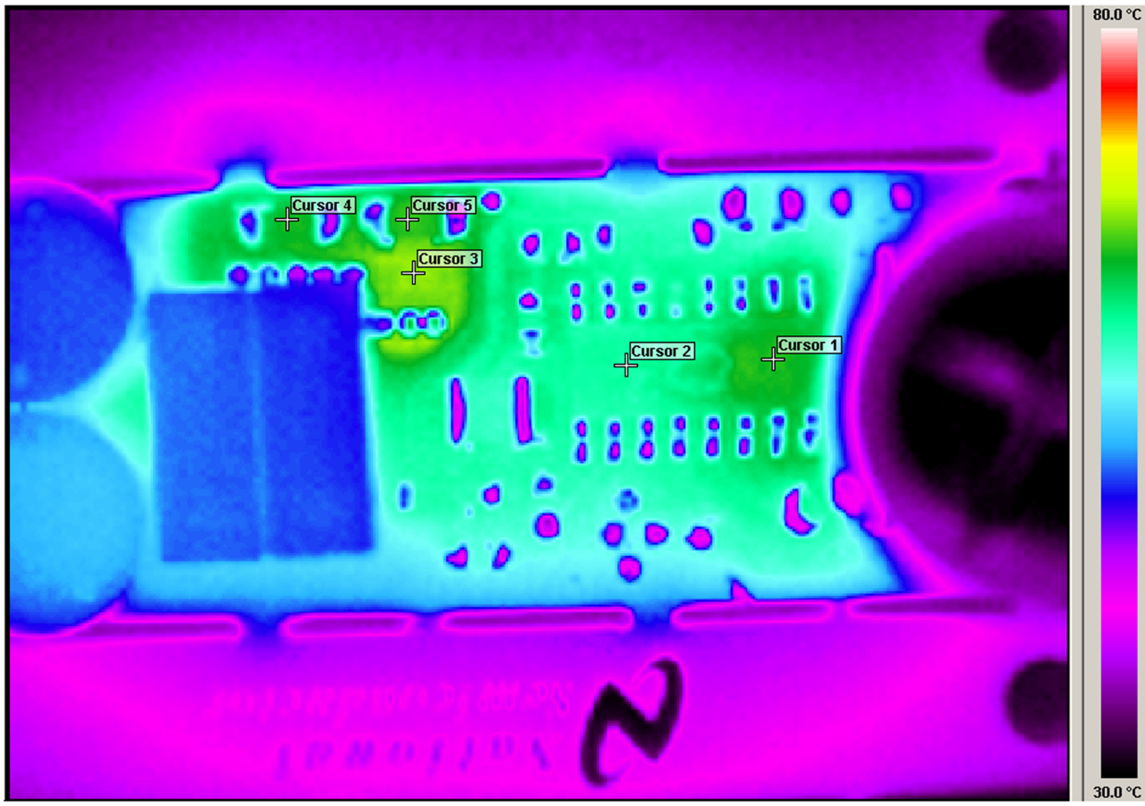


Figure 18. Reverse phase circuit at 135° firing angle

9 Thermal Performance

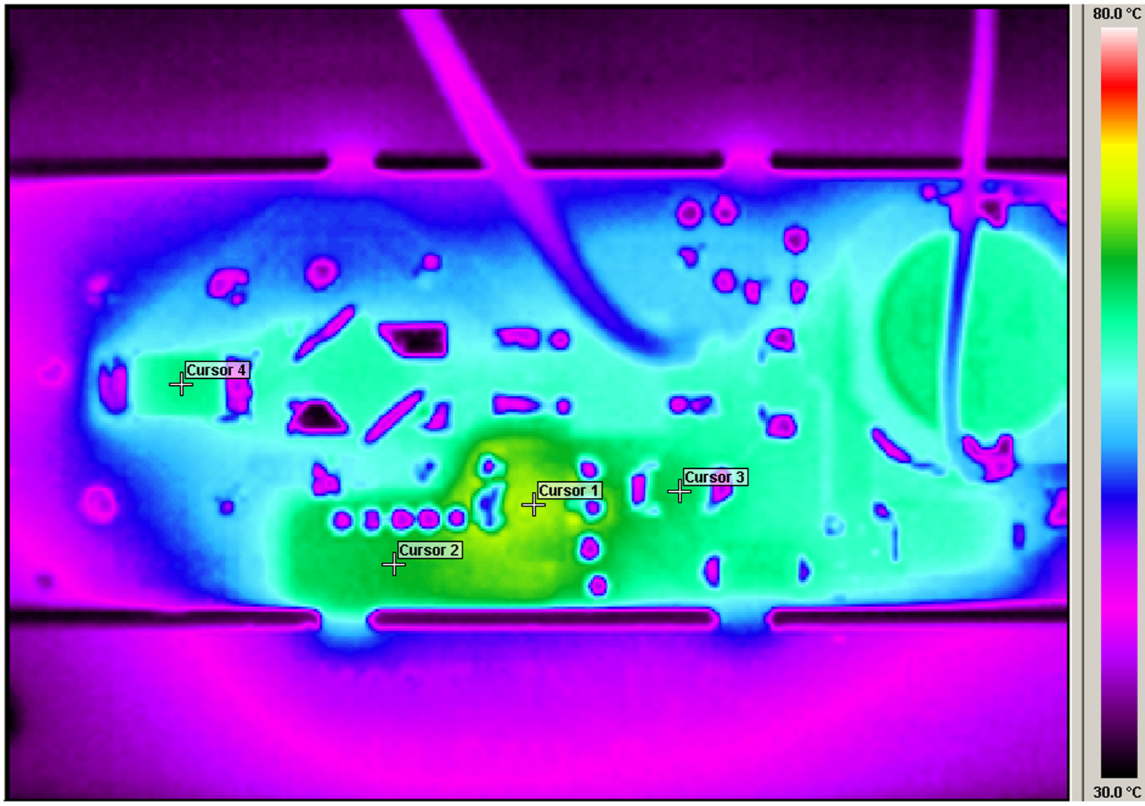
The board temperature was measured using an IR camera (HIS-3000, Wahl) while running under the following conditions: V_{IN} = 120V_{RMS}, I_{LED} = 181mA, # of LEDs = 12, P_{OUT} = 6.5W.

NOTE: Thermal performance is highly dependent on the user's final end-application enclosure, heat-sinking methods, ambient operating temperature, and PCB board layout in addition to the electrical operating conditions. This LM3448 evaluation board is optimized to supply 6.5W of output power at room temperature without exceeding the thermal limitations of the LM3448. However higher output power levels can be achieved if precautions are taken not to exceed the power dissipation limits of the LM3448 package or die junction temperature. Please see the LM3448 datasheet for additional details regarding its thermal specifications.



- Cursor 1: 65.3°C
- Cursor 2: 60.1°C
- Cursor 3: 67.6°C
- Cursor 4: 64.9°C
- Cursor 5: 65.6°C

Figure 19. Top Side - Thermal Scan



- Cursor 1: 68.1°C
- Cursor 2: 64.7°C
- Cursor 3: 62.6°C
- Cursor 4: 61.7°C

Figure 20. Bottom Side - Thermal Scan

10 LM3448 Device Pin-Out

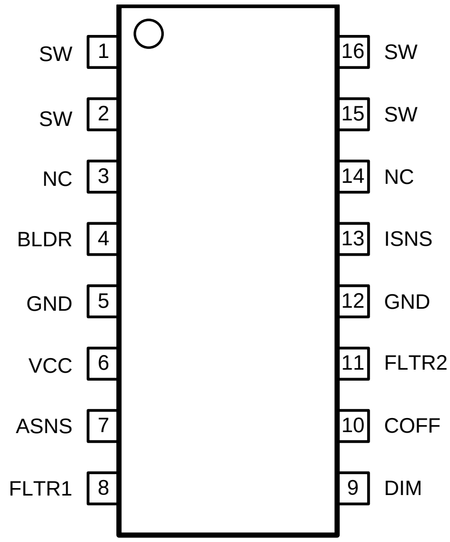


Figure 21. Device Pin-Out

Table 1. Pin Description 16 Pin Narrow SOIC

Pin #	Name	Description
1, 2, 15, 16	SW	Drain connection of internal 600V MOSFET.
3, 14	NC	No connect. Provides clearance between high voltage and low voltage pins. Do not tie to GND.
4	BLDR	Bleeder pin. Provides the input signal to the angle detect circuitry. A 230Ω internal resistor ensures BLDR is pulled down for proper angle sense detection.
5, 12	GND	Circuit ground connection.
6	V_{CC}	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver. Connect a 22µF (minimum) bypass capacitor to ground.
7	ASNS	PWM output of the TRIAC dim decoder circuit. Outputs a 0 to 4V PWM signal with a duty cycle proportional to the TRIAC dimmer on-time.
8	FLTR1	First filter input. The 120Hz PWM signal from ASNS is filtered to a DC signal and compared to a 1 to 3V, 5.85 kHz ramp to generate a higher frequency PWM signal with a duty cycle proportional to the TRIAC dimmer firing angle. Pull above 4.9V (typical) to TRI-STATE® DIM.
9	DIM	Input/output dual function dim pin. This pin can be driven with an external PWM signal to dim the LEDs. It may also be used as an output signal and connected to the DIM pin of other LM3448/LM3445 devices or LED drivers to dim multiple LED circuits simultaneously.
10	COFF	OFF time setting pin. A user set current and capacitor connected from the output to this pin sets the constant OFF time of the switching controller.
11	FLTR2	Second filter input. A capacitor tied to this pin filters the PWM dimming signal to supply a DC voltage to control the LED current. Could also be used as an analog dimming input.
13	ISNS	LED current sense pin (internally connected to MOSFET source). Connect a resistor from ISNS to GND to set the maximum LED current.

11 Demo Board Wiring Overview

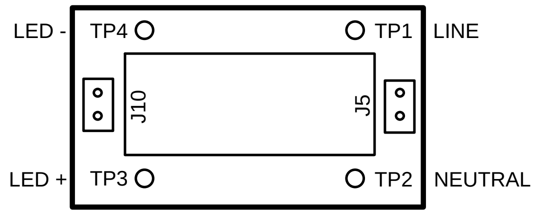


Figure 22. Wiring Connection Diagram

Table 2. Test Points

Test Point	Name	I/O	Description
TP3	LED +	Output	**LED Constant Current Supply** Supplies voltage and constant-current to anode of LED string.
TP4	LED -	Output	**LED Return Connection (not GND)** Connects to cathode of LED string. Do NOT connect to GND.
TP1	LINE	Input	**AC Line Voltage** Connects directly to AC line or output of TRIAC dimmer of a 120VAC system.
TP2	NEUTRAL	Input	**AC Neutral** Connects directly to AC neutral of a 120VAC system.

12 Demo Board Assembly

Figure 23. Top View

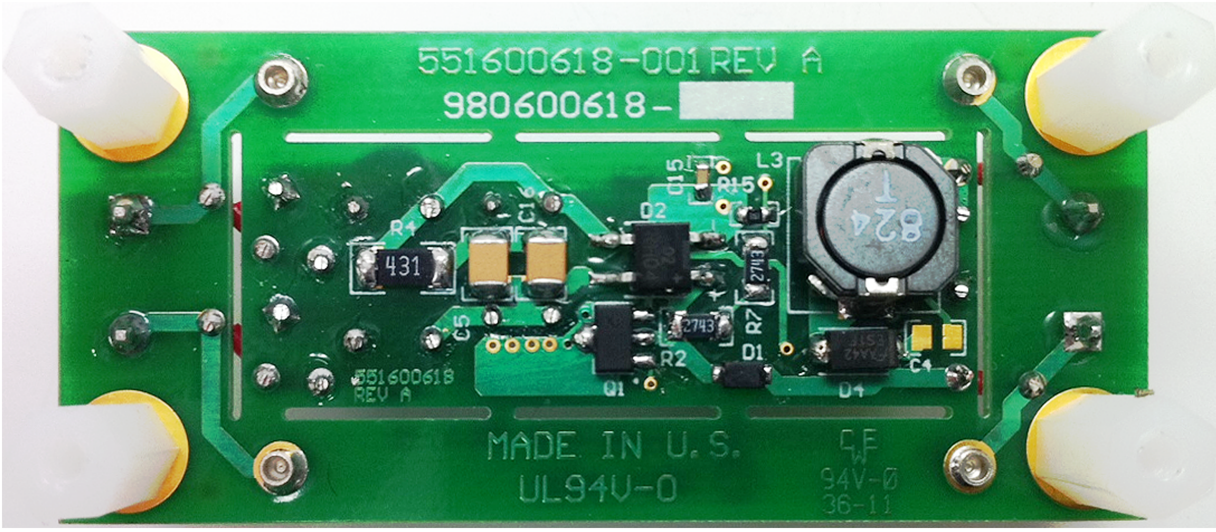


Figure 24. Bottom View

13 Design Guide

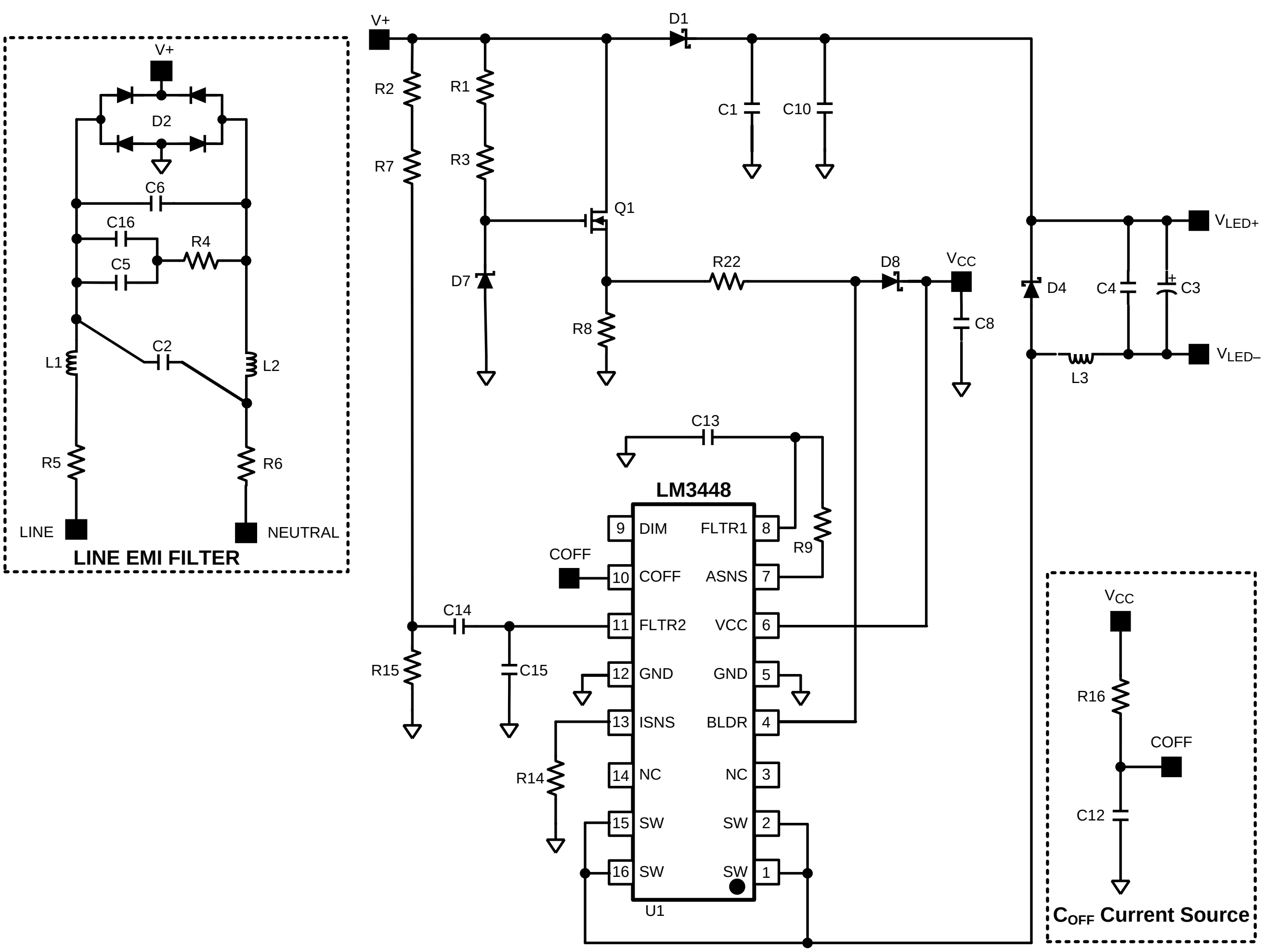


Figure 25. Evaluation Board Schematic

13.1 Buck Converter

The following section explains how to design a non-isolated buck converter using the LM3448. Refer to the LM3448 datasheet for specific details regarding the function of the LM3448 device. All reference designators refer to the Evaluation Board Schematic in Figure 25 unless otherwise noted. The circuit operates in open-loop based on a constant off-time that is set by selecting appropriate circuit components. Like an incandescent lamp, the driver is compatible with both forward and reverse phase dimmers.

AC-Coupled Line Injection

By injecting a voltage V_{INJECT} which is proportional to the line voltage into the FLTR2 pin (see Figure 26), input current shaping is obtained which improves power factor performance. By AC-coupling the V_{INJECT} signal through capacitor C14, improved line-regulation of the LED current is also achieved (see Figure 27).

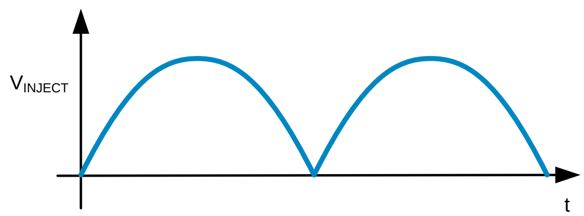


Figure 26. FLTR2 Waveform with No Dimmer

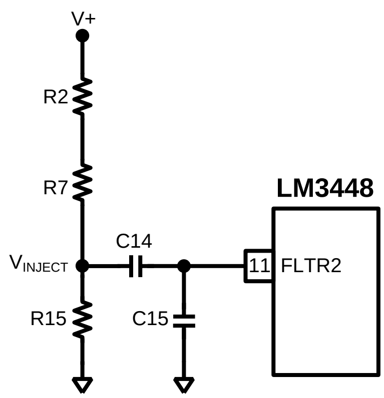


Figure 27. AC-Coupled Line-Injection Circuit

Figure 28 shows how line shaping of the input current is implemented. Peak voltage at the FLTR2 pin should be kept below 1.25V otherwise current limit will be tripped. A good starting point is to set up the resistor divider consisting of resistors R2, R7 and R15 to provide a V_{INJECT} peak input voltage of 1.0V at the input of capacitor C14 at the nominal input voltage. Recommended values for the AC-coupling capacitor C14 is 0.47µF and for the FLTR2 capacitor C15 is 0.1µF.

With a 1.0V V_{INJECT} voltage, the voltage at the FLTR2 pin at the maximum and minimum input voltages can be calculated using the following equations,

$$V_{FLTR2(MAX)} = 0.0024 \times V_{IN(MAX)} + 0.708$$
$$V_{FLTR2(MIN)} = 0.0024 \times V_{IN(MIN)} + 0.708 \quad (1)$$

These V_{FLTR2} voltages will be used later to determine ripple and peak inductor currents.

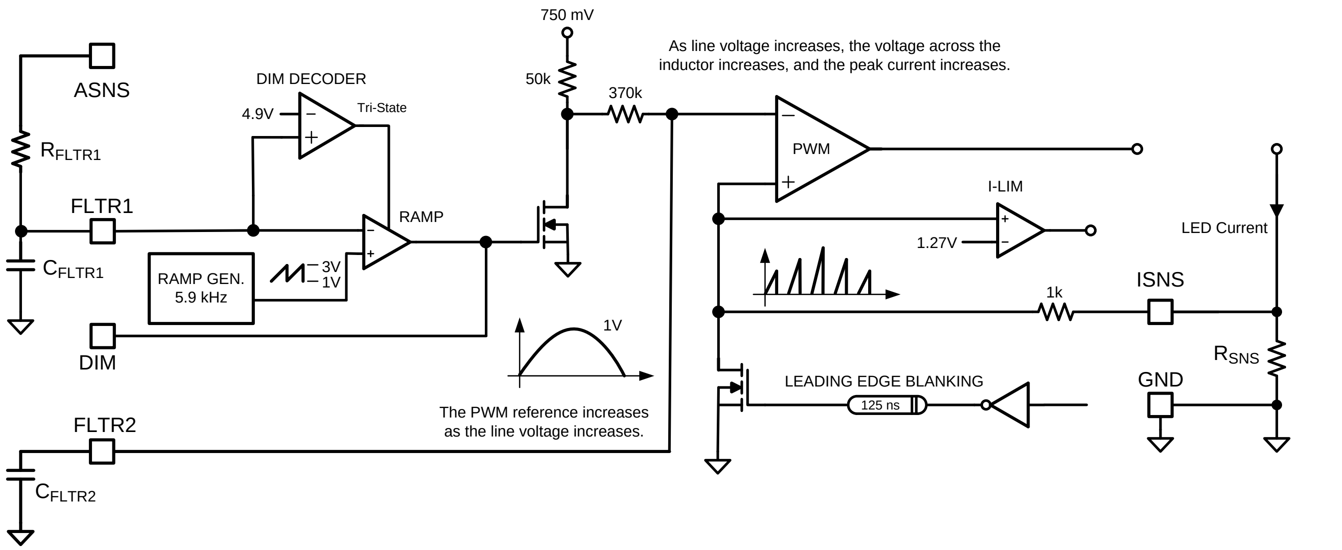


Figure 28. Typical Operation of FLTR2 Pin

Off-time, On-time and Switching Frequency

The AC mains voltage at the line frequency f_L is assumed to be perfectly sinusoidal and the diode bridge ideal. This yields a perfect rectified sinusoid at the input to the buck converter. The maximum, nominal and minimum peak input voltages are defined as follows,

$$V_{IN-PK(MIN)} = V_{IN(MIN)} \times \sqrt{2}$$
$$V_{IN-PK(NOM)} = V_{IN(NOM)} \times \sqrt{2}$$
$$V_{IN-PK(MAX)} = V_{IN(MAX)} \times \sqrt{2} \quad (2)$$

The LM3448 will operate as a constant off-time regulator, and so t_{OFF} will be constant throughout all operating points. The on-time t_{ON} (and subsequently the switching frequency f_{SW}) will vary depending on input voltage and LED stack voltage values. For this buck converter operating in continuous conduction mode (CCM), the minimum on-time $t_{ON(MIN)}$ can be determined for a maximum desired switching frequency $f_{SW(MAX)}$at the maximum peak input voltage,

$$t_{ON(MIN)} = \frac{\left(\frac{1}{\eta}\right)\left(\frac{V_{OUT}}{V_{IN-PK(MAX)}}\right)}{f_{SW(MAX)}} \quad (3)$$

The off-time t_{OFF} is now calculated where $T_{S(MIN)}$ is the minimum switching period,

$$t_{OFF} = T_{S(MIN)} - t_{ON(MIN)} \quad (4)$$

It is important to note that there is a minimum on-time of 200ns that needs to be met in order for proper LED driver operation.

Output Power and Current Sense Resistor

Due to the interaction of the AC-coupled line-injection voltage with the FLTR2 signal, the equations for determining the correct sense resistor R_{SNS} (shown as R14 in the evaluation board schematic) for a desired output power P_{OUT} are complex and beyond the scope of this document. Instead, performance graphs showing the relationship between LED current, P_{OUT} and R_{SNS} are shown in Figure 29, Figure 30 and Figure 31 for common stack voltages of 8, 10 and 12 LEDs. By referring to these graphs, users can choose R14 values that will meet their LED current and output power requirements.

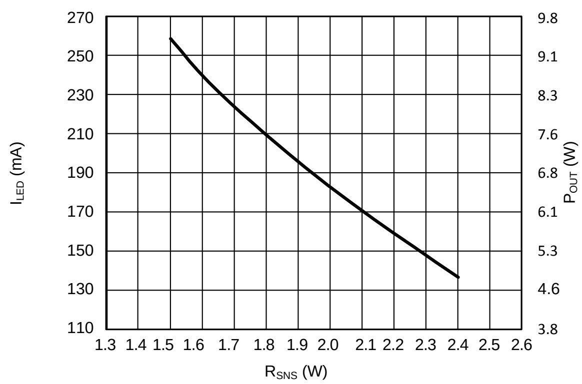


Figure 29. I_{LED} vs. P_{OUT} vs. R_{SNS} for 12 LEDs (V_f=3.0V)

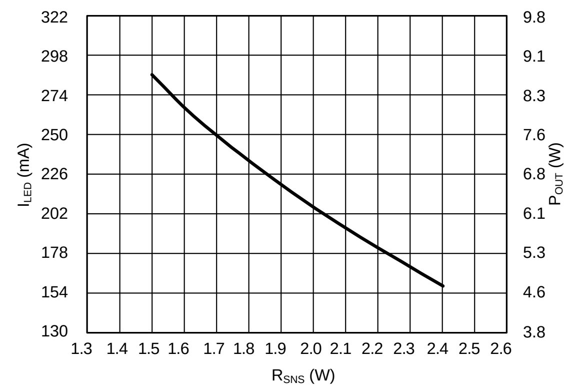


Figure 30. I_{LED} vs. P_{OUT} vs. R_{SNS} for 10 LEDs (V_f=3.0V)

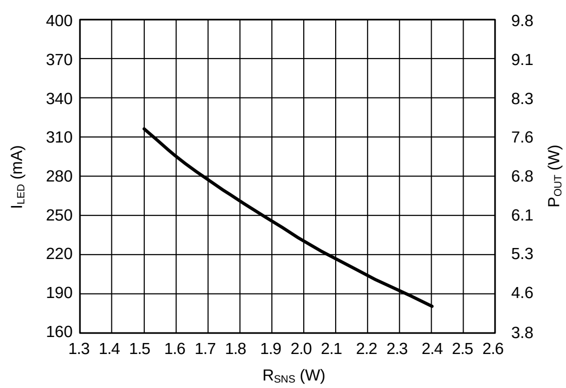


Figure 31. I_{LED} vs. P_{OUT} vs. R_{SNS} for 8 LEDs (V_f=3.0V)

Inductor

Peak inductor currents will need to be calculated as shown below based on the V_{FLTR2} voltages and chosen sense resistor R14 at the maximum and minimum peak input voltages,

$$I_{L-PK-MAX(VIN-PK-MIN)} = \frac{V_{FLTR2(MIN)}}{R14}$$

$$I_{L-PK-MAX(VIN-PK-MAX)} = \frac{V_{FLTR2(MAX)}}{R14} \quad (5)$$

Inductor ripple current will need to be specified by the user based on desired EMI performance, inductor size and other operating conditions. The following equations show how to calculate for maximum and minimum inductor ripple currents respectively by basing the ripple (i.e.$\Delta i_{L(\%)}$ as a percentage of maximum peak inductor currents,

$$\Delta i_{L(VIN-PK-MIN)} = I_{L-PK-MAX(VIN-PK-MIN)} \times \Delta i_{L(\%)}$$
$$\Delta i_{L(VIN-PK-MAX)} = I_{L-PK-MAX(VIN-PK-MAX)} \times \Delta i_{L(\%)} \tag{6}$$

It is recommended that this buck converter design operate in CCM over the full range of operating peak input voltages, and so the minimum inductor peak current at $V_{IN-PK(MIN)}$ should not go below zero,

$$I_{L-PK-MIN(VIN-PK-MIN)} = I_{L-PK-MAX(VIN-PK-MIN)} - \Delta i_{L(VIN-PK-MIN)} \tag{7}$$

The inductor value can be calculated based on the minimum on-time, LED output voltage and the specified inductor ripple current $\Delta i_{L-PK(VIN-PK-MAX)}$ at the maximum peak input voltage as described below,

$$L = t_{ON(MIN)} \left(\frac{V_{IN-PK(MAX)} - V_{OUT}}{\Delta i_{L-PK(VIN-PK-MAX)}} \right) \tag{8}$$

COFF Current Source

The current source used to establish the constant off-time is shown in Figure 32.

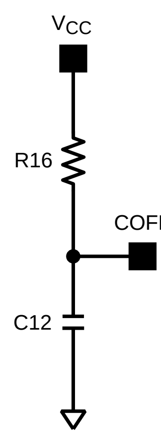


Figure 32. COFF Current Source Circuit

Capacitor C12 will be charged with current from the V_{CC} supply through resistor R16. The COFF pin threshold will therefore be tripped based on the following capacitor equation,

$$1.276V = V_{CC}\left(1 - e^{x}\right) \tag{9}$$

where,

$$x = \frac{-t_{OFF}}{R16 \times C12} \tag{10}$$

Solving for off-time t_{OFF} results in,

$$t_{OFF} = -R16 \times C12 \times \left[\ln\left(1 - \frac{1.276V}{V_{CC}}\right) \right] \tag{11}$$

Re-arranging the above equation results in R16 being calculated where C12 is typically chosen as value around 470pF,

$$R16 = \frac{-t_{OFF}}{C12\left[\ln\left(1 - \frac{1.276V}{V_{CC}}\right)\right]} \quad (12)$$

Additionally, the maximum on-time $t_{ON(MAX)}$ and corresponding minimum switching frequency $f_{SW(MIN)}$ and maximum switching period $T_{S(MAX)}$ occur at the minimum peak input voltage. Using the previously calculated inductor value, these values can now be calculated as,

$$t_{ON(MAX)} = \frac{\left(L \times \Delta i_{L(VIN-PK-MIN)}\right)}{\left(V_{IN-PK(MIN)} - V_{OUT}\right)}$$

$$f_{SW(MIN)} = \frac{1}{\left(t_{ON(MAX)} + t_{OFF}\right)} = \frac{1}{T_{S(MAX)}} \quad (13)$$

Maximum and minimum duty cycles, D_{MAX} and D_{MIN}, will occur at the minimum and maximum peak input voltages respectively,

$$D_{MAX} = \frac{t_{ON(MAX)}}{T_{S(MAX)}}$$

$$D_{MIN} = \frac{t_{ON(MIN)}}{T_{S(MIN)}} \quad (14)$$

Switching MOSFET (SW FET)

Peak and RMS SW FET currents are calculated along with maximum SW FET power dissipation based on the SW FET R_{DS-ON} value using the following equations,

$$I_{SWFET-PK(MAX)} = I_{L-PK-MAX(VIN-PK-MAX)} \quad (15)$$

$$I_{SWFET-RMS(MAX)} = I_{LED} \times \sqrt{D_{MAX}} \times \sqrt{\left(1 + \frac{1}{3}\left(\frac{\Delta i_{L(VIN-PK-MIN)}}{I_{LED}}\right)^2\right)} \quad (16)$$

and,

$$P_{SWFET(MAX)} = I_{SWFET-RMS(MAX)}^{\ 2} \times \left(SW\ FET\ R_{DS-ON}\right) \quad (17)$$

Current Limit

The peak inductor current limit I_{LIM} should be approximately 25% higher than the maximum operating peak inductor current,

$$I_{LIM} = \frac{1.27V}{R_{SNS}} = \frac{1.27V}{R14} \quad (18)$$

The sense resistor will need to be able to dissipate the maximum power,

$$P_{(R14)} = I_{SWFET-RMS(MAX)}^{\ 2} \times R14 \quad (19)$$

Re-circulating Diode

The main re-circulating diode (D4) should be sized to block the maximum reverse voltage $V_{RD4(MAX)}$, operate at the maximum peak $I_{DR\text{-}PK(MAX)}$ and RMS currents $I_{D4\text{-}RMS(MAX)}$, and dissipate the maximum power $P_{D4(MAX)}$ as determined by the following equations,

$$V_{RD4(MAX)} = V_{IN\text{-}PK(MAX)} \quad (20)$$

$$I_{D4\text{-}PK(MAX)} = I_{L\text{-}PK\text{-}MAX(VIN\text{-}PK\text{-}MAX)} \quad (21)$$

$$I_{D4\text{-}RMS(MAX)} = I_{LED} \times \sqrt{(1 - D_{MIN})} \times \sqrt{\left(1 + \frac{1}{3}\left(\frac{\Delta i_{L(VIN\text{-}PK\text{-}MAX)}}{I_{LED}}\right)^2\right)} \quad (22)$$

$$P_{D4(MAX)} = I_{D4\text{-}RMS(MAX)} \times V_{f(D4)} \quad (23)$$

NOTE: For proper converter operation, the chosen diode should have a reverse recovery time that is less than the LM3448's leading edge blanking time of 125ns.

13.2 Bias Supplies and Capacitances

The VCC bias supply circuit is shown in Figure 33. The passFET (Q1) is used in its linear region to stand-off the line voltage from the LM3448 regulator. Both the VCC startup current and discharging of the EMI filter capacitance for proper phase angle detection are handled by Q1. Therefore Q1 has to block the maximum peak input voltage and have both sufficient surge and power handling capability with regards to its safe operating area (SOA). The design equations are,

$$V_{Q1} = V_{IN\text{-}PK(MAX)} \quad (24)$$

$$I_{Q1} = \frac{V_{Z(D7)} - V_{GS(Q1)}}{R8} \quad (25)$$

$$P_{Q1} \approx V_{Q1} \times I_{Q1} \quad (26)$$

Note that if additional TRIAC holding current is to be sourced through Q1, then the transistor will need to be sized appropriately to handle the additional current and power dissipation requirements.

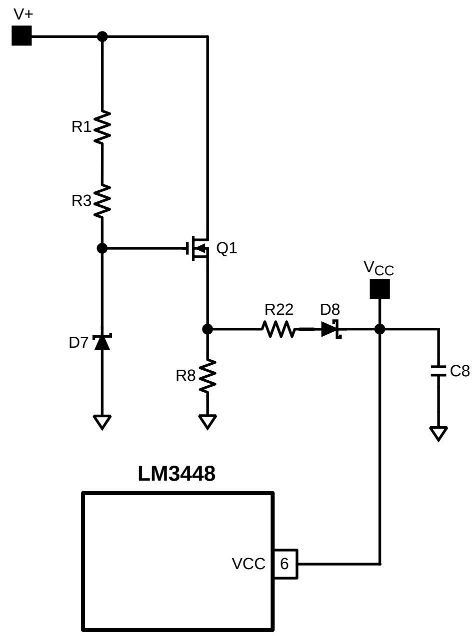


Figure 33. Bias Supply Circuit

Input Capacitance

The input capacitors C1 and C10 have to be able to provide energy during the worst-case switching period at the peak of the AC voltage input. They should be high frequency, high stability capacitors (usually metallized film capacitors, either polypropylene or polyester) with an AC voltage rating equal to the maximum input voltage. They should also have a DC voltage rating exceeding the maximum peak input voltage plus half of the peak to peak input voltage ripple specification. The minimum required input capacitance is calculated given the same ripple specification,

$$(C1 || C10) = \frac{L \times I_{L-PK-MAX(VIN-PK-MIN)}^{2}}{\left(V_{IN-PK(MIN)} + \frac{\Delta V_{IN-PK}}{2}\right)^{2} - \left(V_{IN-PK(MIN)} - \frac{\Delta V_{IN-PK}}{2}\right)^{2}} \quad (27)$$

Output Capacitance

C3 should be a high quality electrolytic capacitor with a voltage rating greater than the specified LED stack voltage. Given the desired voltage ripple, the minimum output capacitance is calculated,

$$C3 = \frac{P_{OUT}}{(2\pi \times f_L \times V_{OUT} \times \Delta V_{OUT})} \quad (28)$$

13.3 Input Filter

Background

Since the LM3448 is used for AC to DC systems, electromagnetic interference (EMI) filtering is critical to pass the necessary standards for both conducted and radiated EMI. This filter will vary depending on the output power, the switching frequencies, and the layout of the PCB. There are two major components to EMI: differential noise and common-mode noise. Differential noise is typically represented in the EMI spectrum below approximately 500kHz while common-mode noise shows up at higher frequencies.

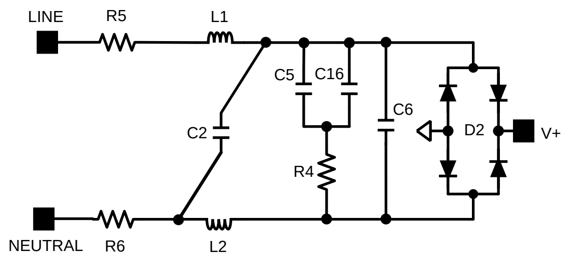


Figure 34. Input EMI Filter

Conducted

Figure 34 shows a typical filter used with this LM3448 flyback design. In order to conform to conducted standards, a fourth order filter is implemented using inductors and "X" rated AC capacitors. If sized properly, this filter design can provide ample attenuation of the switching frequency and lower order harmonics contributing to differential noise. This combination of filter components along with any necessary damping can easily provide a passing conducted EMI signature.

Radiated

Conforming to radiated EMI standards is much more difficult and is completely dependent on the entire system including the enclosure. Reduction of dV/dt on switching edges and PCB layout iterations are frequently necessary. Consult available literature and/or an EMI specialist for help with this. Several iterations of component selection and layout changes may be necessary before passing a specific radiated EMI standard.

Interaction with Dimmers

In general input filters and forward phase dimmers do not work well together. The TRIAC needs a minimum amount of holding current to function. The converter itself is demanding a certain amount of current from the input to provide to its output, and the input filter is providing or taking current depending upon the dV/dt of the capacitors. The best way to deal with this problem is to minimize filter capacitance and increase the regulated hold current until there is enough current to satisfy the dimmer and filter simultaneously.

13.4 Inrush Limiting and Damping

Inrush

With a forward phase dimmer, a very steep rising edge causes a large inrush current every cycle as shown in Figure 35. Series resistance (R5, R6) can be placed between the filter and the TRIAC to limit the effect of this current on the converter and to provide some of the necessary holding current at the same time. This will degrade efficiency but some inrush protection is always necessary in any AC system due to startup. The size of R5 and R6 are best found experimentally as they provide attenuation for the whole system.

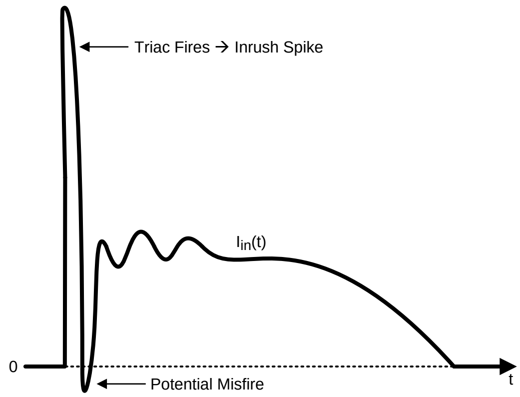


Figure 35. Inrush Current Spike

Damper

The inrush spike can also excite a resonance between the input filter of the TRIAC and the input filter of the converter. The associated interaction can cause the current to ring negative, as shown in Figure 35, thereby shutting off the TRIAC. A TRIAC damper can be placed between the dimmer and the EMI filter to absorb some of the ringing energy and reduce the potential for misfires. The damper is also best sized experimentally due to the large variance in TRIAC input filters. Resistors R5 and R6 can also be increased to help dampen the ringing at the expense of some efficiency and power factor performance.

14 Design Calculations

The following is a step-by-step procedure with calculations for a 120V, 6.5W non-isolated buck converter design.

14.1 Specifications

$V_{IN(MAX)}$ = 135VAC

$V_{IN(NOM)}$ = 120VAC

$V_{IN(MIN)}$ = 85VAC

P_{OUT} = 6.5W

V_{OUT} = 36V

I_{LED} = 181mA

Efficiency,η = 80%

f_L = 60Hz

$f_{SW(MAX)}$ =75kHz

$T_{S(MIN)}$ =13.33µs

Δv_{OUT} = 1V

Δv_{IN-PK} = 35V

SW FET $V_{DS(MAX)}$ = 600V

SW FET R_{DS-ON} = 3.5Ω

$V_{f(D4)}$ = 0.8V

V_{CC} = 12V

$V_{Z(D7)}$=12V

R8=49.9kΩ

$V_{GS(Q1)}$=0.7V

14.2 Preliminary Calculations

Nominal peak input voltage:

$$V_{IN-PK(MAX)} = 135V \times \sqrt{2} = 191V$$
$$V_{IN-PK(NOM)} = 120V \times \sqrt{2} = 170V$$
$$V_{IN-PK(MIN)} = 85V \times \sqrt{2} = 120V \quad (29)$$

Calculate minimum on-time and verify it's greater than 200ns:

$$t_{ON(MIN)} = \frac{\left(\frac{1}{0.8}\right)\left(\frac{36V}{191V}\right)}{75kHz} = 3.14\mu s \quad (30)$$

Calculate off-time:

$$t_{OFF} = 13.33\mu s - 3.14\mu s = 10.19\mu s \quad (31)$$

From Figure 29, choose R14=2.0Ω for 6.5W output power with 12 LEDs.

14.3 FLTR2 AC-LINE Injection

Choose $V_{INJECT(NOM)}$=1.0V

Choose R2=R7=274kΩ

Calculate R15:

$$R15 = \frac{\left(V_{INJECT(NOM)} \times (R2 + R7)\right)}{\left(V_{IN-PK(NOM)} - V_{INJECT(NOM)}\right)} \quad (32)$$

or,

$$R15 = \frac{(1.0V \times 548k\Omega)}{(170V - 1.0V)} = 3.24k\Omega \quad (33)$$

Calculate maximum FLTR2 pin voltage and verify it is less than 1.25V:

$$V_{FLTR2(MAX)} = 0.0024 \times 135V_{RMS} + 0.708V = 1.032V \quad (34)$$

Calculate minimum FLTR2 pin voltage:

$$V_{FLTR2(MIN)} = 0.0024 \times 85V_{RMS} + 0.708V = 0.912V \quad (35)$$

14.4 Inductor

Calculate peak inductor currents at the minimum and maximum peak input voltages:

$$I_{L-PK-MAX(VIN-PK-MIN)} = \frac{0.912V}{2.0\Omega} = 0.456A$$
$$I_{L-PK-MAX(VIN-PK-MAX)} = \frac{1.032V}{2.0\Omega} = 0.516A \quad (36)$$

Calculate inductor ripple currents at the minimum and maximum peak input voltages based on 80% of maximum peak inductor currents:

$$\Delta i_{L(VIN-PK-MIN)} = 0.456A \times 0.8 = 0.365A$$
$$\Delta i_{L(VIN-PK-MAX)} = 0.516A \times 0.8 = 0.413A \quad (37)$$

Verify that converter is in CCM operation at the minimum peak input voltage:

$$I_{L-PK-MIN(VIN-PK-MIN)} = 0.456A - 0.365A = 0.091A \quad (38)$$

Calculate inductor value:

$$L = 3.14\mu s\left(\frac{191V-36V}{0.413A}\right) = 1.18mH \quad (39)$$

14.5 COFF Current Source

Choose capacitor C12=470pF.

Calculate resistor R16:

$$R16 = \frac{-10.19\mu s}{470pF\left[\ln\left(1-\frac{1.276V}{12V}\right)\right]} = 193k\Omega \quad (40)$$

Calculate maximum on-time, minimum switching frequency and maximum switching period:

$$t_{ON(MAX)} = \frac{(1.18mH \times 0.365A)}{(120V-36V)} = 5.11\mu s$$
$$f_{SW(MIN)} = \frac{1}{(5.11\mu s + 10.19\mu s)} = 65.4kHz$$
$$T_{S(MAX)} = \frac{1}{65.4kHz} = 15.3\mu s \quad (41)$$

Calculate maximum and minimum duty cycles:

$$D_{MAX} = \frac{5.11\mu s}{15.3\mu s} = 0.334$$
$$D_{MIN} = \frac{3.14\mu s}{13.33\mu s} = 0.236 \quad (42)$$

14.6 SW FET

Calculate maximum peak SW FET current:

$$I_{SWFET-PK(MAX)} = 0.516A \tag{43}$$

Calculate maximum RMS SW FET current:

$$I_{SWFET-RMS(MAX)} = 181mA \times \sqrt{0.334} \times \sqrt{\left(1 + \frac{1}{3}\left(\frac{0.365}{181mA}\right)^2\right)} = 0.160A \tag{44}$$

Calculate maximum power dissipation:

$$P_{SWFET(MAX)} = (0.160A)^2 \times 3.5\Omega = 0.090W \tag{45}$$

14.7 Current Limit

Calculate peak inductor current limit:

$$I_{LIM} = \frac{1.27V}{2.0\Omega} = 0.635A \tag{46}$$

Power dissipation:

$$P_{(R14)} = (0.160)^2 \times 2.0\Omega = 0.051W \tag{47}$$

Resulting component choice:

$$R14 = 2.0\Omega,\ 0.125W \tag{48}$$

14.8 Re-circulating Diode

Maximum reverse blocking voltage:

$$V_{RD4(MAX)} = 191V \tag{49}$$

Maximum peak diode current:

$$I_{D4-PK(MAX)} = 0.516A \tag{50}$$

Maximum RMS diode current:

$$I_{D4-RMS(MAX)} = 181mA \times \sqrt{0.764} \times \sqrt{\left(1 + \frac{1}{3}\left(\frac{0.413}{181mA}\right)^2\right)} = 0.261A \tag{51}$$

Maximum power dissipation:

$$P_{D4(MAX)} = 0.261A \times 0.8V = 0.209W \tag{52}$$

Resulting component choice:

$$D4 = 300V, 1A \tag{53}$$

14.9 PassFET

Calculate maximum peak voltage:

$$V_{Q1} = V_{IN-PK(MAX)} = 191V \tag{54}$$

Calculate current:

$$I_{Q1} = \frac{12V - 0.7V}{49.9k\Omega} = 226\mu A \tag{55}$$

Calculate maximum power dissipation:

$$P_{Q1} \approx 191V \times 226\mu A = 43mW \tag{56}$$

Resulting component choice:

$$Q1 = 260mA,\ 240V \tag{57}$$

14.10 Input Capacitance

Minimum capacitance:

$$(C1 || C10) = \frac{1.18mH \times (0.456A)^2}{\left(120V + \frac{35V}{2}\right)^2 - \left(120V - \frac{35V}{2}\right)^2} = 29nF \tag{58}$$

AC Voltage rating:

$$V_{C1(AC\ Rating)} > 135\ V_{RMS} \tag{59}$$

DC Voltage rating:

$$V_{C1(DC\ Rating)} > 191V + \frac{35V}{2} > 208V \tag{60}$$

Resulting component choice:

$$C1 = 0.047\mu F, 400V \tag{61}$$

14.11 Output Capacitance

Minimum capacitance:

$$C3 = \frac{6.5W}{(2\pi \times 60Hz \times 36V \times 1V)} = 479\mu F \tag{62}$$

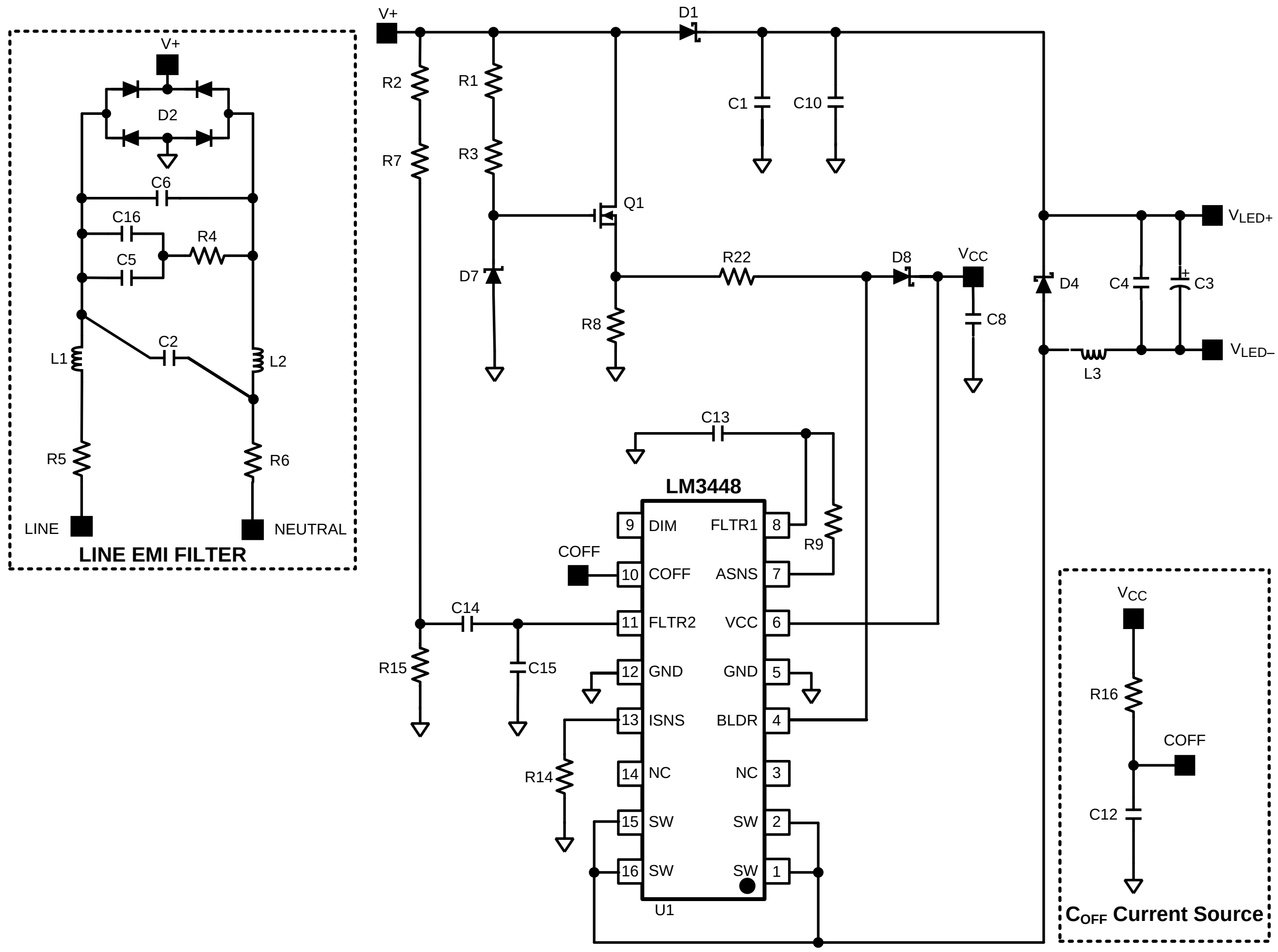
Voltage rating:

$$V_{C3} > 36V \tag{63}$$

Resulting component choice:

$$C3 = 470\mu F, 50V \tag{64}$$

15 Evaluation Board Schematic



WARNING

The LM3448 evaluation board has exposed high voltage components that present a shock hazard. Caution must be taken when handling the evaluation board. Avoid touching the evaluation board and removing any cables while the evaluation board is operating. Isolating the evaluation board rather than the oscilloscope is highly recommended.

16 Bill of Materials

Part ID	Description	Manufacturer	Part Number
C1, C10	CAP CER 47000PF 500V X7R 1210	Johanson Dielectrics	501S41W473KV4E
C2, C6	CAP FILM MKP .015UF 310VAC X2	Vishay/BC Comp	BFC233820153
C3	CAP 470UF 50V ELECT PW RADIAL	Nichicon	UPW1H471MHD
C4	DNP	DNP	DNP
C5, C16	CAP CER .15UF 250V X7R 1210	TDK	C3225X7R2E154K
C8	Ceramic, X5R, 16V, 20%	MuRata	GRM32ER61C476ME15L
C12	Ceramic, X7R, 50V, 10%	MuRata	GRM188R71H471KA01D
C13, C15	Ceramic, X7R, 16V, 10%	MuRata	GRM188R71C104KA01D
C14	Ceramic, X7R, 16V, 10%	MuRata	GRM188R71C474KA88D
D1, D8	DIODE SCHOTTKY 1A 200V PWRDI 123	Diodes Inc.	DFLS1200-7
D2	RECT BRIDGE GP 400V 0.5A MINIDIP	Diodes Inc.	RH04DICT-ND
D4	DIODE FAST 1A 300V SMA	Fairchild	ES1F
D7	DIODE ZENER 15V 500MW SOD-123	Fairchild Semi	MMSZ5245B
J5, J10	CONN HEADER .312 VERT 2POS TIN	Tyco Electronics	1-1318301-2
L1, L2	INDUCTOR 4700UH .13A RADIAL	TDK Corp	TSL0808RA-472JR13-PF
L3	820uH, Shielded Drum Core,	Coilcraft Inc.	MSS1038-824KL
Q1	MOSFET N-CH 240V 260MA SOT-89	Infineon Technologies	BSS87 L6327
R1, R3	1%, 0.25W	Vishay-Dale	CRCW1206200kFKEA
R2, R7	1%, 0.25W	Vishay-Dale	CRCW1206274kFKEA
R4	RES 430 OHM 1/2W 5% 2010 SMD	Vishay\Dale	CRCW2010430RJNEF
R5, R6	RES 33 OHM 3W 5% AXIAL	TT Electronics/Welwyn	ULW3-33RJA1
R8	1%, 0.1W	Vishay-Dale	CRCW060349K9FKEA
R9	1%, 0.1W	Vishay-Dale	CRCW060348K7FKEA
R14	RES, 2.00 ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW12062R00FNEA
R15	RES, 3.16k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06033K16FKEA
R16	RES, 226k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603226KFKEA
R22	1%, 0.125W	Vishay-Dale	CRCW080540R2FKEA
TP1, TP2, TP3, TP4	Terminal, Turret, TH, Double	Keystone Electronics	1502-2
U1	LM3448 LED Driver	Texas Instruments	LM3448

17 PCB Layout

NOTE: Spacing between traces and components of this evaluation board are based on high voltage recommendations for designs that will be potted. Users are cautioned to satisfy themselves as to the suitability of this design for the intended end application and take any necessary precautions where high voltage layout and spacing rules must be followed.

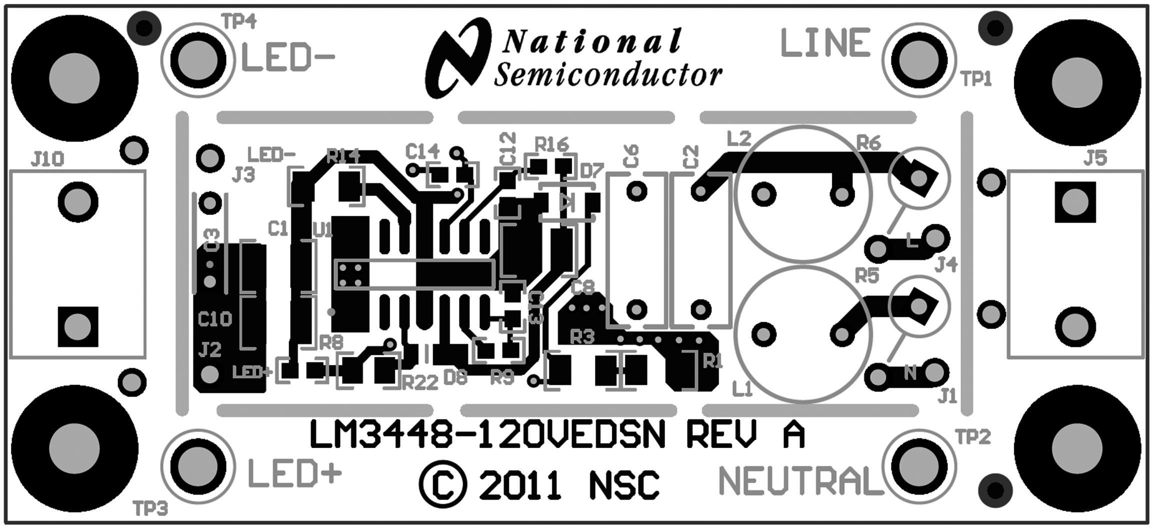


Figure 36. Top Layer

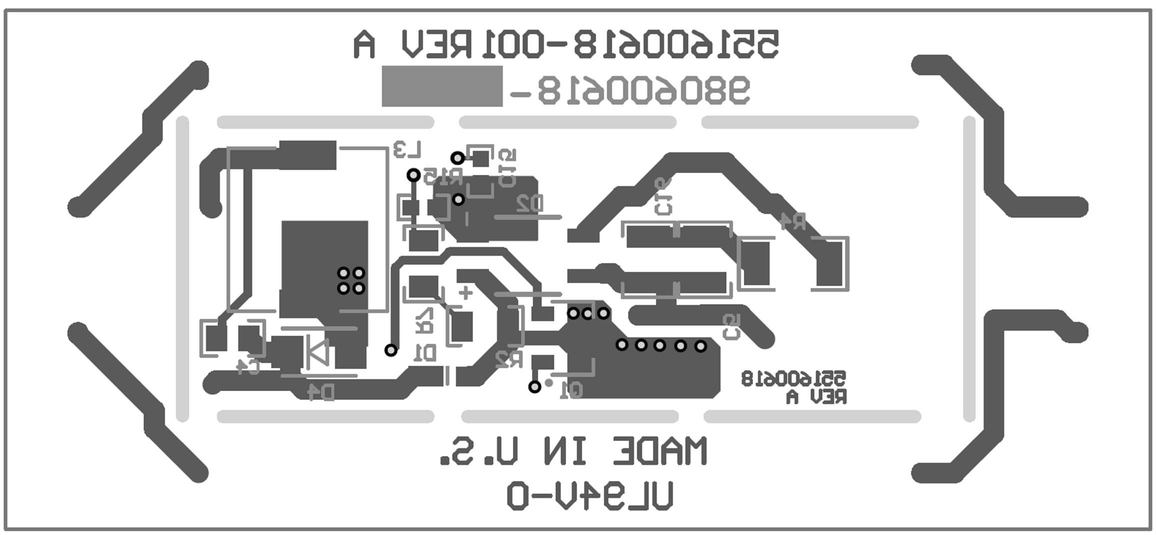


Figure 37. Bottom Layer

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