AN-2107 LM21212-1 Evaluation Board

1 Introduction

This evaluation board provides a solution to examine the high efficiency LM21212-1 buck switching regulator. The LM21212-1 is capable of driving up to 12A of continuous load current with excellent output voltage accuracy due to its ±1% internal reference. This device also features a clock synchronization input that allows the switching frequency to be synchronized to an external clock source. The 300 kHz to 1.5 MHz frequency synchronization range enables the user to minimize the power stage component size, while still allowing for high efficiency. The LM21212-1 is capable of down converting from an input voltage between 2.95V and 5.5V. Fault protection features include current limit, output power good, and output over-voltage protection. The dual function soft-start/tracking pin can be used to control the startup response of the LM21212-1, and the precision enable pin can be used to easily sequence the LM21212-1 in applications with sequencing requirements.

The LM21212-1 evaluation board has been optimized to work from 2.95V to 5.5V, achieving a balance between overall solution size and regulator efficiency. The evaluation board measures just under 2" x 2" on a four layer PCB, and exhibits a junction-to-ambient thermal impedance (θ_{JA}) of 24°C/W with no air flow. The power stage and compensation components of the LM21212-1 evaluation board have been optimized for an input voltage of 5V, but for testing purposes, the input can be varied across the entire operating range. The output voltage of the evaluation board is nominally 1.2V, but this voltage can be easily changed to any voltage between 0.6V and V_{IN} by modifying the feedback resistor network.

2 Evaluation Board Schematic

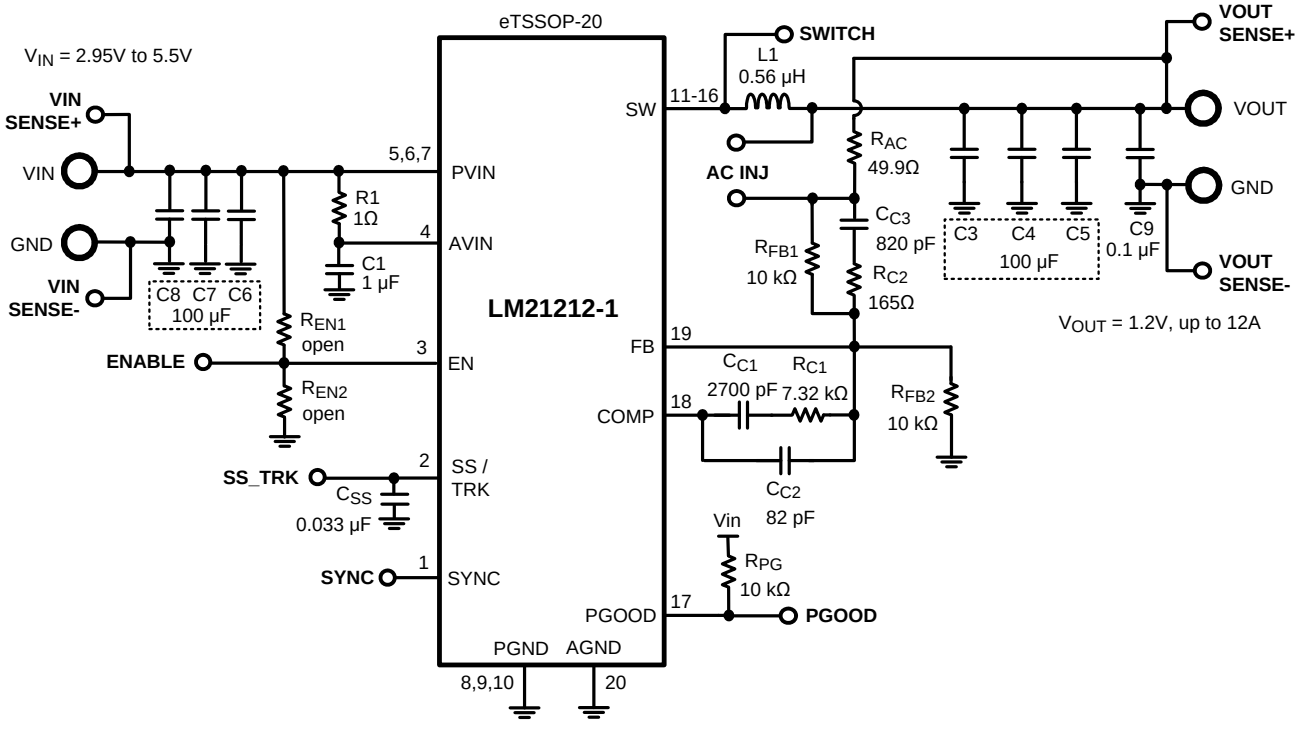

Figure 1. Evaluation Board Schematic

3 Powering and Loading Considerations

Read this entire page prior to attempting to power the evaluation board.

3.1 Quick Setup Procedure

1. Set the input source current limit to 10A. Turn off the input source. Connect the positive output of the input source to V_{IN} and the negative output to the corresponding GND.
2. Connect the load (with 12A capability) to V_{OUT} for the positive connection and GND for the negative connection.
3. Leave the ENABLE pin open for normal operation.
4. Set the input source voltage to 5V. The load voltage should be in regulation with a nominal 1.2V output.
5. Slowly increase the load while monitoring the load voltage at V_{OUT}. It should remain in regulation with a nominal 1.2V output as the load is increased up to 12A.
6. Slowly sweep the input source voltage from 2.95V to 5.5V. The load voltage should remain in regulation with a nominal 1.2V output. If desired, the output of the device can be disabled by connecting the ENABLE pin to GND.
7. Connect a 2.0V square-wave positive signal between SYNC and GND to vary the frequency of operation as desired.

3.2 Powering Up

It is suggested that the load power be kept low during the first power up. Once the device is powered up, immediately check for 1.2V at the output.

A quick efficiency check is the best way to confirm that everything is operating properly. If something is amiss you can be reasonably sure that it will affect the efficiency adversely. Few parameters can be incorrect in a switching power supply without creating losses and potentially damaging heat.

Some voltage supplies can exhibit severe voltage overshoot during high current transients. If a supply overshoots above 6.0V, damage to the LM21212-1 can occur. For these supplies, a large capacitor across the terminals of the supply (1000µF) can alleviate this problem.

3.3 Over Current Protection

The evaluation board is configured with over-current protection. This function is completely contained in the LM21212-1. The peak current is limited to approximately 17A.

Table 1. Connection Descriptions

Terminal Silkscreen	Description
VIN	This terminal is the input voltage to the device. The evaluation board will operate over the input voltage range of 2.95V to 5.5V.
GND	These terminals are the ground connections to the device. The input power ground should be connected next to the input V_{IN} connection, and the output power ground next to the V_{OUT} connection.
VOUT	This terminal connects to the output voltage of the power supply and should be connected to the load.
ENABLE	This terminal connects to the enable pin of the device. This terminal can be left floating or driven externally. If left floating, a 2µA current source will pull the pin high, thereby enabling the device. If driven externally, a voltage typically less than 1.2V will disable the device.
SS/TRK	This terminal provides access to the SS/TRK pin of the device. Connections to this terminal are not needed for most applications. The feedback pin of the device will track the voltage on the SS/TRK pin if it is driven with an external voltage source that is below the 0.6V reference.
PGOOD	This terminal connects to the power good output of the device. This pin is pulled up through a 10 kΩ pull-up resistor to V_{IN}.
AC INJ	This terminal block allows the user to insert an AC injection signal across a 49.9Ω resistor for open-loop gain bode measurements. A jumper shorts out this resistor when it is not needed.
SWITCH	This terminal allows easy probing of the switch node. Do not apply any external voltage source to this pin.
SYNC	This terminal connects to the SYNC pin of the device. The LM21212-1 can synchronize the SWITCH pin to a SYNC signal with a frequency between 300kHz and 1.5MHz. If this pin is left open, the switching frequency will default to 1MHz.
VIN_SENSE+, VIN_SENSE- VOUT_SENSE+, VOUT_SENSE-	These terminals allow a sense connection on the board for accurate V_{IN} and V_{OUT} measurements, respectively.

4 Performance Characteristics

Efficiency Plots

Figure 2 shows the conversion efficiency versus output current for a 5V input voltage for 500kHz, 1MHz, and 1.5MHz f_{SW}.

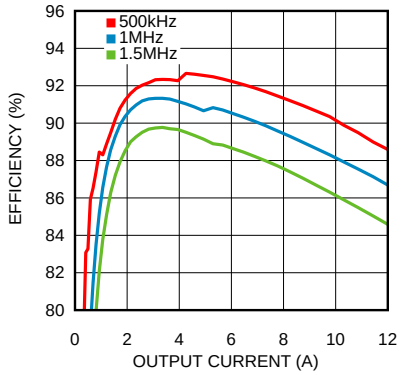

Figure 2. Conversion Efficiency Versus Output Current

Turn-on Waveform

A soft-start sequence occurs when applying power to the LM21212-1 evaluation board. Figure 3 shows the output voltage during a typical start-up sequence.

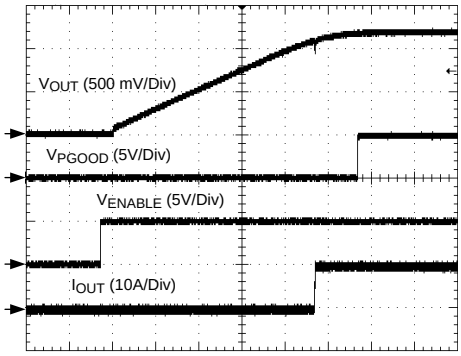

Figure 3. (2 ms/DIV)

Output Ripple Waveform

Figure 4 shows the output voltage ripple. This measurement was taken with the scope probe tip placed on the output capacitor C9 VOUT connection and the scope probe ground "barrel" wired to the GND connection of C9. The scope bandwidth is set to 20 MHz.

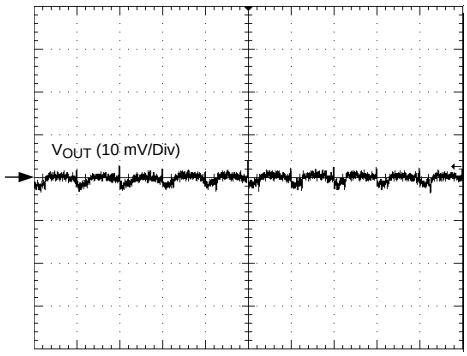

Figure 4. (1 µs/DIV)

Primary Switchnode Waveform

Figure 5 shows the typical SW pin voltage while synchronizing to an external source.

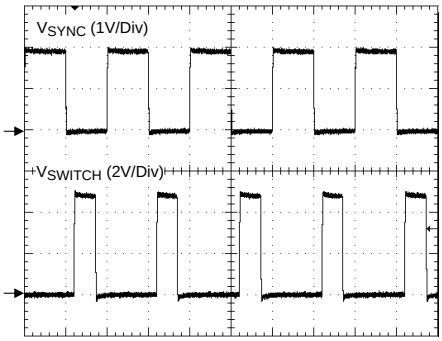

Figure 5. (1 µs/DIV)

Output Transient Response

Figure 6 shows the V_{OUT} deviation for a 3A to 12A output current transient condition.

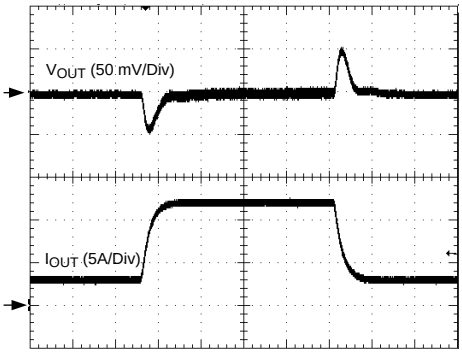

Figure 6. (100 µs/DIV)

Output Current Limit

Figure 7 shows the V_{OUT} output response to an output current limit condition.

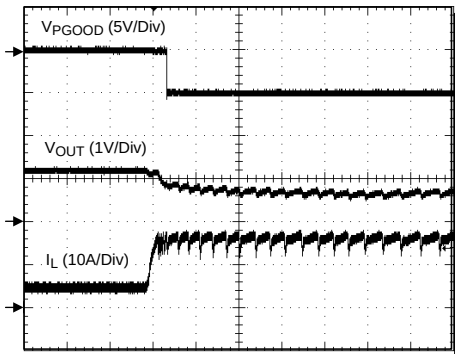

Figure 7. (100 µs/DIV)

Open Loop Bode Response

Figure 8 shows the open loop bode response generated by inserting a stimulus signal across R_{AC} and using a network analyzer to plot the gain and phase.

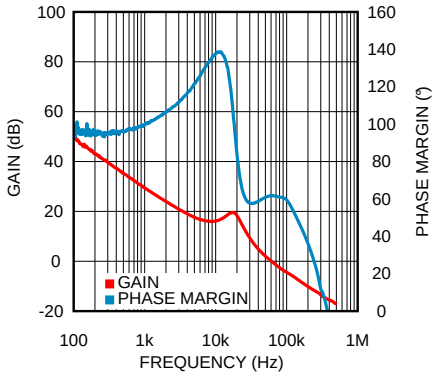

Figure 8. Open Loop Bode Response

5 Bill of Materials

The Bill of Materials is shown below, including the manufacturer and part number.

Table 2. Bill of Materials

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
AC INJ	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-102-07-G-S	1
C1	CAP, CERM, 1 uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C3, C4, C5, C6, C7, C8	CAP, CERM, 100 uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	6
C9	CAP, CERM, 0.1 uF, 50V, +/-10%, X7R, 0603	TDK	C1608X7R1H104K	1
C_{C1}	CAP, CERM, 2700 pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H272JA01D	1
C_{C2}	CAP, CERM, 82 pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H820JA01D	1
C_{C3}	CAP, CERM, 820 pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H821JA01D	1
C_{SS}	CAP, CERM, 0.033 uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
GND_FI, GND_FO, VIN_F, VOUT_F	Standard Banana Jack, Uninsulated, 15A	Johnson Components	108-0740-001	4
L1	Inductor, Shielded Drum Core, Powdered Iron, 560nH, 27.5A, 0.0018 ohm, SMD	Vishay-Dale	IHLP4040DZERR56M01	1
R1	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{AC}	RES, 49.9 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060349R9FKEA	1
R_{C1}	RES, 7.32 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06037K32FKEA	1
R_{C2}	RES, 165 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603165RFKEA	1
R_{FB1}, R_{FB2}, R_{PG}	RES, 10 kohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0JKEA	3
SH-J1	Shunt, 100mil, Gold plated, Black	Samtec Inc.	SNT-100-BK-G	1
U1	12A Buck DC/DC Converter	Texas Instruments	LM21212-1	1

6 Component Selection

This section provides a walk-through of the design process of the LM21212-1 evaluation board. Unless otherwise indicated all equations assume units of amps (A) for current, farads (F) for capacitance, henries (H) for inductance, and volts (V) for voltages.

6.1 Input Capacitors: C1, C2, C3

The required RMS current rating of the input capacitor for a buck regulator can be estimated by the following equation:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{D(1 - D)} \quad (1)$$

The variable D refers to the duty cycle, and can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

From this equation, it follows that the maximum $I_{CIN(RMS)}$ requirement will occur at a full 12A load current with the system operating at 50% duty cycle. Under this condition, the maximum $I_{CIN(RMS)}$ is given by:

$$I_{CIN(RMS)} = 12A \sqrt{0.5 \times 0.5} = 6A \quad (3)$$

Ceramic capacitors feature a very large I_{RMS} rating in a small footprint, making a ceramic capacitor ideal for this application.

The input capacitors also keep the input stable during load transient conditions. If the input capacitance is too low, the input can drop below the UVLO threshold and cause the device to disable the output. This may result in repetitive dropout and re-enable oscillation, or "motorboating". To give the user the ability to operate with a low V_{IN} voltage, three 100 µF ceramic capacitors were used on the input.

6.2 Inductor: L1

The value of the inductor was selected to allow the device to achieve a 5V to 1.2V conversion at 500kHz to provide a peak to peak ripple current of 3.2A, which is about 27% of the maximum output current. To have an optimized design, generally the peak to peak inductor ripple current should be kept to within 20% to 40% of the rated output current for a given input voltage, output voltage and operating frequency. The peak to peak inductor ripple current can be calculated by the equation:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \tag{4}$$

Once an inductance value is calculated, an actual inductor needs to be selected based on a trade-off between physical size, efficiency, and current carrying capability. For the LM21212-1 evaluation board, a Vishay IHLP4040DZERR56M01 inductor offers a good balance between efficiency (1.8 mΩ DCR) and size.

6.3 Output Capacitor: C3, C4, C5, C9

The value of the output capacitor in a buck regulator influences the voltage ripple that will be present on the output voltage as well as the large signal output voltage response to a load transient. Given the peak-to-peak inductor current ripple (ΔI_{P-P}) the output voltage ripple can be approximated by the equation:

$$\Delta V_{OUT} = \Delta I_{P-P} \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right] \tag{5}$$

The variable R_{ESR} above refers to the ESR of the output capacitor. As can be seen in the above equation, the ripple voltage on the output can be divided into two parts, one of which is attributed to the AC ripple current flowing through the ESR of the output capacitor and another due to the AC ripple current actually charging and discharging the output capacitor. The output capacitor also has an effect on the amount of droop that is seen on the output voltage in response to a load transient event.

For the evaluation board, three 100µF ceramic capacitors were selected to provide good transient and DC performance. Ceramic capacitors give the lowest R_{ESR} of any standard capacitor chemistries, resulting in the lowest output ripple for the given ripple current. Ceramic capacitors (especially high capacitance, small package multi-layer types, or MLCC) lose thier capacitance as the DC voltage is increased. For this configuration, the actual capacitance value was approximated to be 50 µF per capacitor, or 150 µF total. This is lower than measured capacitance values for 1.2V, but will allow the user to change the output voltage up to 3.3V and maintain stability.

6.4 Soft-Start Capacitor: C_{SS}

A soft-start capacitor can be used to control the startup time of the LM21212-1 voltage regulator. The startup time of the regulator when using a soft-start capacitor can be estimated by the following equation:

$$t_{SS} = \frac{0.6V \times Css}{I_{SS}} \tag{6}$$

For the LM21212-1, I_{SS} is nominally 5 µA. For the evaluation board, the soft-start time has been designed to be roughly 10 ms, resulting in a C_{SS} capacitor value of 33 nF.

6.5 Compensation Components: C_{C1}, C_{C2}, C_{C3}, R_{C1}, R_{C2}

These components are used in conjunction with the error amplifier to create a type 3 voltage-mode compensation network. The analysis of type 3 compensation is outside the scope of this document, but an example of the step-by-step procedure to generate comensation component values is given. The parameters needed for the compensation values are given in the table below.

Table 3. Parameters Needed for Compensation Values

Parameter	Value
V_{IN}	5.0V
V_{OUT}	1.2V
I_{OUT}	12A
$f_{CROSSOVER}$	80 kHz
L	0.56 µH
R_{DCR}	1.8 mΩ
C_O	150 µF
R_{ESR}	1.0 mΩ
ΔV_{RAMP}	0.8V
f_{SW}	500 kHz

where ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8 V), $f_{CROSSOVER}$ is the frequency at which the open-loop gain is a magnitude of 1, R_{DCR} is the effective DC resistance of the inductor, R_{ESR} is the effective resistance of the output capacitor, and C_O is the effective output capacitance at the programmed output voltage. It is recommended that $f_{CROSSOVER}$ not exceed one-fifth of the switching frequency. The output capacitance, C_O, depends on capacitor chemistry and bias voltage. For Multi-Layer Ceramic Capacitors (MLCC), the total capacitance will degrade as the DC bias voltage is increased. Measuring the actual capacitance value for the output capacitors at the output voltage is recommended to accurately calculate the compensation network. Note that it is more conservative, from a stability standpoint, to err on the side of a smaller output capacitance value in the compensation calculations rather than a larger, as this will result in a lower bandwidth but increased phase margin.

First, the value of R_{FB1} should be chosen. A typical value is 10kΩ. From this, the value of R_{C1} can be calculated to set the mid-band gain so that the desired crossover frequency is achieved.

$$R_{C1} = \frac{f_{CROSSOVER}}{f_{LC}} \bullet \frac{\Delta V_{RAMP}}{V_{IN}} \bullet R_{FB1}$$
$$= \frac{80\ kHz}{17.4\ kHz} \frac{0.8\ V}{5.0\ V} 10\ k\Omega$$
$$= 7.4\ k\Omega \quad (7)$$

Next, the value of C_{C1} can be calculated by placing a zero at half of the LC double pole frequency.

$$C_{C1} = \frac{1}{\pi f_{LC} R_{C1}}$$
$$= 2.49\ nF \quad (8)$$

Now the value of C_{C2} can be calculated to place a pole at half of the switching frequency.

$$C_{C2} = \frac{C_{C1}}{\pi f_{SW} R_{C1} C_{C1} - 1}$$
$$= 90\ pF \quad (9)$$

R_{C2} can then be calculated to set the second zero at the LC double pole frequency.

$$R_{C2} = \frac{R_{FB1} f_{LC}}{f_{ESR} - f_{LC}}$$
$$= 166\Omega \quad (10)$$

Last, C_{C3} can be calculated to place a pole at the same frequency as the zero created by the output capacitor ESR.

$$C_{C3} = \frac{1}{2\pi f_{ESR} R_{C2}}$$
$$= 898\ pF \quad (11)$$

The standard values used for the above calculations are given in the Bill of Materials.

6.6 Feedback Resistors: R_{FB1}, R_{FB2}, and R_{AC}

The resistors labeled R_{FB1} and R_{FB2} create a voltage divider from V_{OUT} to the feedback pin that is used to set the output of the voltage regulator. Nominally, the output of the LM21212-1 evaluation board is set to 1.2V, giving resistor values of R_{FB1}= R_{FB2} = 10kΩ. If a different output voltage is required, the value of R_{FB2} can be adjusted according to the equation:

$$R_{FB1} = \left(\frac{V_{OUT}}{0.6} - 1 \right) \times R_{FB2} \tag{12}$$

R_{FB1} does not need to be changed from its value of 10kΩ. Resistor R_{AC} has a value of 49.9Ω and is provided as an injection point for loop stability measurements, as well as, a way to further tweak the output voltage accuracy to account for resistor tolerance values differing from ideal calculated values. The jumper is used to short out R_{AC} when not needed.

6.7 Programmable UVLO: R_{EN1} and R_{EN2}

The resistors labeled R_{EN1} and R_{EN2} create a voltage divider from V_{IN} to the enable pin that can be used to enable the device above a programmed V_{IN}, effectively creating a programmable UVLO voltage above the device's internal UVLO (nominally 2.7V). To allow evaluation of the device down to 2.95V, these components are not installed. To change the turn-on threshold of the device a 10 kΩ resistor is recommended for R_{EN1} and the value of R_{EN2} can be calculated using the equation:

$$R_{EN1} = \left(\frac{V_{TO}}{1.35} - 1 \right) \times R_{EN2} \tag{13}$$

where V_{TO} is the desired V_{IN} voltage at which the device will enable.

7 PCB Layout

The PCB was manufactured with 2oz. copper outer layers, and 1oz. copper inner layers. Twenty 8 mil. diameter vias placed underneath the device, along with addional vias placed throughout the ground plane around the device, help improve the thermal dissipation of the board.

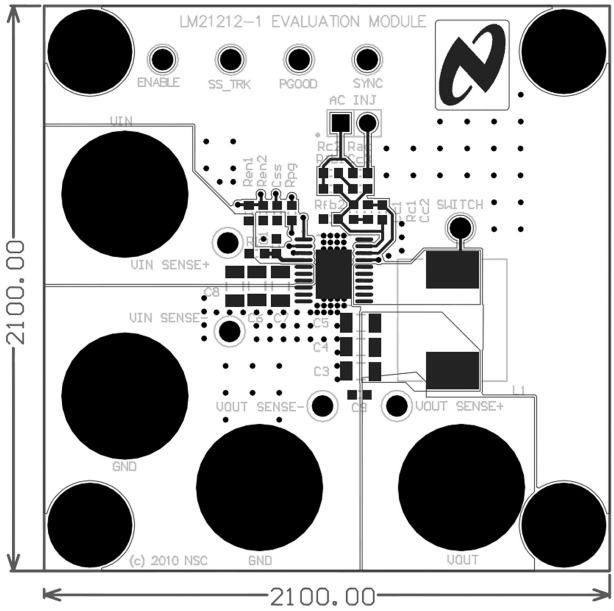

Figure 9. Top Layer (Copper planes outlined in grey)

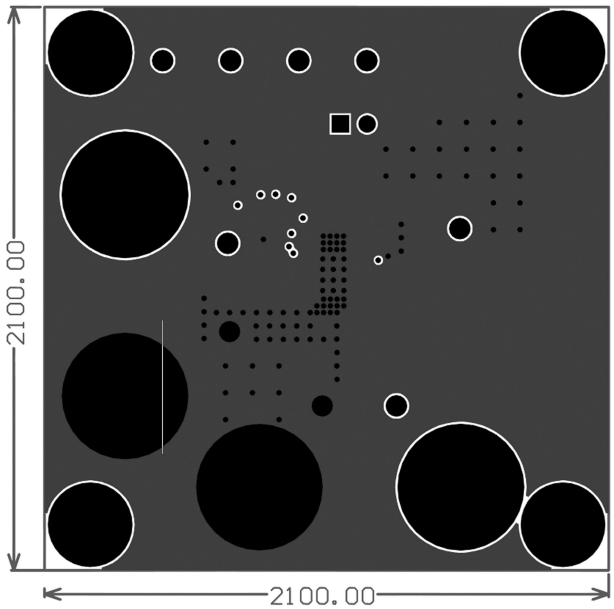

Figure 10. Mid Layer1

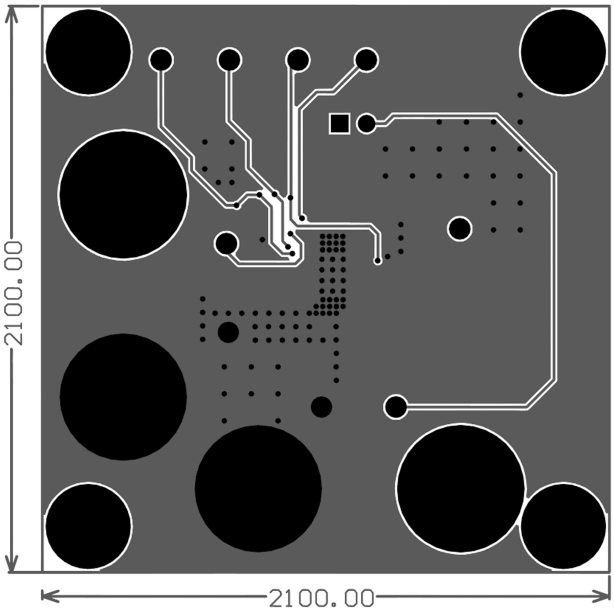

Figure 11. Mid Layer2

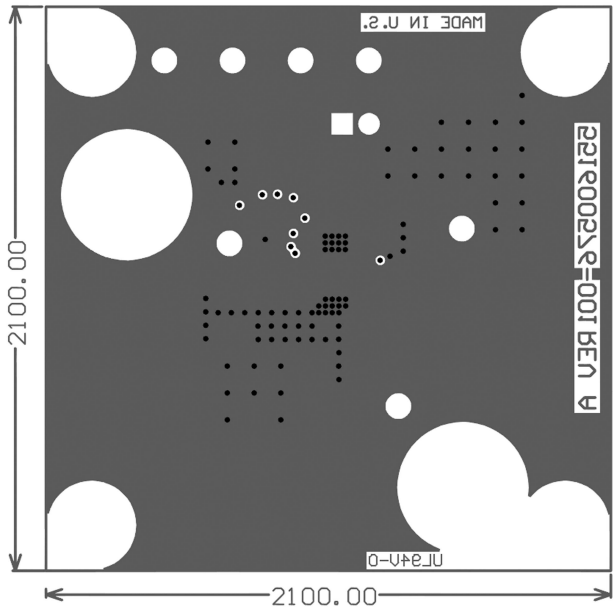

Figure 12. Bottom Layer

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