Application Report
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Design Considerations for LMG1205 Advanced GaN FET Driver During High-Frequency Operation

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ABSTRACT

The LMG1205 device is designed to drive the high-side and low-side enhancement mode Gallium Nitride (GaN) FETs in a half-bridge configuration. The floating high-side gate is capable of driving enhancement mode GaN FETs up to 100 V. Used with the DSBGA package the LMG1205 device is especially suited for high-frequency operation. Care must be taken at high-frequency operation to ensure that adequate thermal design tolerance is present for the worst-case driver power dissipation. Furthermore, a good understanding of the driver losses for different load mechanisms is very helpful in estimating the on die power loss in the GaN driver. This application report demonstrates the operation of LMG1205 device at high-frequency for hard-switching and soft-switching applications. It also provides an estimate of the losses in the driver based on calculations and an analytical approach.

Topic **Page**

1 Introduction

Half-bridge-based topologies are the most popular for medium and low voltage regulators. Due to its extremely good figure-of-merit[1] [2] [3] [4] (for both hard-switching and soft-switching converters), GaN is finding applications in high-efficiency, high-frequency converters.

Equation 1 describes the hard-switching figure-of-merit for low voltage GaN devices.

$$FOM_{HS} = (Q_{GD} + Q_{GS2}) \times R_{DS(on)} \quad (1)$$

Equation 2 describes the soft-switching figure-of-merit of GaN devices.

$$FOM_{SS} = (Q_{OSS} + Q_{G}) \times R_{DS(on)} \quad (2)$$

As hard-switching and soft-switching figures-of-merit for GaN are much better than silicon, GaN HEMT based converters can operate at much higher frequencies than conventional silicon based converters.

It is important to note that to maximize performance improvements due to the GaN superior figures-of-merit, special considerations needs to be taken with respect to the converter design. It is necessary to minimize the power loop inductance and the gate loop inductance (common source inductance) as these have an adverse impact on the converter efficiency as discussed in previously in SLPA009[5] [6].

For high-frequency converters, driver losses become important. At high frequencies, the designer must ensure that the minimum pulse width requirement of the LMG1205 device of 10 ns is not violated and the board thermal design is adequate to ensure that the driver operational junction temperature does not exceed 125°C under all operating conditions.

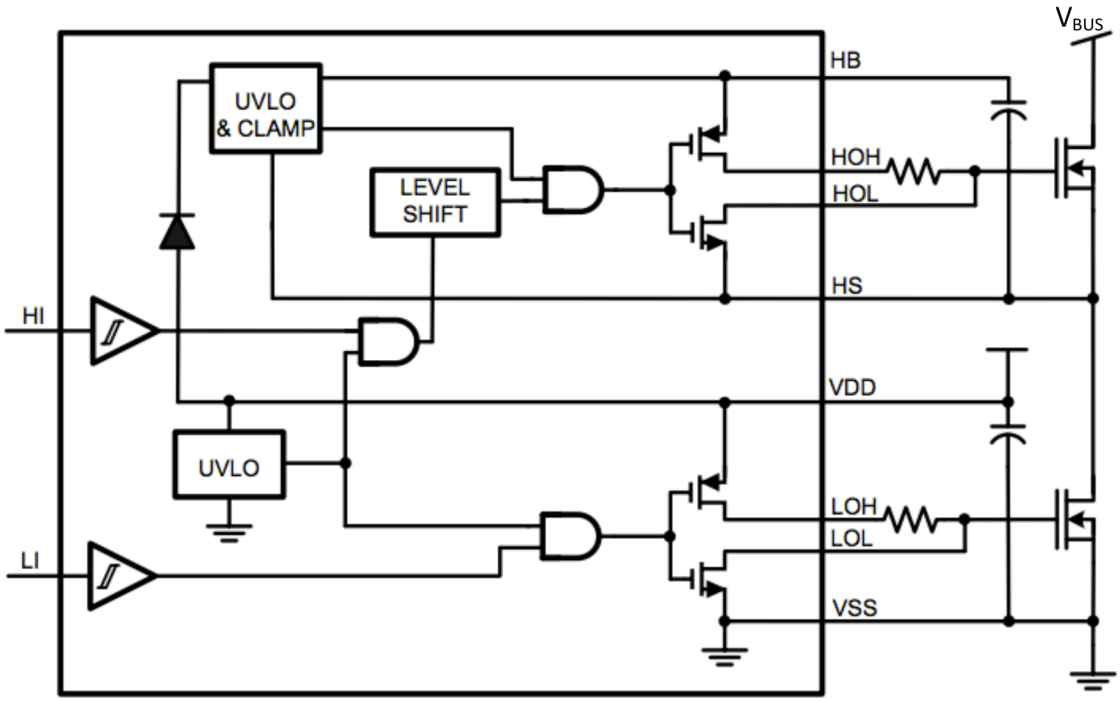


Figure 1. Block Diagram with External GaN FETs

2 Loss Mechanisms in the Gate Driver

The switching action of the GaN HEMT transistor in power applications results in losses in the driver circuit. The gate driver losses are present due to the charging and discharging of the gate capacitance. Equation 3 calculates the associated losses due to the gate capacitance.

$$P_{GATE} = V_{DRV} \times Q_G \times f_{SW}$$

where

- V_{DRV} is the amplitude of the gate drive waveform – which in the case of LM5113 is 5V
- Q_G is the total gate charge at the desired operation V_{DS} (V_{BUS}),
- f_{SW} is the switching frequency of the gate driver. (3)

This power loss (P_{GATE}) dissipats in the driver, gate resistor and the power FET. The loss is proportional to the ratio of the driver pull-up (R_{UP}) and pull-down (R_{DN}) strength, to the total gate loop resistance (R_{SERIES}). An average value of R_{UP} and R_{DN} can be generated from the current vs. voltage curves for the gate driver in the datasheet.

$$P_{DRV\_ON\_LOSS} = \frac{1}{2} x \frac{R_{UP} x P_{GATE}}{R_{UP} + R_G + R_{SERIES}} \quad (4)$$

$$P_{DRV\_OFF\_LOSS} = \frac{1}{2} \times \frac{R_{DN} \times P_{GATE}}{R_{DN} + R_G + R_{SERIES}} \quad (5)$$

$$P_{DRV} = P_{DRV\_ON\_LOSS} + P_{DRV\_OFF\_LOSS}$$

where

- $P_{DRV\_ON\_LOSS}$ is the power dissipated in the driver during the turn on event for the GaN HEMT,
- $P_{DRV\_OFF\_LOSS}$ is the power dissipated in the driver during the turn off event,
- R_G is the gate resistance of the power FET (6)

Calculations and values for R_{UP} and R_{DN} can be found in the datasheet. Note that in case an explicit value of R_{UP} and R_{DN} is not specified in the datasheet due to their non-linear nature, an approximate value can be calculated using the average source/ sink vs output voltage graphs for the drivers. Also note that P_{DRV} is the loss per gate driver and for LMG1205 both the high-side and the low-side gate driver losses need to be accounted for.

$$P_{DRV\_QG} = P_{DRV\ (HI\_SIDE)} + P_{DRV\ (LO\_SIDE)} \quad (7)$$

Added to the external gate capacitance related losses of the FETs being driven, there are also inherent driver related capacitive losses (overhead) that scale linearly with frequency.

$$P_{OVERH} = V_{DD} \times (I_{HB0} + I_{DD0}),$$

where

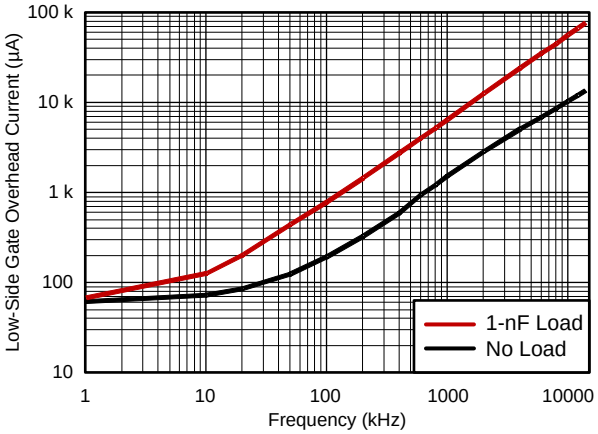
- I_{HB0} = 3.5 mA/MHz × f_{SW}(MHz), and
- I_{DD0} = 3.5 mA/MHz × f_{SW}(MHz) (8)

Thus the total driver losses are given by:

$$P_{DRV\_TOTAL} = P_{OVERH} + P_{DRV\_QG} \quad (9)$$

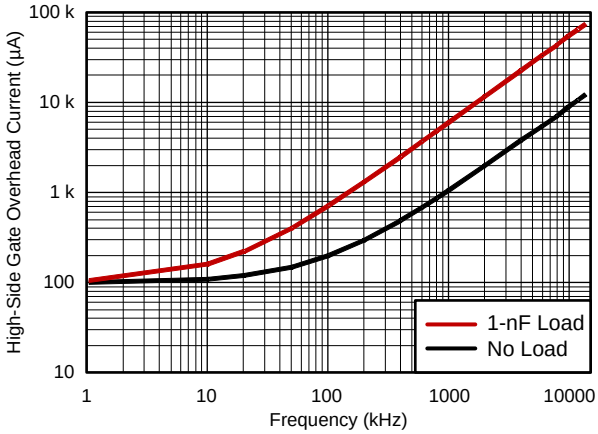
This value is used for thermal analysis purposes. VDD is the input voltage at the gate driver, IHBO and IDDO are the high-side gate and low-side gate overhead currents respectively.

Figure 2 and Figure 3 show the measured IHBO and IDDO for different frequencies. These currents are representative of the gate driver power loss for the high-side and low-side driver, respectively. Figure 2 and Figure 3 also include the LMG1205 quiescent current. Use the 0-nF curve for estimating the IHBO and IDDO current at the desired switching frequency for calculating the overhead losses.



Ta= 27°C

Figure 2. Low-Side Gate Overhead Current vs Frequency



Ta= 27°C

Figure 3. High-Side Gate Overhead Current vs Frequency

3 Loss Mechanisms Due to the Gate Driver

Beyond the actual losses dissipated within the LMG1205 gate driver, there are additional losses that can be incurred in the system due to the gate driver. These losses are related to the following two main items as shown in Figure 4: The parasitic well capacitance C_{PARA_WELL} and the bootstrap diode reverse recovery losses Q_{RR_BTST}. Figure 4 shows a Partial driver and bridge circuit with external GaN FETs showing gate driver parasitic elements.

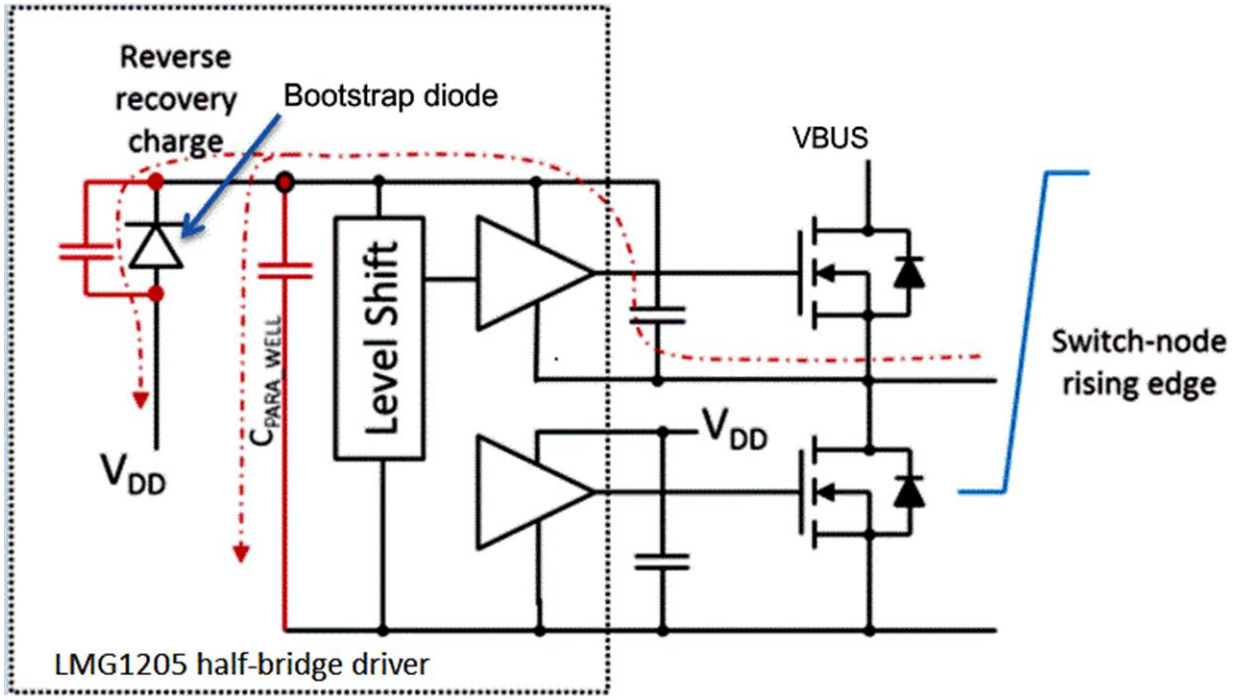


Figure 4. Partial Driver and Bridge Circuit

3.1 Well Capacitance

There is a parasitic loss associated with the well capacitance between the float high-side driver and GND. This capacitance, C_{PARA_WELL}, is in the range of approximately 40 pF for the LMG1205. The well capacitance manifests as additional switch-node to GND capacitance (in parallel with the GaN FET C_{OSS} capacitance). For hard-switching applications, this translates into an additional capacitive loss component.

$$P_{LOSS\_CWELL} = ½ \times C_{PARA\_WELL} \times V_{BUS}^2 \times f_{SW} \quad (10)$$

The additional 40 pF of capacitance is typically insignificant in relation to large MOSFETs or large GaN FETs C_{OSS} values, but when driving small GaN FETs this additional component cannot be neglected. V_{BUS} is the voltage on the power stage half bridge as shown in Figure 4.

This additional loss component is supplied by V_{BUS} supply and is dissipated during the turn-on of the hard-switching device (the high-side device in the case of a buck converter).

For soft-switching applications where the switch-node voltage is load commutated (such as in ZVS switching or the falling edge in a buck converter), the additional well capacitance does not induce any losses (nor does the switching device C_{OSS}), but it increases the commutation time (Δt) as calculated in Equation 11.

$$\Delta t \approx C_{PARA\_WELL} \times V_{BUS} / I_{PEAK} \quad (11)$$

where

- I_{PEAK} is the (constant) inductor current at the start of the ZVS switch-node commutation

The dead-time needs to be adjusted accordingly to accommodate this additional commutation time.

3.2 Bootstrap Diode Reverse Recovery

The bootstrap circuit, along with the built in voltage clamp is required to generate the high-side gate drive. In addition to the power dissipation due to the losses associated with the gate charge, the bootstrap circuitry also contributes to power loss. The LMG1205 datasheet states that the bootstrap diode reverse recovery charge, $Q_{RR\_BTST,}$ is approximately 4 nC. This is taken at 50 V and includes the above mentioned well capacitance (as any reverse recovery measurement will also include this capacitance). Therefore if the well capacitance is accounted for separately (as unlike the reverse recovery, it if present on both rising and falling edges), the actual diode recovery charge is only approximately 2 nC. Some typical values are shown in experimental results section.

The power loss associated with the reverse recovery charge of the bootstrap diode is:

$$P_{QRR\_BTST} = V_{BUS} \times Q_{RR\_BTST} \times f_{SW} \quad (12)$$

where

- V_{BUS} is the voltage at the high-side FET and f_{SW} is the switching frequency

Q_{RR_BTST} has a dependence on the forward current through the diode and rate of change of the forward current.[7] [8]

3.3 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side switch, dc bias power for HB under-voltage lockout circuit. The bootstrap diode reverse recovery charge and well capacitance charge flows through the bootstrap capacitor during switching node rising edges, as shown in Figure 4. The required minimum bypass capacitance can be calculated as follows:

$$C_{BTST} = \frac{Q_{GH} + I_{HB0} \times t_{ON} + Q_{RR\_BTST} + C_{PARA\_WELL} \times V_{BUS}}{\Delta V} \quad (13)$$

Q_{GH} is high-side gate charge, IHB0 is the current of the high-side driver, ton is the maximum on-time period of the high-side transistor, and ΔV is the allowable ripple on the bootstrap capacitor. A good quality, ceramic capacitor should be used for the bootstrap capacitor. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

In practical terms, a value of around 22 nF seems adequate for most applications that operate between approximately 5 MHz and 10 MHz.

4 Experimental Results

To determine experimentally the gate-driver related system losses as explained above can be done using two separate test conditions. All measurements were taken on a half-bridge evaluation board using LMG1205 in the DBGA version and EPC8009 GaN FET devices. A function generator was used to generate the PWM supply. The board included an on-board, 5-V LDO for supplying the power to LMG1205. RCD circuits were used to generate the desired dead-time intervals. In the first test, nothing was added to the switching node output and the gate drive and supply current was monitored as the switching frequency was varied from 0.5 MHz to 10 MHz. The supply voltage was kept constant at 50 V. The total supply losses are calculated and the losses for the EPC8009 devices are subtracted out. The gate driver current is measured with half of it being the high-side driver current. The resulting gate driver related power loss is shown in Figure 5. These losses are related to the well capacitance (dissipated on both switching edges), and the bootstrap diode reverse recovery (on rising edge only). To separate these components out requires a second test.

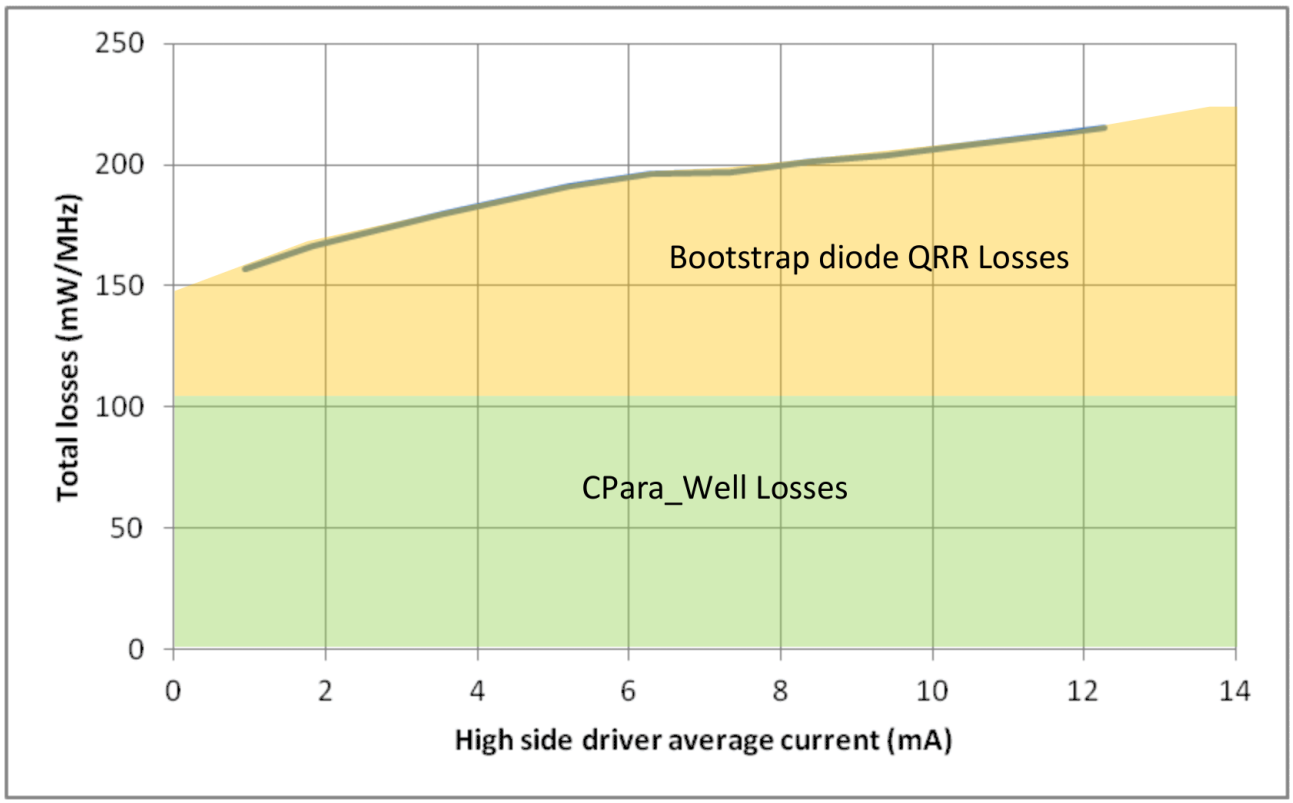


Figure 5. Gate Driver Related System Losses per Mhz vs. Gate Drive Current at 50 V_{BUS}.

For the second test, the half-bridge evaluation board is operated as a no-load buck converter or ZVS class-D converter and the deadtime is adjusted such that complete ZVS is achieved at both edges. The inductor current, I_{PEAK}, and the falling edge transition time, t_{FALL}, is measured. From this, the equivalent switch-node charge QSW_NODE can be calculated as shown in Figure 6:

$$Q_{SW\_NODE} = I_{PEAK} \times t_{fall} = V_{BUS} \times C_{PARA\_WELL} + 2 \times Q_{OSS} \quad (14)$$

In Figure 6, falling edge ZVS transition showing actual transition time and calculated transition time based on device Q_{OSS} only. Equation 15 calculates the unknown well capacitance.

$$C_{PARA\_WELL} = (I_{PEAK} \times t_{fall} - 2 \times Q_{OSS}) / V_{BUS} \quad (15)$$

In Figure 6, falling edge ZVS transition showing actual transition time and calculated transition time based on device Q_{OSS} only.

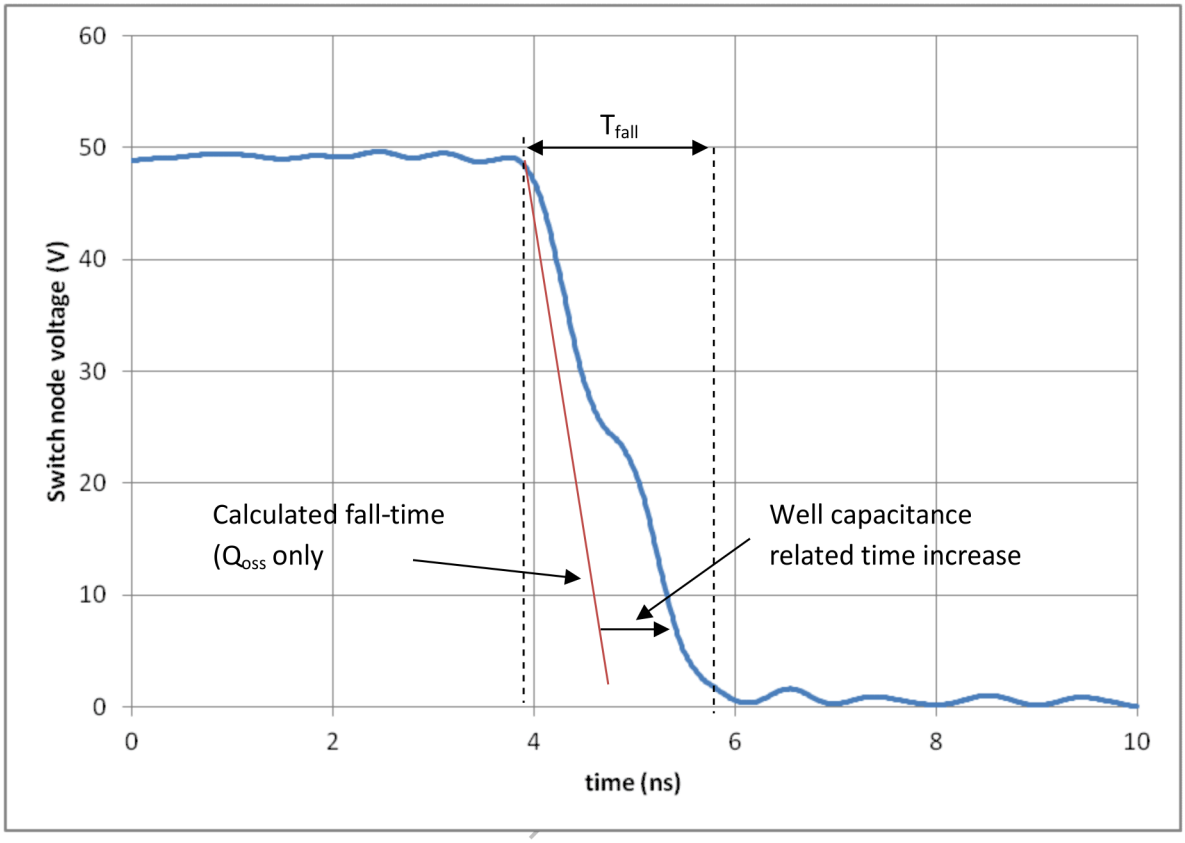


Figure 6. Switching Voltage vs. Time (ns)

Switching voltage is calculated at 50 V (or about 2.25 nC of charge), which equates to about 110 mW/MHz of capacitive switching loss in the first test. The remaining losses incurred are bootstrap diode reverse recovery losses as shown in Figure 7, which shows the measured bootstrap diode reverse recovery losses vs average diode current at 50 V_{BUS} subtracting out parasitic well capacitance losses.

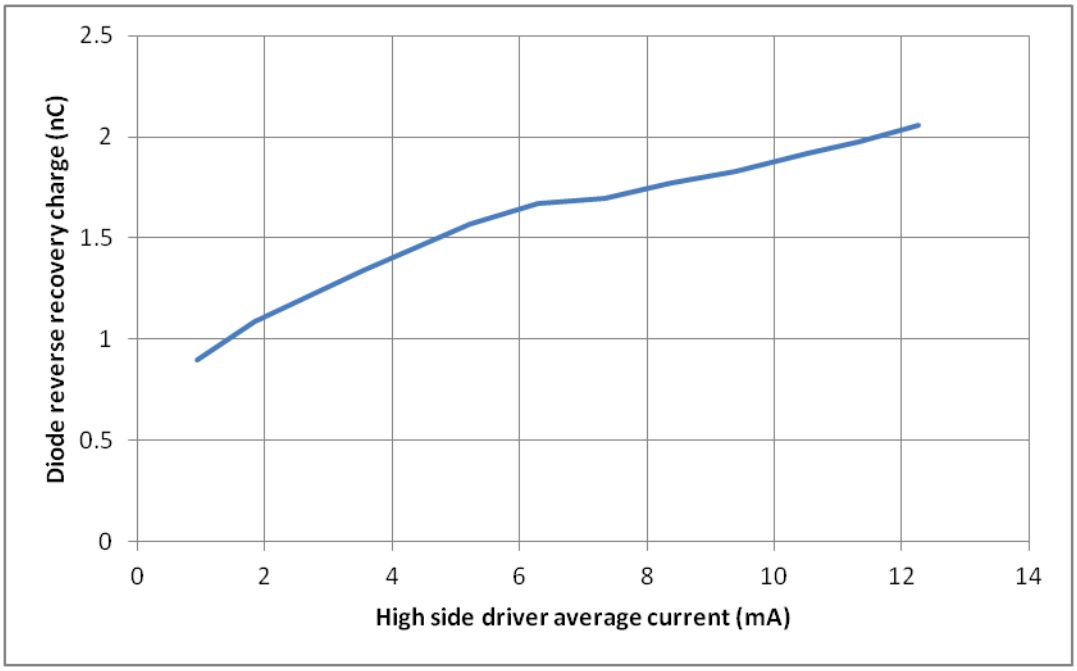


Figure 7. Diode Reverse Recovery Change vs. High-Side Driver Average Current

5 Conclusion

Loss mechanisms in the driver were demonstrated to estimate first order losses and power dissipation. Based on the converter design (hard switching vs soft switching) as demonstrated, the correct total power loss in the driver should be calculated. This calculation is a function of gate driver losses, the parasitic well losses (for hard-switched converters), and the reverse recovery diode losses. It is important to note that LMG1205 device can be run at higher frequencies provided that the minimum pulse width requirement is not violated and the board is designed with thermal consideration of the power dissipation in the driver under worst case conditions to prevent exceeding the maximum operational junction temperature of 125°C.

To limit the system related losses due to the gate driver parasitics, soft-switching topologies such as the ZVS class-D converter can be utilized.

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Revision History

Changes from Original (November 2014) to A Revision	Page
• Changed the LM5113 which is Not Recommended for New Designs and replaced it with the P2P compatible LMG1205.	1

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