LP8731-Q1 Dual High-Current Step-Down DC-DC And Dual Linear Regulators with I²C Interface

1 Features

- Two LDOs for Powering Internal Processor Functions and I/Os
- High-Speed Serial Interface for Independent Control of Device Functions and Settings
- Precision Internal Reference
- Thermal Overload Protection
- Current Overload Protection
- Software Programmable Regulators
- External Power-On-Reset Function for Buck1 and Buck2 (Power Good with Delay Function)
- Undervoltage Lockout (UVLO)
- LP8731-Q1 is an Automotive-Grade Product: AECQ-100 Grade-1 Qualified
- **Step-Down DC/DC Converter (2xBuck)**
  - Programmable V_{OUT} from:
    - Buck1 : 0.8875 V – 1.675 V at 1.2 A
    - Buck2 : 0.8875 V – 1.675 V at 1.2 A
  - Up to 96% Efficiency
  - PWM Switching Frequency of 2.1 MHz
  - ±2% Output Voltage Accuracy
  - Automatic Soft Start
- **Linear Regulators (2xLDO)**
  - Programmable V_{OUT} of 0.8 V to 3.3 V
  - ±3% Output Voltage Accuracy
  - 300-mA Output Current
  - 30-mV (Typical) Dropout

2 Applications

- Configurable Output PMU for ADAS (Advanced Driver Assistance Systems)
- FPGA, DSP Core Power
- Applications Processors

3 Description

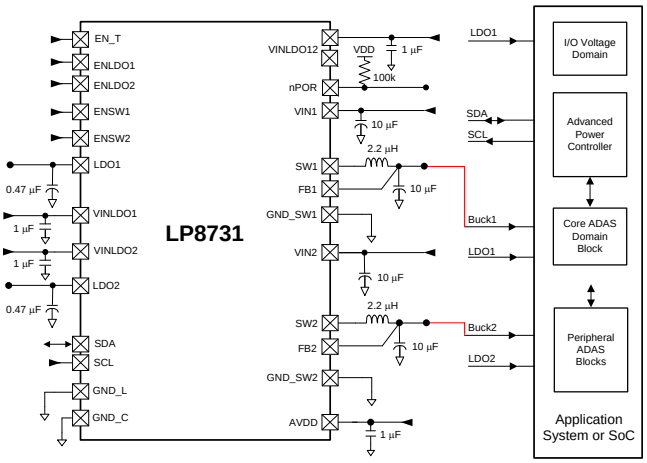
The LP8731-Q1 is a multi-function, programmable Power Management Unit (PMU), optimized for low power FPGAs, microprocessors, and DSPs. This device integrates two highly efficient 1.2-A step-down DC-DC converters with dynamic voltage management (DVM), two 300-mA linear regulators, and a 400-kHz I²C-compatible interface to allow a host controller access to the internal control registers of the LP8731-Q1. The LP8731-Q1 device additionally features programmable power-on sequencing.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LP8731-Q1	DSBGA (25)	2.52 mm x 2.52 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

5 Device Comparison Tables

Table 1. Factory Default Programming(1)

ORDER NUMBER	BUCK1	BUCK2	LDO1	LDO2	DEFAULT I²C ADDRESS
LP8731QYZRRQ1	1.0625 V	1.0625 V	2.8 V	3.3 V	59
	nPOR	**UVLO**	**Start/shutdown sequence**		
	50 µs	Disabled	Buck1 (1.5 ms) → Buck2 (2 ms) → LDO1 (3 ms) → LDO2 (6 ms)		

(1) All numbers are typical.

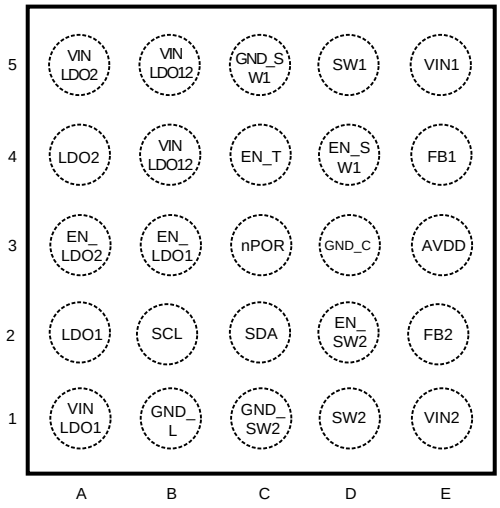
Table 2. Power Block Operation

POWER BLOCK INPUT	POWER BLOCK OPERATION		NOTE
	ENABLED	DISABLED	
VINLDO12	VIN+(1)	VIN+	Always powered
AVDD	VIN+	VIN+	
VIN1	VIN+	VIN+ or 0 V	
VIN2	VIN+	VIN+ or 0 V	
VINLDO 1	≤ VIN+	≤ VIN+	If enabled, min V_{IN} is 2.45 V
VINLDO 2	≤ VIN+	≤ VIN+	

(1) VIN+ is the largest potential voltage on the device.

6 Pin Configuration and Functions

DSBGA (YZR) Package
25 Pins
Top View



Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NUMBER	NAME			
A1	VINLDO1	I	PWR	VINLDO1 power in from either DC source or battery to input pin to LDO1.
A2	LDO1	O	PWR	LDO1 Output
A3	ENLDO2	I	D	LDO2 enable pin, a logic HIGH enables the LDO2
A4	LDO2	O	PWR	LDO2 Output
A5	VINLDO2	I	PWR	VINLDO2 power in from either DC source or battery to input pin to LDO2.

Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NUMBER	NAME			
B1	GND_L	G	G	LDO ground
B2	SCL	I	D	I^2C Clock
B3	ENLDO1	I	D	LDO1 enable pin, a logic HIGH enables the LDO1
B4, B5	VINLDO12	I	PWR	Analog power for internal functions (VREF, BIAS, I^2C, Logic)
C1	GND_SW2	G	G	Buck2 NMOS Power ground
C2	SDA	I/O	D	I^2C Data (bidirectional)
C3	nPOR	O	D	nPOR power-on reset pin for both Buck1 and Buck2. Open drain logic output 100K pull-up resistor. nPOR is pulled to ground when the voltages on these supplies are not good. See *Flexible Power-On Reset (for example, Power Good with Delay)* section for more info.
C4	EN_T	I	D	Enable for preset power-on sequence. (See *Flexible Power-On Reset (for example, Power Good with Delay)*.)
C5	GND_SW1	G	G	Buck1 NMOS power ground
D1	SW2	O	PWR	Buck2 switcher output pin
D2	ENSW2	I	D	Enable pin for Buck2 switcher, a logic HIGH enables Buck2
D3	GND_C	G	G	Non-switching core ground pin
D4	ENSW1	I	D	Enable pin for Buck1 switcher, a logic HIGH enables Buck1
D5	SW1	O	PWR	Buck1 switcher output pin
E1	VIN2	I	PWR	VIN2 power in from either DC source or Battery to Buck2
E2	FB2	I	A	Buck2 input feedback pin
E3	AVDD	I	PWR	Analog Power for Buck converters
E4	FB1	I	A	Buck1 input feedback pin
E5	VIN1	I	PWR	VIN1 power in from either DC source or Battery to Buck1
A: Analog Pin; D: Digital Pin; G: Ground Pin; PWR: Power Pin; I: Input Pin; O: Output Pin; I/O: Input/Output Pin				

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}, SDA, SCL	−0.3	6	V
GND to GND SLUG		±0.3	
Power dissipation (P_{D_MAX})	Internally limited		
Junction temperature ($T_{J\text{-}MAX}$)		150	°C
Maximum lead temperature (soldering)		260	
Storage temperature (T_{stg})	–65	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions (Bucks)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	2.8	5.5	V
V_{EN}	0	(V_{IN} + 0.3)	
Junction temperature (T_J)	–40	125	°C
Ambient temperature (T_A)	–40	125	

7.4 Thermal Information

THERMAL METRIC(1)		LP8731-Q1 DSBGA (YZR) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	8	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 General Electrical Characteristics

Unless otherwise noted, V_{IN} = 3.6 V. Typical values and limits apply for T_J = 25°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	VINLDO12 shutdown current	V_{IN} = 3.6 V		3		µA
V_{POR}	Power-on reset threshold	V_{DD} Falling Edge(2)		1.9		V
T_{SD}	Thermal shutdown threshold			160		°C
T_{SDH}	Thermal shutdown hysteresis			20		
UVLO	Undervoltage lockout	Rising		2.9		V
		Falling		2.7		

(1) All voltages are with respect to the potential at the GND pin.
(2) VPOR is voltage at which the EPROM resets. This is different from the UVLO on VINLDO12, which is the voltage at which the regulators shut off; and is also different from the nPOR function, which signals if the regulators are in a specified range.

7.6 Low Dropout Regulators, LDO1 And LDO2

Unless otherwise noted, V_{IN} = 3.6 V, C_{IN} = 1 µF, C_{OUT} = 0.47 µF. Typical values and limits apply for T_J = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operational voltage range	VINLDO1 and VINLDO2 PMOS pins(4)	2.45(5)		5.5(5)	V
V_{OUT} Accuracy	Output voltage accuracy (default V_{OUT})	Load current = 1 mA	−3%(5)		3%(5)	
ΔV_{OUT}	Line regulation	V_{IN} = (V_{OUT} + 0.3 V) to 5 V(6) Load current = 1 mA			0.2(5)	%/V
	Load regulation	V_{IN} = 3.6 V, Load current = 1 mA to I_{MAX}			0.011(5)	%/mA
I_{SC}	Short circuit current limit	LDO1 to LDO2, V_{OUT} = 0 V		500		mA
$V_{IN} - V_{OUT}$	Dropout voltage	Load current = 50 mA at V_{OUT} = 2.8 V(7)		30	50(5)	mV
		Load current = 250 mA at V_{OUT} = 2.8 V		150	200(5)	
PSRR	Power supply ripple rejection	f = 10 kHz, Load current = I_{MAX}		45		dB
θn	Supply output noise	10 Hz < F < 100 KHz		280		µVrms
I_Q(8)(9)	Quiescent current “on”	I_{OUT} = 0 mA		40		µA
	Quiescent current “on”	I_{OUT} = I_{MAX}		60		µA
	Quiescent current “off”	EN is de-asserted(10)		0.03		µA
T_{ON}	Turn-on time	Start-up from shutdown		300		µs
C_{OUT}	Output capacitance	Capacitance for stability 0°C ≤ T_J ≤ 125°C	0.33	0.47		µF
		−40°C ≤ T_J ≤ 125°C	0.68	1		µF
		ESR	5		500	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and Maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) Pins A1 and/or A5 can operate from V_{IN} min of 1.74 to a V_{IN} max of 5.5 V. This rating is only for the series pass PMOS power FET. It allows the system design to use a lower voltage rating if the input voltage comes from a buck output. However, if V_{IN} is required to operate at a higher voltage than other device supply pins, it is necessary to wire the VINLDO12 pins (B4 an B5) and VINLDO1 and VINLDO2 pins (A1 and/or A5) together to that higher voltage so that the LDO core supply has sufficient head-room to operate the gate of the PMOS.
(5) Limits apply over the entire operating junction temperature range for operation, –40°C to 125°C.
(6) V_{IN} minimum for line regulation values is 1.8 V.
(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(8) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
(9) The **I_Q** can be defined as the standing current of the LP8731-Q1 when the I^2C bus is **activated** and all other power blocks have been **disabled via the I^2C bus**, or it can be defined as the I^2C bus **active**, and the other power blocks are **active under no load condition**. These two values can be used by the system designer when the LP8731-Q1 is powered using a battery.
(10) The I_Q exhibits a higher current draw when the EN pin is de-asserted because the I^2C buffer pins draw an additional 2 µA.

7.7 Buck Converters SW1, SW2

Unless otherwise noted, V_{IN} = 3.6 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, L_{OUT} = 2.2 µH ceramic. Typical values and limits apply for T_J = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage		−3%(4)		3%(4)	
V_{OUT}	Line regulation	2.8 V < V_{IN} < 5.5 V I_{OUT} = 10 mA		0.089%		/V
	Load regulation	100 mA < I_O < I_{MAX}		0.0013%		/mA
	Output accuracy(5)	V_{IN} = 3.3 V, V_{OUT} from 0.8875 V to 1.1625 V Load from 0 mA to 600 mA	–2%(4)		2%(4)	
Eff	Efficiency	Load current = 250 mA		90%		
I_{SHDN}	Shutdown supply current	EN is de-asserted		0.01		µA
f_{OSC}	Internal oscillator frequency		1.7(4)	2.1		MHz
I_{PEAK}	Buck1 peak switching current limit			1.7		A
	Buck2 peak switching current limit			1.7		
I_Q(6)	Quiescent current “on”	No load PWM Mode		2		mA
R_{DSON} (P)	Pin-pin resistance PFET			200		mΩ
R_{DSON} (N)	Pin-pin resistance NFET			180		mΩ
T_{ON}	Turn-on time	Start-up from shutdown		500		µs
C_{IN}	Input capacitance	Capacitance for stability	10			µF
C_O	Output capacitance	Capacitance for stability	10			µF

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and Maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) Limits apply over the entire operating junction temperature range for operation, –40°C to 125°C
(5) Based on closed loop, bench test data with LP8731YZREVM.
(6) The **I_Q** can be defined as the standing current of the LP8731-Q1 when the I^2C bus is **active** and all other power blocks have been **disabled via the I^2C bus**, or it can be defined as the I^2C bus **active**, and the other power blocks are **active under no load condition**. These two values can be used by the system designer when the LP8731-Q1 is powered using a battery.

7.8 I/O Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.4(1)	V
V_{IH}	Input high level		1.2(1)			

(1) This specification is ensured by design.

7.9 Power-On Reset Threshold/Function (POR)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
nPOR	nPOR = Power-on reset for Buck1 and Buck2	Default		50		µs
nPOR threshold	Percentage of target voltage Buck1 or Buck2	V_{BUCK1} AND V_{BUCK2} rising		94%		
		V_{BUCK1} OR V_{BUCK2} falling		85%		
V_{OL}	Output level low	Load = I_{OL} = 0.2 mA		0.23	0.5(1)	V

(1) This specification is ensured by design.

7.10 I²C-Compatible Interface Timing

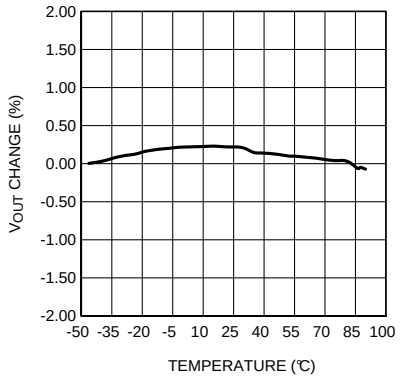
Unless otherwise noted, V_{IN} = 3.6 V. Nominal values and limits apply for T_J = 25°C.(1)

			MIN	NOM	MAX	UNIT
f_{CLK}	Clock frequency				400	kHz
t_{BF}	Bus-free time between start and stop	See(1)	1.3			µs
t_{HOLD}	Hold time repeated start condition	See(1)	0.6			µs
t_{CLKLP}	CLK low period	See(1)	1.3			µs
t_{CLKHP}	CLK high period	See(1)	0.6			µs
t_{SU}	Setup time repeated start condition	See(1)	0.6			µs
$t_{DATAHLD}$	Data hold time	See(1)	0			µs
t_{DATASU}	Data setup time	See(1)	100			ns
T_{SU}	Setup time for start condition	See(1)	0.6			µs
T_{TRANS}	Maximum pulse width of spikes that must be suppressed by the input filter of both DATA & CLK signals	See(1)		50		ns

(1) This specification is ensured by design.

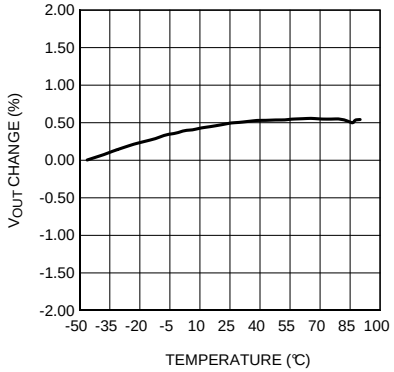
7.11 Typical Characteristics

T_A = 25°C unless otherwise noted



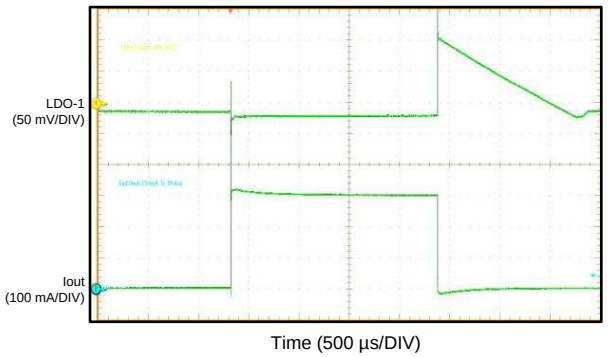
V_{IN} = 3.6 V V_{OUT} = 2.6 V 100-mA load

Figure 1. Output Voltage Change vs. Temperature (LDO1)



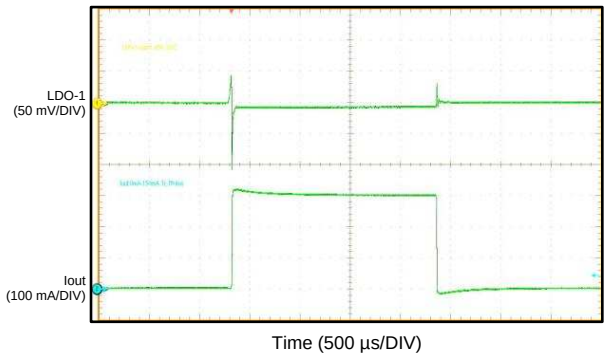
V_{IN} = 3.6 V V_{OUT} = 3.3 V 100-mA load

Figure 2. Output Voltage Change vs. Temperature (LDO2)



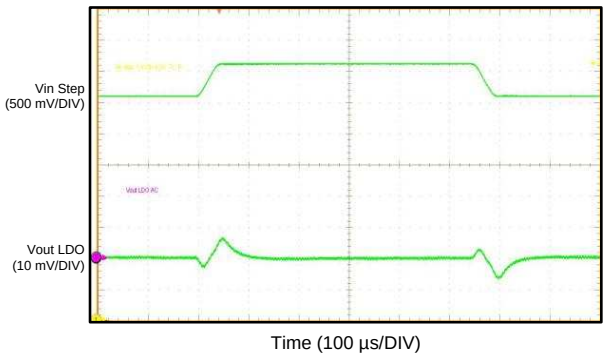
V_{OUT} = 3.6 V I_{LOAD} = 0 to 300 mA
V_{OUT} = 1.8 V Tr = Tf = 1 µs

Figure 3. Load Transient 1-µs Edge Rate



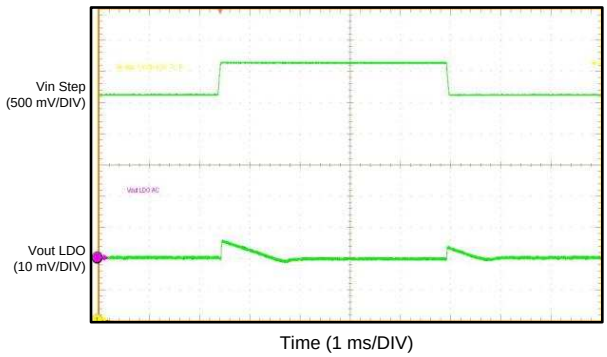
V_{OUT} = 3.6 V I_{LOAD} = 0 to 300 mA
V_{OUT} = 1.8 V Tr = Tf = 4 µs

Figure 4. Load Transient 4-µs Edge Rate



V_{IN} = 3.6 V to 4.2 V I_{LOAD} = 300 mA
V_{OUT} = 1.8 V Tr = Tf = 20 µs

Figure 5. Line Transient 300-mA, 4-µs Edge Rate

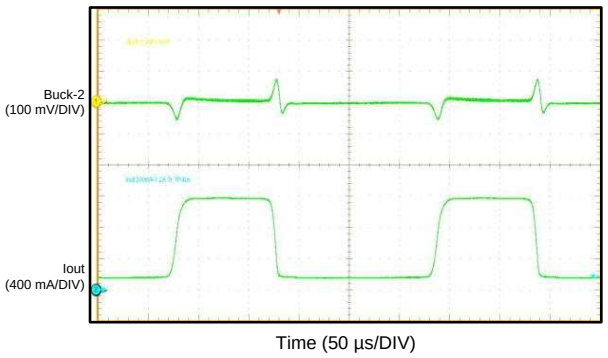


V_{IN} = 3.6 V to 4.2 V I_{OUT} = 1 mA
V_{OUT} = 1.8 V Tr = Tf = 30 µs

Figure 6. Line Transient 1-mA, 30-µs Edge Rate

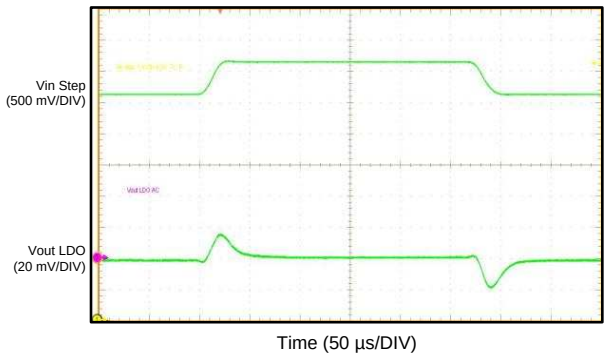
Typical Characteristics (continued)

T_A = 25°C unless otherwise noted



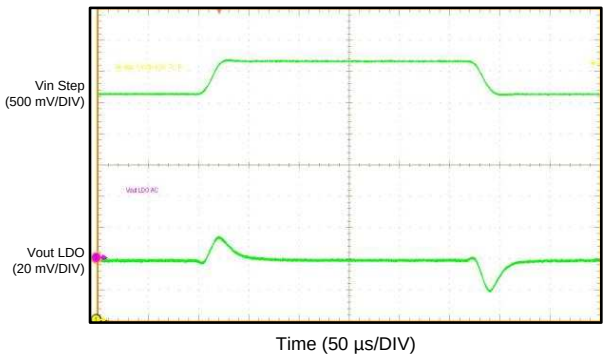
I_{OUT} = 200 mA to 1.2 A PWM

Figure 7. Buck Load Transient PWM Mode



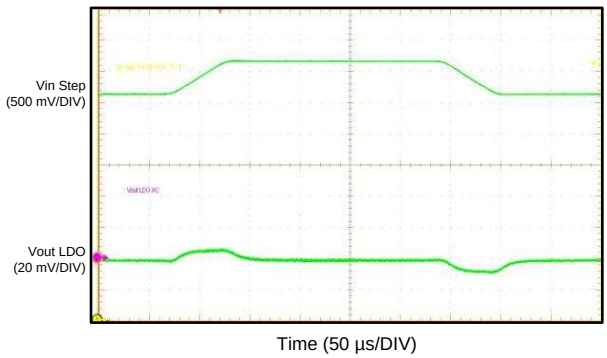
V_{IN} Step I_{OUT} = 300 mA Tr = Tf = 30 µs

Figure 8. Buck Line Transient PWM



V_{IN} Step I_{OUT} = 1.2 A Tr = Tf = 10 µs

Figure 9. Buck Line Transient PWM



V_{IN} Step I_{OUT} = 1.2 A Tr = Tf = 30 µs

Figure 10. Buck Line Transient PWM

8 Detailed Description

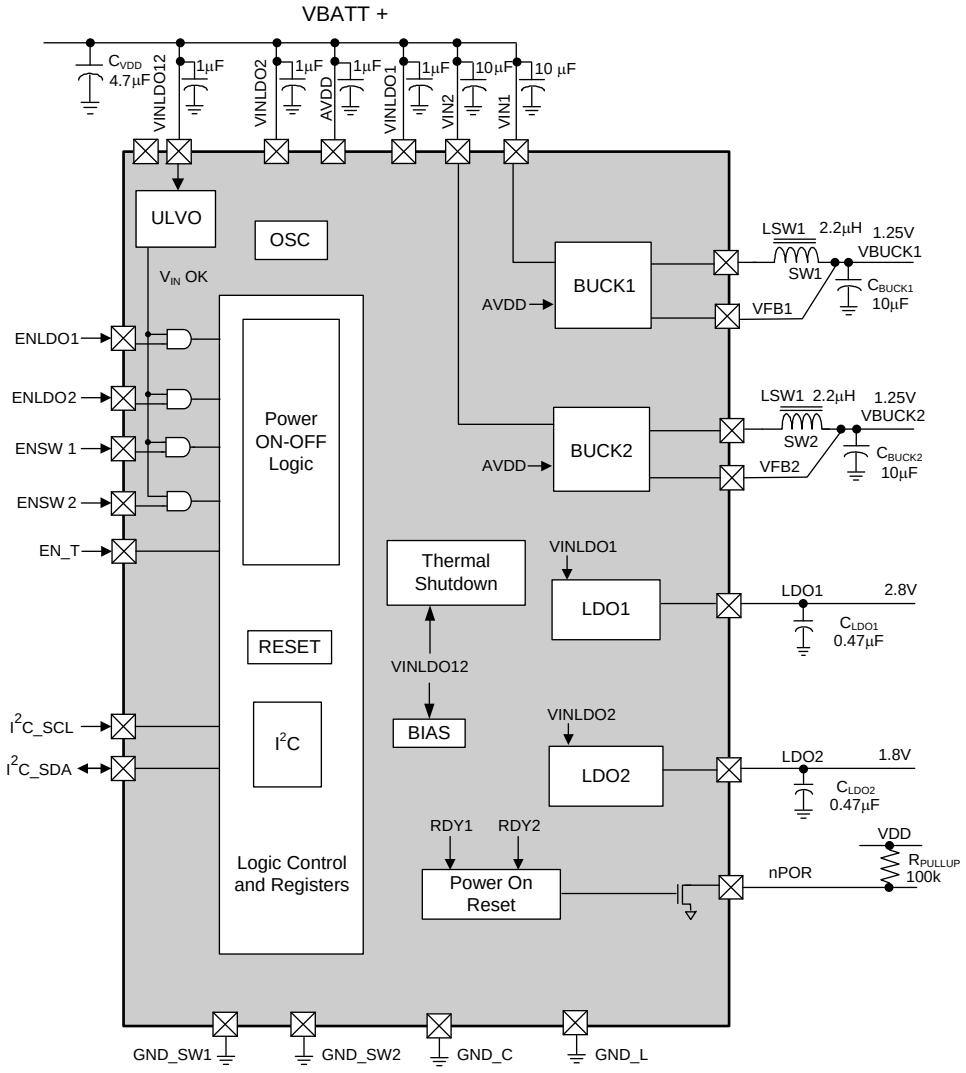
8.1 Overview

The LP8731-Q1 supplies the various power needs of the application by means of two Linear Low Drop Regulators (LDO1 and LDO2) and two Buck converters (SW1 and SW2). Table 3 lists the output characteristics of the various regulators.

Table 3. Supply Specification

SUPPLY	LOAD	OUTPUT		
		V_{OUT} RANGE (V)	RESOLUTION (mV)	I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
LDO1	analog	0.8 to 3.3	100	300
LDO2	analog	0.8 to 3.3	100	300
SW1	digital	0.8875 to 1.675	12.5	1200
SW2	digital	0.8875 to 1.675	12.5	1200

8.2 Functional Block Diagram



8.3 Features Description

8.3.1 Linear Low Dropout Regulators (LDOs)

LDO1 and LDO2 are identical linear regulators targeting analog loads characterized by low noise requirements. LDO1 and LDO2 are enabled through the ENLDO pin or through the corresponding LDO1 or LDO2 control register. The output voltages of both LDOs are register programmable. The default output voltages are factory programmed during Final Test, which can be tailored to the specific needs of the system designer.

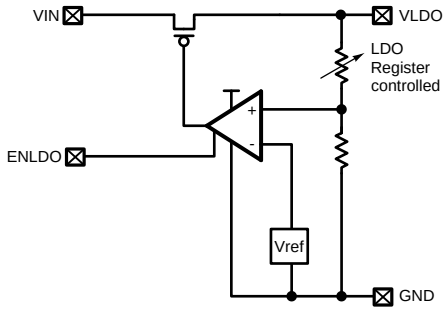


Figure 11. LDO Functional Block Diagram

8.3.2 No-Load Stability

The LDOs remain stable and in regulation with no external load. This is an important consideration in some circuits, for example, CMOS RAM keep-alive applications.

8.3.3 LDO1 and LDO2 Control Registers

LDO1 and LDO2 can be configured by means of the LDO1 and LDO2 control registers. The output voltage is programmable in steps of 100 mV from 1 V to 3.5 V by programming bits D4 to D0 in the LDO Control registers. Both LDO1 and LDO2 are enabled by applying a logic 1 to the ENLDO1 and ENLDO2 pin. Enable/disable control is also provided through enable bit of the LDO1 and LDO2 control registers. The value of the enable LDO bit in the register is logic 1 by default. The output voltage can be altered while the LDO is enabled.

8.3.4 SW1, SW2: Synchronous Step-Down Magnetic DC-DC Converters

8.3.4.1 Functional Description

The LP8731-Q1 incorporates two high-efficiency synchronous switching buck regulators, SW1 and SW2, that deliver a constant voltage from a single Li-Ion battery to the portable system processors. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 1200 mA, depending on the input voltage and output voltage (voltage head room), and the inductor chosen (maximum current capability).

Both SW1 and SW2 can operate up to a 100% duty cycle (PMOS switch always on) for low dropout control of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage.

Additional features include soft-start, undervoltage lockout, current overload protection, and thermal overload protection.

8.3.4.2 Circuit Operation

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground (BUCKGND pin) and a feedback path. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN} - V_{OUT}}{L} \quad (1)$$

Features Description (continued)

by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

8.3.4.3 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, a feedforward voltage inversely proportional to the input voltage is introduced.

8.3.4.4 Internal Synchronous Rectification

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

8.3.4.5 Current Limiting

A current limit feature allows the converter to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1.7 A for Buck1 and Buck2 (typical). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

8.3.4.6 SW1, SW2 Operation

SW1 and SW2 have selectable output voltages ranging from 0.8875 V to 1.675 V (typ.). Both SW1 and SW2 in the LP8731-Q1 are I^2C register controlled and are enabled by default through the internal state machine of the LP8731-Q1 following a power-on event that moves the operating mode to the Active state. (See *Flexible Power Sequencing of Multiple Power Supplies*.) The SW1 and SW2 output voltages revert to default values when the power-on sequence has been completed. The default output voltage for each buck converter is factory programmable. (See *Application and Implementation*.)

8.3.4.7 SW1, SW2 Control Registers

SW1, SW2 can be enabled/disabled through the corresponding control register.

8.3.4.8 Shutdown Mode

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch is on in shutdown to discharge the output. When the converter is enabled, soft start is activated. It is recommended to disable the converter during the system power up and undervoltage conditions when the supply is less than 2.8 V.

8.3.4.9 Soft Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing startup stresses and surges. The two LP8731-Q1 buck converters have a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.8 V. Soft start is implemented by increasing switch current limit in steps of 180 mA, 300 mA, and 720 mA for Buck1; 180 mA, 300 mA and 720 mA for Buck2 (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up.

Features Description (continued)

8.3.4.10 Low Dropout Operation

The LP8731-Q1 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is

$$V_{IN,\ MIN} = I_{LOAD} \times (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT} \quad (3)$$

where

- I_{LOAD}: Load current
- $R_{DSON,\ PFET}$: Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$: Inductor resistance

8.3.4.11 Flexible Power Sequencing of Multiple Power Supplies

The LP8731-Q1 provides several options for power on sequencing. The two bucks can be individually controlled with ENSW1 and ENSW2. The two LDOs can also be individually controlled with ENLDO1 and ENLDO2.

If the user desires a set power-on sequence, the device can be programmed through I^2C by raising EN_T from LOW to HIGH.

8.3.4.12 Power-Up Sequencing Using the EN_T Function

EN_T assertion causes the LP8731-Q1 to emerge from Standby mode to Full Operation mode at a preset timing sequence. By default, the enables for the LDOs and Bucks (ENLDO1, ENLDO2, EN_T, ENSW1, ENSW2) are internally pulled down by a 500-kΩ resistor, which causes the part to stay OFF until enabled. If the user wishes to use the preset timing sequence to power on the regulators, transition the EN_T pin from LOW to HIGH. Otherwise, simply tie the enables of each specific regulator HIGH to turn on automatically.

EN_T is edge triggered with rising edge signaling the device to power on. The EN_T input is deglitched, and the default is set at 1 ms. As shown in Figure 12 and Figure 13, a rising EN_T edge starts a power-on sequence, while a falling EN_T edge starts a shutdown sequence. If EN_T is high, toggling the external enables of the regulators has no effect on the device.

The regulators can also be programmed through I^2C to turn on and off. By default, I^2C enables for the regulators on ON.

The regulators are on following the pattern: Regulators on = (I^2C enable) AND (External pin enable OR EN_T high).

NOTE

The EN_T power-up sequencing may also be employed immediately after V_{IN} is applied to the device. However, V_{IN} must be stable for approximately 8 ms minimum before EN_T be asserted high to ensure internal bias, reference, and the Flexible POR timing are stabilized. This initial EN_T delay is necessary only upon first time device power on for power-sequencing function to operate properly.

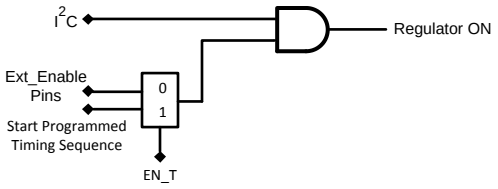


Figure 12. Enable Logic Diagram

Features Description (continued)

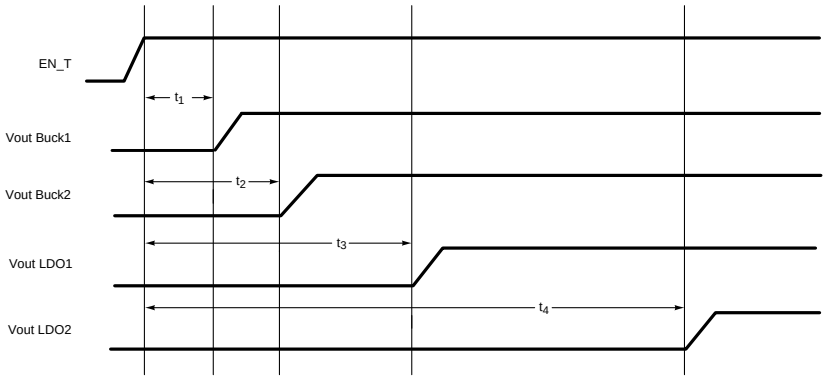


Figure 13. LP8731-Q1 Default Power-Up Sequence

Table 4. Power-On Timing Specification

		MIN	NOM	MAX	UNIT
t_1	Programmable delay from EN_T assertion to V_{CC}_Buck1 on		1.5		ms
t_2	Programmable delay from EN_T assertion to V_{CC}_Buck2 on		2		ms
t_3	Programmable delay from EN_T assertion to V_{CC}_LDO1 on		3		ms
t_4	Programmable delay from EN_T assertion to V_{CC}_LDO2 on		6		ms

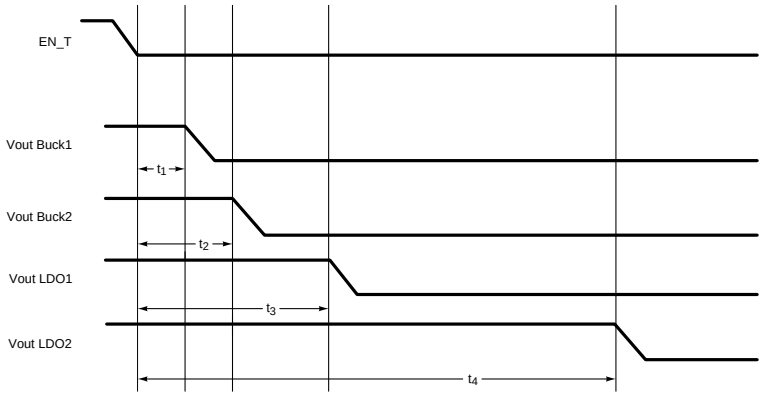


Figure 14. LP8731-Q1 Default Power-Off Sequence

		MIN	NOM	MAX	UNIT
t_1	Programmable delay from EN_T deassertion to V_{CC}_Buck1 off		1.5		ms
t_2	Programmable delay from EN_T deassertion to V_{CC}_Buck2 off		2		ms
t_3	Programmable delay from EN_T deassertion to V_{CC}_LDO1 off		3		ms
t_4	Programmable delay from EN_T deassertion to V_{CC}_LDO2 off		6		ms

NOTE

The LP8731-Q1 default power-off delay setting is the same as the on sequence.

8.3.5 Flexible Power-On Reset (for example, Power Good with Delay)

The LP8731-Q1 is equipped with an internal Power-On-Reset (“POR”) circuit which monitors the output voltage levels on bucks 1 and 2. The nPOR is an open-drain logic output which is logic LOW when either of the buck outputs are below 91% of the rising value, or when one or both outputs fall below 82% of the desired value. The time delay between output voltage level and when nPOR is enabled is (50 µs, 50 ms, 100 ms, 200 ms), 50 µs by default. The system designer can choose the external pull-up resistor (for example, 100 kΩ) for the nPOR pin.

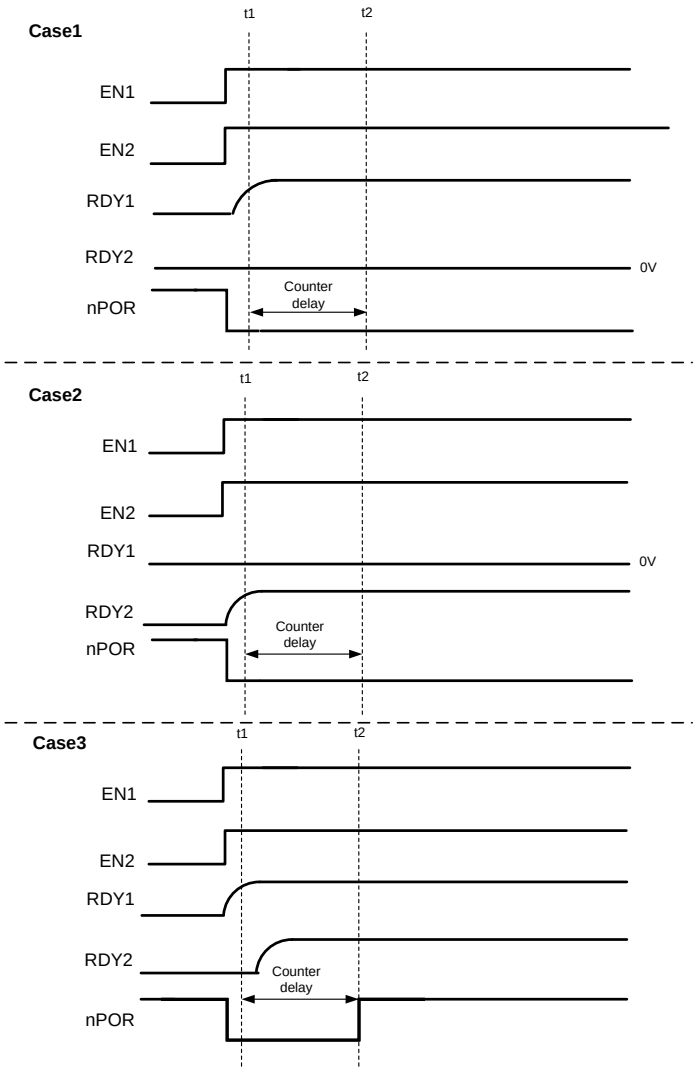


Figure 15. nPOR With Counter Delay

Figure 15 shows the simplest application of the Power-On Reset, where both switcher enables are tied together. In Case 1, EN1 causes nPOR to transition LOW and triggers the nPOR delay counter. If the power supply for Buck2 does not come on within that period, nPOR stays LOW, indicating a power fail mode. Case 2 indicates the vice-versa scenario if Buck1 supply did not come on. In both cases the nPOR remains LOW.

Case 3 shows a typical application of the Power On Reset, where both switcher enables are tied together. Even if RDY1 ramps up slightly faster than RDY2 (or vice versa), then nPOR signal triggers a programmable delay before going HIGH, as explained in Figure 16.

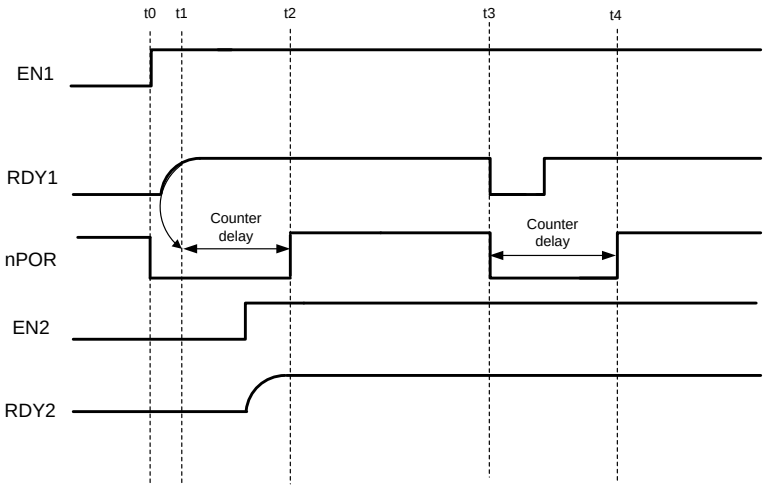


Figure 16. Faults Occurring in Counter Delay after Start-Up

The Figure 16 timing diagram details the power-good with delay with respect to the enable signals EN1, and EN2. The RDY1, RDY2 are internal signals derived from the output of two comparators. Each comparator has been trimmed as follows:

COMPARATOR LEVEL	BUCK SUPPLY LEVEL
HIGH	Greater than 94%
LOW	Less than 85%

The circuits for EN1 and RDY1 are symmetrical to EN2 and RDY2, so each reference to EN1 and RDY1 also works for EN2 and RDY2 and vice versa.

If EN1 and RDY1 signals are HIGH at time t1, then the RDY1 signal rising edge triggers the programmable delay counter (50 µs, 50 ms, 100 ms, 200 ms). This delay forces nPOR LOW between time interval t1 and t2. nPOR is then pulled HIGH after the programmable delay is completed. If EN2 and RDY2 are initiated during this interval, the nPOR signal ignores this event.

If either RDY1or RDY2 were to go LOW at t3 then the programmable delay is triggered again.

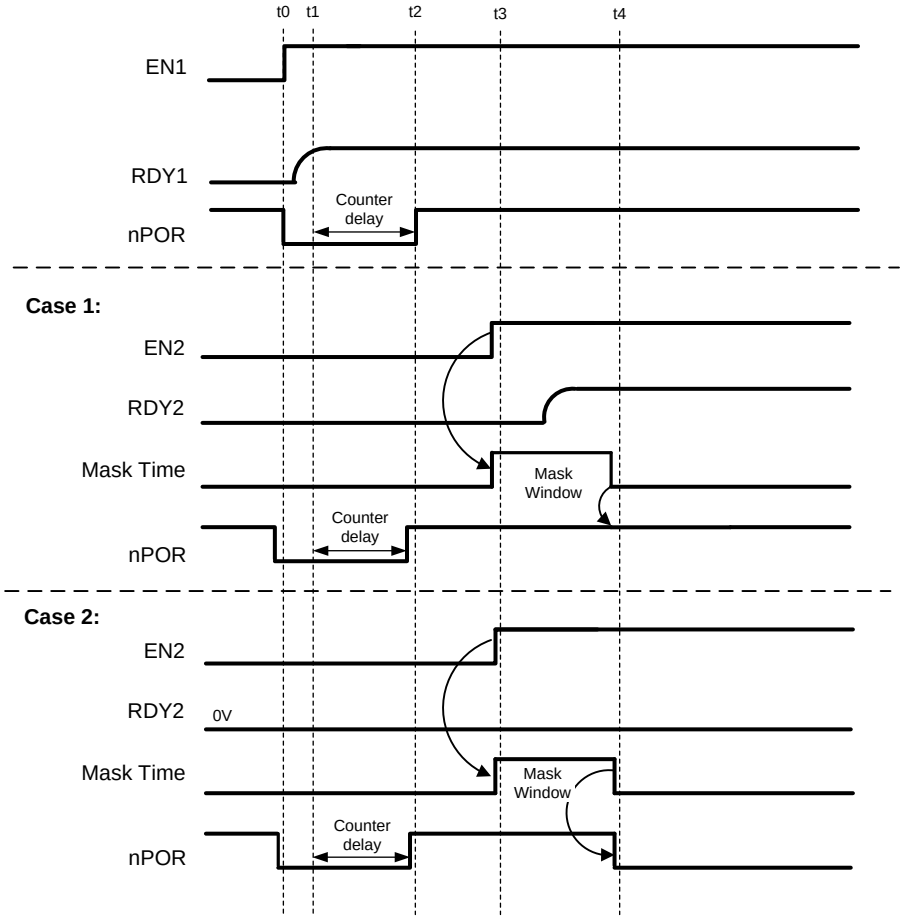


Figure 17. nPOR Mask Window

If the EN1 and RDY1 are initiated in normal operation, then nPOR is asserted and deasserted .

Case 1 in Figure 17 shows a case where EN2 and RDY2 are initiated after triggered programmable delay. To prevent the nPOR being asserted again, a masked window (5 ms) counter delay is triggered off the EN2 rising edge. nPOR is still held HIGH for the duration of the mask, whereupon the nPOR status afterwards depends on the status of both RDY1 and RDY2 lines.

Case 2 shows the case where EN2 is initiated after the RDY1 triggered programmable delay, but RDY2 never goes HIGH (Buck2 never turns on). Normal operation of nPOR occurs with respect to EN1 and RDY1, and the nPOR signal is held HIGH for the duration of the mask window. nPOR goes LOW after the masking window has timed out because it is now dependent on RDY1 and RDY2, where RDY2 is LOW.

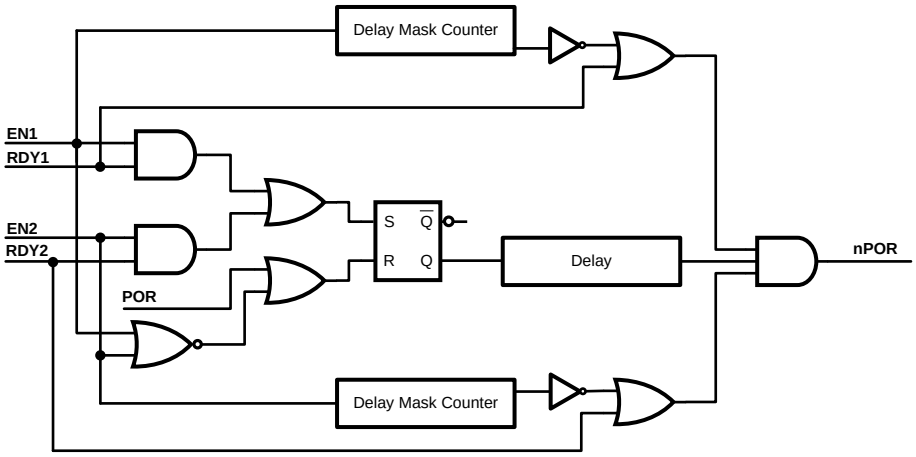


Figure 18. Design Implementation Of The Flexible Power-On Reset

An internal power-on reset of the device is used with EN1 and EN2 to produce a reset signal (LOW) to the delay timer nPOR. EN1 and RDY1 or EN2 and RDY2 are used to generate the set signal (HIGH) to the delay timer. S = R = 1 never occurs. The mask timers are triggered by EN1 and EN2 which are gated with RDY1 and RDY2 to generate outputs to the final AND gate to generate the nPOR.

8.3.6 Undervoltage Lockout

The LP8731-Q1 features an undervoltage lockout circuit. The function of this circuit is to continuously monitor the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8 VDC.

The circuit incorporates a bandgap-based circuit that establishes the reference used to determine the 2.8-VDC trip point for a V_{IN} OK – Not OK detector. This V_{IN} OK signal is then used to gate the enable signals to the four regulators of the LP8731-Q1. When VINLDO12 is greater than 2.8 VDC, the four enables control the four regulators, when VINLDO12 is less than 2.8 VDC, the four regulators are disabled by the V_{IN} detector being in the “Not OK” state. The circuit has built-in hysteresis to prevent chattering from occurring.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

During shutdown the PFET switch, reference, control, and bias circuitry of the converters are turned off. The NFET switch is turned on during shutdown to discharge the output. When the converter is enabled, soft start is activated. It is recommended that the converter be disabled during the system power up and undervoltage conditions when the supply is less than 2.8 V.

8.5 Programming

8.5.1 I²C-Compatible Serial Interface

8.5.1.1 I²C Signals

The LP8731-Q1 features an I²C-compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data, respectively. Both signals need a pullup resistor according to the I²C specification. The LP8731-Q1 interface is an I²C slave that is clocked by the incoming SCL clock.

Signal timing specifications are according to the I²C bus specification. The maximum bit rate is 400 kbit/s. See I²C specification from NXP Semiconductors for further details.

8.5.1.2 I²C Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL), that is, the state of the data line can only be changed when CLK is LOW.

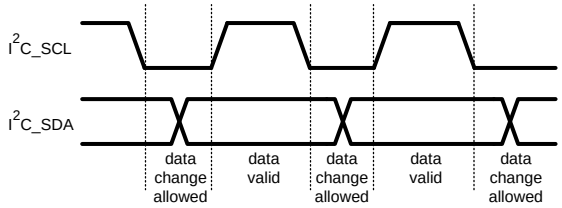


Figure 19. I²C Signals: Data Validity

8.5.1.3 I²C Start and Stop Conditions

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

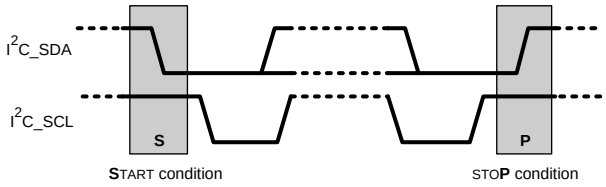


Figure 20. Start And Stop Conditions

8.5.1.4 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledged related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying acknowledgment. A receiver which has been addressed must generate an acknowledgment (“ACK”) after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W).

Programming (continued)

NOTE

According to industry I²C standards for 7-bit addresses, the MSB of an 8-bit address is removed, and communication actually starts with the 7th most significant bit. For the eighth bit (LSB), a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

The LP8731-Q1 has factory-programmed I²C addresses. The device has a chip address of 59'h.

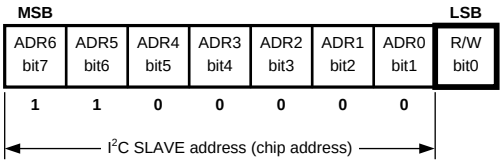
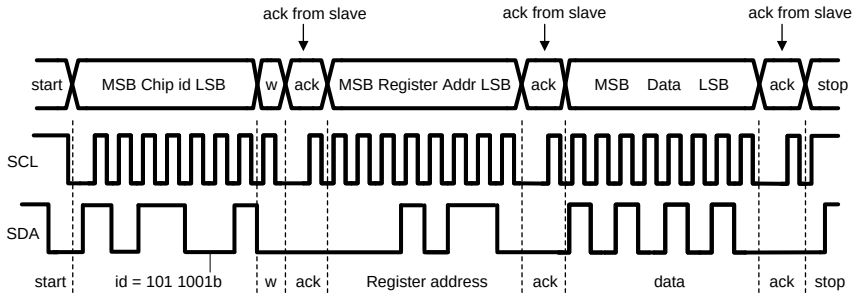


Figure 21. I²C Chip Address (see NOTE above)



w = write (SDA = "0")
r = read (SDA = "1")
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = LP8731-Q1 chip address: **0x59**

Figure 22. I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

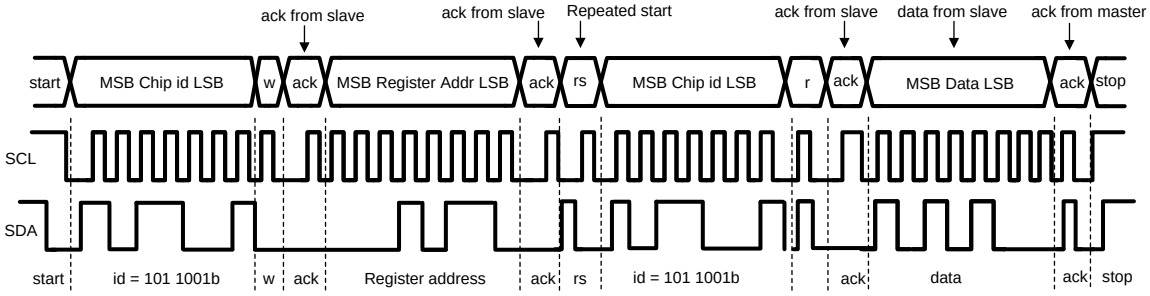


Figure 23. I²C Read Cycle

8.6 LP8731-Q1 Register Maps

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	REGISTER DESCRIPTION
0x02	ICRA	R	Interrupt Status Register A
0x07	SCR1	R/W	System Control 1 Register
0x10	BKLDOEN	R/W	Buck and LDO Output Voltage Enable Register
0x11	BKLDOSR	R	Buck and LDO Output Voltage Status Register
0x20	VCCR	R/W	Voltage Change Control Register 1
0x23	B1TV1	R/W	Buck1 Target Voltage 1 Register
0x24	B1TV2	R/W	Buck1 Target Voltage 2 Register
0x25	B1RC	R/W	Buck1 Ramp Control
0x29	B2TV1	R/W	Buck2 Target Voltage 1 Register
0x2A	B2TV2	R/W	Buck2 Target Voltage 2 Register
0x2B	B2RC	R/W	Buck2 Ramp Control
0x38	BFCR	R/W	Buck Function Register
0x39	LDO1VCR	R/W	LDO1 Voltage control Registers
0x3A	LDO2VCR	R/W	LDO2 Voltage control Registers

8.6.1 Interrupt Status Register (ISRA) 0x02

This register informs the system engineer of the temperature status of the chip.

	D7-D2	D1	D0
Name	—	Temp 125°C	—
Access	—	R	—
Data	Reserved	Status bit for thermal warning PMIC T > 125°C 0 – PMIC Temp. < 125°C 1 – PMIC Temp. > 125°C	Reserved
Reset	0	0	0

8.6.2 System Control 1 Register (SCR1) 0x07

This register allows the user to select the preset delay sequence for power-on timing and to select between an internal and external clock for the bucks.

	D7	D6-D4	D3	D2	D1	D0
Name	—	EN_DLY	—	FPWM2 (1)	FPWM1 (1)	ECEN
Access	—	R/W	—	R/W	R/W	R/W
Data	Reserved	Selects the preset delay sequence from EN_T assertion (shown below)	Reserved	Buck2 PWM /PFM Mode select 0 – Auto Switch PFM - PWM operation 1 – PWM Mode Only	Buck 1 PWM /PFM Mode select 0 – Auto Switch PFM - PWM operation 1 – PWM Mode Only	Reserved
Reset	0	Factory-Programmed Default	1	Factory-Programmed Default	Factory-Programmed Default	0

(1) Default PWM mode only — please contact TI sales office if Auto switch/PFM mode operation is needed.

8.6.3 EN_DLY Preset Delay Sequence after EN_T Assertion

EN_DLY<2:0>	DELAY (ms)			
	Buck1	Buck2	LDO1	LDO2
000	1	1	1	1
001	1	1.5	2	2
010	1.5	2	3	6
011	1.5	2	1	1
100	1.5	2	3	6
101	1.5	1.5	2	2
110	3	2	1	1.5
111	2	3	6	11

8.6.4 Buck and LDO Output Voltage Enable Register (BKLDOEN) – 0x10

This register controls the enables for the Bucks and LDOs.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	—	LDO2EN	—	LDO1EN	—	BK2EN	—	BK1EN
Access	—	R/W	—	R/W	—	R/W	—	R/W
Data	Reserved	0 – Disable 1 – Enable	Reserved	0 – Disable 1 – Enable	Reserved	0 – Disable 1 – Enable	Reserved	0 – Disable 1 – Enable
Reset	0	1	1	1	0	1	0	1

8.6.5 Buck and LDO Status Register (BKLDOSR) – 0x11

This register monitors whether the Bucks and LDOs meet the voltage output specifications.

	D7	D6	D5	D4	D3	D2	D1	D0
Name	BKS_OK	LDOS_OK	LDO2_OK	LDO1_OK	—	BK2_OK	—	BK1_OK
Access	R	R	R	R	—	R	—	R
Data	0 – Buck 1-2 Not Valid 1 – Bucks Valid	0 – LDO 1-2 Not Valid 1 – LDOs Valid	0 – LDO2 Not Valid 1 – LDO2 Valid	0 – LDO1 Not Valid 1 – LDO1 Valid	Reserved	0 – Buck2 Not Valid 1 – Buck2 Valid	Reserved	0 – Buck1 Not Valid 1 – Buck1 Valid
Reset	0	0	0	0	0	0	0	0

8.6.6 BUCK Voltage Change Control Register 1 (VCCR) – 0x20

This register selects and controls the output target voltages for the buck regulators.

	D7-D6	D5	D4	D3-2	D1	D0
Name	—	B2VS	B2GO	—	B1VS	B1GO
Access	—	R/W	R/W	—	R/W	R/W
Data	Reserved	Buck2 Target Voltage Select 0 – B2VT1 1 – B2VT2	Buck2 Voltage Ramp CTRL 0 – Hold 1 – Ramp to B2VS selection	Reserved	Buck1 Target Voltage Select 0 – B1VT1 1 – B1VT2	Buck1 Voltage Ramp CTRL 0 – Hold 1 – Ramp to B1VS selection
Reset	00	0	0	00	0	0

8.6.7 BUCK1 Target Voltage 1 Register (B1TV1) – 0x23

This register allows the user to program the output target voltage of Buck1 (target voltage 1).

	D7-D6	D5	D4-0	BUCK1 OUTPUT VOLTAGE (V)
Name	—	Buck1 12p5 mV step	B1TV1	—
Access	—	R/W	R/W	—
Data	Reserved	1’h0	5’h00	0.8875
		1'h1	5’h00	0.9000
		1’h0	5’h01	0.9125
		1'h1	5’h01	0.9250
		1’h0	5’h02	0.9375
		1'h1	5’h02	0.9500
		1’h0	5’h03	0.9625
		1'h1	5’h03	0.9750
		1’h0	5’h04	0.9875
		1'h1	5’h04	1.0000
		1’h0	5’h05	1.0125
		1'h1	5’h05	1.0250
		1’h0	5’h06	1.0375
		1'h1	5’h06	1.0500
		1’h0	5’h07	1.0625
		1'h1	5’h07	1.0750
		1’h0	5’h08	1.0875
		1'h1	5’h08	1.1000
		1’h0	5’h09	1.1125
		1'h1	5’h09	1.1250
		1’h0	5’h0A	1.1375
		1'h1	5’h0A	1.1500
		1’h0	5’h0B	1.1625
		1'h1	5’h0B	1.1750
		1’h0	5’h0C	1.1875
		1'h1	5’h0C	1.2000
		1’h0	5’h0D	1.2125
		1'h1	5’h0D	1.2250
		1’h0	5’h0E	1.2375
		1'h1	5’h0E	1.2500
		1’h0	5’h0F	1.2625
		1'h1	5’h0F	1.2750

	D7-D6	D5	D4-0	BUCK1 OUTPUT VOLTAGE (V)
Data	Register	1’h0	5'h10	1.2875
		1'h1	5'h10	1.3000
		1’h0	5'h11	1.3125
		1’h0	5'h11	1.3250
		1'h1	5'h12	1.3375
		1’h0	5'h12	1.3500
		1'h1	5'h13	1.3625
		1’h0	5'h13	1.3750
		1'h1	5'h14	1.3875
		1’h0	5'h14	1.4000
		1'h1	5'h15	1.4125
		1’h0	5'h15	1.4250
		1'h1	5'h16	1.4375
		1’h0	5'h16	1.4500
		1'h1	5'h17	1.4625
		1’h0	5'h17	1.4750
		1’h0	5'h18	1.4875
		1'h1	5'h18	1.5000
		1’h0	5'h19	1.5125
		1'h1	5'h19	1.5250
		1’h0	5'h1A	1.5375
		1'h1	5'h1A	1.5500
		1’h0	5'h1B	1.5625
		1'h1	5'h1B	1.5750
		1’h0	5'h1C	1.5875
		1'h1	5'h1C	1.6000
		1'h0	5'h1D	1.6125
		1'h1	5'h1D	1.6250
		1'h0	5'h1E	1.6375
		1'h1	5'h1E	1.6500
		1'h0	5'h1F	1.6625
		1'h1	5'h1F	1.6750

8.6.8 BUCK1 Target Voltage 2 Register (B1TV2) - 0x24

This register allows the user to program the output target voltage of Buck1 (target voltage 2).

	D7-D6	D5	D4-D0	BUCK1 OUTPUT VOLTAGE (V)
Name	—	Buck1 12p5 mV step	B1TV2	—
Access	—	R/W	R/W	—
Data	Reserved	1’h0	5’h00	0.8875
		1'h1	5’h00	0.9000
		1’h0	5’h01	0.9125
		1'h1	5’h01	0.9250
		1’h0	5’h02	0.9375
		1'h1	5’h02	0.9500
		1’h0	5’h03	0.9625
		1'h1	5’h03	0.9750
		1’h0	5’h04	0.9875
		1'h1	5’h04	1.0000
		1’h0	5’h05	1.0125
		1'h1	5’h05	1.0250
		1’h0	5’h06	1.0375
		1'h1	5’h06	1.0500
		1’h0	5’h07	1.0625
		1'h1	5’h07	1.0750
		1’h0	5’h08	1.0875
		1'h1	5’h08	1.1000
		1’h0	5’h09	1.1125
		1'h1	5’h09	1.1250
		1’h0	5’h0A	1.1375
		1'h1	5’h0A	1.1500
		1’h0	5’h0B	1.1625
		1'h1	5’h0B	1.1750
		1’h0	5’h0C	1.1875
		1'h1	5’h0C	1.2000
		1’h0	5’h0D	1.2125
		1'h1	5’h0D	1.2250
		1’h0	5’h0E	1.2375
		1'h1	5’h0E	1.2500
		1’h0	5’h0F	1.2625
		1'h1	5’h0F	1.2750

	D7-D6	D5	D4-D0	BUCK1 OUTPUT VOLTAGE (V)
Data	Reserved	1’h0	5'h10	1.2875
		1'h1	5'h10	1.3000
		1’h0	5'h11	1.3125
		1’h0	5'h11	1.3250
		1'h1	5'h12	1.3375
		1’h0	5'h12	1.3500
		1'h1	5'h13	1.3625
		1’h0	5'h13	1.3750
		1'h1	5'h14	1.3875
		1’h0	5'h14	1.4000
		1'h1	5'h15	1.4125
		1’h0	5'h15	1.4250
		1'h1	5'h16	1.4375
		1’h0	5'h16	1.4500
		1'h1	5'h17	1.4625
		1’h0	5'h17	1.4750
		1’h0	5'h18	1.4875
		1'h1	5'h18	1.5000
		1’h0	5'h19	1.5125
		1'h1	5'h19	1.5250
		1’h0	5'h1A	1.5375
		1'h1	5'h1A	1.5500
		1’h0	5'h1B	1.5625
		1'h1	5'h1B	1.5750
		1’h0	5'h1C	1.5875
		1'h1	5'h1C	1.6000
		1'h0	5'h1D	1.6125
		1'h1	5'h1D	1.6250
		1'h0	5'h1E	1.6375
		1'h1	5'h1E	1.6500
		1'h0	5'h1F	1.6625
		1'h1	5'h1F	1.6750

8.6.9 BUCK1 Ramp Control Register (B1RC) - 0x25

This register allows the user to program the rate of change between the target voltages of Buck1.

	D7	D6-D4	D3-D0	
Name	- - - -	- - - -	B1RS	
Access	- - - -	- - - -	R/W	
Data	Reserved	Reserved	Data Code	Ramp Rate mV/us
			4'h0	Instant
			4'h1	1
			4'h2	2
			4'h3	3
			4'h4	4
			4'h'5	5
			4'h6	6
			4'h7	7
			4'h8	8
			4'h9	9
			4'hA	10
			4'hB - 4'hF	10

8.6.10 BUCK2 Target 1 Register (B2TV1) - 0x29

This register allows the user to program the output target voltage of Buck2 (target voltage 1).

	D7-D6	D5	D4-D0	BUCK2 OUTPUT VOLTAGE (V)
Name	—	Buck1 12.5 mV step	B2TV1	—
Access	—	R/W	R/W	—
Data	Reserved	1’h0	5’h00	0.8875
		1'h1	5’h00	0.9000
		1’h0	5’h01	0.9125
		1'h1	5’h01	0.9250
		1’h0	5’h02	0.9375
		1'h1	5’h02	0.9500
		1’h0	5’h03	0.9625
		1'h1	5’h03	0.9750
		1’h0	5’h04	0.9875
		1'h1	5’h04	1.0000
		1’h0	5’h05	1.0125
		1'h1	5’h05	1.0250
		1’h0	5’h06	1.0375
		1'h1	5’h06	1.0500
		1’h0	5’h07	1.0625
		1'h1	5’h07	1.0750
		1’h0	5’h08	1.0875
		1'h1	5’h08	1.1000
		1’h0	5’h09	1.1125
		1'h1	5’h09	1.1250
		1’h0	5’h0A	1.1375
		1'h1	5’h0A	1.1500
		1’h0	5’h0B	1.1625
		1'h1	5’h0B	1.1750
		1’h0	5’h0C	1.1875
		1'h1	5’h0C	1.2000
		1’h0	5’h0D	1.2125
		1'h1	5’h0D	1.2250
		1’h0	5’h0E	1.2375
		1'h1	5’h0E	1.2500
		1’h0	5’h0F	1.2625
		1'h1	5’h0F	1.2750

	D7-D6	D5	D4-D0	BUCK2 OUTPUT VOLTAGE (V)
Data	Reserved	1’h0	5'h10	1.2875
		1'h1	5'h10	1.3000
		1’h0	5'h11	1.3125
		1’h0	5'h11	1.3250
		1'h1	5'h12	1.3375
		1’h0	5'h12	1.3500
		1'h1	5'h13	1.3625
		1’h0	5'h13	1.3750
		1'h1	5'h14	1.3875
		1’h0	5'h14	1.4000
		1'h1	5'h15	1.4125
		1’h0	5'h15	1.4250
		1'h1	5'h16	1.4375
		1’h0	5'h16	1.4500
		1'h1	5'h17	1.4625
		1’h0	5'h17	1.4750
		1’h0	5'h18	1.4875
		1'h1	5'h18	1.5000
		1’h0	5'h19	1.5125
		1'h1	5'h19	1.5250
		1’h0	5'h1A	1.5375
		1'h1	5'h1A	1.5500
		1’h0	5'h1B	1.5625
		1'h1	5'h1B	1.5750
		1’h0	5'h1C	1.5875
		1'h1	5'h1C	1.6000
		1'h0	5'h1D	1.6125
		1'h1	5'h1D	1.6250
		1'h0	5'h1E	1.6375
		1'h1	5'h1E	1.6500
		1'h0	5'h1F	1.6625
		1'h1	5'h1F	1.6750

8.6.11 BUCK2 Target 2 Register (B2TV2) - 0x2A

This register allows the user to program the output target voltage of Buck2 (target voltage 2).

	D7-D6	D5	D4-D0	BUCK2 OUTPUT VOLTAGE (V)
Name	—	Buck1 12.5 mV step	B2TV2	—
Access	—	R/W	R/W	—
Data	Reserved	1’h0	5’h00	0.8875
		1'h1	5’h00	0.9000
		1’h0	5’h01	0.9125
		1'h1	5’h01	0.9250
		1’h0	5’h02	0.9375
		1'h1	5’h02	0.9500
		1’h0	5’h03	0.9625
		1'h1	5’h03	0.9750
		1’h0	5’h04	0.9875
		1'h1	5’h04	1.0000
		1’h0	5’h05	1.0125
		1'h1	5’h05	1.0250
		1’h0	5’h06	1.0375
		1'h1	5’h06	1.0500
		1’h0	5’h07	1.0625
		1'h1	5’h07	1.0750
		1’h0	5’h08	1.0875
		1'h1	5’h08	1.1000
		1’h0	5’h09	1.1125
		1'h1	5’h09	1.1250
		1’h0	5’h0A	1.1375
		1'h1	5’h0A	1.1500
		1’h0	5’h0B	1.1625
		1'h1	5’h0B	1.1750
		1’h0	5’h0C	1.1875
		1'h1	5’h0C	1.2000
		1’h0	5’h0D	1.2125
		1'h1	5’h0D	1.2250
		1’h0	5’h0E	1.2375
		1'h1	5’h0E	1.2500
		1’h0	5’h0F	1.2625
		1'h1	5’h0F	1.2750

	D7-D6	D5	D4-D0	BUCK2 OUTPUT VOLTAGE (V)
Data	Reserved	1’h0	5'h10	1.2875
		1'h1	5'h10	1.3000
		1’h0	5'h11	1.3125
		1’h0	5'h11	1.3250
		1'h1	5'h12	1.3375
		1’h0	5'h12	1.3500
		1'h1	5'h13	1.3625
		1’h0	5'h13	1.3750
		1'h1	5'h14	1.3875
		1’h0	5'h14	1.4000
		1'h1	5'h15	1.4125
		1’h0	5'h15	1.4250
		1'h1	5'h16	1.4375
		1’h0	5'h16	1.4500
		1'h1	5'h17	1.4625
		1’h0	5'h17	1.4750
		1’h0	5'h18	1.4875
		1'h1	5'h18	1.5000
		1’h0	5'h19	1.5125
		1'h1	5'h19	1.5250
		1’h0	5'h1A	1.5375
		1'h1	5'h1A	1.5500
		1’h0	5'h1B	1.5625
		1'h1	5'h1B	1.5750
		1’h0	5'h1C	1.5875
		1'h1	5'h1C	1.6000
		1'h0	5'h1D	1.6125
		1'h1	5'h1D	1.6250
		1'h0	5'h1E	1.6375
		1'h1	5'h1E	1.6500
		1'h0	5'h1F	1.6625
		1'h1	5'h1F	1.6750

8.6.12 BUCK2 Ramp Control Register (B2RC) - 0x2B

This register allows the user to program the rate of change between the target voltages of Buck2.

	D7	D6-D4	D3-D0	
Name	- - - -	- - - -	B2RS	
Access	- - - -	- - - -	R/W	
Data	Reserved	Reserved	Data Code	Ramp Rate mV/us
			4'h0	Instant
			4'h1	1
			4'h2	2
			4'h3	3
			4'h4	4
			4'h5	5
			4'h6	6
			4'h7	7
			4'h8	8
			4'h9	9
			4'hA	10
			4'hB - 4'hF	10
Reset	0	010	1000	

8.6.13 BUCK Function Register (BFCR) – 0x38

This register allows the Buck switcher clock frequency to be spread across a wider range, allowing for less Electro-magnetic Interference (EMI). The spread spectrum modulation frequency refers to the rate at which the frequency ramps up and down, centered at 2 MHz.

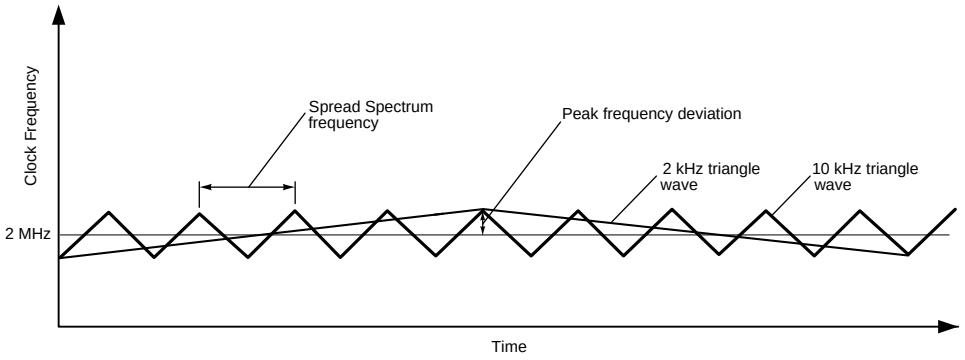


Figure 24. Spread Spectrum Frequency Modulation

8.6.14 Spread Spectrum Function

Periodic switching in the buck regulator is inherently a noisier function block compared to an LDO. It can be challenging in some critical applications to comply with stringent regulatory standards or simply to minimize interference to sensitive circuits in space limited portable systems. The regulator's switching frequency and harmonics can cause "noise" in the signal spectrum. The magnitude of this noise is measured by its power spectral density. The power spectral density of the switching frequency, FC, is one parameter that system designers want to be as low as practical to reduce interference to the environment and subsystems within their products. The LP8731-Q1 has a user-selectable function on the device, allowing a noise-reduction technique known as spread spectrum to be employed to ease customer's design and production issues.

The principle behind spread spectrum is to modulate the switching frequency slightly and slowly, and spread the signal frequency over a broader bandwidth. Thus, its power spectral density becomes attenuated, used as a spread spectrum clock via two I_2C control register bits bk_ssen, and slomod. With this feature enabled, the intense energy of the clock frequency can be spread across a small band of frequencies in the neighborhood of the center frequency. The results in a reduction of the peak energy!

The LP8731-Q1 spread spectrum clock uses a triangular modulation profile with equal rise and fall slopes. The modulation has the following characteristics:

- The center frequency: FC = 2 MHz, and
- The modulating frequency, fM = 6.8 kHz or 12 kHz.
- Peak frequency deviation: Δ_f = ±100 kHz (or ±5%)
- Modulation index $\beta = \Delta_f / f$M = 14.7 or 8.3

This register also allows dynamic scaling of the nPOR Delay Timing. The LP8731-Q1 is equipped with an internal Power-On Reset (POR) circuit which monitors the output voltage levels on the buck regulators, allowing the user to more actively monitor the power status of the device. The undervoltage lockout feature continuously monitor the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8 VDC. This prevents the user from damaging the power source (for example, the battery), but can be disabled if the user wishes.

The UVLO feature continuously monitor the raw input supply voltage (VINLDO12) and automatically disables the four voltage regulators whenever this supply voltage is less than 2.8 VDC. This prevents the user from damaging the power source (for example, the battery), but can be disabled if the user wishes.

NOTE

If the supply to VINs is close to 2.8 V with a heavy load current on the regulators, the device could power down due to UVLO. If the user wishes to keep the device active under those conditions, the bypass UVLO feature should be enabled.

	D7-D5	D4	D3-D2	D1	D0
Name	—	BP_UVLO	TPOR	BK_SLOMOD	BK_SSEN
Access	—	R/W	R/W	R/W	R/W
Data	Reserved	Bypass UVLO monitoring 0 - Allow UVLO 1 - Disable UVLO	nPOR Delay Timing 00 - 50 µs 01 - 50 ms 10 - 100 ms 11 - 200 ms	Buck Spread Spectrum Modulation 0 – 10-kHz triangular wave 1 – 2-kHz triangular wave	Spread Spectrum Function Output 0 – Disabled 1 – Enabled
Reset	000	Factory-Programmed Default		1	0

8.6.15 LDO1 Control Register (LDO1VCR) – 0x39

This register allows the user to program the output target voltage of LDO1.

	D7-D5	D4-D0	
Name	—	LDO1_OUT	
Access	—	R/W	
Data	Reserved	LDO1 Output voltage (V)	
		5'h00	0.8
		5'h01	0.9
		5'h02	1.0
		5'h03	1.1
		5'h04	1.2
		5'h05	1.3
		5'h06	1.4
		5'h07	1.5
		5'h08	1.6
		5'h09	1.7
		5'h0A	1.8
		5'h0B	1.9
		5'h0C	2.0
		5'h0D	2.1
		5'h0E	2.2
		5'h0F	2.3
		5'h10	2.4
		5'h11	2.5
		5'h12	2.6
		5'h13	2.7
		5'h14	2.8
		5'h15	2.9
		5'h16	3.0
		5'h17	3.1
		5'h18	3.2
		5'h19	3.3

8.6.16 LDO2 Control Register (LDO2VCR) – 0x3A

This register allows the user to program the output target voltage of LDO2.

	D7-D5	D4-D0	
Name	—	LDO2_OUT	
Access	—	R/W	
Data	Reserved	LDO2 Output voltage (V)	
		5'h00	0.8
		5'h01	0.9
		5'h02	1.0
		5'h03	1.1
		5'h04	1.2
		5'h05	1.3
		5'h06	1.4
		5'h07	1.5
		5'h08	1.6
		5'h09	1.7
		5'h0A	1.8
		5'h0B	1.9
		5'h0C	2.0
		5'h0D	2.1
		5'h0E	2.2
		5'h0F	2.3
		5'h10	2.4
		5'h11	2.5
		5'h12	2.6
		5'h13	2.7
		5'h14	2.8
		5'h15	2.9
		5'h16	3.0
		5'h17	3.1
		5'h18	3.2
		5'h19	3.3

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

One of the key features of this integrated PMU is that it requires effectively no design procedures because the output voltage is digitally programmable and bounded, compensation components are internally fixed or selected, and the external support capacitors and inductors and optimized for typical applications and performance. Given the I/O range and maximum loading are fixed and target transient and output ripple are prescribed, as reflected in *Design Requirements*, the external components values are optimized as follows:

- LDO C_{IN} = 1 µF, C_{OUT} = 0.47 µF
- Buck C_{IN} = C_{OUT} = 10 µF
- Buck Inductor = 2.2 µH

The *Component Selection* section also details the background and sample calculations for capacitor and inductor selections, should users choose to operate with different component values than those recommended in order to achieve other performance characteristics that typically suggested.

9.2 Typical Application

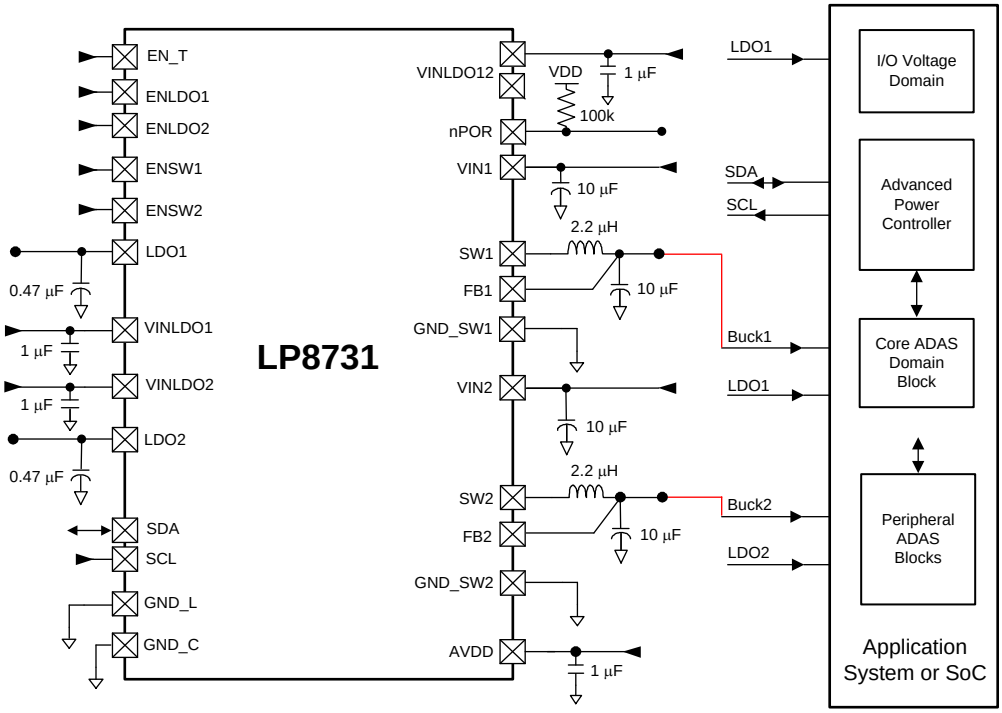


Figure 25. LP8731-Q1 Simplified Schematic

Typical Application (continued)

9.2.1 Design Requirements

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.8 V to 5.5 V
Switching frequency	2 MHz ±10%
Output voltage range: bucks	0.8875 V to 1.675 V
Output current rating: bucks	1.2 A
Output voltage range: LDOs	0.8 V to 3.3 V
Output current rating: LDOs	300 mA
Transient response at max load with Tr = Tf = 10 µs	ΔV_{OUT} approximately equals ±1%
Bucks output typical ripple voltage	< 10 mV PWM, < 20 mV PFM

9.2.2 Detailed Design Procedure

9.2.2.1 Component Selection

9.2.2.1.1 Inductors for SW1 and SW2

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating:

9.2.2.1.1.1 Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as follows:

$$I_{sat} > I_{outmax} + I_{ripple}$$

where $$I_{ripple} = \left(\frac{1}{f}\right) \times \left(\frac{V_{IN} - V_{OUT}}{2L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right)$$

where

- I_{RIPPLE}: Average to peak inductor current
- I_{OUTMAX}: Maximum load current
- V_{IN}: Maximum input voltage to the buck
- L: Min inductor value including worse case tolerances (30% drop can be considered for method 1)
- f: Minimum switching frequency (1.6 MHz)
- V_{OUT}: Buck Output voltage

(4)

9.2.2.1.1.2 Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the maximum current limit of 1800 mA for Buck1 and Buck2.

Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least:

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

(5)

Table 6. Suggested Inductors

INDUCTOR	VALUE	UNIT	L × W × H (mm)	DCR	IRMS RATING TYP	VENDORS	PART ID
L_{SW}1,2	2.2	µH	3.2 × 2.5 × 1.2	70 mΩ	2.1 A	Toko	DFE322512C
L_{SW}1,2	2.2	µH	3.2 × 2.5 × 1.55	64 mΩ	1.85 A	Murata	LQH32PN2R2NNCL
L_{SW}1,2	2.2	µH	3.2 × 2.5 × 1.2	70 mΩ	2.1 A	Chilisin	MHCD322512-2R2M-A8DY
L_{SW}1,2	2.2	µH	5.0 × 5.0 × 1.5	70 mΩ	2 A	Taiyo Yuden	NP04SZB 2R2N

9.2.2.1.2 External Capacitors

The regulators on the LP8731-Q1 require external capacitors for regulator stability. These are specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.2 LDO Capacitor Selection

9.2.2.2.1 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge currents when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains approximately 1 µF over the entire operating temperature range.

9.2.2.2.2 Output Capacitor

The LDOs on the LP8731-Q1 are designed specifically to work with very small ceramic output capacitors. A 0.47-µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, is suitable in the application circuit.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost.

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

9.2.2.2.3 Capacitor Characteristics

The LDOs are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive, and have the lowest ESR values, thus making them best for eliminating high-frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDOs.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values also show some decrease over time due to aging. The capacitor parameters are also dependent on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 26 is typical graph comparing different capacitor case sizes in a capacitance vs DC bias plot.

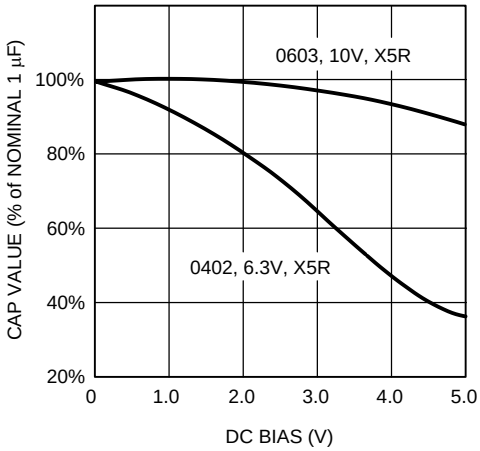


Figure 26. Typical Variation In Capacitance vs DC Bias

As shown in Figure 26, increasing the DC bias condition can result in the capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to 125°C, only varies the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to 85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature changes significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

9.2.2.2.4 Input Capacitor Selection for SW1 And SW2

A ceramic input capacitor of 10 µF, 6.3 V is sufficient for the magnetic DC-DC converters. Place the input capacitor as close as possible to the input of the device. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the DC-DC converter in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low Equivalent Series Resistance (ESR) provides the best noise filtering of the input voltage spikes due to fast current transients. A capacitor with sufficient ripple current rating should be selected. The Input current ripple can be calculated as:

$$I_{rms} = I_{outmax} \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 + \frac{r^2}{12}\right)} \text{ where } \quad r = \frac{(V_{in} - V_{out}) \times V_{out}}{L \times f \times I_{outmax} \times V_{in}} \tag{6}$$

The worse case is when $V_{IN} = 2 \times V_{OUT}$.

9.2.2.2.5 Output Capacitor Selection for SW1, SW2

A 10-µF, 6.3-V ceramic capacitor should be used on the output of the SW1 and SW2 magnetic DC-DC converters. The output capacitor needs to be mounted as close as possible to the output of the device. A large value may be used for improved input voltage filtering. The recommended capacitor types are X7R or X5R. Y5V type capacitors should not be used. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and DC bias curves should be requested from them and analyzed as part of the capacitor selection process.

The output filter capacitor of the magnetic DC-DC converter smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESD to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its ESR and can be calculated as follows:

$$V_{pp\text{-}c} = \frac{I_{ripple}}{4 \times f \times C} \quad (7)$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows:

$$V_{PP-ESR} = 2 \times I_{RIPPLE} \times R_{ESR} \quad (8)$$

Because the $V_{PP\text{-}C}$ and $V_{PP\text{-}ESR}$ are out of phase, the rms value can be used to get an approximate value of the peak-to-peak ripple:

$$V_{pp\text{-}rms} = \sqrt{V_{pp\text{-}c}^{2} + V_{pp\text{-}esr}^{2}} \quad (9)$$

NOTE

The output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}). The R_{ESR} is frequency dependent as well as temperature dependent. The R_{ESR} should be calculated with the applicable switching frequency and ambient temperature.

Table 7. Suggested Capacitors

CAPACITOR	VALUE	L × W × H (mm)	TYPE	TOLERANCE	VENDORS	PART ID
CLDO1, CLDO2	0.47 µF	1.0 × 0.5 × 0.5 (0402)	X7S, 10 V	10%	Murata	GCM155C71A474KE36
CSW1, CSW2	10 µF	3.2 × 1.6 × 1.6 (1206)	X7R, 16 V	20%	TDK	C3216XR71C106M
CSW1, CSW2	10 µF	2 × 1.25 × 1.45 (0805)	X5R, 16 V	20%	TDK	CGA4J1X5R1C106M125AC
CIN	1 µF	0.6 × 0.3 × 0.1 (0603)	X7R, 6.3 V	20%	TDK	C2012XR71C105K
CIN	1 µF	1.0 × 0.5× 0.5 (0402)	X7S, 10 V	10%	Murata	GCM155C71A105KE38

9.2.2.2.6 I^2C Pull-up Resistor

Both SDA and SCL pins need to have pull-up resistors connected to VINLDO12 or to the power supply of the I^2C master. The values of the pull-up resistors (typical approximately1.8 kΩ) are determined by the capacitance of the bus. Too large of a resistor combined with a given bus capacitance results in a rise time that would violate the maximum rise time specification. A too small resistor results in a contention with the pull-down transistor on either slave(s) or master.

9.2.2.2.7 Operation Without I^2C Interface

Operation of the LP8731-Q1 without the I^2C interface is possible if the system can operate with default values for the LDO and buck regulators. The I^2C-less system must rely on the correct default output values of the LDO and Buck converters.

9.2.2.3 Junction Temperature

The maximum junction temperature $T_{J\text{-}MAX\text{-}OP}$ is 125°C of the IC package.

The following equations demonstrate junction temperature determination, ambient temperature $T_{A\text{-}MAX}$, and total device power must be controlled to keep T_J below this maximum:

$\mathbf{T_{J\text{-}MAX\text{-}OP}} = T_{A\text{-}MAX} + (R_{\theta JA})$ [°C/ Watt] * ($P_{D\text{-}MAX}$) [Watts]

Total IC power dissipation $P_{D\text{-}MAX}$ is the sum of the individual power dissipation of the four regulators plus a minor amount for device overhead. Device overhead is Bias, TSD and LDO analog.

$\mathbf{P_{D\text{-}MAX}} = P_{LDO1} + P_{LD02} + P_{BUCK1} + P_{BUCK2} + (0.0001\ A \times V_{IN})$ [Watts].

Power dissipation of LDO1

$P_{LDO1} = (V_{INLDO1} - V_{OUTLDO1}) \times I_{OUTLDO1}$ [V × A]

Power dissipation of LDO2

$P_{LDO2} = (V_{INLDO2} - V_{OUTLDO2}) \times I_{OUTLDO2}$ [V × A]

Power dissipation of Buck1

$P_{Buck1} = P_{IN} - P_{OUT} =$

$V_{OUTBuck1} \times I_{OUTBuck1} \times (1 - \eta_1) / \eta_1$ [V × A]

η_1 = efficiency of buck 1

Power dissipation of Buck2

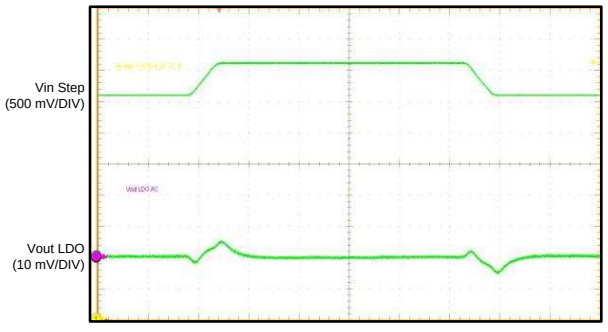
$P_{Buck2} = P_{IN} - P_{OUT} =$

$V_{OUTBuck2} \times I_{OUTBuck2} \times (1 - \eta_2) / \eta_2$ [V × A]

η_2 = efficiency of Buck2

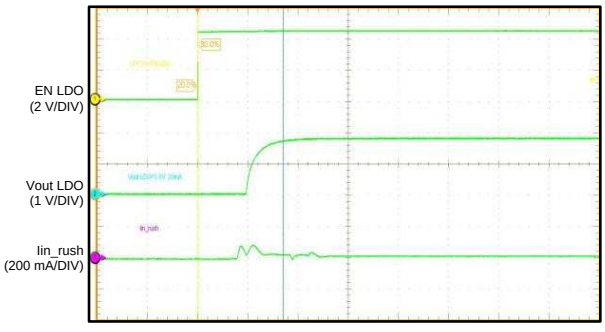
Where η is the efficiency for the specific condition taken from efficiency graphs.

9.2.3 Application Curves (LDO)



V_{IN} = 3.6 V to 4.2 V
V_{OUT} = 1.8 V
I_{OUT} = 300 mA
Tr = Tf = 30 µs

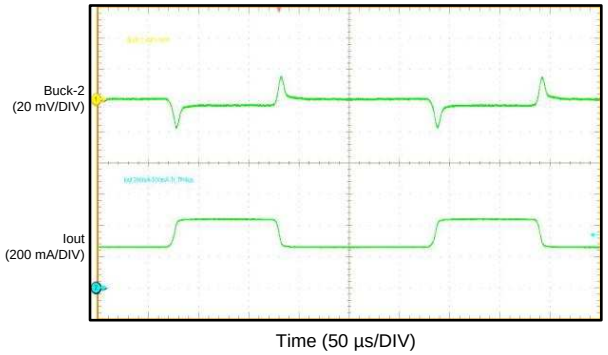
Figure 27. Line Transient 300-mA, 30-µs Edge Rate



V_{IN} = 3.6 V
V_{OUT} = 1.8 V
I_{OUT} = 200 mA
EN Tr = 18 ns

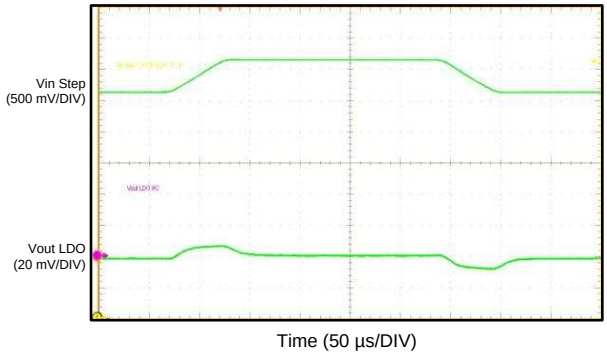
Figure 28. LDO Enable Start-Up Time and Inrush

9.2.4 Application Curves (BUCK)



I_{OUT} = 300 mA to 500 mA PWM

Figure 29. Buck Load Transient PWM Mode



V_{IN} Step I_{OUT} = 300 mA Tr = Tf = 30 µs

Figure 30. Buck Line Transient PWM

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. This input supply may be a battery or regulated source with sufficient low internal resistance such that it is able to deliver the maximum input current and maintain stable voltage without significant voltage drop during start-up and at load transient conditions. Additional bulk capacitance may be necessary should the supply source is located more than five centimeters away from the LP8731-Q1.

10.1 Analog Power Signal Routing

All power inputs should be tied to the main VDD source (for example, battery), unless the user wishes to power it from another source. (that is, external LDO output).

The analog VDD input pins power the internal bias and error amplifiers, so they should be tied to the main VDD. The analog VDD inputs must have an input voltage between 2.8 and 5.5 V, as specified in the *General Electrical Characteristics* table.

The other input pins (VINLDO1, VINLDO2, VIN1, and VIN2) can actually have inputs lower than 2.8 V, as long as it is higher than the programmed output (0.3 V, to be safe).

The analog and digital grounds should be tied together outside of the device to reduce noise coupling.

11 Layout

11.1 Layout Guidelines

The LP8731-Q1 is a monolithic device with integrated power FETs. For that reason, it is important to pay special attention to the use of appropriate to input, output, power, and ground track dimensions in the PCB layout in order to achieve low impedance small current loop paths and tracks with adequate current density to carry the target currents.

The device pin solder bumps are arranged with power and ground bumps at the edges of the package to facilitate PCB layout considerations. This enables using the top metal layer to route the power and ground tracks. Thus, the current loops for the bucks can be very short and this also makes placing the bypass caps on the device side of the PCB possible. (See Figure 31.) Avoid using vias to tap power and ground planes for the switcher supply pins, because they can be very inductive and could incur large i*dv/dt transient voltage drops. If vias are unavoidable, use them liberally to minimize the impedance they may present.

For more information on board layout techniques, refer to Texas Instruments AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009). This application note also discusses recommended PCB pad geometry, package handling, solder stencil and the assembly process. See also Texas Instruments AN-1229 *SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054) and Texas Instruments AN-2078 *PCB Layout for Texas Instrument' SIMPLE SWITCHER® Power Modules* (SNVA452).

11.2 Layout Example

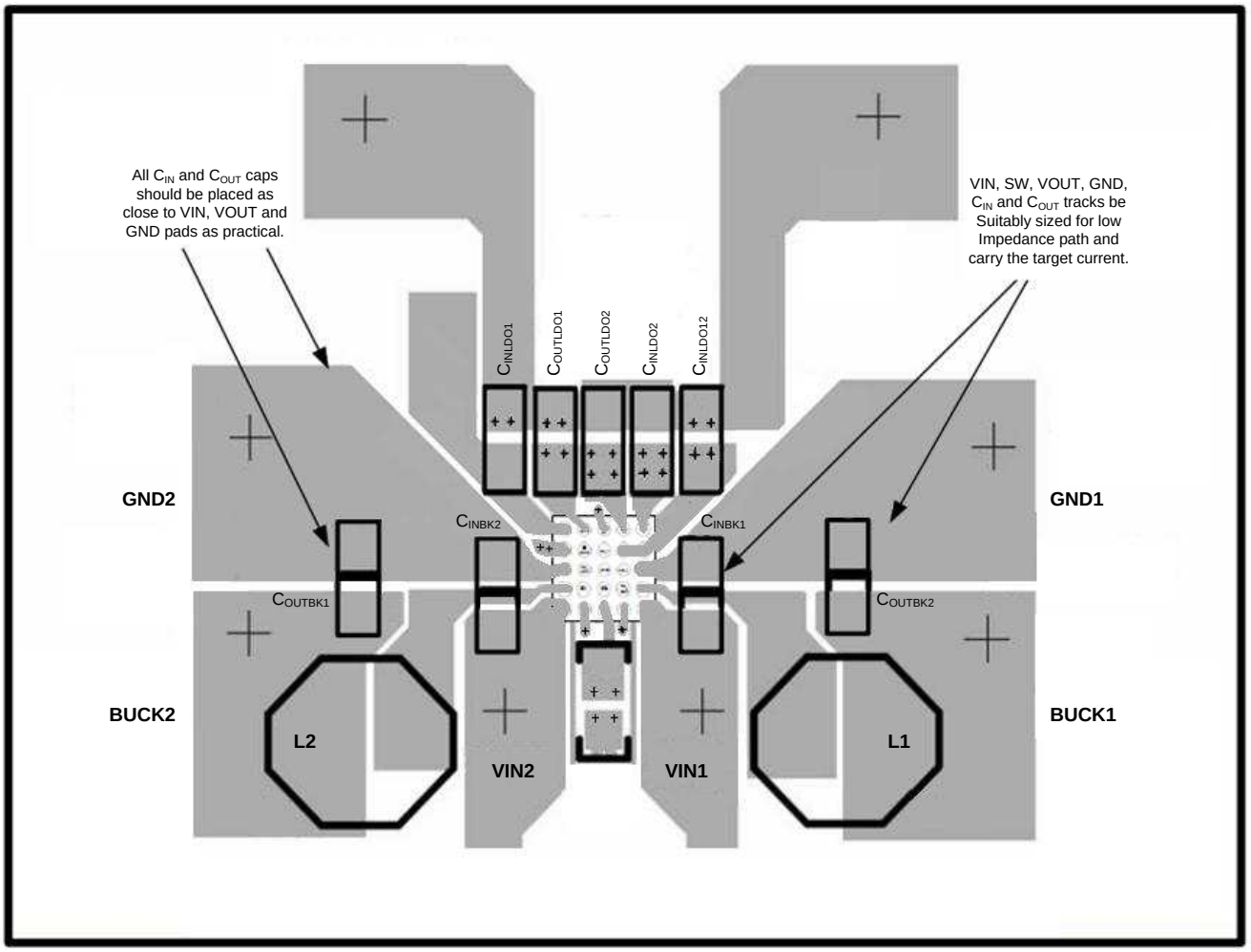


Figure 31. LP8731-Q1 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

Texas Instrument AN-1229 *SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054).

Texas Instruments AN-2078 *PCB Layout for Texas Instrument'sSIMPLE SWITCHER® Power Modules* (SNVA452).

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8731QYZRRQ1	ACTIVE	DSBGA	YZR	25		TBD	Call TI	Call TI	-40 to 125	RAEQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

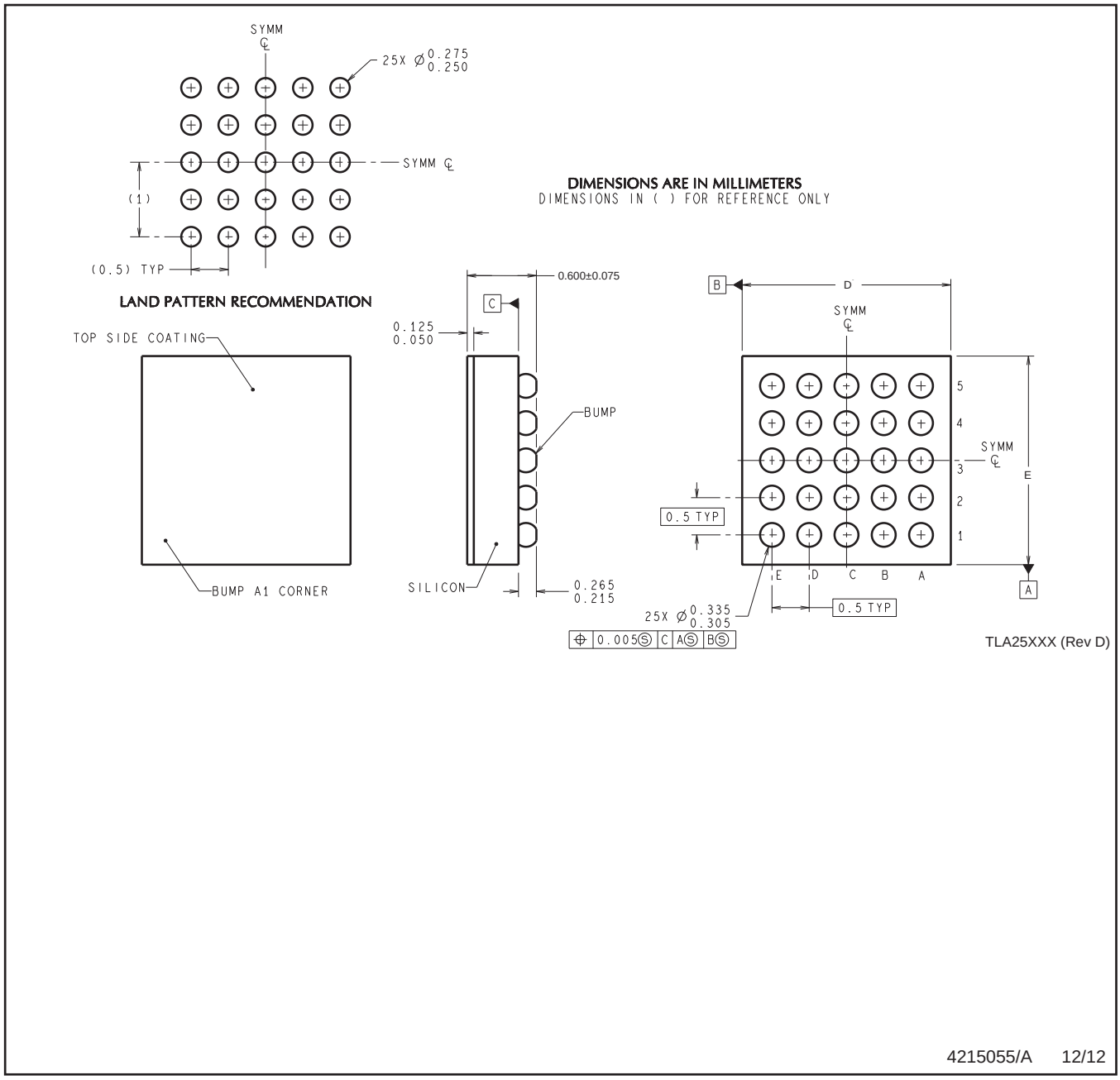
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YZR0025



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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