TMS470R1x General-Purpose Input/ Output (GIO) Reference Guide

Literature Number: SPNU192D
January 2005

Texas Instruments

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REVISION HISTORY

REVISION	DATE	NOTES
D	1/05	Modified document to reflect 8 ports, A–H.
C	10/03	Updates: Throughout, changed from 8 to a maximum of 64 ports Throughout, all ports are now I/O capable Page 6, internal register table updated Page 15, Table 2 updated Page 22, updated GIO control registers table Pages 33-51, added GIOENA2, GIOPOL2, GIOFLG2 and GIOPRY2 registers Pages 33-51, changed GIOENAn, GIOPOLn, GIOFLGn and GIO-PRYn registers to 32 bits Pages 37-42, changed GIOOFFA, GIOEMUA, GIOOFFB and GIOEMUB to seven bits Page 51, updated register names
B	10/02	Updates: Page 12, Wakeup Condition note added Page 21, Pullup/pulldown function description
A	9/02	Converted to a stand-alone book
*	10/98	*Initial version*

Contents

Figures

Tables

General-Purpose Input/Output

The general-purpose input/output (GIO) module provides the TMS470R1x family of devices with input/output (I/O) capability. The I/O pins are bidirectional and bit-programmable. The GIO module supports up to 64 external interrupts; these interrupt pins are multiplexed with I/O pins within all the GIO ports.

Topic **Page**

1 Overview

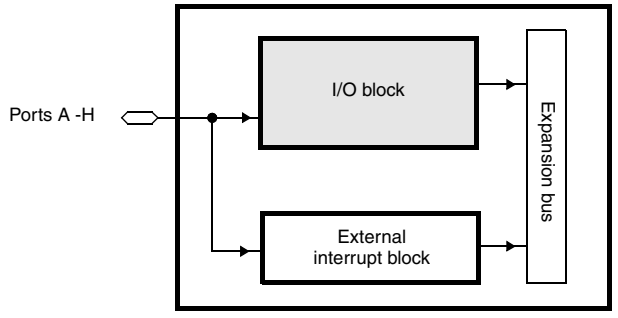
The GIO module has the following features:

- ❏ Each I/O pin is controlled by bits in five registers:
  - ■ Data direction (GIODIR)
  - ■ Data input (GIODIN)
  - ■ Data output (GIODOUT)
  - ■ Data set (GIODSET)
  - ■ Data clear (GIODCLR)
- ❏ The interrupts have the following characteristics:
  - ■ Programmable edge-detection (set in GIOPOL register)
  - ■ Individual interrupt flags (set in GIOFLG register)
  - ■ Individual enables (set in GIOENA register)
  - ■ Programmable priority (set in GIOPRY register)
- ❏ Internal pullup/pulldown allows you to leave unused I/O pins unconnected.

2 Functional Description of GIO Module

The GIO module (see Figure 1) comprises two separate components: an input/output (I/O) block and an external interrupt block.

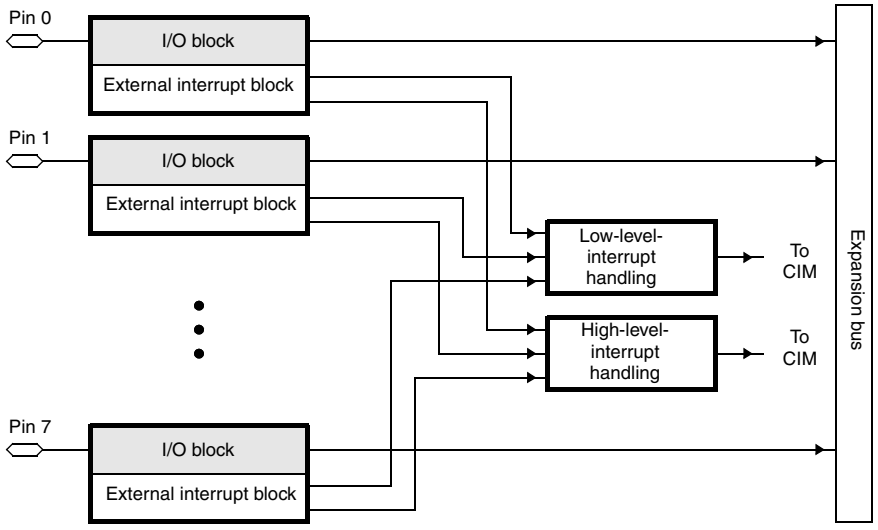
Figure 1. GIO Module Diagram



The pins on ports A, B, C, D, E, F, G, and H (shown in Figure 2) are all interrupt-capable pins and can be used to handle either general I/O functions or external interrupt signals. The GIO module can support up to 64 external interrupt pins; however, the actual number of pins is device-specific. Please refer to the device-specific data sheet for the exact number of external interrupt pins.

All port pins are connected to both an I/O block and an external interrupt block. Each of the 64 I/O blocks is connected to the expansion bus, whereas the interrupt blocks are physically attached to a single high-level- interrupt-handling block and to a single low-level-interrupt-handling block. The high-level-interrupt-handling block and the low-level-interrupt-handling block each send one signal to the central interrupt manager (CIM) in the system module for processing.

Figure 2. GIO Port A-H Module Diagram

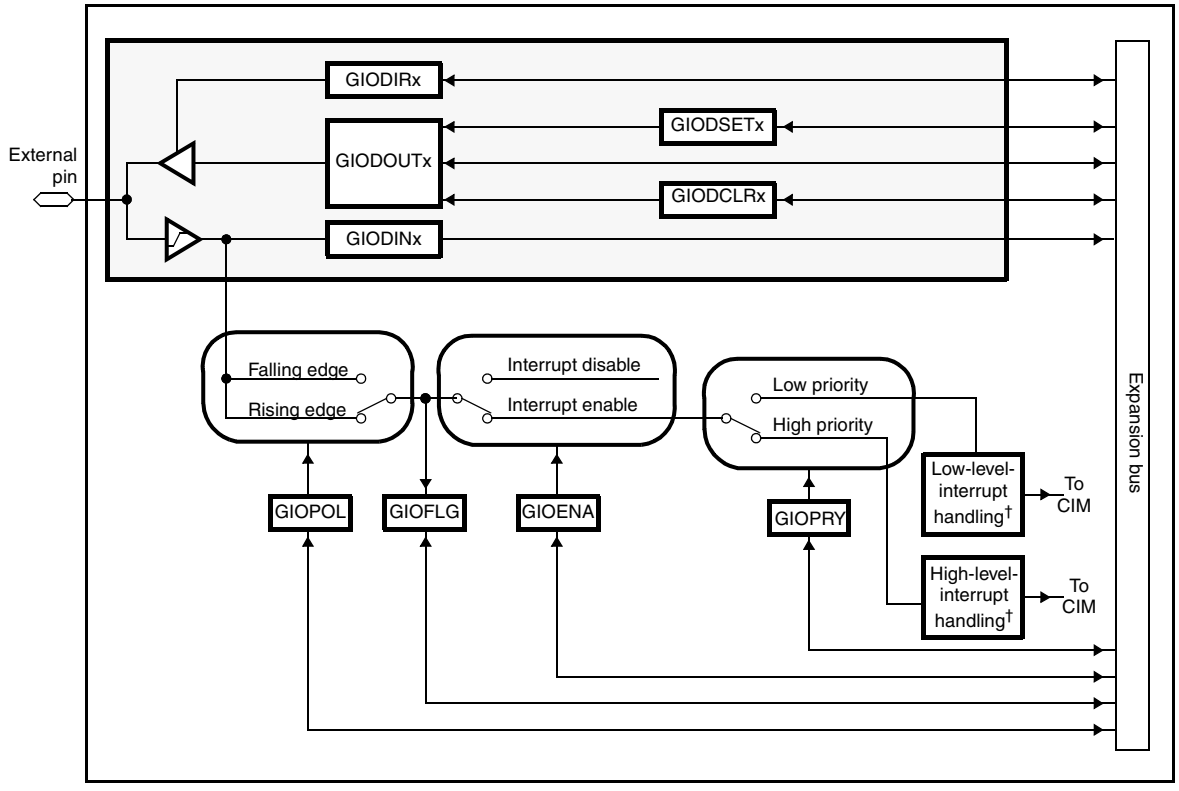


Note: Not all devices have 64 external interrupts. Consult the device specification for details.

2.1 GIO Block Diagram

The GIO block diagram (see Figure 3) represents the flow of information through a pin. The shaded area corresponds to the I/O block; the unshaded area corresponds to the external interrupt block.

Figure 3. GIO Block Diagram



† A single low-level-interrupt-handling block and a single high-level-interrupt-handling block service all of the interrupt-capable external pins, but only one pin can be serviced by an interrupt block at a time.

The high-level and the low-level-interrupt-handling blocks each contain an offset register and an emulation register. The high-level interrupts are denoted as level A (GIOOFFA and GIOEMUA); the low-level interrupts are denoted as level B (GIOOFFB and GIOEMUB). For details on interrupt levels, see Section 2.4.2 on page 11.

2.2 GIO Internal Registers

A general representation of the GIO internal registers is shown in Table 1. The page column provides a cross-reference to additional information on the individual registers. For a more detailed description of the individual bits, see Table 3.

Table 1. GIO Internal Registers

Offset Address†	Mnemonic	Name	Description	Page
0x00	GIOPWDN	GIO Power Down	Controls the module power-down status	29
0x04	GIOENA1	GIO Interrupt Enable	Configures corresponding pins as interrupts	30
0x08	GIOPOL1	GIO Interrupt Polarity	Causes flag to set on falling or rising edge	32
0x0C	GIOFLG1	GIO Interrupt Flag	Indicates that an appropriate transition edge has occurred	34
0x10	GIOPRY1	GIO Interrupt Priority	Sets interrupts for high or low priority	36
0x14	GIOOFFA	GIO Offset A	Provides offset that represents the pending external high-priority interrupt	38
0x18	GIOEMUA	GIO Emulation A	Reflects contents of GIOOFFA register	39
0x1C	GIOOFFB	GIO Offset B	Provides offset that represents the pending external low-priority interrupt	40
0x20	GIOEMUB	GIO Emulation B	Reflects contents of GIOOFFB register	41
0x24 ‡	GIODIRx	GIO Data Direction	Configures corresponding pin as an input or output	42
0x28	GIODINx	GIO Data Input	Reflects current value on input pins	44
0x2C	GIODOUTx	GIO Data Output	Specifies value output to pins	47
0x30	GIODSETx	GIO Data Set	Sets bits in the GIODOUTx register	49
0x34	GIODCLRx	GIO Data Clear	Clears bits in the GIODOUTx register	52
0xC4	GIOENA2	GIO Interrupt Enable	Configures corresponding pins as interrupts	56
0xC8	GIOPOL2	GIO Interrupt Polarity	Causes flag to set on falling or rising edge	58
0xCC	GIOFLG2	GIO Interrupt Flag	Indicates that an appropriate transition edge has occurred	60
0xD0	GIOPRY2	GIO Interrupt Priority	Sets interrupts for high or low priority	62

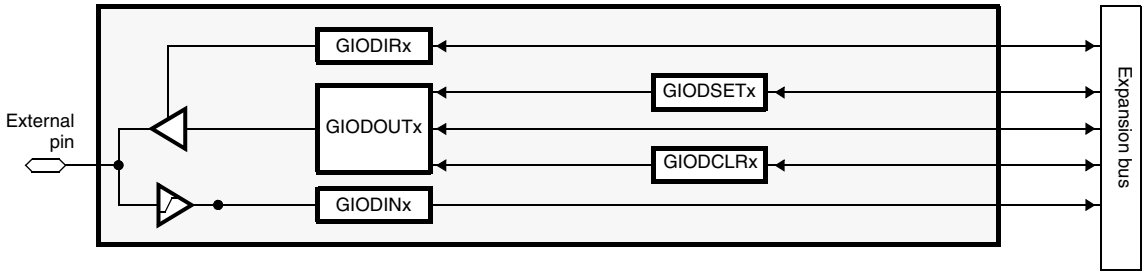
† The physical address of these registers is device-specific. If the GIO memory begins at 0xFFF7EC00, the GIOENA register is located at 0xFFF7EC04. See the specific device data sheet to verify the register addresses.

‡ The shaded registers (GIODIRx, GIODINx, GIODOUTx, GIODSETx, GIODCLRx) exist for each I/O port. The beginning offset addresses for each sequence of five registers are: 0x24, 0x38, 0x4C, 0x60, 0x74, 0x88, 0x9C and 0xB0. See the specific device data sheet to verify the register addresses.

2.3 I/O Block

Each pin serviced by port A, B, C, D, E, F, G and H contains its individual I/O block. See Figure 4.

Figure 4. I/O Block

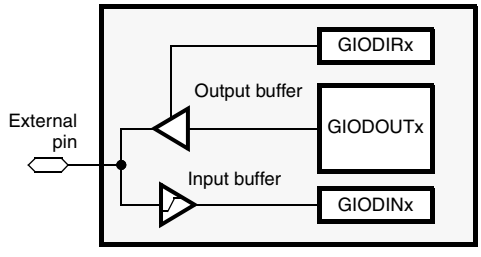


2.3.1 I/O Function

The GIO module sends data to the external pin through the output buffer and receives data from the external pin through the input buffer (see Figure 5). The three registers used are:

- ❏ GIODIRx controls the direction that information is sent. The GIODIRx register determines whether or not values in the data output register are sent to the external pin. The input buffer is always enabled. Therefore, the information that is sent to the external pin is also received in the input buffer.
- ❏ GIODOUTx controls what information is sent to the external pin.
- ❏ GIODINx receives the information from the external pin.

Figure 5. I/O Buffers



A high voltage (V_{IH} or greater) applied to the pin causes a high value (1) in the data input register (GIODINx). When a low voltage (V_{IL} or less) is applied to the pin, the data input register reads a low value (0).

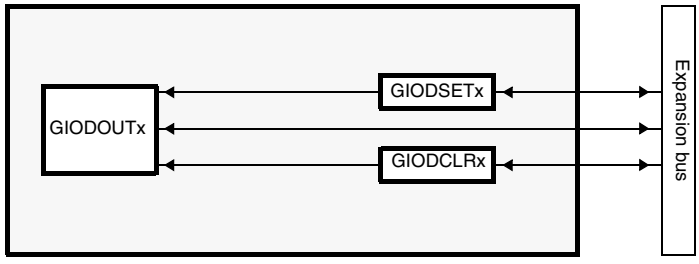
The output buffer can be enabled or disabled through the data direction register (GIODIRx). To enable the output buffer, the data direction register must be set to 1.

When the output buffer is enabled, writing values to the data output register (GIODOUTx) applies a voltage to the output pin. A low value (0) written to the data output register forces the pin to a low output voltage (V_{OL} or lower). A high value (1) written to the data output register forces the pin to a high output voltage (V_{OH} or higher).

2.3.2 Output Control Registers

When the output buffer is enabled, the value in the data output register (GIODOUTx) specifies the voltage applied to the external pin. The GIO module provides three ways of communicating with the data output control register (see Figure 6).

Figure 6. Communication With the Data Output Register



- ❏ The control register bit can be written directly by moving an appropriate value to the data output register. A low value (0) written to the data output register forces the pin to a low output voltage (V_{OL} or lower), whereas a high value (1) written to the data output register forces the pin to a high output voltage (V_{OH} or higher).
- ❏ The data output register bit can be set to 1 by using the data set register (GIODSETx). A low value (0) written to the data set register does not affect the value in the data output register. A high value (1) written to the data set register sets the data output register (GIODOUTx) bit high (1).
- ❏ The data output register bit can be cleared to 0 by using the data clear register (GIODCLRx). A low value (0) written to the data clear register does not affect the value in the data output register. A high value (1) written to the data clear register clears (0) the corresponding bit in the data output register (GIODOUTx).

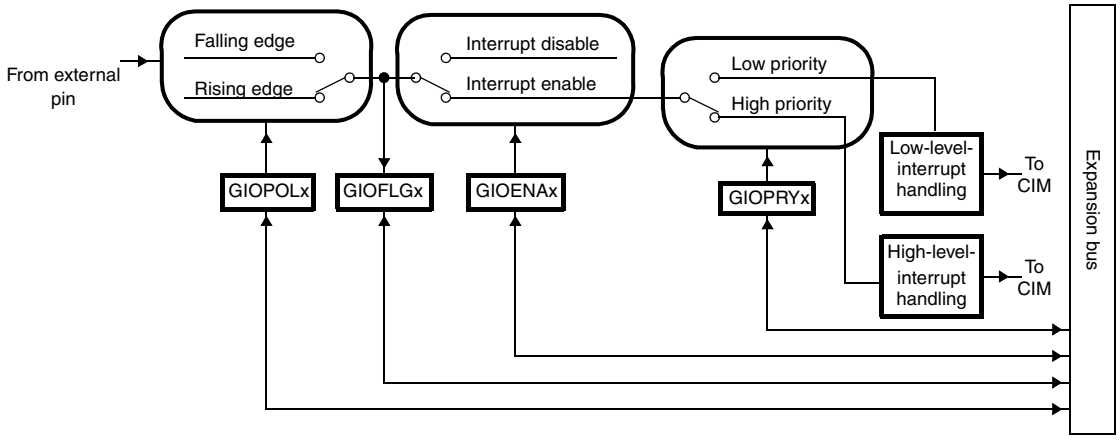
The GIODSETx and GIODCLRx registers allow improved handling of data. The data set and data clear registers remove any possibility of a read-modify-write (RMW) operation.

Note: RMW is possible when the CPU reads a register, performs some action (for example, an OR operation), and then writes the values back into the register. It is possible that the contents of the original register (GIODOUTx) can change (for example, an interrupt procedure) between the time when the CPU originally reads the register and the time when the CPU writes the new value. In this case, the new value written by the CPU overwrites the existing value, and the overwritten value is lost.

2.4 External Interrupt Block

All port interrupt-capable pins connect to the GIO module's single low-level-interrupt-handling block and single high-level-interrupt-handling block. Depending on the priority, the interrupt signal is sent through the appropriate offset register to the central interrupt manager (CIM) in the system module (see Section 2.4.3 on page 12). Figure 7 shows the external interrupt block.

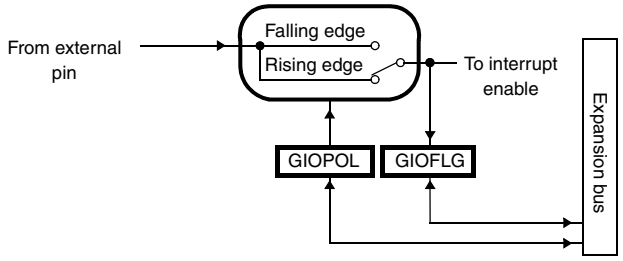
Figure 7. External Interrupt Block



2.4.1 Edge Detection and the Flag Register

The edge-detection hardware and flag register, like the input buffer, are always enabled. The GIOPOLx register (see Figure 8) specifies that the edge-detect flag is set on either the rising or falling edge.

Figure 8. Edge Detection and Flag Register



A rising edge occurs when the voltage on a given pin changes from a low value (V_{IL} or lower) to a high value (V_{IH} or higher). The voltage on the external pin must remain at the high level for at least one ICLK cycle to ensure recognition. (For an explanation of ICLK, see the clock portion of the *TMS470 System Module*, literature number SPNU189.)

A falling edge occurs when the voltage on the external pin changes from a high value (V_{IH} or higher) to a low value (V_{IL} or lower). The voltage on the external pin must remain at the low level for at least one ICLK cycle to ensure recognition. (GIOPOL behaves differently in a power-down state. See Section 3.3 on page 18, for more information.)

The corresponding flag in the GIOFLGx register is set when a transition appearing on the external pin matches the edge chosen in the GIOPOLx register. For example, to set the flag on a rising edge on pin 2 of GIO port A, set the bit in the polarity register (GIOPOL1.2 = 1). Then, when the signal transition takes place, the GIO module will set the appropriate flag in the flag register (GIOFLG1.2 = 1).

Note: Setting Flag With Interrupt Disabled

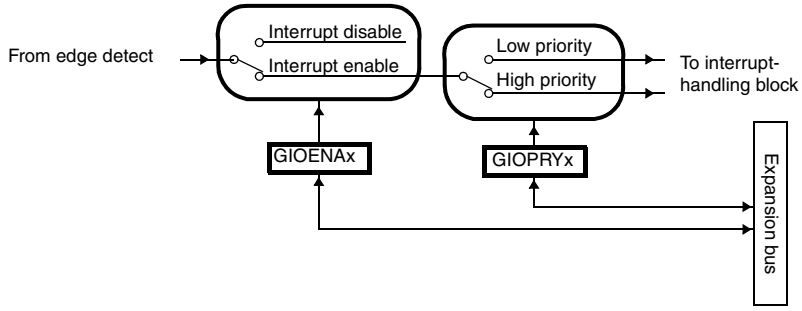
The flag can be set regardless of whether or not the interrupt is enabled. The flag register can then be polled instead of driving an interrupt. Additionally, you should ensure that the flag is not set before enabling the interrupt; specifically, you should clear the flag register before enabling the interrupt.

The edge-detection hardware responds to voltages on the external pin and does not discriminate between the source of these voltages. Therefore, if the output is enabled, the interrupt will respond to the correct edge though it is generated by the output buffer. Typically, the output buffer should be disabled when the flag is used.

2.4.2 Interrupts and Interrupt Levels

The interrupt flag is set when a transition on the external pin matches the edge chosen in the GIOPOLx register. An interrupt can be generated from the set flag if the interrupt is enabled (see Figure 9).

Figure 9. Interrupt Enable and Priority Level



The GIOENAx register enables the interrupt. If the interrupt is enabled, the signal with an appropriate edge leads to an interrupt. If multiple interrupts occur simultaneously, the GIO module must prioritize the interrupts so that they can be handled in order.

The order in which simultaneous GIO interrupts are processed is determined by the following criteria:

- The GIO priority control register (GIOPRYx) provides a software-implemented prioritization scheme. Each pin can be set as either a high-priority or low-priority interrupt. Interrupts with a high priority are serviced before ones with a low priority.
- The handling of interrupts with the same priority is determined by the interrupt with the lowest bit value, which has the highest priority. This prioritization is hardwired into the module.

When multiple interrupts occur simultaneously, as in Example 1, the GIO module sends the lowest bit for each level to the central interrupt manager (CIM) in the system module for processing, according to the criteria above. (For additional information on the CIM, see the *TMS470 System Module*, literature number SPNU189.)

Note: Wakeup Condition

GIO interrupts are also used to awaken the device from halt and standby modes.

Example 1. Determining Interrupt Priority

Pin	3	2	1	0
Priority	High	Low	High	Low
Order	2	4	1	3

In Example 1, four interrupts occur simultaneously on GIO port A, pins 3–0 and are handled as described in the following:

1) The interrupts on pin 1 and pin 0 are both sent to the CIM for servicing because they have the lowest values among the high-level and low-level interrupts. Assuming that the CIM is set to service the high priority before low priority, pin 1 is serviced first because it is the high-priority interrupt.
2) Next, the interrupts on pin 3 and pin 0 are sent to the CIM for servicing. The interrupt on pin 3 is serviced because it is the only remaining high-priority interrupt.
3) The interrupt on pin 0 is serviced third because it has the lowest bit value.
4) The interrupt on pin 2 is serviced last because it is the only remaining interrupt.

2.4.3 High-Level-Interrupt Block and Low-Level-Interrupt Block

The interrupt-handling blocks each contain two registers — an offset register and an emulation register. The high-level interrupts are denoted as level A and consequently, the registers within the high-level-interrupt-handling block are GIOOFFA and GIOEMUA (see Figure 10). Likewise, the registers within the low-level-interrupt-handling block are GIOOFFB and GIOEMUB (Figure 11).

Figure 10. High-Level-Interrupt-Handling Block

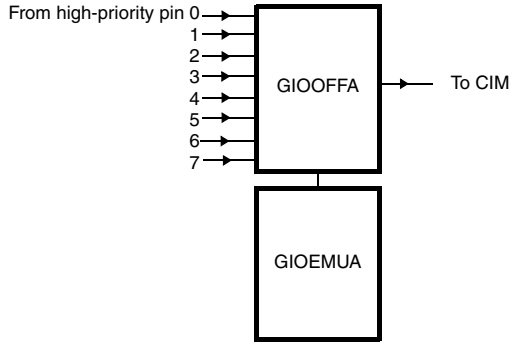
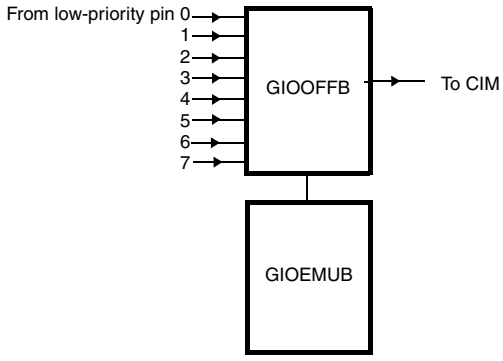


Figure 11. Low-Level-Interrupt-Handling Block



The read-only registers, GIOOFFA and GIOOFFB, generate a numerical offset value that represents the pending external interrupt (see Table 2). The offset can be used to locate the position of the interrupt routine in the vector table. A read of the offset register clears the offset register and the corresponding flag bit in the GIOFLG register.

The high-level offset register, GIOOFFA, receives signals from each active interrupt that is configured as high priority. The GIOOFFA displays the high-level interrupt with the highest priority (that is, the interrupt that was generated by the lowest bit in the flag register). Similarly, the GIOOFFB displays the low-level interrupt with the highest priority.

The emulation control registers (GIOEMUA and GIOEMUB) mirror the offset registers. The emulation registers contain a numerical offset value that represents the pending external interrupt (see Table 2). A read of the emulation registers does not clear any register or any bit. These registers allow the device emulator to read and display the offset register values without affecting interrupt execution..

Table 2. GIO Offset Table of High and Low Priority External Interrupts†

GIOOFF.6	GIOOFF.5	GIOOFF.4	GIOOFF.3	GIOOFF.2	GIOOFF.1	GIOOFF.0	Pending External Interrupt
0	0	0	0	0	0	0	No interrupt
0	0	0	0	0	0	1	Interrupt 0
0	0	0	0	0	1	0	Interrupt 1
0	0	0	0	0	1	1	Interrupt 2
0	0	0	0	1	0	0	Interrupt 3
0	0	0	0	1	0	1	Interrupt 4

† The interrupt values in this table are the same for GIO offset A and GIO offset B.

Table 2. GIO Offset Table of High and Low Priority External Interrupts†

GIOOFF.6	GIOOFF.5	GIOOFF.4	GIOOFF.3	GIOOFF.2	GIOOFF.1	GIOOFF.0	Pending External Interrupt
0	0	0	0	1	1	0	Interrupt 5
0	0	0	0	1	1	1	Interrupt 6
0	0	0	1	0	0	0	Interrupt 7
0	0	0	1	0	0	1	Interrupt 8
0	0	0	1	0	1	0	Interrupt 9
0	0	0	1	0	1	1	Interrupt 10
0	0	0	1	1	0	0	Interrupt 11
0	0	0	1	1	0	1	Interrupt 12
0	0	0	1	1	1	0	Interrupt 13
0	0	0	1	1	1	1	Interrupt 14
0	0	1	0	0	0	0	Interrupt 15
0	0	1	0	0	0	1	Interrupt 16
0	0	1	0	0	1	0	Interrupt 17
0	0	1	0	0	1	1	Interrupt 18
0	0	1	0	1	0	0	Interrupt 19
0	0	1	0	1	0	1	Interrupt 20
0	0	1	0	1	1	0	Interrupt 21
0	0	1	0	1	1	1	Interrupt 22
0	0	1	1	0	0	0	Interrupt 23
0	0	1	1	0	0	1	Interrupt 24
0	0	1	1	0	1	0	Interrupt 25
0	0	1	1	0	1	1	Interrupt 26
0	0	1	1	1	0	0	Interrupt 27
0	0	1	1	1	0	1	Interrupt 28
0	0	1	1	1	1	0	Interrupt 29
0	0	1	1	1	1	1	Interrupt 30
0	1	0	0	0	0	0	Interrupt 31
0	1	0	0	0	0	1	Interrupt 32
0	1	0	0	0	1	0	Interrupt 33
0	1	0	0	0	1	1	Interrupt 34
0	1	0	0	1	0	0	Interrupt 35
0	1	0	0	1	0	1	Interrupt 36
0	1	0	0	1	1	0	Interrupt 37
0	1	0	0	1	1	1	Interrupt 38
0	1	0	1	0	0	0	Interrupt 39

† The interrupt values in this table are the same for GIO offset A and GIO offset B.

Table 2. GIO Offset Table of High and Low Priority External Interrupts†

GIOOFF.6	GIOOFF.5	GIOOFF.4	GIOOFF.3	GIOOFF.2	GIOOFF.1	GIOOFF.0	Pending External Interrupt
0	1	0	1	0	0	1	Interrupt 40
0	1	0	1	0	1	0	Interrupt 41
0	1	0	1	0	1	1	Interrupt 42
0	1	0	1	1	0	0	Interrupt 43
0	1	0	1	1	0	1	Interrupt 44
0	1	0	1	1	1	0	Interrupt 45
0	1	0	1	1	1	1	Interrupt 46
0	1	1	0	0	0	0	Interrupt 47
0	1	1	0	0	0	1	Interrupt 48
0	1	1	0	0	1	0	Interrupt 49
0	1	1	0	0	1	1	Interrupt 50
0	1	1	0	1	0	0	Interrupt 51
0	1	1	0	1	0	1	Interrupt 52
0	1	1	0	1	1	0	Interrupt 53
0	1	1	0	1	1	1	Interrupt 54
0	1	1	1	0	0	0	Interrupt 55
0	1	1	1	0	0	1	Interrupt 56
0	1	1	1	0	1	0	Interrupt 57
0	1	1	1	0	1	1	Interrupt 58
0	1	1	1	1	0	0	Interrupt 59
0	1	1	1	1	0	1	Interrupt 60
0	1	1	1	1	1	0	Interrupt 61
0	1	1	1	1	1	1	Interrupt 62
1	0	0	0	0	0	0	Interrupt 63

† The interrupt values in this table are the same for GIO offset A and GIO offset B.

Example 2 illustrates how to identify the interrupt being serviced. This example assumes that interrupts 0 and 2 occur simultaneously (both low priority) on a device with three interrupt-capable pins. Reading the flag control register, GIOFLG, returns a value of xxxxx101. The first five values are indeterminate. Reading the offset B control register, GIOOFFB, returns a value of 00000001, indicating that the interrupt on pin 0 is being processed (see Table 2).

Example 2. Reading the Offset Register to Determine Serviced Interrupt

Bits	7	6	5	4	3	2	1	0
GIOENA1			Reserved			1	1	1
GIOPOL1			Reserved			1	0	0
GIOFLG1			Reserved			1	0	1
GIOPRY1			Reserved			0	0	0

Bits	7	6	5	4	3	2	1	0
GIOOFFA	0	0	0	0	0	0	0	0
GIOEMUA	0	0	0	0	0	0	0	0
GIOOFFB	0	0	0	0	0	0	0	1
GIOEMUB	0	0	0	0	0	0	0	1

2.4.4 Special Considerations for Interrupts

Please note that interrupts are subject to the following special considerations:

- ❏ On devices where fewer than 64 interrupts are available, the unused control register bits are reserved.
- ❏ To use the enabled pins as interrupts, the I/O function of the pins is typically set as input. If the pin's I/O function is set as output, the signal feeds directly into the input. In this case, interrupts are only generated when the device toggles the data output register, thereby creating the appropriate interrupt edge. (See Example 6 on page 69.)
- ❏ The interrupt flag can be set even though the interrupt is not enabled. Therefore, you must clear the flag register before enabling the interrupts to ensure that a spurious interrupt is not generated. (See Example 5 on page 68.)
- ❏ If interrupts are enabled when GIODIN0 is read, the least significant bits (those bits corresponding to the enabled interrupts) must be masked to avoid ambiguous results. For example, if pins 2:0 are configured as interrupts and pins 7:3 are configured as inputs (V_{IH} applied), then a read of GIODIN0 will read 11111xxx, where the x values are interrupt levels and not inputs. Mask the input register against (in this case) 11111000. (See Example 3, on page 66.)

3 Device Modes of Operation

The GIO module behaves differently in different modes of operation. Three main operating modes are discussed:

- Operating modes
  - Normal (user) mode
  - Privilege modes
- Emulation mode
- Power-down mode

3.1 Operating Modes

Operating modes can be broken down into two subgroups: normal mode and privilege modes.

3.1.1 Normal (User) Mode

Most application programs operate within user mode. The device can enter into normal mode in one of two ways:

- Drive the $\overline{\text{TRANS}}$ signal low.
- Load the binary value 10000 into control bits of the current program status register (CPSR), CPSR.4:0 = 10000b.

3.1.2 Privilege Modes

Privilege modes include the modes in which the device handles interrupts, aborts, and supervisor mode. The device can enter privilege modes in one of two ways:

- Drive the $\overline{\text{TRANS}}$ signal high.
- Load the current program status register control bits accordingly. See *TMS470R1x: 32-Bit RISC Microcontroller Family User's Guide* (SPNU134A) for more details.

3.2 Emulation Mode

Emulation mode is used by debugger tools to stop the CPU at breakpoints in order to read registers. When the device is in emulation mode, it pulls the SUSPEND signal high.

Note: Emulation Mode

Emulation mode is separate from the GIO emulation registers (GIOEMUA and GIOEMUB). Emulation mode is a mode of operation for the device.

During emulation mode:

- ❏ External interrupts are not captured because the CIM is unable to service interrupts.
- ❏ Any register can be read without affecting the state of the system.
- ❏ A write to a register affects the state of the system.

3.3 Power-Down Modes

The GIO module has two power-down modes: module-level power down and device-level power down.

3.3.1 Module-Level Power Down

The GIO module can be placed into a power-down state (GIOPWDN.0 = 1) only in privilege mode. As a safety feature, the peripheral power-down override in the system module must be set (CLKCNTL.7 = 1) as well as the POWERDOWN bit in the GIO module.

In the power-down state, the clock signal to the GIO module is disabled. Thus, there is no switching, and the only current draw comes from leakage current. In low-power mode, interrupt pins become level-sensitive rather than edge-sensitive. The polarity bit changes function from falling edge and rising edge to low and high. A corresponding level on an interrupt pin pulls the module out of low-power mode.

3.3.2 Device-Level Power Down

The entire device can be placed in low-power mode. When the device is switched to a low-power mode (halt or standby), the clocking to all peripheral modules is stopped. In low-power mode, interrupt pins become level-sensitive rather than edge-sensitive, and a corresponding level on an interrupt pin pulls the device out of low-power mode.

4 Pullup/Pulldown Function

GIO module pins can have either an internal active pullup or active pulldown that makes it possible to leave the pins unconnected externally. The pullup/pulldown is deactivated when a bidirectional pin is configured as an output. Please see the specific data sheet for the current supplied by the pullup/pulldown.

5 GIO Control Registers

Table 3 assumes eight ports of eight pins. These registers are accessible in 8-, 16-, and 32-bit reads or writes. Consult the device-specific data sheet to verify the pin configuration.

Table 3. GIO Control Registers †

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x00		GIOPWDN	Reserved															
			Reserved															GIOP-WDN
0x04		GIOENA1	ENA_D								ENA_C							
			ENA_B								ENA_A							
0x08		GIOPOL1	POL_D								POL_C							
			POL_B								POL_A							
0x0C		GIOFLG1	FLG_D								FLG_C							
			FLG_B								FLG_A							
0x10		GIOPRY1	PRY_D								PRY_C							
			PRY_B								PRY_A							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x14		GIOOFFA	Reserved															
			Reserved									GIOOFFA[6:0]						
0x18		GIOEMUA	Reserved															
			Reserved									GIOEMUA[6:0]						
0x1C		GIOOFFB	Reserved															
			Reserved									GIOOFFB[6:0]						
0x20		GIOEMUB	Reserved															
			Reserved									GIOEMUB[6:0]						
0x24		GIODIRx	Reserved															
			Reserved								GIODIRx[7:0]							
0x28		GIODINx	Reserved															
			Reserved								GIODINA[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x2C		GIODOUTx	Reserved															
			Reserved								GIODOUTx[7:0]							
0x30		GIODSETA	Reserved															
			Reserved								GIODSETA[7:0]							
0x34		GIODCLRA	Reserved															
			Reserved								GIODCLRA[7:0]							
0x38		GIODIRB	Reserved															
			Reserved								GIODIRB[7:0]							
0x3C		GIODINB	Reserved															
			Reserved								GIODINB[7:0]							
0x40		GIODOUTB	Reserved															
			Reserved								GIODOUTB[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x44		GIODSETB	Reserved															
			Reserved								GIODSETB[7:0]							
0x48		GIODCLRB	Reserved															
			Reserved								GIODCLRB[7:0]							
0x4C		GIODIRC	Reserved															
			Reserved								GIODIRC[7:0]							
0x50		GIODINC	Reserved															
			Reserved								GIODINC[7:0]							
0x54		GIODOUTC	Reserved															
			Reserved								GIODOUTC[7:0]							
0x58		GIODSETC	Reserved															
			Reserved								GIODSETC[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x5C		GIODCLRC	Reserved															
			Reserved								GIODCLRC[7:0]							
0x60		GIODIRD	Reserved															
			Reserved								GIODIRD[7:0]							
0x64		GIODIND	Reserved															
			Reserved								GIODIND[7:0]							
0x68		GIODOUTD	Reserved															
			Reserved								GIODOUTD[7:0]							
0x6C		GIODSETD	Reserved															
			Reserved								GIODSETD[7:0]							
0x70		GIODCLRD	Reserved															
			Reserved								GIODCLRD[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x74		GIODIRE	Reserved															
			Reserved								GIODIRE[7:0]							
0x78		GIODINE	Reserved															
			Reserved								GIODINE[7:0]							
0x7C		GIODOUTE	Reserved															
			Reserved								GIODOUTE[7:0]							
0x80		GIODSETE	Reserved															
			Reserved								GIODSETE[7:0]							
0x84		GIODCLRE	Reserved															
			Reserved								GIODCLRE[7:0]							
0x88		GIODIRF	Reserved															
			Reserved								GIODIRF[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0x8C	GIODINF	Reserved															
		Reserved								GIODINF[7:0]							
0x90	GIODOUTF	Reserved															
		Reserved								GIODOUTF[7:0]							
0x94	GIODSETF	Reserved															
		Reserved								GIODSETF[7:0]							
0x98	GIODCLRF	Reserved															
		Reserved								GIODCLRF[7:0]							
0x9C	GIODIRG	Reserved															
		Reserved								GIODIRG[7:0]							
0xA0	GIODING	Reserved															
		Reserved								GIODING[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0xA4		GIODOUTG	Reserved															
			Reserved								GIODOUTG[7:0]							
0xA8		GIODSETG	Reserved															
			Reserved								GIODSETG[7:0]							
0xAC		GIODCLRG	Reserved															
			Reserved								GIODCLRG[7:0]							
0xB0		GIODIRH	Reserved															
			Reserved								GIODIRH[7:0]							
0xB4		GIODINH	Reserved															
			Reserved								GIODINH[7:0]							
0xB8		GIODOUTH	Reserved															
			Reserved								GIODOUTH[7:0]							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

Table 3. GIO Control Registers (Continued)†

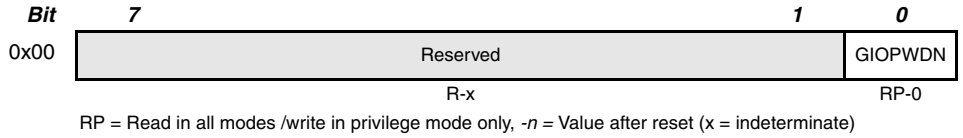
Offset	Address	Register	31 15	30 14	29 13	28 12	27 11	26 10	25 9	24 8	23 7	22 6	21 5	20 4	19 3	18 2	17 1	16 0
0xBC		GIODSETH	Reserved															
			Reserved								GIODSETH[7:0]							
0xC0		GIODCLRH	Reserved															
			Reserved								GIODCLRH[7:0]							
0xC4		GIOENA2	ENA_H								ENA_G							
			ENA_F								ENA_E							
0xC8		GIOPOL2	POL_H								POL_G							
			POL_F								POL_E							
0xCC		GIOFLG2	FLG_H								FLG_G							
			FLG_F								FLG_E							
0xD0		GIOPRY2	PRY_H								PRY_G							
			PRY_F								PRY_E							

† The physical address is device-specific. If the base address of the GIO starts at 0xFF7EC00, then GIOENA1 is located at 0xFFF7EC04.

5.1 GIO Power Down Register (GIOPWDN)

The GIOPWDN register contains one bit that controls the module power-down status. In power-down mode, GIO internal clocks are stopped, which leaves the module in a static state where it consumes the lowest possible current. Figure 12 and Table 4 describe this register.

Figure 12. GIO Power Down Register (GIOPWDN)



RP = Read in all modes /write in privilege mode only, *-n* = Value after reset (x = indeterminate)

Table 4. GIO Power Down Register 2 (GIOPWDN) Field Descriptions

Bit	Name	Value	Description
7–1	Reserved		Read values are indeterminate, and write values have no effect.
0	GIOPWDN		GIO power down Writing to the GIOPWDN bit is only allowed in privilege mode. Reading of the GIOPWDN bit is allowed in all modes.
			Privilege mode (write):
		0	Normal operation proceeds; clocks are enabled to GIO module.
		1	Power-down mode is in effect.
			User mode (write):
			Writes have no effect in user mode.
			User or privilege mode (read):
		0	Normal operation proceeds; clocks are enabled to GIO module.
		1	Power-down mode is used.
			Note: The clock control register (CLKCNTL) in the system module contains a peripheral power-down override bit (CLKCNTL.7 = 1) that must be set before the GIOPWDN bit will have any effect.

5.2 GIO Interrupt Enable 1 (GIOENA1)

The GIOENA1 register controls which interrupt-capable pins in ports A, B, C, and D are configured as interrupts. Figure 13 and Table 5 describe this register.

Figure 13. GIO Interrupt Enable 1 Register 2 (GIOENA1)

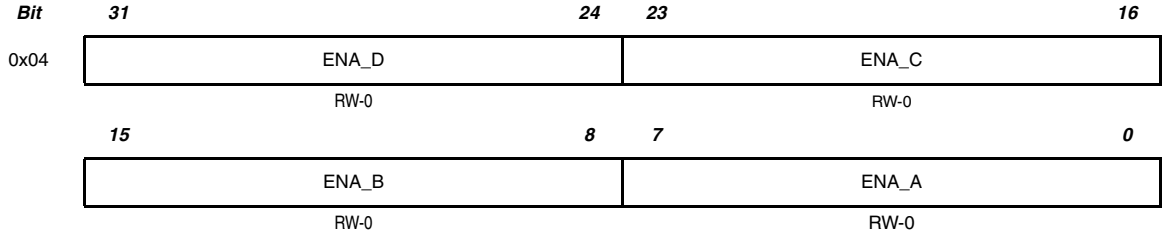


Table 5. GIO Interrupt Enable 1 Register 2 (GIOENA1) Field Descriptions

Bit	Name	Value	Description
31–24	ENA1_D		Interrupt enable 1 for port D
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two B must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.

Table 5. GIO Interrupt Enable 1 Register 2 (GIOENA1) Field Descriptions (Continued)

Bit	Name	Value	Description
23–16	ENA1_C		Interrupt enable 1 for port C
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.
15–8	ENA1_B		Interrupt enable 1 for port B
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.
7–0	ENA1_A		Interrupt enable 1 for port A
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.

5.3 GIO Interrupt Polarity 1 Register (GIOPOL1)

The GIOPOL1 register controls the polarity—rising edge (low to high) or falling edge (high to low)—that sets the flag for ports A, B, C, and D. To ensure recognition of the signal as an edge, the signal must maintain the new level for at least one ICLK cycle. Figure 14 and Table 6 describe this register.

Figure 14. GIO Interrupt Polarity 1 Register 2 (GIOPOL1)

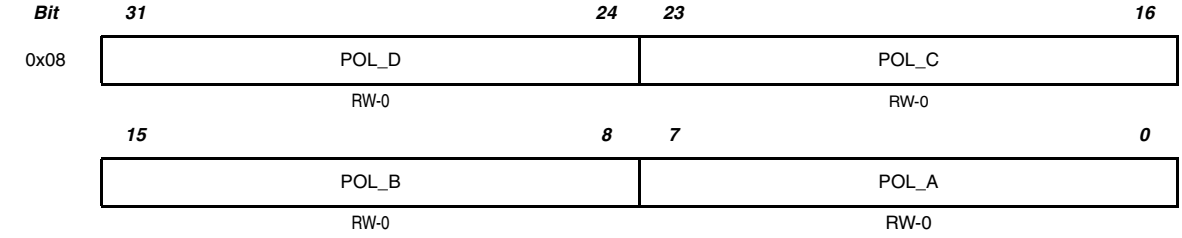


Table 6. GIO Interrupt Polarity 1 Register 2 (GIOPOL1) Field Descriptions

Bit	Name	Value	Description
31–24	POL_D		Interrupt enable 1 for port D
			User or privilege mode (read/write):
		0	Flag sets on falling edge on the corresponding pin.
		1	Flag sets on rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on the low level.
		1	The interrupt is triggered on the high level.
23–16	POL_C		Interrupt enable 1 for port C
			User or privilege mode (read/write):
		0	Flag sets on falling edge on the corresponding pin.
		1	Flag sets on rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on the low level.
		1	The interrupt is triggered on the high level.

Table 6. GIO Interrupt Polarity 1 Register 2 (GIOPOL1) Field Descriptions (Continued)

Bit	Name	Value	Description
15–8	POL_B		Interrupt enable 1 for port B
			User or privilege mode (read/write):
		0	Flag sets on falling edge on the corresponding pin.
		1	Flag sets on rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on the low level.
		1	The interrupt is triggered on the high level.
7–0	POL_A		Interrupt enable 1 for port A
			User or privilege mode (read/write):
		0	Flag sets on falling edge on the corresponding pin.
		1	Flag sets on rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on the low level.
		1	The interrupt is triggered on the high level.

5.4 GIO Interrupt Flag 1 Register (GIOFLG1)

The GIOFLG1 register contains flags indicating that the transition edge (type set in GIOPOL1) has occurred for ports A, B, C, and D. The flag is also cleared by reading the appropriate offset register. See Section 2.4.3 on page 12.

Figure 15 and Table 7 describe this register.

Figure 15. GIO Interrupt Flag 1 Register (GIOFLG1)

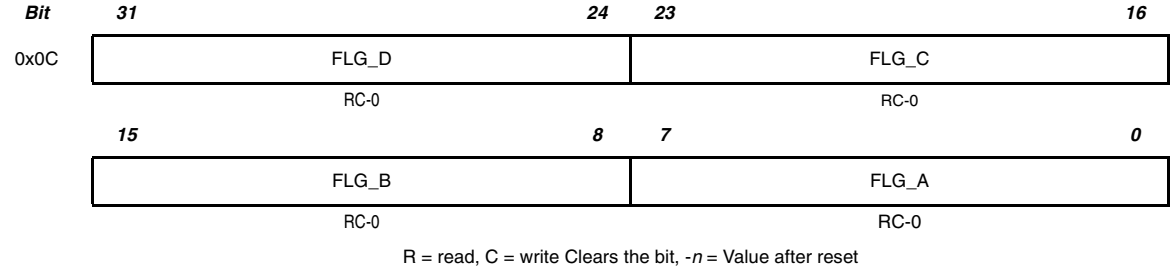


Table 7. GIO Interrupt Flag 1 Register (GIOFLG1)

Bit	Name	Value	Description
31–24	FLG_D		GIO flag 1 for port D When the GIOFLG1_D bit is set to 1, the selected transition on the corresponding pin of port D has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No change has occurred in the flag register.
		1	The corresponding bit clears to 0.

Table 7. GIO Interrupt Flag 1 Register (GIOFLG1) (Continued)

Bit	Name	Value	Description
23–16	FLG_C		GIO flag 1 for port C When the GIOFLG1_D bit is set to 1, the selected transition on the corresponding pin of port C has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No change has occurred in the flag register.
		1	The corresponding bit clears to 0.
15–8	FLG_B		GIO flag 1 for port B When the GIOFLG1_B bit is set to 1, the selected transition on the corresponding pin of port B has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No change has occurred in the flag register.
		1	The corresponding bit clears to 0.
7–0	FLG_A		GIO flag 1 for port A When the GIOFLG1_A bit is set to 1, the selected transition on the corresponding pin of port A has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No change has occurred in the flag register.
		1	The corresponding bit clears to 0.

5.5 GIO Interrupt Priority 1 (GIOPRY1)

The GIOPRY1 register configures the interrupts as high priority (A) or low priority (B) for ports A, B, C, and D. Each interrupt can be individually configured as high priority or low priority.

- ❏ The high-priority interrupts are recorded to GIOOFFA and GIOEMUA.
- ❏ The low-priority interrupts are recorded to GIOOFFB and GIOEMUB.

Figure 16 and Table 8 describe this register.

Figure 16. GIO Interrupt Priority 1 Register (GIOPRY1)

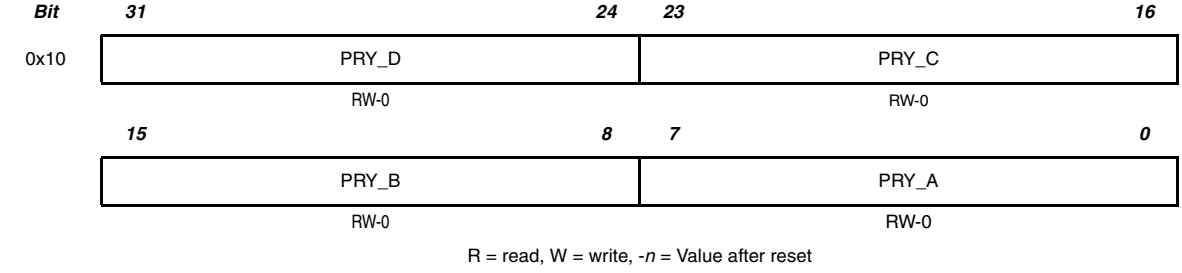


Table 8. GIO Interrupt Priority 1 Register (GIOPRY1) Field Descriptions

Bit	Name	Value	Description
31–24	PRY_D		GIO priority 1 for port D
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority.
23–16	PRY_C		GIO priority 1 for port C
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority.

Table 8. GIO Interrupt Priority 1 Register (GIOPRY1) Field Descriptions (Continued)

Bit	Name	Value	Description
15–8	PRY_B		GIO priority 1 for port B
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority.
7–0	PRY_A		GIO priority 1 for port A
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority.

5.6 GIO Offset A (GIOOFFA)

The GIOOFFA register provides a numerical offset value that represents the pending external interrupt with high priority, as shown in Table 2, on page 13. The offset value can be used to locate the position of the interrupt routine in a vector table. Reading this register clears it and the corresponding flag bit in the GIOFLG register. However, in emulation mode, a read to this register does not clear the corresponding flag bit.

Figure 17 and Table 9 describe this register.

Figure 17. GIO Offset A Register (GIOOFFA)

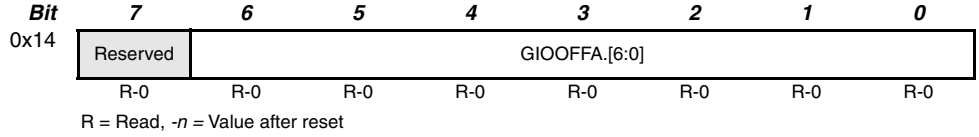


Table 9. GIO Offset A Register (GIOOFFA) Field Descriptions

Bit	Name	Value	Description
7	Reserved		Always reads 0. Writes to this bit have no effect.
6–0	GIOOFFA.[6:0]		GIO offset A GIOOFFA.6:0 index the currently pending high-priority interrupt. Bit values and the interrupts are listed in Table 2. Any mode (write): Writes to these bits have no effect. User or privilege mode (read): A read of these bits determines the pending external interrupt; this register and the flag bit (in the GIOFLG register) are also cleared. Emulation mode (read): A read of these bits determines the pending external interrupt, but the corresponding flag bit is not cleared.

5.7 GIO Emulation A (GIOEMUA)

The GIOEMUA register, a read-only register, is provided for use by the debug monitor in normal operation. The contents of this register are identical to the contents of GIOOFFA. The corresponding flag in the GIOFLGx register is not cleared when the GIOEMUA register is read. Figure 18 and Table 10 describe this register.

Figure 18. GIO Emulation A Register (GIOEMUA)

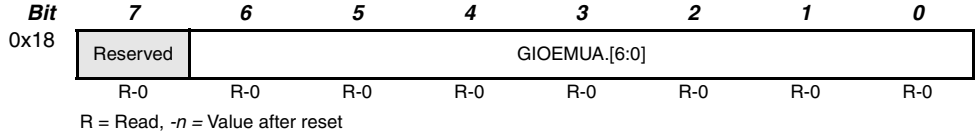


Table 10. GIO Emulation A Register (GIOEMUA) Field Descriptions

Bit	Name	Value	Description
7	Reserved		Always reads 0. Writes to this bit have no effect.
6–0	GIOEMUA.[6:0]		GIO Emulation A GIOEMUA.6:0 index the currently pending high-priority interrupt. Bit values and the interrupts are listed in Table 2. Any mode (write): Writes to these bits have no effect. User or privilege mode (read): A read of these bits determines the pending external interrupt.

5.8 GIO Offset B (GIOOFFB)

The GIOOFFB register provides a numerical offset value that represents the pending external interrupt with low priority, as shown in Table 2. The offset value can be used to locate the position of the interrupt routine in a vector table. Reading this register clears it and the corresponding flag bit in the GIOFLG register. However, in emulation mode, a read to this register does not clear the corresponding flag bit. Figure 19 and Table 11 describe this register.

Figure 19. GIO Offset B Register (GIOOFFB)

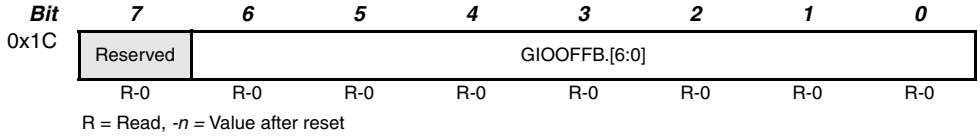


Table 11. GIO Offset B Register (GIOOFFB) Field Descriptions

Bit	Name	Value	Description
7	Reserved		Always reads 0. Writes to this bit have no effect.
6–0	GIOOFFB.[6:0]		GIO offset B GIOOFFB.6:0 index the currently pending high-priority interrupt. Bit values and the interrupts are listed in Table 2. Any mode (write): Writes to these bits have no effect. User or privilege mode (read): A read of these bits determines the pending external interrupt; this register and the flag bit (in the GIOFLG register) are also cleared. Emulation mode (read): A read of these bits determines the pending external interrupt, but the corresponding flag bit is not cleared.

5.9 GIO Emulation B (GIOEMUB)

The GIOEMUB register, a read-only register, address is provided for use by the debug monitor in normal operation. The contents of this register are identical to the contents of GIOOFFB. The corresponding flag in the GIOFLGx register is not cleared when the GIOEMUB register is read. Figure 20 and Table 12 describe this register.

Figure 20. GIO Emulation B Register (GIOEMUB)

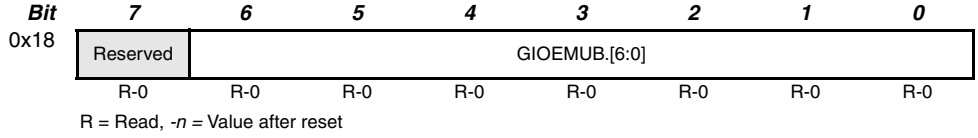


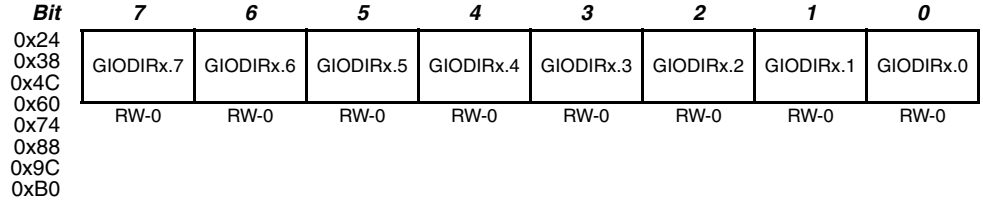
Table 12. GIO Emulation B Register (GIOEMUB) Field Descriptions

Bit	Name	Value	Description
7	Reserved		Always reads 0. Writes to this bit have no effect.
6–0	GIOEMUB.[6:0]		GIO Emulation B GIOEMUB.6:0 index the currently pending high-priority interrupt. Bit values and the interrupts are listed in Table 2. Any mode (write): Writes to these bits have no effect. User or privilege mode (read): A read of these bits determines the pending external interrupt.

5.10 GIO Data Direction Registers (GIODIRx)

The eight GIODIRx registers control whether the pins of ports A–H are configured as inputs or outputs. Figure 21 and Table 13 describe these registers.

Figure 21. GIO Data Direction Registers (GIODIRx)



R = Read, Write = Write, *-n* = Value after reset

Table 13. GIO Data Direction Registers (GIODIRx) Field Descriptions

Bit	Name	Value	Description
7	GIODIRx.7		GIO data direction for port [H:A], pin 7
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
6	GIODIRx.6		GIO data direction for port[H:A], pin 6
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
5	GIODIRx.5		GIO data direction for port [H:A], pin 5
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.

Table 13. GIO Data Direction Registers (GIODIRx) Field Descriptions (Continued)

Bit	Name	Value	Description
4	GIODIRx.4		GIO data direction for port[H:A], pin 4
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
3	GIODIRx.3		GIO data direction for port[H:A], pin 3
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
2	GIODIRx.2		GIO data direction for port[H:A], pin 2
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
1	GIODIRx.1		GIO data direction for port[H:A], pin 1
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
0	GIODIRx.0		GIO data direction for port[H:A], pin 0
			User or privilege mode (read/write):
		0	Output buffer is disabled.
		1	Output buffer is enabled.
			Note: Pin 0 of Port A is not output-capable. For some devices, the GIODIRA.0 bit is frozen to 0, making pin 0 of port A an input with external interrupt capability. Please consult the device specification for more details.

5.11 GIO Data Input Registers (GIODINx)

Values in the eight GIODINx registers reflect the current state (high = 1 or low = 0) of the logic on the pins of ports A–H. Figure 22 and Table 14 describe these registers.

Figure 22. GIO Data Input Register (GIODINx)

Bit	7	6	5	4	3	2	1	0
0x28 0x3C 0x50 0x64 0x78 0x8C 0xA0 0xB4	GIODINx.7	GIODINx.6	GIODINx.5	GIODINx.4	GIODINx.3	GIODINx.2	GIODINx.1	GIODINx.0
	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

R = Read, -*n* = Value after reset (x = indeterminate)

Table 14. GIO Data Input Registers (GIODINx) Field Descriptions

Bit	Name	Value	Description
7	GIODINx.7		GIO data input for port[H:A], pin 7
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.
6	GIODINx.6		GIO data input for port[H:A], pin 6
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.

Table 14. GIO Data Input Registers (GIODINx) Field Descriptions (Continued)

Bit	Name	Value	Description
5	GIODINx.5		GIO data input for port[H:A], pin 5
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.
4	GIODINx.4		GIO data input for port[H:A], pin 4
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.
3	GIODINx.3		GIO data input for port[H:A], pin 3
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.
2	GIODINx.2		GIO data input for port[H:A], pin 2
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.

Table 14. GIO Data Input Registers (GIODINx) Field Descriptions (Continued)

Bit	Name	Value	Description
1	GIODINx.1		GIO data input for port[H:A], pin 1
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.
0	GIODINx.0		GIO data input for port[H:A], pin 0
			User or privilege mode (read):
		0	The logic is low (input voltage is V_{IL} or lower).
		1	The logic is high (input voltage is V_{IH} or higher).
			User or privilege mode (write): Writes to these bits have no effect.

5.12 GIO Data Output Registers (GIODOUTx)

Values in the GIODOUTx register specify the output state (high = 1 or low = 0) of the pins if the pins are configured as outputs. Figure 23 and Table 15 describe these registers.

Figure 23. GIO Data Output Registers (GIODOUTx)

Bit	7	6	5	4	3	2	1	0
0x2C 0x40 0x54 0x68 0x7C 0x90 0xA4 0xB8	GIOD-OUTx.7	GIOD-OUTx.6	GIOD-OUTx.5	GIOD-OUTx.4	GIOD-OUTx.3	GIOD-OUTx.2	GIOD-OUTx.1	GIOD-OUTx.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = Read, W = Write, *-n* = Value after reset

Table 15. GIO Data Output Registers (GIODOUTx) Field Descriptions

Bit	Name	Value	Description
7	GIODOUTx.7		GIO data output for port[H:A], pin 7
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).
6	GIODOUTx.6		GIO data output for port[H:A], pin 6
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).
5	GIODOUTx.5		GIO data output for port[H:A], pin 5
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).

Table 15. GIO Data Output Registers (GIODOUTx) Field Descriptions (Continued)

Bit	Name	Value	Description
4	GIODOUTx.4		GIO data output for port[H:A], pin 4
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).
3	GIODOUTx.3		GIO data output for port[H:A], pin 3
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).
2	GIODOUTx.2		GIO data output for port[H:A], pin 2
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	1 = Logic is high (output voltage is V_{OH} or higher).
1	GIODOUTx.1		GIO data output for port[H:A], pin 1
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).
0	GIODOUTx.0		GIO data output for port[H:A], pin 0
			User or privilege mode (read/write):
		0	Logic is low (output voltage is V_{OL} or lower).
		1	Logic is high (output voltage is V_{OH} or higher).
			Note: Pin 0 of port A is not output-capable. For some devices, the GIODOUTA.0 bit is reserved. Writes to pin 0 of port A are ignored. Please consult the device specification for more details.

5.13 GIO Data Set Registers (GIODSETx)

Values in the eight GIODSETx registers set the data output control register bits for ports A–H to 1 regardless of the current value in the GIODOUTx bits. Figure 24 and Table 16 describe these registers.

Figure 24. GIO Data Set Registers (GIODSETx)

Bit	7	6	5	4	3	2	1	0
0x30 0x44 0x58 0x6C 0x80 0x9F 0xA8 0xBC	GIOD-SETx.7	GIOD-SETx.6	GIOD-SETx.5	GIOD-SETx.4	GIOD-SETx.3	GIOD-SETx.2	GIOD-SETx.1	GIOD-SETx.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = Read, W = Write, *-n* = Value after reset

Table 16. GIO Data Set Registers (GIODSETx) Field Descriptions

Bit	Name	Value	Description
7	GIODSETx.7		GIO data set for port[H:A], pin 7
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.7 is unchanged.
		1	Bit GIODOUTx.7 is set to 1.
6	GIODSETx.6		GIO data set for port[H:A], pin 6
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.6 is unchanged.
		1	Bit GIODOUTx.6 is set to 1.

Table 16. GIO Data Set Registers (GIODSETx) Field Descriptions (Continued)

Bit	Name	Value	Description
5	GIODSETx.5		GIO data set for port[H:A], pin 5
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.5 is unchanged.
		1	Bit GIODOUTx.5 is set to 1.
4	GIODSETx.4		GIO data set for port[H:A], pin 4
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.4 is unchanged.
		1	Bit GIODOUTx.4 is set to 1.
3	GIODSETx.3		GIO data set for port[H:A], pin 3
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.3 is unchanged.
		1	Bit GIODOUTx.3 is set to 1.

Table 16. GIO Data Set Registers (GIODSETx) Field Descriptions (Continued)

Bit	Name	Value	Description
2	GIODSETx.2		GIO data set for port[H:A], pin 2
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.2 is unchanged.
		1	Bit GIODOUTx.2 is set to 1.
1	GIODSETx.1		GIO data set for port[H:A], pin 1
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.1 is unchanged.
		1	Bit GIODOUTx.1 is set to 1.
0	GIODSETx.0		GIO data set for port[H:A], pin 0
			User or privilege mode (read): GIODSETx reflects the contents of GIOOUTx.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.0 is unchanged.
		1	Bit GIODOUTx.0 is set to 1.

5.14 GIO Data Clear Registers (GIODCLRx)

Values in the eight GIODCLRx registers clear the data output register bit for ports A–H to 0 regardless of its current value. Figure 25 and Table 17 describe these registers.

Figure 25. GIO Data Clear Registers (GIODCLRx)

Bit	7	6	5	4	3	2	1	0
0x34 0x48 0x5C 0x70 0x84 0x98 0xAC 0xC0	GIOD-CLRx.7	GIOD-CLRx.6	GIOD-CLRx.5	GIOD-CLRx.4	GIOD-CLRx.3	GIOD-CLRx.2	GIOD-CLRx.1	GIOD-CLRx.0
	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

R = Read W = Write, *-n* = Value after reset

Table 17. GIO Data Clear Registers (GIODCLRx) Field Descriptions

Bit	Name	Value	Description
7	GIODCLRx.7		GIO data clear for port[H:A], pin 7
			User or privilege mode (read): GIODCLRx.7 reflects the contents of GIOOUTx.7.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.7 remains unchanged.
		1	Bit GIODOUTx.7 is cleared to 0.

Table 17. GIO Data Clear Registers (GIODCLRx) Field Descriptions (Continued)

Bit	Name	Value	Description
6	GIODCLRx.6		GIO data clear for port[H:A], pin 6
			User or privilege mode (read): GIODCLRx.6 reflects the contents of GIOOUTx.6.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.6 remains unchanged.
		1	Bit GIODOUTx.6 is cleared to 0.
5	GIODCLRx.5		GIO data clear for port[H:A], pin 5
			User or privilege mode (read): GIODCLRx.5 reflects the contents of GIOOUTx.5.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.5 remains unchanged.
		1	Bit GIODOUTx.5 is cleared to 0.
4	GIODCLRx.4		GIO data clear for port[H:A], pin 4
			User or privilege mode (read): GIODCLRx.4 reflects the contents of GIOOUTx.4.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.4 remains unchanged.
		1	Bit GIODOUTx.4 is cleared to 0.

Table 17. GIO Data Clear Registers (GIODCLRx) Field Descriptions (Continued)

Bit	Name	Value	Description
3	GIODCLRx.3		GIO data clear for port[H:A], pin 3
			User or privilege mode (read): GIODCLRx.3 reflects the contents of GIOOUTx.3.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.3 remains unchanged.
		1	Bit GIODOUTx.3 is cleared to 0.
2	GIODCLRx.2		GIO data clear for port[H:A], pin 2
			User or privilege mode (read): GIODCLRx.2 reflects the contents of GIOOUTx.2.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.2 remains unchanged.
		1	Bit GIODOUTx.2 is cleared to 0.
1	GIODCLRx.1		GIO data clear for port[H:A], pin 1
			User or privilege mode (read): GIODCLRx.1 reflects the contents of GIOOUTx.1.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.1 remains unchanged.
		1	Bit GIODOUTx.1 is cleared to 0.

Table 17. GIO Data Clear Registers (GIODCLRx) Field Descriptions (Continued)

Bit	Name	Value	Description
0	GIODCLRx.0		GIO data clear for port[H:A], pin 0
			User or privilege mode (read): GIODCLRx.0 reflects the contents of GIOOUTx.0.
		0	The logic is low (output voltage is V_{OL} or lower).
		1	The logic is high (output voltage is V_{OH} or higher).
			User or privilege mode (write):
		0	Bit GIODOUTx.0 remains unchanged.
		1	Bit GIODOUTx.0 is cleared to 0.

5.15 GIO Interrupt Enable 2 Register (GIOENA2)

The GIOENA2 register controls which interrupt-capable pins in ports E, F, G, and H are configured as interrupts. Figure 26 and Table 18 describe this register.

Figure 26. GIO Interrupt Enable 2 Register (GIOENA2)

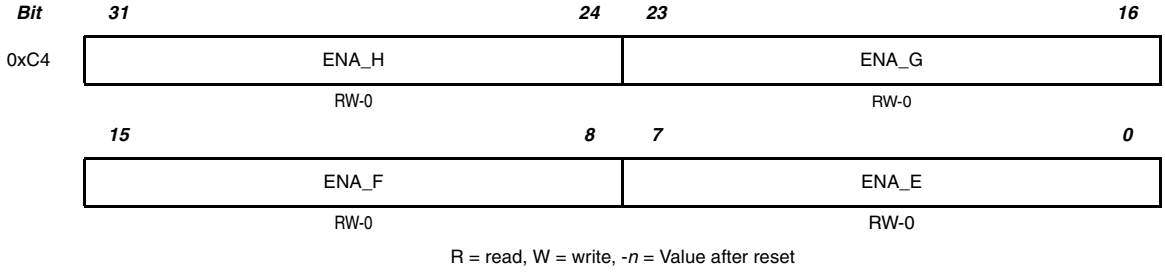


Table 18. GIO Interrupt Enable 2 Register (GIOENA2) Field Descriptions

Bit	Name	Value	Description
31–24	ENA_H		Interrupt enable 2 for port H
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.

Table 18. GIO Interrupt Enable 2 Register (GIOENA2) Field Descriptions (Continued)

Bit	Name	Value	Description
23–16	ENA_G		Interrupt enable 2 for port G
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.
15–8	ENA_F		Interrupt enable 2 for port E
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.
7–0	ENA_E		Interrupt enable 2 for port H
			User or privilege mode (read/write):
		0	The interrupt is disabled; the pin acts like an I/O pin.
		1	The interrupt is enabled.
			Note: Two bits must be set within the CIM (central interrupt manager) in the interrupt mask register (REQMASK). The REQMASK register must be configured to enable the appropriate interrupts. Additionally, the CPU must be configured to recognize interrupt requests.

5.16 GIO Interrupt Polarity 2 Register (GIOPOL2)

The GIOPOL2 register controls the polarity—rising edge (low to high) or falling edge (high to low)—that sets the flag, for ports E, F, G, and H. To ensure recognition of the signal as an edge, the signal must maintain the new level for at least one ICLK cycle.

Figure 27 and Table 19 describe this register.

Figure 27. GIO Interrupt Polarity Register (GIOPOL2)

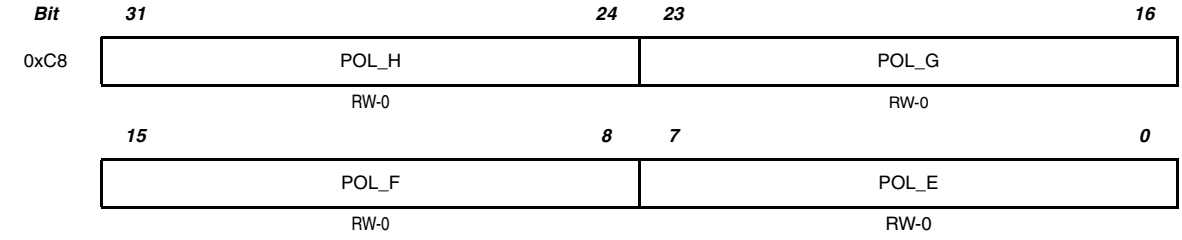


Table 19. GIO Interrupt Polarity Register (GIOPOL2) Field Descriptions

Bit	Name	Value	Description
31–24	POL_H		Interrupt polarity select 2 for port H
			User or privilege mode (read/write):
		0	The flag sets on the falling edge on the corresponding pin.
		1	The flag sets on the rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on low level.
		1	The interrupt is triggered on high level.

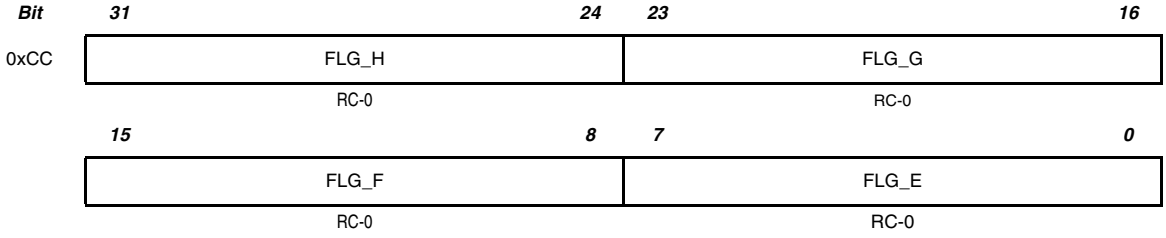
Table 19. GIO Interrupt Polarity Register (GIOPOL2) Field Descriptions (Continued)

Bit	Name	Value	Description
23–16	POL_G		Interrupt polarity select 2 for port G
			User or privilege mode (read/write):
		0	The flag sets on the falling edge on the corresponding pin.
		1	The flag sets on the rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on low level.
		1	The interrupt is triggered on high level.
15–8	POL_F		Interrupt polarity select 2 for port F
			User or privilege mode (read/write):
		0	The flag sets on the falling edge on the corresponding pin.
		1	The flag sets on the rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on low level.
		1	The interrupt is triggered on high level.
7–0	POL_E		Interrupt polarity select 2 for port E
			User or privilege mode (read/write):
		0	The flag sets on the falling edge on the corresponding pin.
		1	The flag sets on the rising edge on the corresponding pin.
			Low-power mode (halt or standby):
		0	The interrupt is triggered on low level.
		1	The interrupt is triggered on high level.

5.17 GIO Interrupt Flag 2 Register (GIOFLG2)

The GIOFLG2 register contains flags indicating that the transition edge (type set in GIOPOL2) has occurred for ports E, F, G, and H. The flag is also cleared by reading the appropriate offset register. See Section 2.4.3 on page 12. Figure 28 and Table 20 describe this register.

Figure 28. GIO Interrupt Flag 2 Register (GIOFLG2)



R = read, C = write Clears the bit, -*n* = Value after reset

Table 20. GIO Interrupt Flag 2 Register (GIOFLG2) Field Descriptions

Bit	Name	Value	Description
31–24	FLG_H		GIO flag 2 for port H When the GIOFLG2 bit is set to 1, the selected transition on the corresponding pin of port H has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No changes have occurred in the flag register.
		1	The corresponding bit is cleared to 0.

Table 20. GIO Interrupt Flag 2 Register (GIOFLG2) Field Descriptions (Continued)

Bit	Name	Value	Description
23–16	FLG_G		GIO flag 2 for port G When the GIOFLG2 bit is set to 1, the selected transition on the corresponding pin of port G has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No changes have occurred in the flag register.
		1	The corresponding bit is cleared to 0.
15–8	FLG_F		GIO flag 2 for port F When the GIOFLG2 bit is set to 1, the selected transition on the corresponding pin of port F has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No changes have occurred in the flag register.
		1	The corresponding bit is cleared to 0.
7–0	FLG_E		GIO flag 2 for port E When the GIOFLG2 bit is set to 1, the selected transition on the corresponding pin of port E has occurred.
			User or privilege mode (read):
		0	Transition has not occurred since the last clear.
		1	Transition has occurred since the last clear.
			User or privilege mode (write):
		0	No changes have occurred in the flag register.
		1	The corresponding bit is cleared to 0.

5.18 GIO Interrupt Priority 2 (GIOPRY2)

The GIOPRY2 register configures the interrupts as high priority (1) or low priority (0) for ports E, F, G, and H. Each interrupt can be individually configured as high priority or low priority.

- ❏ The high-priority interrupts are recorded to GIOOFFA and GIOEMUA.
- ❏ The low-priority interrupts are recorded to GIOOFFB and GIOEMUB.

Figure 29 and Table 21 describe this register.

Figure 29. GIO Interrupt Priority 2 Register (GIOPRY2)

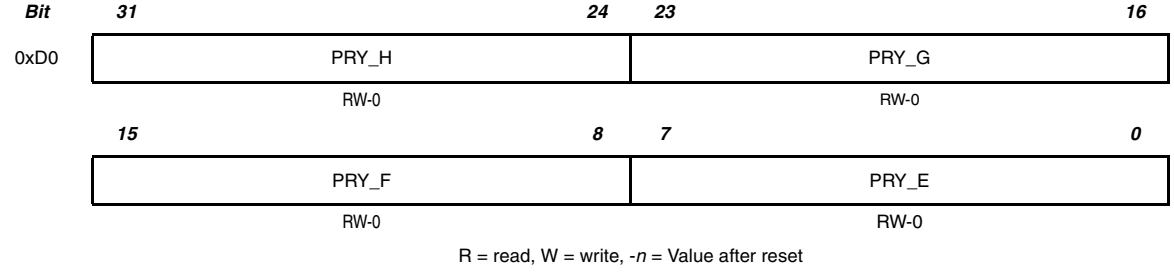


Table 21. GIO Interrupt Priority 2 Register (GIOPRY2) Field Descriptions

Bit	Name	Value	Description
31–24	PRY_H		GIO priority 2 for port H
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority
23–16	PRY_G		GIO priority 2 for port G
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority

Table 21. GIO Interrupt Priority 2 Register (GIOPRY2) Field Descriptions (Continued)

Bit	Name	Value	Description
15–8	PRY_F		GIO priority 2 for port F
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority
7–0	PRY_E		GIO priority 2 for port E
			User or privilege mode (read/write):
		0	The interrupt is low priority.
		1	The interrupt is high priority

6 Applications

The application examples in this section assume a typical configuration of five I/O functional ports. Port A has three external interrupt-capable pins, 2-0. Table 22 illustrates the GIO register.

Table 22. Example GIO Register Showing Reserved Bits

Register	Address	7	6	5	4	3	2	1	0
GIOPWDN	0x00								
GIOENA1	0x04								
GIOPOL1	0x08								
GIOFLG1	0x0C								
GIOPRY1	0x10								
GIOOFFA	0x14								
GIOEMUA	0x18								
GIOOFFB	0x1C								
GIOEMUB	0x20								
GIODIRA	0x24								
GIODINA	0x28								
GIODOUTA	0x2C								
GIODSETA	0x30								
GIODCLRA	0x34								
GIODIRB	0x38								
GIODINB	0x3C								
GIODOUTB	0x40								
GIODSETB	0x44								
GIODCLRB	0x48								
GIODIRC	0x4C								
GIODINC	0x50								
GIODOUTC	0x54								
GIODSETC	0x58								
GIODCLRC	0x5C								
GIODIRD	0x60								
GIODIND	0x64								
GIODOUTD	0x68								
GIODSETD	0x6C								
GIODCLRD	0x70								
GIODIRE	0x74								
GIODINE	0x78								
GIODOUTE	0x7C								
GIODSETE	0x80								
GIODCLRE	0x84								

Note: The shaded area indicates bits that are reserved for use with Example 3, Example 4, Example 5, and Example 6.

The code in Example 3 demonstrates how to set the interrupts. In the example, two of the interrupts are enabled, and the third pin of port A is configured for output. R2 keeps the same value, and the other registers act as temporary storage for addresses and values.

Example 3. Setting Interrupts and Configuring Pins for Output

```
GIO_LOC     .word 0xFFF7EC00          ;device specific address for the GIO registers.
GIOENA .equ    0x04                   ;setting up equate statements
GIOPOL .equ    0x08
GIOFLG .equ    0x0C
GIOPRY .equ    0x10
GIOOFFA .equ    0x14
GIOEMUA .equ    0x18
GIOOFFB .equ    0x1C
GIOEMUB .equ    0x20
GIODIRA .equ    0x24
GIODINA .equ    0x28
GIODOUTA .equ    0x2C
GIODSETA .equ    0x30
GIODCLRA .equ    0x34
    LDR R2, GIO_LOC                   ;loads GIO base address into register 2.
                                      ; **SET THE POLARITY OF THE INTERRUPTS.**
    MOV R3, #GIOPOL                   ; loads GIOPOL offset address into register 3.
    MOV R4, #0x02                     ; loads a value of 0x02 into register 4.
                                      ; Sets bit 1.
    STR R4, [R2, R3]                  ; sets interrupt 0 to trigger on falling edge
                                      ; and interrupt 1 to trigger on rising edge.
                                      ; **SET THE PRIORITY ON BOTH INTERRUPTS AS LOW**
    MOV R3, #GIOPRY                   ; loads the GIOPRY address into register 3.
    MOV R4, #0x00                     ; loads a value of 0 into register 4.
    STR R4, [R2, R3]                  ; priority on interrupts 0 and 1 is set LOW.
                                      ; ** SET PORT A FOR OUTPUT (EXCEPT FOR INTERRUPTS
                                      ; WHICH MUST BE CONFIGURED AS INPUTS)**
    MOV R3, #GIODIRA                  ; loads GIODIRA offset address into register 3.
    MOV R4, #0xFC                     ; loads a binary value of 11111100
    STR R4, [R2, R3]                  ; sets pins 0 and 1 as input to insure proper
                                      ; interrupt behavior pin 2 configured as
                                      ; output
    MOV R3, #GIOFLG                   ; loads GIOFLG offset address into register 3.
    MOV R4, #0xFF                     ; sets 32 bits.
    STR R4, [R2, R3]                  ; clears all bits of the flag register.
                                      ; **ENABLE THE FIRST TWO INTERRUPTS 1:0.**
    MOV R3, #GIOENA                   ; loads GIOENA offset address into register 3.
    MOV R4, #0x03                     ; sets first 2 bits 1:0
    STR R4, [R2, R3]                  ; enables the first two interrupts
```

The code in Example 4 demonstrates how to toggle the output buffer port B using the GIODSET and GIODCLR buffers.

Example 4. Toggling Output Buffers

```
GIO_LOC .word 0xFFF7EC00          ; device specific address for the GIO registers.
GIOENA .equ    0x04               ;setting up equate statements
...
GIODIRB .equ 0x38
GIODINB .equ 0x3C
GIODOUTB.equ 0x40
GIODSETB.equ 0x44
GIODCLRB .equ 0x48
   LDR R2, GIO_LOC                ; loads absolute address of the GIO memory
                                  ; location (device specific).
                                  ; **SET ALL BITS IN GIODOUTB AS 1.**
   MOV R3, #GIODSETB              ; loads offset address of GIODSETB
   MOV R4, #0xFF                  ; loads a binary value of 11111111
   STR R4, [R2, R3]               ; sets all bits of GIODOUTB.
                                  ; **CONFIGURE PORT 1 AS OUTPUT.**
   MOV R3, #GIODIRB               ; loads offset address of GIODIRB.
   MOV R4, #0xFF                  ; loads a binary value of 11111111.
   STR R4, [R2, R3]               ; configures port 1 as output
                                  ; **TOGGLE BITS 0, 2, 4, 6.**
   MOV R3, #GIODSETB              ; loads offset address of GIODSETB
   MOV R4, #GIODCLRB              ; loads GIODCLRB offset address
   MOV R5, #0x55                  ; loads a binary value of 01010101
TOGGLE
   STR R5, [R2, R4]               ; clears GIODOUTB bits 0, 2, 4, 6
   STR R5, [R2, R3]               ; sets GIODOUTB bits 0, 2, 4, 6
   B TOGGLE                       ; loops back to TOGGLE
```

The code in Example 5 demonstrates how interrupt flags should be cleared before interrupts are enabled. In this example, all three interrupt-capable pins are set as interrupts (See also Table 3.)

Example 5. Clearing Interrupt Flags and Setting Interrupts

```
GIO_LOC.word 0xFFF7EC00          ; device specific address for GIO registers
GIOENA .equ    0x04              ;setting up equate statements
...
GIODIRB .equ 0x38
GIODINB .equ 0x3C
GIODOUTB.equ 0x40
GIODSETB.equ 0x44
GIODCLRB .equ 0x48

   LDR R2, GIO_LOC               ;loads absolute address of the GIO memory
   MOV R3, #GIOFLG               ;loads GIOFLG offset address into R3.
   MOV R4, #0x07                 ;loads a value of 00000111 into R4.
   STR R4, [R2, R3]              ;clears the interrupt-capable bits of the
                                 ;GIOFLG control register.

   MOV R3, #GIOENA               ;loads GIOENA offset address into R3.
   MOV R4, #0x07                 ;loads 00000111 into R4.
   STR R4, [R2, R3]              ;enables pins 2:0 of port A as interrupts.
```

The code in Example 6 demonstrates how to read the input register of port A when interrupts are enabled. Pin 0 is set as an interrupt, and pins 2 and 1 are configured as inputs.

Example 6. Reading Port A Input Register

```
GIO_LOC.word 0xFFF7EC00          ;device specific address for GIO registers
GIOENA .equ    0x04              ;setting up equate statements
...
GIODIRB .equ 0x38
GIODINB .equ 0x3C
GIODOUTB.equ 0x40
GIODSETB.equ 0x44
GIODCLRB .equ 0x48

   LDR R2, GIO_LOC               ;loads absolute address of the GIO memory
                                 ;**MASK OUTPUTS AND INTERRUPTS SO INPUT IS UNAMBIGUOUS.*
   MOV R3, #GIODINB              ;loads the offset address of GIODINB.
   LDR R4, [R2, R3]              ;loads the value in GIODINB register into R4.
   MOV R3, #0xFE                 ;loads 11111110 into R3. This value is used
                                 ;to mask the input so that only the input
                                 ;values are read. The 1's appear in the places
                                 ;where the input register is reading input
                                 ;voltages.
   AND R4, R4, R3                ;loads masked input value into R4.
```