TMS470R1x Zero-Pin Phase-Locked Loop (ZPLL) Clock Module Reference Guide

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Zero-Pin Phase-Locked Loop (ZPLL) Clock Module

This reference guide describes the zero-pin phase-locked loop (ZPLL) clock module that provides SYSCLK to the clock control module (CCM) located in the system module. The CCM provides SYSCLK and ICLK for all other TMS470 modules. In this document, ACLK should not be confused with the ADC internal clock, ADCLK.

1   Overview

The ZPLL clock module synthesizes the generally higher frequency continuous clock, ACLK, from an external resonator/crystal reference. ACLK goes to the clock control module (CCM), which generates the global system clock, SYSCLK.

Using a PLL enables you to multiply the external frequency reference to a higher frequency for internal use. This avoids placing the high-frequency signals on external package pins, which can cause excessive electromagnetic interference (EMI). PLLs also avoid the use of crystals above 20–25 MHz. Such crystals usually operate in overtone mode and require extra tank circuit components.

The ZPLL clock module contains a phased-locked loop (PLL), crystal oscillator, clock monitor circuit, clock enable circuit, and prescaler.

Using a PLL-based clock module has the following advantages:

❏ Lowers EMI due to lower external oscillator frequencies
❏ Uses lower cost crystals and resonators
❏ Avoids overtone crystals which require tank circuits

The main disadvantage of the PLL in contrast with a simple oscillator is that the PLL can be sensitive to noise if proper board decoupling and layout practices are not adhered to. Therefore, it requires more system-level design effort to ensure low jitter, robust operation.

1.1   Features

The main features of the ZPLL clock module are:

❏ Oscillator operates with both resonators and crystals.

❏ Bypass mode covers external OSCIN frequencies from 4.0 MHz to 20 MHz and produces SYSCLK frequencies from 263 kHz to 20 MHz.

❏ Nonbypass (PLL) mode covers OSCIN frequencies from 4.0 MHz to 20 MHz and synthesizes SYSCLK frequencies from 2.4 MHz up to the device limit.

❏ $f_{SYSCLK} = M * f_{OSCIN}$ / prescale, where M can be 4 or 8

❏ Prescale value can be 1, 2, 3, 4, 5, 6, 7, or 8.

❏ It can be used with the PLL bypassed ($f_{SYSCLK} = f_{OSCIN}$ / prescale).

❏ Phase-frequency detector ensures locking only to the fundamental reference frequency.

❏ User option bit can be used to reset the device if resonator/crystal failure is detected.

❏ Control/Status registers are superset compatible with analog phase-locked loop (APLL) registers.

1.2 Definition of Terms

Terms used in this chapter are defined as follows:

❏ Zero-pin phase-locked loop (ZPLL): A module consisting of a PLL subblock and support circuitry. It is called *zero-pin* because the internal PLL submodule does not require any pins for an external filter circuit.

❏ Charge pump and loop filter(CP and LF): A circuit used to convert the pulse-width modulated correction signals into an analog control voltage.

❏ Electromagnetic interference (EMI): The radio frequency noise radiated by a circuit which can disturb the proper operation of other equipment, or the radio frequency noise radiated by other equipment which can disturb the proper operation of the subject circuit.

❏ Jitter: The maximum positive or negative deviation of a clock edge with respect to its nominal position within a single clock period, expressed in nanoseconds or in percentage of one clock period.

❏ Lock: The condition in which the output of a PLL is synchronized to the phase and frequency of its reference input.

❏ Phase-frequency detector (PFD): A circuit that compares two signals in both phase and frequency and distinguishes when one signal is a harmonic or subharmonic of another signal.

❏ Phase-locked loop (PLL): An oscillator circuit with output frequency that is typically an integer multiple of its reference input frequency.

❏ Voltage-controlled oscillator (VCO): An oscillator with output frequency that is proportional to a control voltage input.

2   Functional Description

The following section provides a functional overview of the clock module. The simplified block diagram of Figure 1 illustrates the clock module and its components.

Figure 1. Clock Module Block Diagram
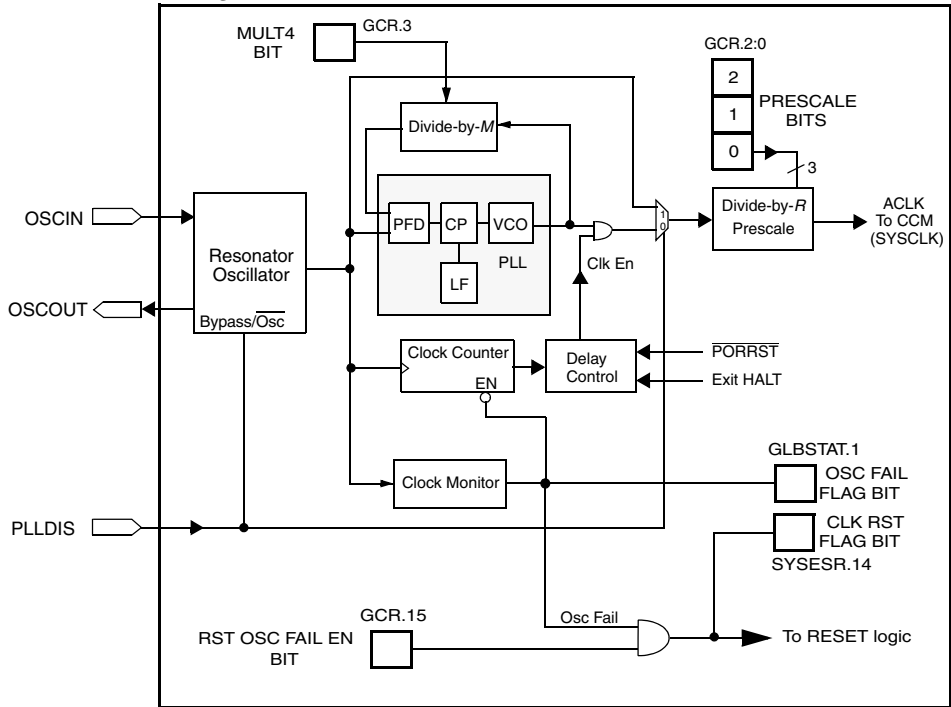
2.1   Basic ZPLL Clock Module Operation

The resonator/crystal is made to oscillate by the oscillator circuit. This creates a reference frequency which is used as the input of the PLL. The PLL then multiplies the reference frequency by four or eight to produce the VCO output, which is then scaled by the prescaler block to produce SYSCLK.

During power up or exit from HALT mode, the clock counter and delay control blocks control the release of SYSCLK and/or RESET. These blocks create a delay which keeps the device from executing instructions until the PLL has had time to lock.

The clock monitor detects failures of the external resonator/crystal and generates the OSC FAIL flag bit (GLBSTAT.1) to the system module. Optionally, a system reset can be forced when such a failure is detected.

2.2   Module Pins

Three pins are required to operate the clock module shown in Figure 1. The crystal oscillator requires two pins (OSCIN and OSCOUT) for the crystal and the external load capacitors. The load capacitors tie back to the nearest VSS pin. The bias resistor of the oscillator is integrated, so generally no external resistors are necessary.

The PLLDIS pin enables bypassing the PLL for emulation and testing. This pin is essential for speeding up test time, which reduces chip cost. It cannot be multiplexed with another pin or general purpose input-output (GPIO) due to the various pin permutations required during test. The device can be used in bypass mode with only the crystal oscillator (PLL disabled); however, to obtain the same SYSCLK operating frequency, the crystal frequency can be up to eight times the frequency required if the PLL is used.

The ZPLL module uses an internal loop filter circuit; therefore, no external loop filter components are required for proper operation of the PLL.

3 Operation

This section explains the operation of the functional blocks of the ZPLL clock module that are illustrated in Figure 1.

3.1 Resonator/Crystal Oscillator

The oscillator requires two external pins, OSCIN and OSCOUT, which are connected to the resonator/crystal and load capacitors (see Figure 2). The oscillator is a single-stage inverter held in bias by an integrated bias resistor of approximately 100 kΩ. This resistor is disabled during HALT mode. It is connected during normal PLL and bypass mode operation.

Figure 2. Reference Resonator/Crystal
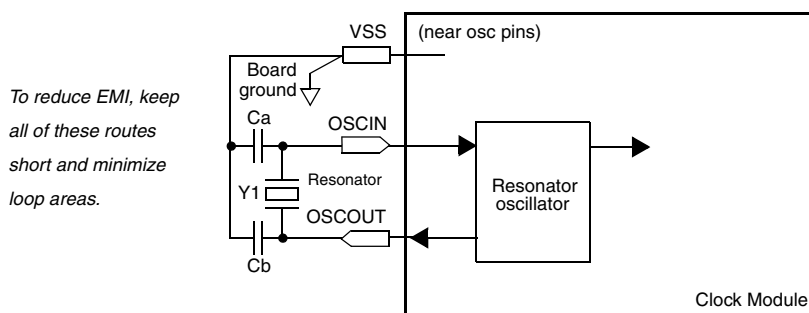
Note: Validating Resonator/Crystal Vendors

Texas Instruments strongly encourages customers to submit samples of the microcontroller device to their resonator/crystal vendor for validation. The vendor is equipped to determine the load capacitors that best tune their resonator/crystal to the device for optimum start-up margin and operation over temperature/voltage extremes. The vendor also factors in margin for variations in the microcontroller's process variations.

The load capacitors should be grounded back to the nearest device ground pin with a private run as short as practical to minimize electromagnetic interference (EMI). Keep loop areas formed by the crystal/resonator, load capacitors, and the OSCIN, OSCOUT, and GND pins as small as practical. EMI requires an antenna, but do not build one any larger than necessary!

3.2   **Phase-Locked Loop (PLL)**

The PLL block consists of three logical subblocks: a phase-frequency detector (PFD), a charge pump (CP), and a voltage-controlled oscillator (VCO), as shown in Figure 3.

Figure 3. Basic PLL Circuit
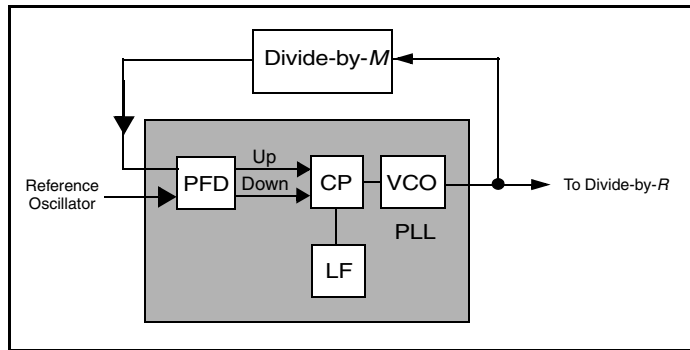
3.2.1   *Phase-Frequency Detector (PFD)*

The PFD compares the input reference phase and frequency to the feedback phase and frequency of the divider and generates two signals: an *up* pulse and a *down* pulse. These signals drive a charge pump. After this charge is integrated by the internal filter circuit, it produces a VCO control voltage, as shown in Figure 4.
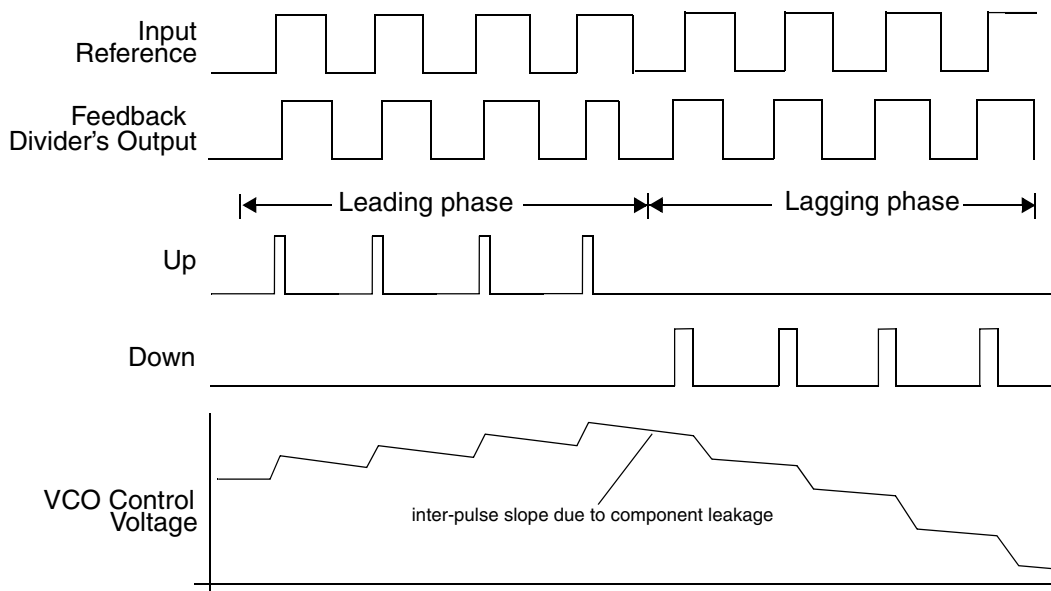
Figure 4. PDF Timing

Input Reference

Feedback Divider's Output

|← Leading phase →|← Lagging phase →|

Up

Down

VCO Control Voltage

inter-pulse slope due to component leakage

The width of the up pulse and the down pulse depends on the difference in phase between the two inputs. If, for example, the reference input leads the feedback input by 10 ns, then an up pulse of approximately 10 ns is generated (see Figure 4). If, on the other hand, the reference input lags the feedback input by 25 ns, then a down pulse of approximately 25 ns is generated. When the two inputs are exactly in phase, the up pulses and down pulses become essentially zero-width. These pulses are fed to the charge pump block, which meters charge into the low-pass loop filter.

The advantage of a phase-frequency detector (PFD) over a phase-only detector is that a PFD cannot lock to a harmonic or subharmonic of the reference frequency. This property ensures that the output frequency of the VCO is always exactly four or eight times the reference frequency.

3.2.2   Charge Pump (CP)

The charge pump (see Figure 5) consists of two gated current sources that either add or remove charge from the filter capacitors of the internal low-pass filter, depending on the pulses coming from the PFD.

Figure 5. Charge Pump Functional Model
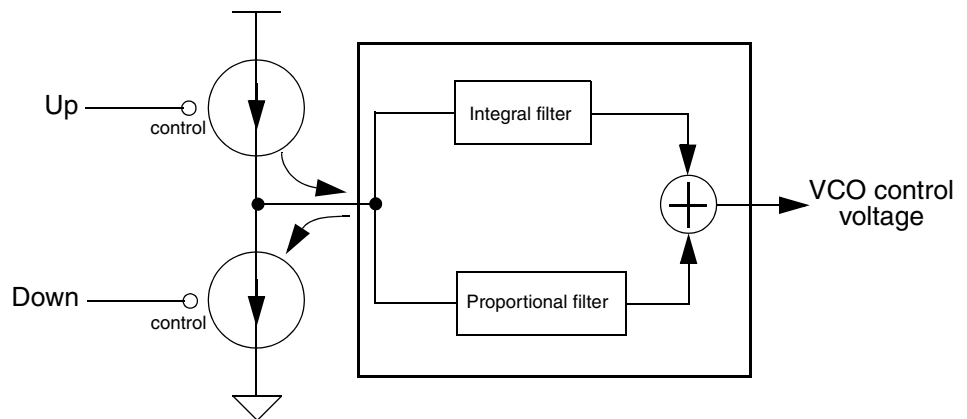
The filter output signal has two components that are summed together: an integral component and a proportional component. Effectively, the integral component supplies a DC level to the VCO to maintain its frequency, and the proportional component makes the VCO track changes in phase. In this ZPLL module, the capacitors and resistors required for the filter are integrated into the device.

3.2.3   *Voltage-Controlled Oscillator (VCO)*

The VCO is an oscillator with output frequency that is proportional to its input control voltage, which is generated by the charge pump through the low-pass filter.

If the VCO oscillates too slowly, the feedback phase begins to lag the reference phase at the PFD, and the control voltage at the VCO increases. Conversely, if the VCO oscillates too fast, the feedback phase begins to lead the reference phase at the PFD, and the control voltage at the VCO decreases. These two actions keep the VCO running at the correct frequency multiple of the reference.

In bypass mode, the VCO is disabled, and the input of the prescaler block is connected to the OSCIN pin through an amplifier. External frequency sources must be driven into the OSCIN pin and the OSCOUT pin should be left open.

If a crystal/oscillator failure occurs, the VCO frequency falls rapidly (although not instantly) to zero because the ZPLL module has no limp frequency.

3.3 Bypass Multiplexer

The multiplexer is used to bypass the PLL when the PLLDIS pin is high. When PLLDIS is low, the multiplexer selects the output of the VCO through the clock-enable gate (see Figure 1). In both bypass and non bypass modes, the divide-by-*R* prescaler is used to divide down the source frequency to produce SYSCLK.

3.4 Feedback Divider (Divide-by-*M*)

The feedback divider is a modulo-4 (default) or modulo-8 counter that divides the VCO output frequency by four or eight, respectively. The MULT4 bit in the Global Control register (GCR.3) controls the divider's modulus, *M*, where $M = 4$ or 8.

The output of the divider becomes the *feedback phase* referred to earlier. By dividing the VCO frequency by *M*, the reference frequency from the resonator oscillator is effectively multiplied by *M*. This occurs because the VCO now has to run *M* times as fast in order to produce a feedback signal with the same frequency as the reference signal. Changing the divider by writing a different state to the MULT4 bit (GCR.3) causes the system clocks to stop for 4096 oscillator cycles while the PLL locks to the new frequency.

3.5 Clock Monitor

If the oscillator slows to less than a hundred kilohertz or stops (including OSCIN *stuck high* or *stuck low* condition), the output of the clock monitor becomes active and sets the OSC FAIL flag bit (GLBSTAT.1). See the specific device data sheet for the minimum and maximum oscillator detection frequencies.

The clock monitor output sets the OSC FAIL flag bit in the Global Status register (GLBSTAT.1) of the system module to indicate that a failure of the oscillator has been detected. This bit is provided for software polling. The OSC FAIL flag bit remains set until it is cleared by software or until a system reset ($\overline{\text{RESET}}$) or power-on reset ($\overline{\text{PORRST}}$) occurs.

Setting the RST OSC FAIL EN bit in the Global Control register (GCR.15) of the system module causes the device to undergo a system reset when an oscillator failure is detected. In this case, the CLK RST flag in the System Exception Status register (SYSESR.14) of the system module is also set and remains set until a zero is written to it, or until a power-on reset is performed.

A system reset holds the system clocks for 4096 oscillator cycles. See Section 5, Application Information, page -16 for details.

The common failure mode of the oscillator is to stop if any of the PC board traces are opened (detectable failure); however, it is possible for the resonator to become damaged and speed up in frequency. This type of failure is *not* detected by the clock monitor circuit. If the oscillator stops, no operation is possible except for a system reset (if the RST OSC FAIL EN bit [GCR.15] is set prior to the failure).

3.6   Clock Counter and Delay Control

The clock counter and delay control are used to delay start of code execution following a power-up reset, when HALT mode is exited, or after the MULT4 bit (GCR.3) changes to allow for the ZPLL module to reestablish lock. The clock counter counts 4096 oscillator cycles after the oscillator monitor detects resonator/crystal oscillation.

After $\overline{\text{PORRST}}$ occurs, the timer holds off $\overline{\text{RESET}}$ until the 4096 oscillator cycles have elapsed. When the MULT4 bit (GCR.3) is being changed or when HALT mode is exited, SYSCLK is held for 4096 OSCIN cycles. Both of these mechanisms prevent code execution until the VCO frequency has stabilized.

3.7   Divide-by-*R* Prescaler

After the VCO has generated a frequency *M* times the reference frequency, you can divide the VCO output by any integer value from one to eight by programming the PLL clock divider prescale bits, CLK DIV PRE 2:0, in the Global Control register (GCR.2:0) of the system module (see Table 1) Programming these bits causes a glitch-free transition from the current frequency to the frequency specified by the bits.

The default at power-up is divide-by-eight; therefore, the initial frequency is equal to 1/2 the resonator/crystal frequency in non bypass mode, and 1/8 the resonator/crystal frequency in bypass mode.

Table 1. Multiplier M and Clock Divider R Control Bits

MULT 4	CLK DIV PRE 2	CLK DIV PRE 1	CLK DIV PRE 0	F_{SYSCLK}/F_{OSCIN}	
1	1	1	1	1/2 (default at power-up)	0.5
1	1	1	0	4/7	0.571
1	1	0	1	2/3	0.667
1	1	0	0	4/5	0.8

Table 1. Multiplier M and Clock Divider R Control Bits (Continued)

MULT 4	CLK DIV PRE 2	CLK DIV PRE 1	CLK DIV PRE 0	F_{SYSCLK}/F_{OSCIN}	
1	0	1	1	1	1
1	0	1	0	4/3	1.333
1	0	0	1	2	2
1	0	0	0	4	4
0	1	1	1	1	1
0	1	1	0	8/7	1.143
0	1	0	1	4/3	1.333
0	1	0	0	8/5	1.6
0	0	1	1	2	2
0	0	1	0	8/3	2.667
0	0	0	1	4	4
0	0	0	0	8	8

4   Control Registers

The ZPLL clock module has no registers of its own; it relies on bits in three different registers within the system module. Figure 6 shows a summary of all clock module bits.

Figure 6.   Clock Module Control Bits and Flags
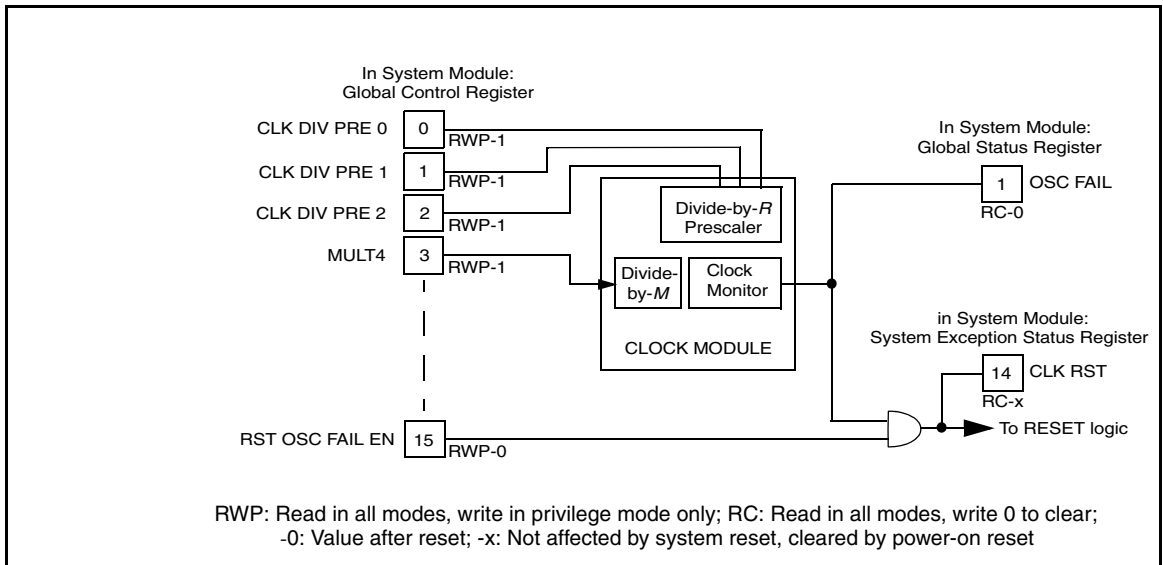
The clock module generates the OSC FAIL flag bit (GLBSTAT.1). When this flag is set, you have the option to enable a system reset using the RST OSC FAIL EN bit (GCR.15). When this bit is enabled and an oscillator failure is detected, the CLK RST flag bit (SYSESR.14) is also set to indicate that the source of the reset is the clock monitor.

4.1   Global Control Register (GCR)

All but one bit of the Global Control register bits are reserved for the clock module; one bit enables configuring the flash module. Any write to this register asserts three wait states. See Table 7.

Figure 7.   Global Control Register (GCR)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0xFFFF_FFDC	Reserved															
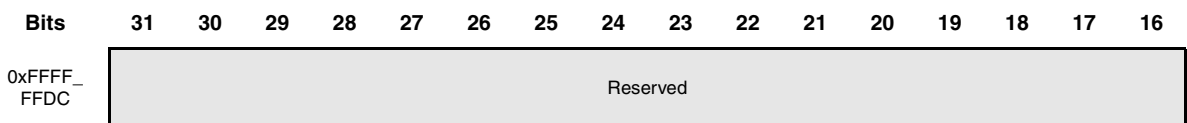
Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RST OSC FAIL EN	RTI CTRL					Reserved					FL CON-FIG	MULT 4		CLK DIV PRE[2:0]	
	RWP-0	RWP-0					U					RWP-0	RWP-1		RWP-111	

R = Read in all modes; WP = Write in privilege mode only; U = Undefined; *-n* = Value after reset

Bits 31:16   **Reserved.**

Read values are indeterminate. Writes have no effect.

Bit 15   **RST OSC FAIL EN.** Reset on Oscillator Failure Enable.

When set, this bit causes a system reset to occur if a detectable oscillator failure occurs. When this bit is cleared, the status of the oscillator monitor can be checked by reading the OSC FAIL flag bit (GLBSTAT.1) in the Global Status register of the system module.

Bit 14   **RTI CTRL.** RTI Control**.**

This bit allows RTI to change clock domains and this bit description is contained in the system module. Please see the device-specific data sheet to verify that your device provides this feature.

Bits 13:5   **Reserved.**

Read values are indeterminate. Writes have no effect.

Bit 4   **FLCONFIG.** Flash Configuration Enable.

This bit enables write access to the control registers of the flash module. See the chapter on the flash module for details on using this bit.

Bit 3   **MULT4.** Multiply-by-4.

When this bit is set (default), it causes the PLL to multiply the reference frequency by four. When it is cleared, the PLL is multiplied by eight.

Bits 2:0   **CLK DIV PRE[2:0].** Clock Divider Prescale bits.

The clock divider prescale bits determine the divisor of the VCO output. Programming these bits causes a glitch-free transition from the current frequency to the frequency specified by the bits (see Table 2).

The default at power up is divide-by-eight; therefore, the initial frequency is 1/2 the resonator/crystal frequency.

Table 2. Clock Divider Prescale Bits

GCR 2	GCR 1	GCR 0	Clock Divisor
1	1	1	8 (default at power up)
1	1	0	7
1	0	1	6
1	0	0	5
0	1	1	4
0	1	0	3
0	0	1	2
0	0	0	1

5   Application Information

This section provides practical information about using the clock module.

## 5.1   Clock Start-up From Power Up

With the onset of power, the following sequence of events occurs before the system clocks are enabled. Figure 8 illustrates this timing. Note that the timing at power-on reset is different from the timing when HALT mode is exited primarily because Vcc is already present and stable.

1) **Power-up ramp:** You supply Vcc to the device along with $\overline{\text{PORRST}}$, which should be valid above Vop (Vop is the Vcc voltage below which the device is nonoperational, typically around 0.6 V).

2) **Oscillator start-up:** As Vcc ramps up, the oscillator starts even before Vcc_{min} is achieved. The oscillations increase in amplitude with time. After the oscillations are large enough, the oscillator output starts switching, allowing subsequent logic to start functioning.

3) **ACLK starts:** ACLK starts as soon as the oscillator starts.

4) **4096 oscillator cycles:** The clock counter starts incrementing as soon as $\overline{\text{PORRST}}$ has been released and the oscillator has started. After the clock counter has counted to 4096, it releases the internal reset logic. The PLL is responsible for locking during this time. If the clock monitor detects a pause in the output of the oscillator for any reason, the counter is reset and the countdown of the 4096 cycles start again.

5) **8 SYSCLK cycles:** After the reset logic is released, the system module continues to hold internal reset as well as external $\overline{\text{RESET}}$ active for an additional eight SYSCLK cycles before releasing them.

6) **Reset held off by external circuit:** Any external pulldowns or RC networks connected to $\overline{\text{RESET}}$ further delay the release of $\overline{\text{RESET}}$ (both internally and externally).

> **Note: Other Devices Connected to RESET Externally**
>
> If other devices are connected to RESET externally, keep in mind that the exact time at which internal reset is released in the TMS470R1x can differ significantly from the time when these other devices are released internally. This is due to differences in threshold levels on the reset pins of the different devices in your circuit. The time difference is made worse as the slope (rise time) of the RESET signal increases. While this is typically not a difficult problem to avoid, it needs to be comprehended in software when communication to external devices occurs immediately after power up.

Figure 8. Start-up From Power Up
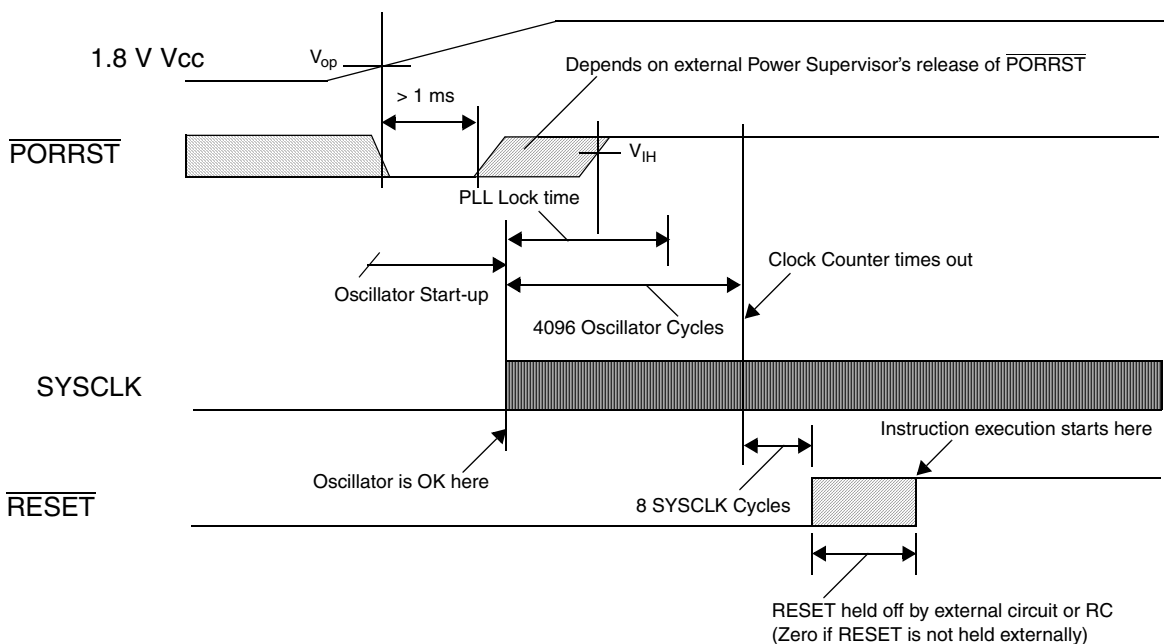
5.2   Clock Start-up From Exit HALT Mode

During HALT mode, the oscillator and PLL are shut off. When HALT mode is exited, the following sequence of events occurs before the CPU can start executing instructions.

Also, if the RST OSC FAIL EN bit (GCR.15) is set and the oscillator fails, a reset occurs. If the oscillator condition is temporary and it becomes operational again, the same sequence of events as described for exiting HALT mode occurs. See Figure 9.

1) **Exit HALT mode (or osc restarts):** Both of these events imply that the oscillator starts to oscillate again.

2) **Oscillator start-up:** The oscillations increase in amplitude with time. After the oscillations are large enough, the oscillator output starts switching, allowing subsequent logic to start functioning.

Figure 9. Start-up From HALT Mode
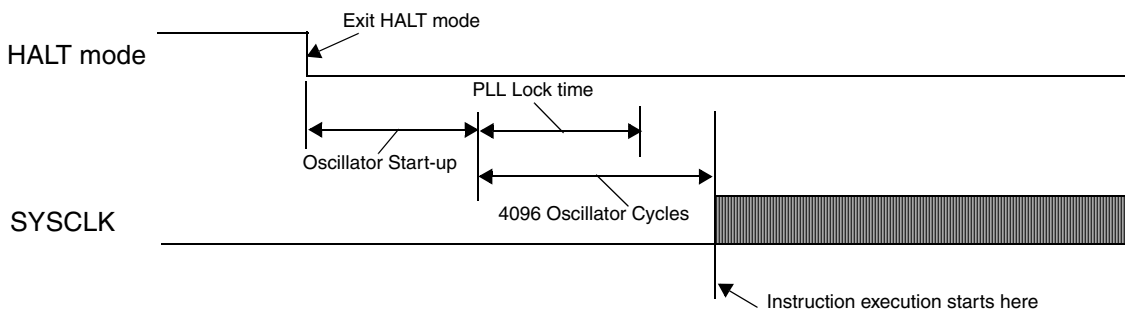
3) **4096 oscillator cycles:** The PLL is required to lock within 4096-cycle delay. After the clock counter has counted to 4096, it enables SYSCLK. If the clock monitor detects a pause in the output of the oscillator for any reason, the counter is reset and the countdown of the 4096 cycles starts again.

4) **ACLK release:** ACLK is enabled by the completion of the 4096 clock cycles. When ACLK starts, the CPU resumes instruction execution if no other modules request wait states.
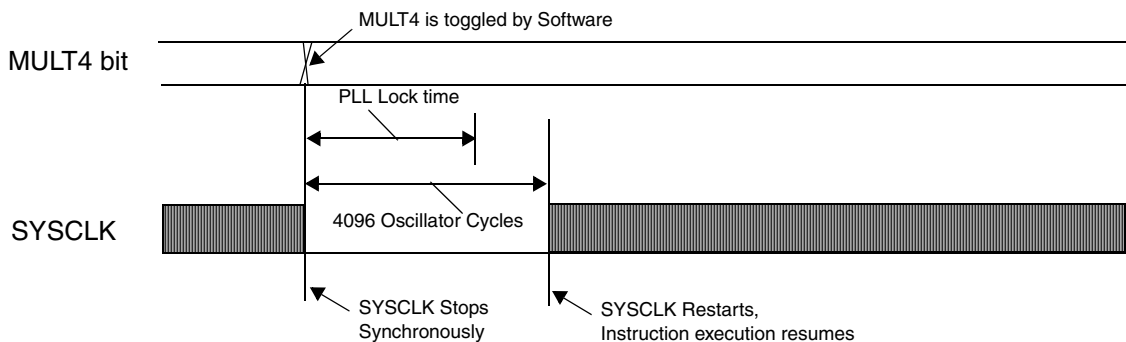
5.3   Clock Delay After Modifying MULT4 Bit

After changing the state of the MULT4 bit (GCR.3) by writing to it, the PLL must lock to a new frequency. This necessitates delaying the system clocks until the PLL is stabilized at the new frequency. The following sequence of events occurs before the CPU can continue executing instructions. See Figure 10.

1) **MULT4 bit is toggled:** You write the opposite state to the GCR.3 bit.

2) **SYSCLK stops:** After some synchronizing cycles, SYSCLK is stopped and the delay counter is cleared.

Figure 10. SYSCLK Start-up After MULT4 is Changed

MULT4 is toggled by Software

MULT4 bit

PLL Lock time

4096 Oscillator Cycles

SYSCLK

SYSCLK Stops
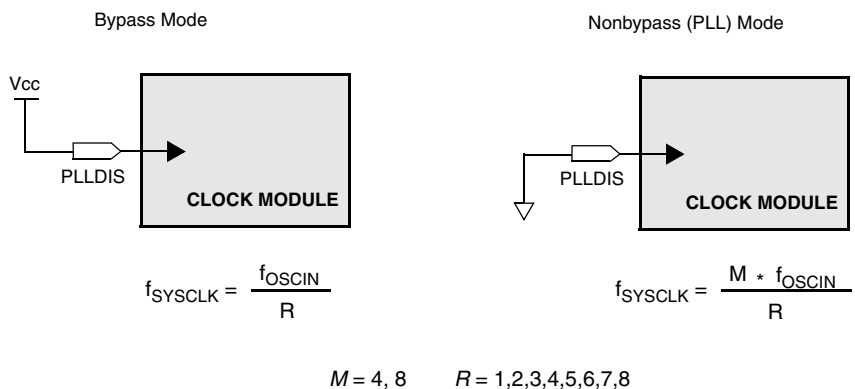Synchronously

SYSCLK Restarts,
Instruction execution resumes

3) **4096 oscillator cycles:** The PLL is required to lock within 4096-cycle delay. After the clock counter has counted to 4096, it enables ACLK. When ACLK starts, the CPU resumes instruction execution if no other modules request wait states.

5.4   Operating Modes

The ZPLL module operates in bypass and non bypass mode. These modes are described in Section 3.3, Bypass Multiplexer, page -10. To place the ZPLL module in one of these modes, the PLLDIS pin can be tied (or pulled using a resistor) either high or low, as shown in Figure 11.

Figure 11. Bypass and Nonbypass Modes

Bypass Mode

Vcc

PLLDIS

CLOCK MODULE

$$f_{SYSCLK} = \frac{f_{OSCIN}}{R}$$

Nonbypass (PLL) Mode

PLLDIS

CLOCK MODULE

$$f_{SYSCLK} = \frac{M * f_{OSCIN}}{R}$$

$M = 4, 8$ $R = 1,2,3,4,5,6,7,8$

5.5 Using One Oscillator for Two Microcontrollers

It is possible to connect two microcontrollers and use only a single crystal/ resonator if you understand the restrictions.

5.5.1 *Connections*

The master microcontroller is the one with the crystal/resonator circuit connected to it. The OSCOUT pin of the master is connected via a short lead to the OSCIN pin of the slave and the slave's OSCOUT pin is left open. The slave microcontroller has no other components connected to it (see Figure 12). Stray capacitances of the additional wiring and input should be accounted for and subtracted from the value of the OSCOUT load cap of the master.

5.5.2 *Restrictions*

The two microcontrollers lock to opposite phases of the reference oscillator. This is normally not a problem in PLL mode because the PLL multiplies by at least 4 (making 0, 90, 180, and 270 degrees of the reference frequency indistinguishable). In bypass mode, the prescaler clocks on opposite phases of the reference oscillator, and SYSCLK is further divided from there.

A second restriction is that the microcontrollers cannot be used in HALT mode.

Figure 12. Two TMS470R1x Devices Using One Resonator/Crystal
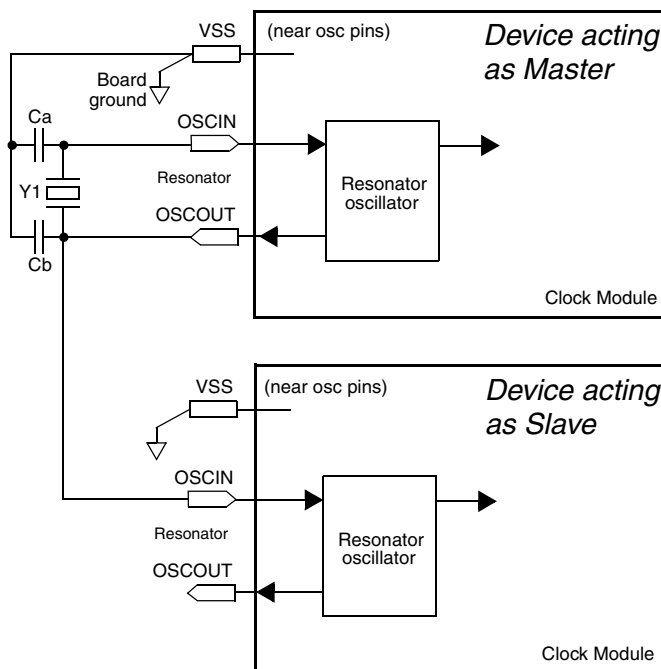
When a TMS470R1x microprocessor enters HALT mode, the OSCIN pin is grounded in order to stop the oscillator quickly, the internal bias resistor is opened to minimize quiescent power, and the OSCOUT pin is taken to the high-impedance state (high-Z).

If the master enters HALT mode first, it takes the OSCOUT pin to high-impedance state, and the slave loses its reference clock. Because the internal bias resistor of the slave is still connected, the OSCIN and OSCOUT pins of the slave are biased to approximately Vcc/2, causing excessive current in the transistors of the oscillator (not destructive).

If the slave enters HALT mode first, its OSCIN pin is grounded, which inadvertently shorts the OSCOUT pin of the master to ground and stops both microprocessors.