TMS470R1x Expansion Bus Multiplexer Module (EBM) Reference Guide

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REVISION HISTORY

REVISION	DATE	NOTES
C	8/09	Corrected description for the EBADDR bits in the EBM Address Control Register 3.
B	11/04	Added overview diagram. Updated register names/information, Added individual register information for all registers. Added example, section 5.
A	10/2002	Converted to a standalone book. Page 6, EBMXCRx bit description corrected.
*	7/2002	Initial Version

Contents

Figures

Tables

Expansion Bus Multiplexer Module (EBM)

The expansion bus multiplexer module (EBM) is a stand-alone module providing bond out for both general purpose input/output pins and expansion bus interface pins for the Texas Instruments (TI) TMS470 microcontroller family. The module supports the multiplexing of the input/output (I/O) functions and the expansion bus interface. When the I/O functions are not used, the EBM can be used to interface 8- or 16-bit memories.

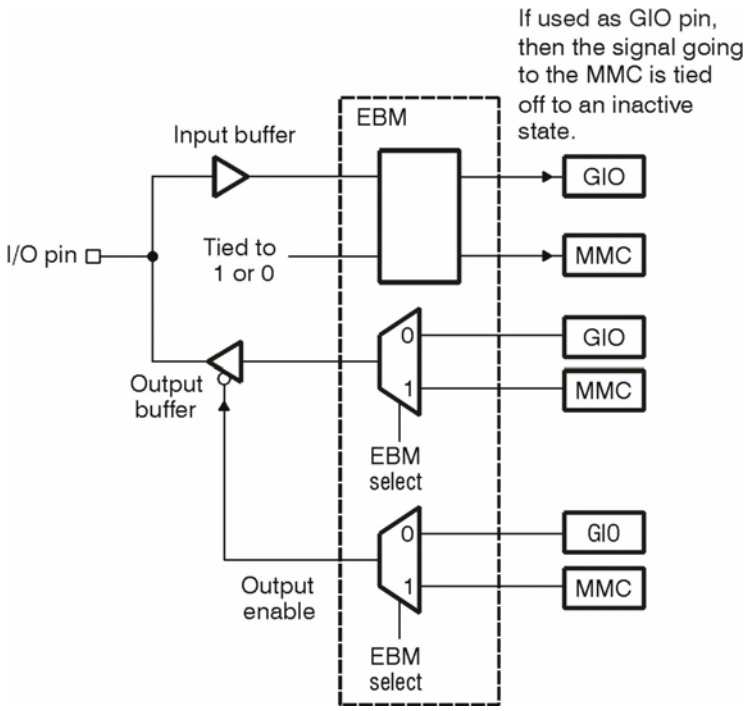
1 Overview

The expansion bus multiplexer module (EBM) has the following features:

- Multiplexing of I/O signals to an expansion memory interface or a peripheral interface
- Supports 8- and 16- bit expansion bus memory interface mappings
- Supports mapping of the following expansion bus signals:
  - Up to 30-bit address bus (EBADDR[29:0]) for 8- bit data bus
  - Up to 22-bit address bus (EBADDR[21:0]) for 16- bit data bus
  - 8- or 16- bit data bus (EBDATA[7:0] or EBDATA[15:0])
  - Up to 2 write strobes
  - Up to 4 memory chip selects
  - 1 output enable
  - 1 external hold signal for interfacing to slow memories
  - Up to 8 DMA request lines

Figure 1provides a diagram of the EBM.

Figure 1. EBM Overview



2 Description

This section describes the EBM signals and provides the timing parameters.

2.1 EBM Signals

Table 1 contains the names of the EBM signals and their descriptions.

Table 1. EBM Pin Description

PIN	DESCRIPTION
EBDMAREQ	Expansion bus DMA request
$\overline{\text{EBOE}}$	Expansion bus output enable
$\overline{\text{EBWR}}$	Expansion bus write strobe. $\overline{\text{WR1}}$ controls EBDATA[15:8] and $\overline{\text{WR0}}$ controls EBDATA[7:0]
$\overline{\text{EBCS}}$	Expansion bus chip select
EBADDR	Expansion bus address pin
EBDATA	Expansion bus data pin
$\overline{\text{EBHOLD}}$	Expansion bus hold. An external device may assert this signal to add wait states to an expansion bus transaction.

Note:

Please refer to the specific data sheet for the actual EBM signal mappings to the device functional pins.

Note:

Signals that are not used for expansion bus functions can be used as I/O signals.

3 EBM Register Overview

Table 2 displays a general representation of the EBM internal registers. Writes have no effect on the upper 16 bits of these registers. Figure 2 shows the summary of the register bits.

Table 2. EBM Internal Registers

Address Offset (1)	Label	Name	Description
0x00	EBDMACR	EBM DMA Request Control Register	Controls the multiplexing of the expansion bus DMA requests with the functional I/O pins.
0x04	EBRWCR	EBM Read Write Control Register	Controls the multiplexing of the expansion bus chip selects, the read enable, the write enable and the hold signals with the functional I/O pins.
0x08	EBACR1	EBM Address Control Register 1	Controls the multiplexing of the expansion bus address lines 5 down to 0 with the functional I/O pins. Also controls the multiplexing of the write enable signals 3–2.
0x0C	EBDCR	EBM Data Control Register	Controls the multiplexing of the expansion bus data lines 7–0 with the functional I/O pins.
0x10	EBADCR	EBM Address/Data Control Register	*8-bit mode:* Controls the multiplexing of the expansion bus address lines 13–6. *16-bit mode:* Controls the multiplexing of the expansion bus data lines 15–8 in 16-bit mode.
0x14	EBACR2	EBM Address Control Register 2	*8-bit mode:* Controls the multiplexing of the expansion address lines 21–14 with the functional I/O pins. *16-bit mode:* Controls the multiplexing of the expansion address lines 13–6 with the functional I/O pins.
0x18	EBACR3	EBM Address Control Register 3	*8-bit mode:* Controls the multiplexing of the expansion bus address lines 29–22 with the functional I/O pins. *16-bit mode:* Controls the multiplexing of the expansion bus address lines 21–14 with the functional I/O pins.
0x1C	EBMCR1	EBM Control Register 1	Controls the type of expansion bus interface.

1) The actual address of these registers is device- and CPU-specific. See the specific device data sheet to verify the EBM register addresses.

Figure 2. EBM Register Summary

Offset Address †	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	EBDMACR	Reserved								EBDMAREQ[7:0]							
0x04	EBRWCR	Reserved								$\overline{\text{EBHOLD}}$	$\overline{\text{EBCS[3:0]}}$				$\overline{\text{EBWR[1:0]}}$		$\overline{\text{EBOE}}$
0x08	EBACR1	Reserved								EBWR[3:2]	EBADDR[5:0]						
0x0C	EBDCR	Reserved								EBDATA[7:0]							
0x10	EBADCR	Reserved								EBADDR[13:6]/EBDATA[15:8]							
0x14	EBACR2	Reserved								EBADDR[21:14]/EBADDR[13:6]							
0x18	EBACR3	Reserved								EBADDR[29:22]/EBADDR[21:14]							
0x1C	EBMCR1	Reserved										0			DSIZE		LPM

4 EBM Register Detailed Description

The following sections describe the registers individually.

4.1 EBM Request Control Register (EBDMACR)

Figure 3 and Table 3 describe this register.

Figure 3. EBM Request Control Register (EBDMACR)

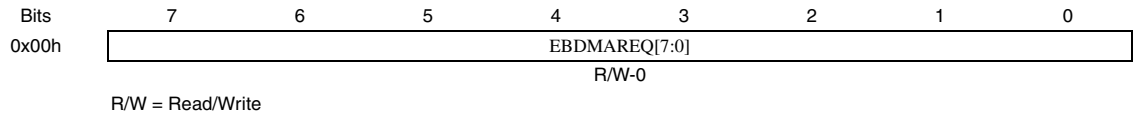


Table 3. EBM Request Control Register (EBDMACR) Field Descriptions

Bit	Name	Value	Description
7–0	EBDMAREQ[7:0]		DMA Request
		0	I/O signals are mapped to the mux output.
		1	Expansion bus DMA signals 7–0 are mapped to the output.

4.2 EBM Read/Write Control Register (EBRWCR)

Figure 4 and Table 4 describe this register.

Figure 4. EBM Read/Write Control Register (EBRWCR)

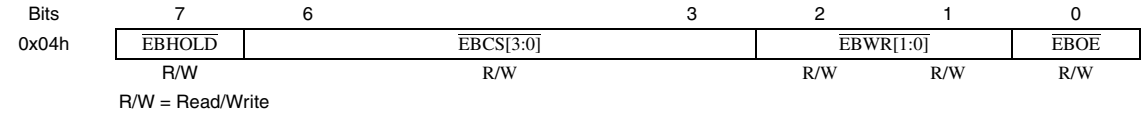


Table 4. EBM Read/Write Control Register (EBRWCR) Field Descriptions

Bit	Name	Value	Description
7	$\overline{\text{EBHOLD}}$		Hold
			Note: See note in Examples section
		0	The I/O signal is mapped to the mux output.
		1	This pin is available to be asserted by an external device to add wait states to an expansion bus transaction.
6–3	$\overline{\text{EBCS[3:0]}}$		Chip Selects
		0	The I/O signal is mapped to the mux output.
		1	The expansion bus chip selects 3–0 are mapped to the mux output.
2–1	$\overline{\text{EBWR[1:0]}}$		Write Enable
		0	The I/O signal is mapped to the mux output.
		1	The write enable bits are mapped to the mux output.
0	$\overline{\text{EBOE}}$		Output Enable
		0	The I/O signal is mapped to the mux output.
		1	The output enable bits are mapped to the mux output.

4.3 EBM Address Control Register 1 (EBACR1)

Figure 5 and Table 5 describe this register.

Figure 5. EBM Address Control Register 1 (EBACR1)

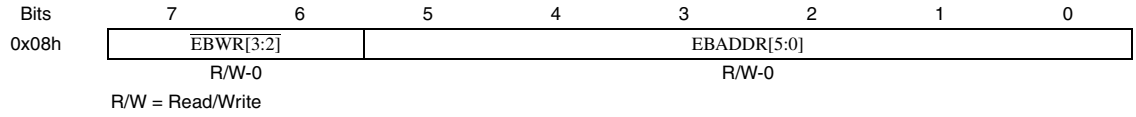


Table 5. EBM Address Control Register 1 (EBACR1) Field Descriptions

Bit	Name	Value	Description
7–6	$\overline{\text{EBWR}}$[3:2]		Write Enable
		0	The I/O signal is mapped to the mux output.
		1	The write enables are mapped to the mux output.
5–0	EBADDR[5:0]		Address Line
		0	The I/O signal is mapped to the mux output.
		1	The address lines 5–0 are mapped to the mux output.

4.4 EBM Data Control Register (EBDCR)

Figure 6 and Table 6 describe this register.

Figure 6. EBM Data Control Register (EBDCR)

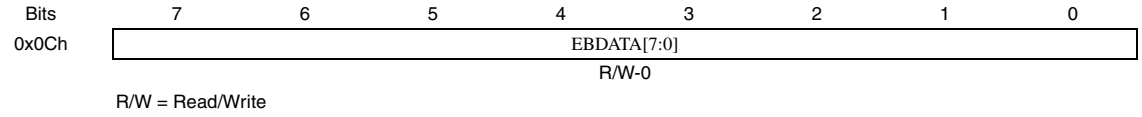


Table 6. EBM Data Control Register (EBDCR) Field Descriptions

Bit	Name	Value	Description
7–0	EBDATA[7:0]		Expansion Bus Data
		0	The I/O signal is mapped to the mux output.
		1	The data lines 7–0 are mapped to the mux output.

4.5 EBM Address/Data Control Register (EBADCR)

Figure 7 and Table 7 describe this register.

Figure 7. EBM Address/Data Control Register (EBADCR)

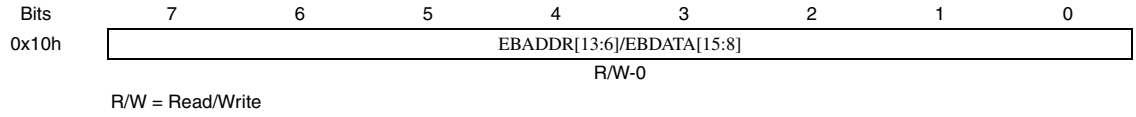


Table 7. EBM Address/Data Control Register (EBADCR) Field Descriptions

Bit	Name	Value	Description
7-0	EBADDR[13:6]/ EBDATA[15:8]		Address/Data
		0	*In both 8-bit and 16-bit modes:* The I/O signal is mapped to the mux output.
		1	*In 8-Bit Mode:* The address lines 13–6 are mapped to the mux output. *In 16-Bit Mode:* The data lines 15–8 are mapped to the mux output.

4.6 EBM Address Control Register 2 (EBACR2)

Figure 8 and Table 8 describe this register.

Figure 8. EBM Address Control Register 2 (EBACR2)

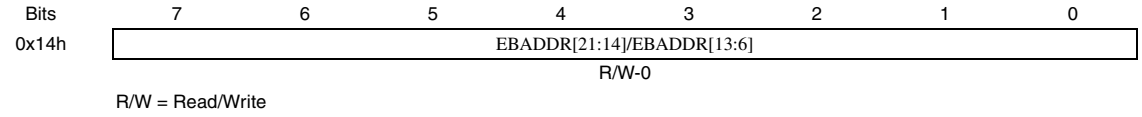


Table 8. EBM Address Control Register 2 (EBACR2) Field Descriptions

Bit	Name	Value	Description
7-0	EBADDR[21:14]/ EBADDR[13:6]		Address/Data
		0	*In both 8-bit and 16-bit modes:* The I/O signal is mapped to the mux output.
		1	*In 8-Bit Mode:* The address lines 21–14 are mapped to the mux output. *In 16-Bit Mode:* The address lines 13–6 are mapped to the mux output.

4.7 EBM Address Control Register 3 (EBACR3)

Figure 9 and Table 9 describe this register.

Figure 9. EBM Address Control Register 3 (EBACR3)

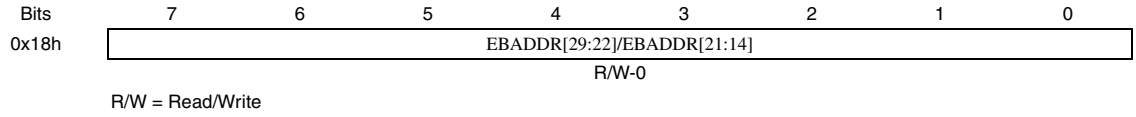


Table 9. EBM Address Control Register 3 (EBACR3) Field Descriptions

Bit	Name	Value	Description
7–0	EBADDR[29:22]/ EBADDR[21:14]		Address/Data
		0	*In both 8-bit and 16-bit modes:* The I/O signal is mapped to the mux output.
		1	*In 8-Bit Mode:* The address lines 29–22 are mapped to the mux output. *In 16-Bit Mode:* The address lines 21–14 are mapped to the mux output.

4.8 EBM Control Register 1 (EBMCR1)

Figure 10 and Table 10 describe the EBM control register 1.

Figure 10. EBM Control Register 1 (EBMCR1)

hex	7	6	5	4	3	2	1	0
0x1Ch	Reserved		0			DSIZE		LPM
	RW-0		R-0			RW-0		RW-0

R = Read, W = Write

Table 10. EBM Control Register 1 (EBMCR1) Bit Descriptions

Bit	Name	Value	Description
7–6	Reserved		Reads are zero and writes have no effect.
5–3	0	000	These bits are tied to 0 by default
2–1	DSIZE		Memory Interface Data Size
		00	8-bit data bus width
		01	16-bit data bus width
		10	Reserved
		11	Reserved
0	LPM		Local Power Down Mode
		0	Module is not locally powered down.
		1	Module is locally powered down.

5 Example for Interfacing 64k of External 16-Bit Memory

Only the setup of registers pertinent to the EBM are mentioned here. Assumptions:

- 64k of 16-bit memory is connected to chip select 5.
- Chip select 5 corresponds to MCBAHR2/MCBALR2 and SMCR5.

To implement interfacing 64k of external 16-bit memory, follow these steps.

1) Configure system clock. For example:
```
GLBCTRL = 0x09;
```

2) Set the memory course base address registers (MCBAHRx, MCBALRx) for the chip select connected to the EBM memory or peripheral. Enable the memory map. For example:
```
MCBAHR2 = 0x0030; //EBM RAM base addr at 0x00300000
MCBALR2 = 0x0020; //Size of 64k
MFBALR0 = 0x0100; //Enable the memory map
```

3) In the SMCR register, set the memory location as “external” and set the wait states, if needed. For example:
```
SMCR5 = 0x35; //16-bit data width/External/Big Endian/3 wait
states
```

   For expansion bus clock and wait states information, please refer to SPNU189. Please refer to the specific device data sheet for expansion bus timing information.

Note: Slow Memory

For interfaces to slow **memory,** allow the wait states to be generated by the CPU. The wait state generation is configured in the SMCR register.

Note: Slow Peripherals

For optimum performance when interfacing to slow **peripherals**, reads need to be accompanied by an $\overline{\text{EBHOLD}}$ signal from the peripheral to generate the wait states. However, if the peripheral cannot generate $\overline{\text{EBHOLD}}$, and it is not possible to do so with an external programmable logic device, then allow the wait state generation to be handled by the CPU, as is the case when interfacing to memories.

4) Configure peripheral ICLK. For example:

```
PCR = 0x02;
```

For expansion bus clock and wait states information, please refer to SPNU189.

5) Release peripheral reset. For example:

```
PCR |= 0x01; // Enable Peripherals
```

6) Set the EBM address, data and control lines that are required in the application in the EBM control registers. Configure the data bus bit width in EBMCR1. For example:

```
EBDMACR = 0x01;
EBRWCR  = 0x0F;
EBACR1  = 0x3F;
EBDCR   = 0xFF;
EBADCR  = 0xFF;
EBACR2  = 0xFF;
EBACR3  = 0x07;
EBMCR1  = 0x02;
```

7) (If needed) Set up the DMA registers for the DMA channel(s) that the expansion bus DMA request line(s) (EBDMAREQx) maps to.