TMS470R1Vx Microcontroller Peripherals Overview Reference Guide

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Read This First

About This Manual

This brief document provides an overview of the peripherals available in the TMS470R1Vx family of devices. Each peripheral is described, and a table is provided to show the peripherals available for each device.

Related Documentation From Texas Instruments

For additional information on the TMS470R1Vx devices or their peripherals, click on a device or peripheral name within the table to open a PDF of the related data sheet or peripheral reference guide.

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TMS470R1Vx 16/32-Bit RISC F05 Microcontroller Peripherals

The TMS470R1Vx generation of devices has been developed with the 16/32–bit ARM7TDMI™ (Thumb®) core licensed by Texas Instruments (TI) from Advanced RISC Machines (ARM®). A standard in the industry, the ARM7TDMI design is noted for its code density and low power consumption.

The TMS470R1Vx devices have been embedded with Flash memory and intelligent peripherals for integrated systems, including HET (timing coprocessor), Analog-to-Digital Converter (ADC), CAN controllers, a watchdog, and serial interfaces. These user-accessible peripherals are configured using a set of memory-mapped control registers.

This document provides an overview and briefly describes the peripherals of the TMS470R1Vx devices.

1 Class II Serial Interface A (C2SIa)

The Class II Serial Interface A (C2SIa) is a communication module used for transmitting and receiving data over a multi-master network. The C2SIa module is the interface from the digital logic of the TMS470R1Vx generation of microcontrollers to an external analog interface chip. This implementation is equipped with some enhancements for supporting transmit errors, breaks and calibration.

2 Class II Serial Interface B(C2SIb)

The Class II Serial Interface B (C2SIb) is a communication module used for transmitting and receiving data over a multi-master network. The C2SIb module is the interface from the digital logic of the TMS470R1Vx generation of microcontrollers to an external analog interface chip. This implementation is equipped like C2SIa, with some additional enhancements to the transmit and receive buffers, the transmit byte counter, and the status register.

3 Controller Area Network (CAN)

The Controller Area Network (CAN) uses established protocol to communicate serially with other controllers in harsh environments. The CAN documentation covers both the Standard CAN Controller (SCC) and the High-End CAN Controller (HECC).

4 Clock Divider Module (CDM)

The Clock Divider Module (CDM) provides ACLK to the clock control module (CCM), located in the System Module. The CCM subsequently provides SYSCLK and ICLK for all other TMS470 modules.

5 Direct Memory Access (DMA) Controller

The Direct Memory Access (DMA) controller transfers data between address ranges in the memory map without intervention by the CPU, maximizing system performance.

6 TMS470R1x DSP Interface

This interface between the TMS470R1x system and the TMS320C54x Mega-Module is comprised of an API RAM, API Wrapper (APIW), a Virtual Channel Interface (VCI), and a shared DMA controller.

7   Expansion Bus Module (EBM)

The Expansion Bus Module (EBM) is a stand-alone module providing bondout for both general-purpose input/output (GIO) pins and expansion bus interface pins. EBM supports the multiplexing of the GIO functions and the expansion bus interface. When the GIO functions are not used, the EBM can be used to interface 8- or 16-bit memories.

8   External Clock Prescaler (ECP)

The External Clock Prescaler (ECP) provides the TMS470R1x generation of devices with an external output clock (ECLK).

9   Event Manager (EVM)

The Event Manager Lite (EVM) is a timer specialized for digital motor control. It is a peripheral designed for the LF24xx DSP family and its native interface is to a RHEA bus. This document describes a bridge between the TMS470R1x SAR expansion bus peripheral interface protocol and the Event Manager Lite.

10   Flash Memory (F05 Flash)

The Flash Electrically Erasable Programmable Read Only Memory (Flash EEPROM or Flash) module is a type of nonvolatile memory which has fast read time, but slower write/erase times. In addition, erasing is performed in bulk (by sector) rather than one word at a time, as in regular EEPROM.

11   Frequency-Modulated Phase-Locked Loop Clock (FMPLL)

The Frequency-Modulated Phase-Locked Loop (FMPLL) clock module synthesizes the continuous clock, ACLK, from an external resonator/crystal reference. The frequency can be modulated in order to reduce the electromagnetic emissions from the clock capacitance. The FMPLL allows the application to use a lower frequency external crystal/oscillator.

12   General-Purpose Input/Output (GIO)

The General-Purpose Input/Output (GIO) module provides a dedicated set of general-purpose input/output signals to the TMS470R1x device. The I/O pins are bidirectional and bit-programmable.

13   High-End Timer (HET)

The High-End Timer (HET) is a software-controlled timer with a dedicated specialized timer micromachine and a set of twenty-one instructions. The HET micromachine is connected to a port of I/O pins.

14   Hardware Angle Generator (HWAG)

The Hardware Angle Generator (HWAG) generates angle value from toothed wheels, allowing the microcontroller to generate signals at precise engine angles. The HWAG could also be used as a complement of the High‑End Timer (HET) to generate complex angle-angle or angle-time waveforms.

15   Inter-Integrated Circuit (I2C)

The Inter-Integrated Circuit (I2C) module is a multi-master communication module providing an interface between the Texas Instruments TMS470 microcontroller and an I2C-compatible device via the I2C serial bus. This module will support any slave or master I2C-compatible device.

16   Interrupt Expansion Module (IEM)

The Interrupt Expansion Module (IEM) works with the Central Interrupt Module (CIM) to extend the TMS470R1x system to support up to 64 interrupt sources and provide programmable‑interrupt priorities.

17   Multi-Buffered Analog-to-Digital Converter (MibADC)

The Multi-Buffered Analog-to-Digital Converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value. The MibADC can function in two modes: compatibility mode or buffered mode. In addition, the MibADC includes improvement in the event-triggering capabilities over the TMS470R1x ADC module.

18   Multi-Buffered Serial Peripheral Interface (MibSPI)

The Multi-Buffered Serial Peripheral Interface (MibSPI) is a highspeed, synchronous input/output port that allows a serial bit stream of programmed length to be shifted into and out of the device at a programmed bittransfer rate. Its multiple buffers allow multiple transmissions with different peripherals without any CPU action.

19 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals utilizing the standard Non-Return-to-Zero (NRZ) format.

20 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) provides a convenient method of serial interaction for high-speed communication between similar shift-register type devices.

21 Spread-Spectrum Phase-Locked Loop Clock (SSPLL)

The Spread-Spectrum Phase-Locked Loop (SSPLL) clock module synthesizes the continuous clock, ACLK, from an external resonator/crystal reference. ACLK goes to the system control module (CCM), which generates the global system clock (SYSCLK). When enabled, the Spread-Spectrum mode modulates the system clock frequency and it intended to spread out the RF energy emitted from the device.

22 System

The System module provides an interface from the ARM CPU to the TI TMS470R1x generation of devices. The module defines the CPU bus and the expansion bus. The system module is responsible for memory interface and protection, interrupt prioritization, reset generation, and clock synthesis.

23 Zero-Pin Phase-Locked Loop Clock (ZPLL)

The Zero-Pin Phase-Locked Loop (ZPLL) clock module synthesizes the continuous clock, ACLK, from an external resonator/crystal reference. ACLK goes to the system control module (CCM), which generates the global system clock (SYSCLK). It is called *zero-pin* because the internal PLL does not require any pins for an external filter circuit.