Application Report
SPRAAU2A–April 2008–Revised October 2009

TMS320C6472/TMS320TCI6486 EMAC Implementation Guide

Thomas Johnson, Yanmin Wu — *Digital Signal Processing Solutions*

ABSTRACT

The TMS320TCI6486/TMS320C6472 device contains two independent Ethernet MAC modules, EMAC0 and EMAC1, and a shared MDIO controller. This document describes system implementation details of the EMAC and MDIO modules on TCI6486/C6472 device. For a detailed functional description of the EMAC/MDIO modules such as architecture and operation as well as register definitions, see the *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (SPRUEF8). For AC timings and register offsets, see the *TMS320TCI6486 Communications Infrastructure Digital Signal Processor* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). This document includes some overlapped information from both the user's guide and the data manual that is important for system integration. If the overlapped information does not match, the data manual information takes precedence.

Contents

List of Figures

List of Tables

1 Related Documentation

Specific examples of the implementation of this specification including schematics and a PCB layout can be obtained from the TCI6486/C6472 EVM documentation. In addition, the interested reader may refer to the *High-Speed DSP Systems Design Reference Guide* (SPRU889) and the *High-Speed Layout Guidelines* application report (SCAA082).

For configuration of the EMAC interface, see the *TMS320C6472/TMS320TCI6486 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module User's Guide* (SPRUEF8).

2 Abbreviations

DSP — Digital Signal Processor

GMII — Gigabit Media Independent Interface

MAC — Media Access Control

MII — Media Independent Interface

RGMII — Reduced Gigabit Media Independent Interface

RMII — Reduced Media Independent Interface

S3MII — Source-Synchronous Serial Independent Interface

Rx — Receive

Tx — Transmit

3 EMAC Interface Configuration

Both EMAC ports on the TCI6486/C6472 device and the MDIO interface can be configured to use HSTL levels and be compatible with RGMII v2.0. Alternately, these modules can be configured to use separate pins that support 3.3-V LVCMOS I/O through the interface modes GMII, MII, RMII, or S3MII.

Only one mode can be used at a time for each EMAC port. The mode used is selected at device reset based on the MACSEL0[2:0] and MACSEL1[1:0] configuration pins. EMAC1_EN is an input pin that is used to disable/enable EMAC1 during reset on TCI6486/C6472. The enable/disable of EMAC1 can also be controlled by software updating the EMAC1_EN bit of the DEVCTL register after power-up. For more detailed information regarding the DEVCTL register, see the *TMS320TCI6486 Communications Infrastructure Digital Signal Processor* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). Table 1 lists EMAC interface selection on the TCI6486/C6472 device.

Table 1. MACSEL Configuration Inputs

MACSEL0[2:0]	EMAC0 Interface	IPU/IPD	I/O
000	MII	IPU	LVCMOS
001	RMII	IPU	LVCMOS
010	GMII	IPD	LVCMOS
011	RGMII	IPD	HSTL
100	Reserved	IPD	
101	SS-SMII (SS mode)	IPD	LVCMOS
110	Reserved	IPD	
111	Disabled	IPD	
MACSEL1[1:0]	**EMAC1 Interface**	**IPU/IPD**	**I/O**
00	Reserved	IPD	
01	SS-SMII (SS mode)	IPD	LVCMOS
10	RGMII	IPD	HSTL
11	RMII	IPD	LVCMOS
EMAC1_EN	IPU/IPD enable/disable and output buffer disable/enable on EMAC1	IPD	

Because some of these pins are shared, not all combinations are valid. To see how these pins are shared, see the *TMS320TCI6486 Communications Infrastructure Digital Signal Processor* data manual (SPRS300), the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612), or Section 5 in this document.

The RGMII interface HSTL buffers can either be operated at 1.5 V or 1.8 V. This is done by powering the DV_{DD15} supply at either 1.5 V or 1.8 V. Operation at either of these voltages uses the same AC timings. 1.8-V operation consumes slightly more power than 1.5 V but eliminates the need for provision of a separate 1.5-V supply. $V_{REFHSTL}$ is generated using a resistor divider from DV_{DD15} and, therefore, scales accordingly.

All LVCMOS EMAC pins contain internal pull-up or pull-down resistors. Signals that are not used can be left not connected. For unused RGMII signals, these can be left floating if DV_{DD15} and $V_{REFHSTL}$ are connected to GND or left not connected. Alternately, if these supplies are powered, the unused RGMII input pins should be pulled to ground.

4 MDIO Interface Configuration

There are two sets of MDIO interfaces (LVCMOS and HSTL). The selection follows that for EMAC0. If EMAC0 is configured for RGMII mode, then the MDIO controller uses its HSTL pins. Otherwise, it uses its LVCMOS pins. Table 2 lists the pins associated with MDIO interfaces.

Table 2. MDIO Port Signals

Name	I/O	Description
RGMDCLK	O	RGMII (HSTL) Management Clock
RGMDIO	I/O	RGMII (HSTL) Management Data
GMDCLK	O	GMII/RMII/S3MII (LVCMOS) Management Clock
GMDIO	I/O	GMII/RMII/S3MII (LVCMOS) Management Data

Note that since the MDIO interface used is based on the configuration of EMAC0, you may have to use level translators in order to connect the management interface to different devices. For example, if EMAC0 is configured for RGMII and EMAC1 is configured for RMII, the RGMDCLK/RGMDIO pins are used for the management interface and it likely occurs that these HSTL pins need to be level-translated to interface to the RMII device. For the recommendations regarding the level-translation, see Section 9.3.3.

5 EMAC/MDIO Multiplexed Pins

Table 3 lists EMAC/MDIO multiplexed pins.

Table 3. EMAC/MDIO Multiplexed Pins

Pin Number	Signal Name	MII0	GMII0	RMII0	RMII1	S3MII0	S3MII1
AH11	MRXD00/RMRXD00/SRXD0	MRXD00	MRXD00	RMRXD00		SRXD0	
AG12	MRXD01/RMRXD01/SRXSYNC0	MRXD01	MRXD01	RMRXD01		SRXSYNC0	
AJ11	MRXD02/SRXD1	MRXD02	MRXD02				SRXD1
AG10	MRCLK0/SRXCLK1	MRCLK0	MRCLK0				SRXCLK1
AJ10	MRXD03/SRXSYNC1	MRXD03	MRXD03				SRXSYNC1
AH9	MRXD04/RMRXD10		MRXD04		RMRXD10		
AG7	MRXD05/RMRXD11		MRXD05		RMRXD11		
AJ13	MRXD06/RMRXER1		MRXD06		RMRXER1		
AJ6	MRXD07		MRXD07				
AE12	MRXDV0/RMCRSDV1	MRXDV0	MRXDV0		RMCRSDV1		
AF12	MRXER0/RMRXER0/SRXCLK0	MRXER0	MRXER0	RMRXER0		SRXCLK0	
AF10	MCRS0/RMCRSDV0	MCRS0	MCRS0	RMCRSDV0			
AG6	GMTCLK0/REFCLK1/SREFCLK1		GMTCLK0		REFCLK1		SREFCLK1
AJ9	MTCLK0/REFCLK0/SREFCLK0	MTCLK0	MTCLK0	REFCLK0		SREFCLK0	
AF8	MTXD00/RMTXD00/STXD0	MTXD00	MTXD00	RMTXD00		STXD0	
AH7	MTXD01/RMTXD01/STXSYNC0	MTXD01	MTXD01	RMTXD01		STXSYNC0	
AG8	MTXD02/STXD1	MTXD02	MTXD02				STXD1
AF9	MTXD03/STXSYNC1	MTXD03	MTXD03				STXSYNC1
AE7	MTXD04/RMTXD10/STXCLK1		MTXD04		RMTXD10		STXCLK1
AJ7	MTXD05/RMTXD11		MTXD05		RMTXD11		
AE11	MTXD06/RMTXEN1		MTXD06		RMTXEN1		
AG11	MTXD07/STXCLK0		MTXD07			STXCLK0	
AF11	MTXEN0/RMTXEN0	MTXEN0	MTXEN0	RMTXEN0			
AE8	MCOL0	MCOL0	MCOL0				
AH10	GMDIO	GMDIO	GMDIO				
AG9	GMDCLK	GMDCLK	GMDCLK				

6 Decoding EMAC Modes

Table 4 explains the decoding of MACSEL0[2:0], MACSEL1[1:0], and EMAC1_EN bits of the DEVCTL register to decide which interfaces are enabled and which are disabled. Only use the valid combinations of MACSEL0[2:0], MACSEL1[1:0], and EMAC1_EN listed in this table. Use of setting combinations not listed in this table will result in undefined operation.

Table 4. EMAC Decoding

MACSEL02	MACSEL01	MACSEL00	MACSEL11	MACSEL10	EMAC1_EN	EMAC0	EMAC1
0	0	0	X	X	0	MII	None
0	0	0	0	X	1	MII	None
0	0	0	1	0	1	MII	RGMII
0	1	0	X	X	0	GMII	None
0	1	0	0	X	1	GMII	None
0	1	0	1	0	1	GMII	RGMII
0	0	1	X	X	0	RMII	None
0	0	1	0	1	1	RMII	S3MII
0	0	1	1	0	1	RMII	RGMII
0	0	1	1	1	1	RMII	RMII
0	1	1	X	X	0	RGMII	None
0	1	1	0	1	1	RGMII	S3MII
0	1	1	1	0	1	RGMII	RGMII
0	1	1	1	1	1	RGMII	RMII
1	0	1	X	X	0	S3MII	None
1	0	1	0	1	1	S3MII	S3MII
1	0	1	1	0	1	S3MII	RGMII
1	0	1	1	1	1	S3MII	RMII
1	1	1	X	X	0	None	None
1	1	1	0	1	1	None	S3MII
1	1	1	1	0	1	None	RGMII
1	1	1	1	1	1	None	RMII

7 EMAC Boot Configuration

The TCI6486/C6472 device supports a bootloading process through the Ethernet. After $\overline{\text{POR}}$ and $\overline{\text{RESET}}$ asserted resets, the boot controller on the TCI6486/C6472 device selects the boot mode based on the status of the BOOTMODE[3:0] pins. The Ethernet boot modes will not operate in gigabit mode unless the core clock is running faster than 375 MHz. Packet errors will occur if this requirement is not met. This will occur if using EMAC boot mode over GMII or RGMII and CFGGP[4] = 0 when CLKIN1 <37.5 MHz or regardless of CFGGP[4] setting with the CLKIN1 rate <18.75 MHz. Table 5 lists different EMAC boot configurations.

Table 5. EMAC Boot Configuration Inputs

BOOTMODE[3:0]	Description	Type	CFGGP[4:0]
1001	Ethernet MAC0 Boot (mode and speed determined by MACSEL0 pins, see table 1)	ROM	CFGGP[4] = 0, PLLx10 mode of main PLLCTL CFGGP[4] = 1, PLLx20 mode of main PLLCTL CFGGP [3:0]: Device ID (when RMII is selected, CFGGP [3] controls speed; 1 for 100 Mbps, 0 for 10 Mbps and Device ID[3] is 0.)
1010	Ethernet MAC1 Boot (mode and speed determined by MACSEL1 pins, see table 1)	ROM	CFGGP[4] = 0, PLLx10 mode of main PLLCTL CFGGP[4] = 1, PLLx20 mode of main PLLCTL CFGGP [3:0]: Device ID (when RMII is selected, CFGGP [3] controls speed; 1 for 100 Mbps, 0 for 10 Mbps and Device ID[3] is 0.)

NOTE: When a system reset occurs, the boot mode used is determined by the BOOTMODE field in the DEVSTAT register (the CFGGP pins are not re-sampled). For a summary of the boot modes supported see the *TMS320TCI6486 Communications Infrastructure Digital Signal Processor* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612). For details regarding boot modes, see the *TMS320TCI648x Bootloader User's Guide* (SPRUEA7) or the *TMS320C645x/C647x Bootloader User's Guide* (SPRUEC6).

8 Clock for EMAC

All EMAC modules and interfaces require that PLL2 be enabled and that the input clock at CLKIN2 be 25 MHz. Otherwise, operation is undefined.

The CLKIN2 input contains an internal pull-down resistor and it can be left not connected if EMAC is not needed.

8.1 Clock PLL and PLL Controller

A description of PLL2 and its PLL Controller along with register definitions can be found in the *TMS320TCI6486 Communications Infrastructure Digital Signal Processor* data manual (SPRS300) or the *TMS320C6472 Fixed-Point Digital Signal Processor* data manual (SPRS612) and in the *TMS320C6472/TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller User's Guide* (SPRU806).

8.2 Clock2 Requirement

For details on a few solutions for designing a reference clock for CLKIN2, see the *TMS320C6472/TMS320TCI6486 Hardware Design Guide* application report (SPRAAQ4).

9 Connections

This section describes the interfacing of one or multiple TCI6486/C6472 DSPs to Ethernet PHYs and switches using the various Ethernet interfaces available in the TCI6486/C6472 device. For termination, follow the switch/PHY recommendations. If none are provided, it is recommended to use series resistance terminations on the clock lines and, optionally, on the data lines. Typical values of 22 Ω or 33 Ω are normally adequate, but IBIS simulations can be used to choose the best value for a specific board implementation.

9.1 GMII/MII

The GMII/MII interface on the TCI6486/C6472 device is compliant with the IEEE Std. 802.3. The standard-related documents can be downloaded or purchased through the following website: http://www.ieee802.org/3/purchase/index.html.

The TCI6486/C6472 DSP has one GMII/MII Ethernet port available via EMAC0. Table 6 lists the pins associated with the GMII/MII port.

The TCI6486/C6472 GMII/MII port does not implement the optional transmit error signal. The GMII/MII pins use +3.3-V I/O. Note that the clock rates for this interface are 125 MHz for 1000Base-T, 25 MHz for 100Base-T, and 2.5 MHz for 10Base-T. The I/O column is with reference to the TCI6486/C6472 (MAC).

Table 6. TCI6486/C6472 GMII/MII Port Signals

Name	I/O	Description
GMTCLK	O	GMII Transmit Clock (125 MHz)
MTCLK	I	MII Transmit Clock (25 MHz/2.5 MHz)
MTXEN	O	GMII/MII Transmit Enable
MTXD[7:0]	O	GMII/MII Transmit Data; MTXD[7:0] used for GMII mode; MTXD[3:0] used for MII mode
MRCLK	I	GMII/MII Receive Clock (125 MHz/25 MHz/2.5 MHz)
MRXDV	I	GMII/MII Receive Data Valid
MRXER	I	GMII/MII Receive Error
MRXD[7:0]	I	GMII/MII Receive Data; MRXD[7:0] used for GMII mode; MRXD[3:0] used for MII mode
MCRS	I	GMII/MII Carrier Sense
MCOL	I	GMII/MII Collision

The TCI6486/C6472 GMII/MII pins are multiplexed with other 3.3-V EMAC interface signals. When using the GMII/MII port on EMAC0, the EMAC1 Ethernet interfaces not available due to pin multiplexing are RMII1 and S3MII1. The RGMII1 port is the only available EMAC1 Ethernet interface when using the GMII/MII port on EMAC0.

9.1.1 GMII/MII PHY Connectivity

Figure 1 shows representative connectivity of the TCI6486/C6472 GMII/MII port to a single GMII/MII PHY. This interface is a typical MAC-to-PHY connection and uses +3.3-V I/O.

If only MII is desired, the unused data nibble (TXD[7:4]) pins should be pulled down via resistors at the PHY to avoid floating inputs. The TCI6486/C6472 has internal resistors to keep the MRXD[7:4] pins from floating in MII mode.

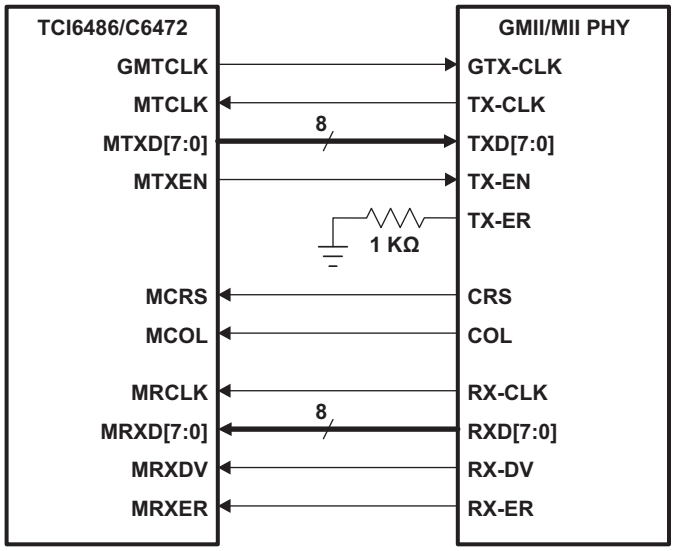

Figure 1. GMII/MII PHY Connectivity Diagram

9.1.2 GMII/MII Switch Connectivity

Because of the clocking differences associated with GMII vs. MII, the switch connectivity for these interfaces will be described separately in the following sections.

9.1.2.1 GMII Switch Connectivity

Figure 2 shows representative connectivity of TCI6486/C6472 GMII ports to an Ethernet switch. This interface is a MAC-to-MAC connection and uses +3.3-V I/O. As such, the carrier sense and collision signals are not necessary since full-duplex operation is forced. Also, since this is strictly a GMII connection, the TCI6486/C6472 MTCLK for MII modes is not needed.

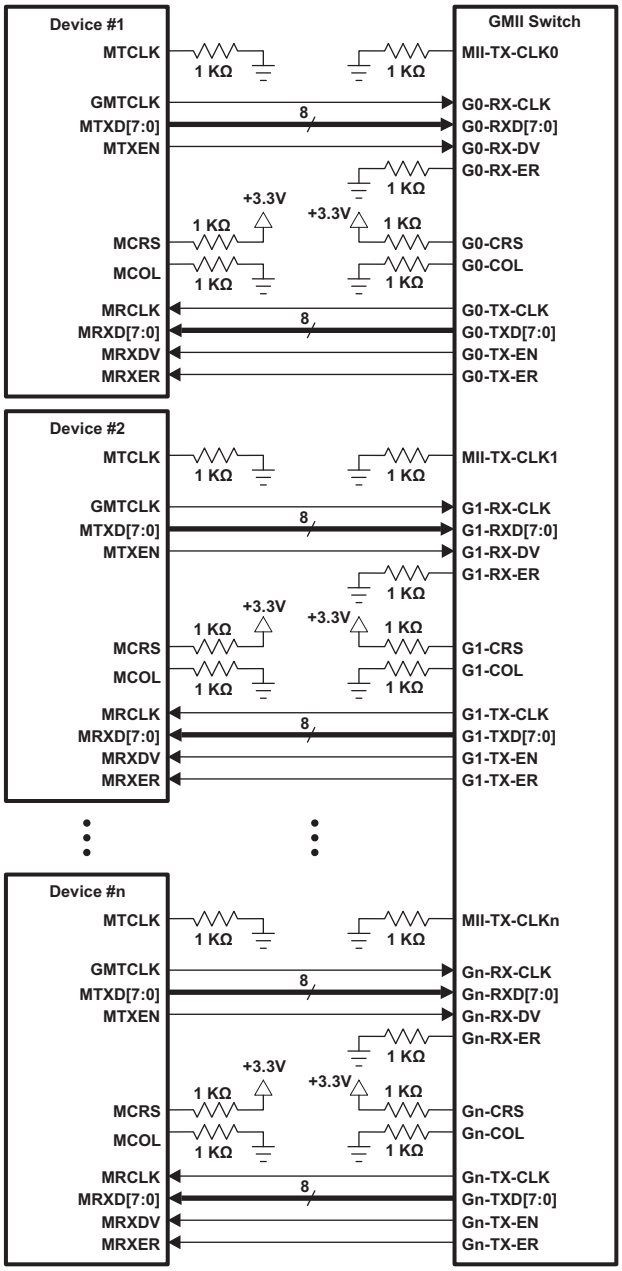

Figure 2. GMII Switch Connectivity Diagram

9.1.2.2 MII Switch Connectivity

The MII interface expects to receive MTCLK and MRCLK as inputs. This is the standard configuration for connecting directly to a PHY. When implementing the MII interface with an Ethernet switch, the one chosen must be configurable such that it can drive both clocks as outputs.

Figure 3 shows representative connectivity of TCI6486/C6472 MII ports to an Ethernet Switch. This interface is a MAC-to-MAC connection and uses +3.3-V I/O. As such, the carrier sense and collision signals are not necessary since full-duplex operation is forced. Note that this connectivity assumes the switch has the ability to source the MII clocks (as a PHY would). Also, since this is strictly an MII connection, the TCI6486/C6472 GMTCLK for GMII modes is not needed.

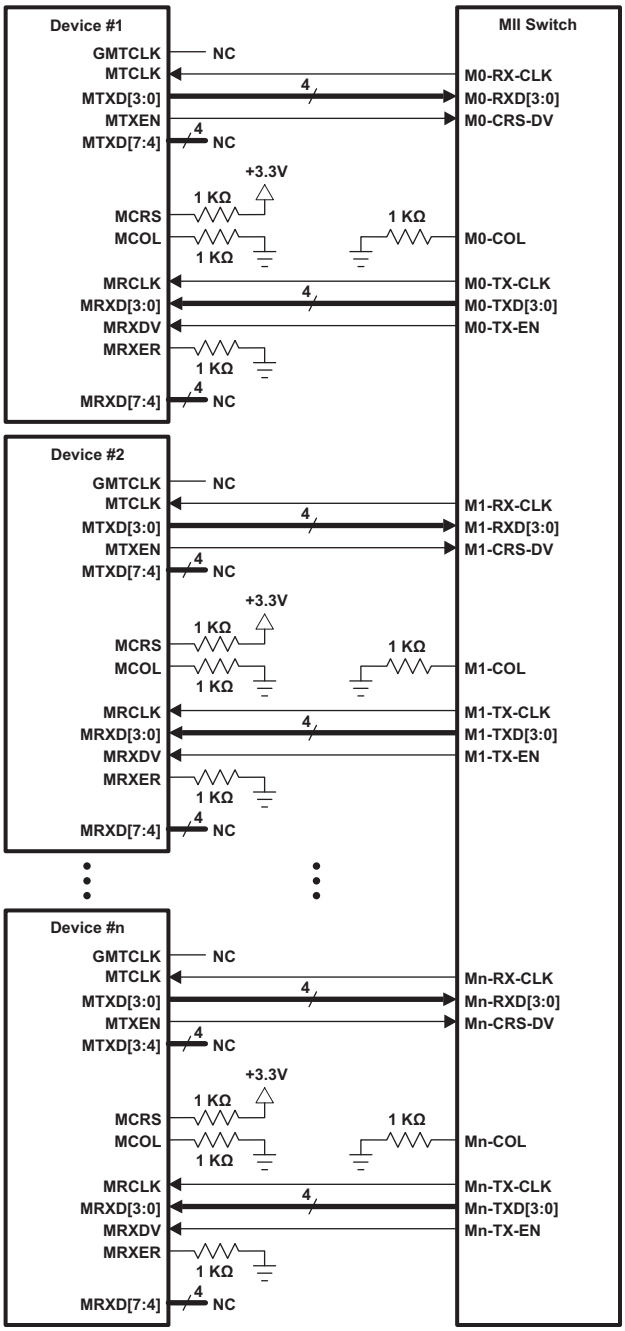

Figure 3. MII Switch Connectivity Diagram

9.2 RMII Interfaces

The RMII interfaces on the TCI6486/C6472 device are compliant with the RMII specification rev. 1.2 from the RMII Consortium in 1998. The specification can be found at the following link: www.national.com/appinfo/networks/files/rmii_1_2.pdf.

The TCI6486/C6472 RMII reference clock is an input. This allows the EMAC port to be connected to either a switch or a PHY. An external clock source should provide an aligned reference clock to the RMII reference clock input and to the RMII device connected to the other side of the interface. This clock should be provided to both RMII endpoints by a zero-delay clock buffer such as TI CDCV304 with matched-length clock traces.

The TCI6486/C6472 DSP has two RMII Ethernet ports available via EMAC0 and EMAC1. Table 7 lists the pins associated with an RMII port. The I/O column is with reference to the TCI6486/C6472 (MAC).

Table 7. TCI6486/C6472 RMII Port Signals

Name	I/O	Description
REFCLK	I	RMII Reference Clock (50 MHz)
RMTXEN	O	RMII Transmit Enable
RMTXD[1:0]	O	RMII Transmit Data
RMCRSDV	I	RMII Carrier Sense/Data Valid
RMRXER	I	RMII Receive Error
RMRXD[1:0]	I	RMII Receive Data

The RMII pins use +3.3-V I/O. The TCI6486/C6472 RMII pins are multiplexed with other non-RGMII pins. When using the RMII0 port on EMAC0, there are no restrictions on the available EMAC1 Ethernet interfaces (RMII1, S3MII1, and RGMII1 are useable). When using the RMII1 port on EMAC1, the EMAC0 Ethernet interfaces not available due to pin multiplexing are GMII0/MII0. The RMII0, S3MII0, and RGMII0 ports are available EMAC0 Ethernet interfaces when using the RMII1 port on EMAC1.

9.2.1 RMII PHY Connectivity

Figure 4 shows representative connectivity of a TCI6486/C6472 RMII port to an RMII PHY. This interface is a typical MAC-to-PHY connection and uses +3.3-V I/O.

The 50-MHz reference clock for the RMII interface must be externally sourced. This RMII PHY only has one RMII reference clock input, so if multiple RMII PHY ports are used, all TCI6486/C6472 RMII reference clocks must come from the same zero-delay clock buffer. A low-skew clock buffer may be used in place of the zero-delay clock buffer as long as the timing budget is acceptable.

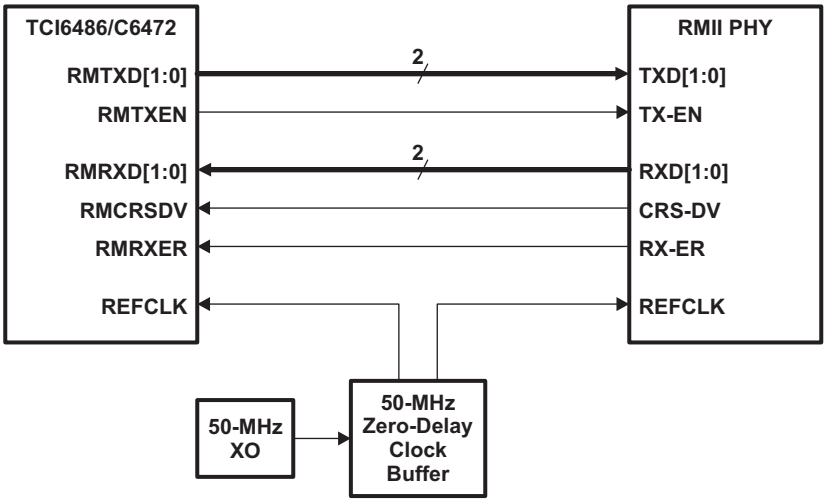

Figure 4. RMII PHY Connectivity Diagram

9.2.2 RMII Switch Connectivity

Figure 5 shows representative connectivity of TCI6486/C6472 RMII ports to an Ethernet switch. This interface is a MAC-to-MAC connection and uses +3.3-V I/O. As such, the receiver error signal is not necessary since full-duplex operation is forced. The 50-MHz reference clock for the RMII interface must be externally sourced. This RMII switch has only one RMII reference clock input.

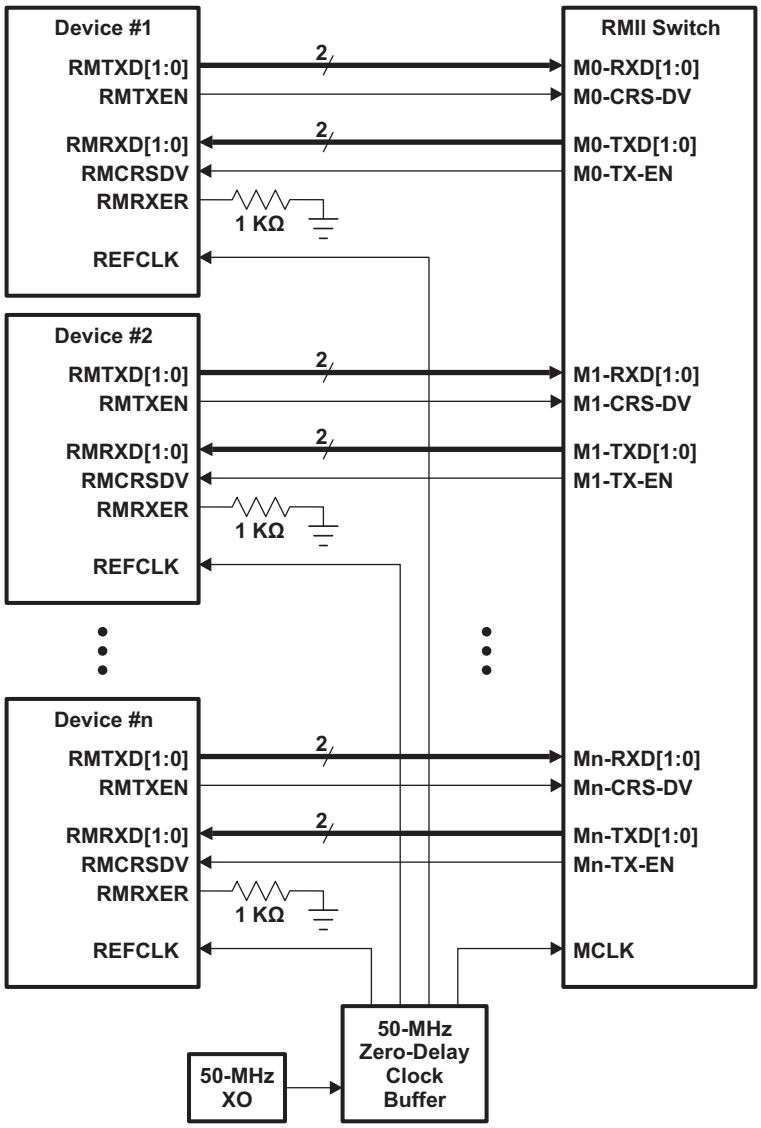

Figure 5. RMII Switch Connectivity Diagram

9.3 RGMII Interfaces

The RGMII interface on the TCI6486/C6472 device is compliant with the RGMII version 2.0 specification found at the following link: http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf.

The electrical signaling is compatible to JEDEC specification JESD8-6: http://www.jedec.org/download/search/jesd8-6.pdf.

Although the JEDEC specification specifically details 1.5-V HSTL signaling, the TCI6486/C6472 device and most other RGMII v2.0 devices also support operation at 1.8 V. Some devices support RGMII v1.3 (LVCMOS levels) but not RGMII v2.0 levels. An application report on how to perform voltage translation from the TCI6486/C6472 1.5-V/1.8-V interface to an LVCMOS 2.5-V/3.3-V interface that operates at gigabit speeds (125 MHz) is given in Appendix A.

The RGMII interface operates at 125 MHz and clocks data on both edges of the clocks. This connection should be routed with high-speed interface routing rules. The RGMII specification provides timing information at both the receiver and the transmitter. The user must verify that the timing variations due to board topology are not more than allowed by the RGMII specification. The TCI6486/C6472 HSTL IBIS models are provided to aid in this analysis. Also, the source-synchronous data traces should be routed along the same general path as the clock and control going in each direction. The data and control traces should be about the same length with a tolerance of about ±250 mils.

The TCI6486/C6472 device implements an internal delay (referred to as RGMII-ID in the RGMII specification) on the transmit signals but not on the receive signals. So, the connected device should use normal mode on the transmit side (no delay) and internal delay mode on the receive side. If the connected device does not support internal delay on the receive side, the proper delay needs to be created at the board level by routing the receive clock (RXC) signal longer than the receive data signals (RD[3:0]). The RGMII specification calls for this trace delay to be between 1.5 ns and 2.0 ns. Assuming a trace flight time of 170 ps/inch, the clock should be routed about 10.3 inches longer than the data and control. Flight time is dependent on board stackup and this length should be adjusted for the flight time of the specific board design.

The TCI6486/C6472 RGMII interface supports the optional in-band signaling defined in the v2.0 interface specification. It can automatically detect and adapt to the reported link status. The implementation also offers a feature to force the internal state of link status, link speed, and duplex, so that the in-band signaling is not required.

The TCI6486/C6472 DSP has two RGMII Ethernet ports available via EMAC0 and EMAC1. Table 8 lists the pins associated with an RGMII port. The I/O column is with reference to the TCI6486/C6472 (MAC).

Table 8. TCI6486/C6472 RGMII Port Signals

Name	I/O	Description
RGCLK	O	RGMII Reference Clock (125 MHz)
RGTXC	O	RGMII Transmit Clock (125 MHz/25 MHz/2.5 MHz)
RGTXCTL	O	RGMII Transmit Control
RGTD[3:0]	O	RGMII Transmit Data
RGRXC	I	RGMII Receive Clock (125 MHz/25 MHz/2.5 MHz)
RGRXCTL	I	RGMII Receive Control
RGRD[3:0]	I	RGMII Receive Data

The TCI6486/C6472 RGMII ports have optional RGCLK signals that can provide 125-MHz reference clocks. Note this is not a free running clock. It will not be present when the DSP is in reset or whenever PLL2 is disabled.

The TCI6486/C6472 RGMII pins are dedicated for this interface (i.e., they are not multiplexed with other interfaces). The RGMII pins are +1.5-V/+1.8-V HSTL I/O and require a +0.75-V/+0.90-V reference voltage on the $V_{REFHSTL}$ pin.

Note that the clock rates for this interface are 125 MHz for 1000Base-T, 25 MHz for 100Base-T, and 2.5 MHz for 10Base-T.

9.3.1 RGMII PHY Connectivity

Figure 6 shows representative connectivity of a TCI6486/C6472 RGMII port to an RGMII PHY. This interface is a typical MAC-to-PHY connection and uses +1.5-V/+1.8-V HSTL I/O. Note that unused input pins of the RGMII PHY should have pull-down resistors to avoid floating inputs.

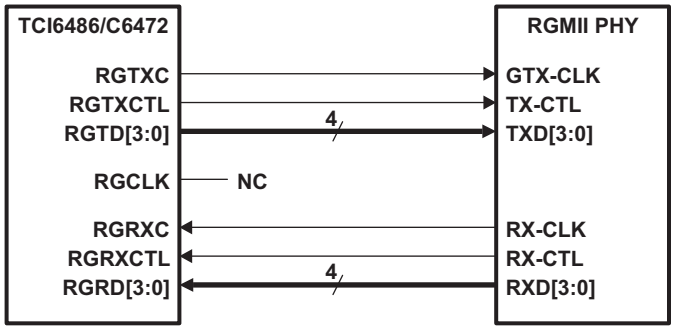

Figure 6. RGMII PHY Connectivity Diagram

9.3.2 RGMII Switch Connectivity

Figure 7 shows representative connectivity of TCI6486/C6472 RGMII ports to an Ethernet switch. Since most Gigabit Ethernet switches have SGMII interfaces, an RGMII PHY can be used to convert the RGMII interface into an SGMII interface. The TCI6486/C6472 to RGMII PHY is a MAC-to-PHY connection. The PHY to Ethernet switch is a MAC-to-MAC connection (transmit and receive pairs are crossed). The unused input pins of the RGMII PHY should have pull-down resistors to avoid floating inputs.

Note that the TCI6486/C6472 EVM board uses the SGMII-to-RGMII Ethernet PHY (88E1143) to convert from the DSPs' RGMII ports to the SGMII interfaces needed by the Gigabit Ethernet Switch. No Gigabit Ethernet Switches with RGMII ports could be located. Texas Instruments also provides an RGMII PHY that has been proven in this application. It is a 6-port RGMII Gigabit Ethernet PHY known as the TLK2226. For detailed information regarding the TLK2226, see the link:
http://focus.ti.com/docs/prod/folders/print/tlk2226.html.

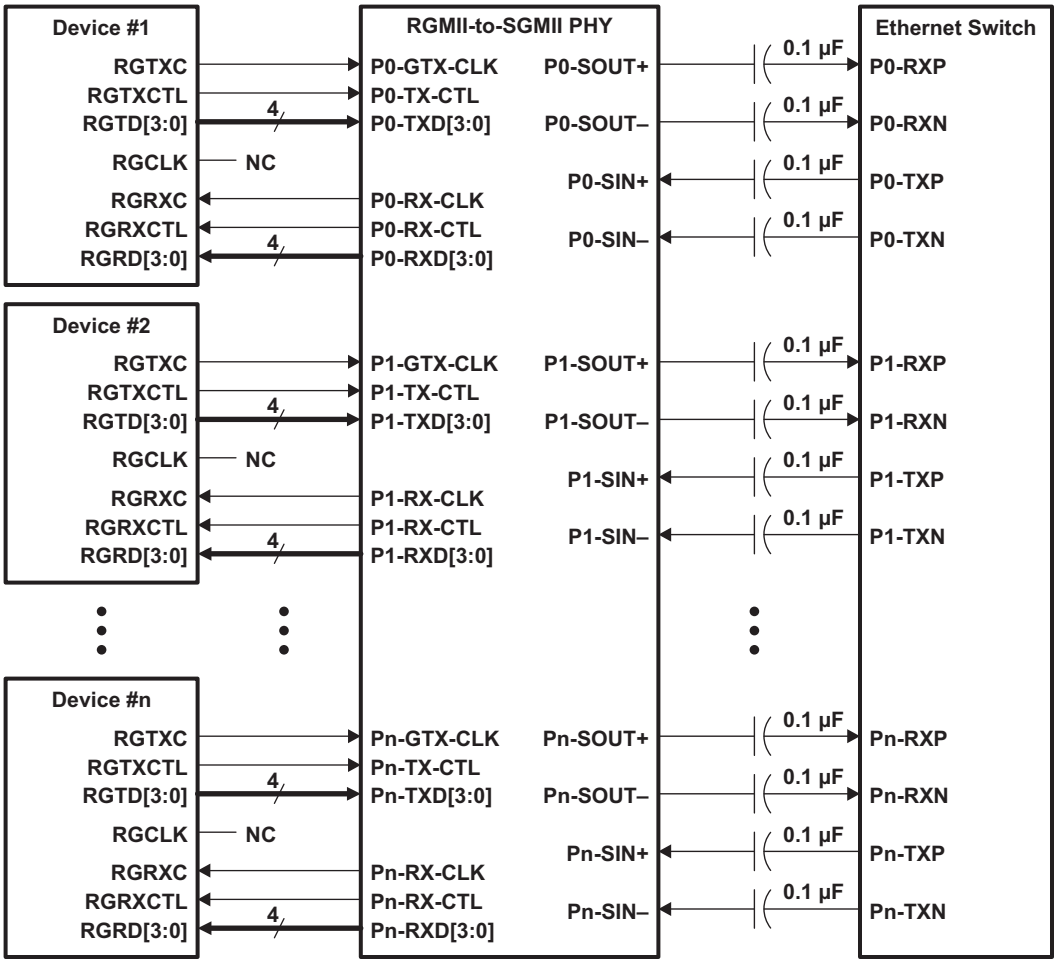

Figure 7. RGMII Switch Connectivity Diagram

9.3.3 HSTL MDIO-to-LVCMOS MDIO Translation Under RGMII Mode

Some RGMII v2.0 devices have the MDIO interface implemented as 2.5-V/3.3-V LVCMOS, even though its MAC interface pins are 1.5 V/1.8 V. If RGMII is selected on the TCI6486/C6472 device for EMAC0, only the HSTL MDIO interface is active. A circuit is needed to translate from 1.5 V/1.8 V to 2.5 V or 3.3 V. The circuit shown in Figure 8 has been tested for this purpose. For more information and additional voltage translation options, see the *Selecting the Right Level-Translation Solution* application report (SCEA035).

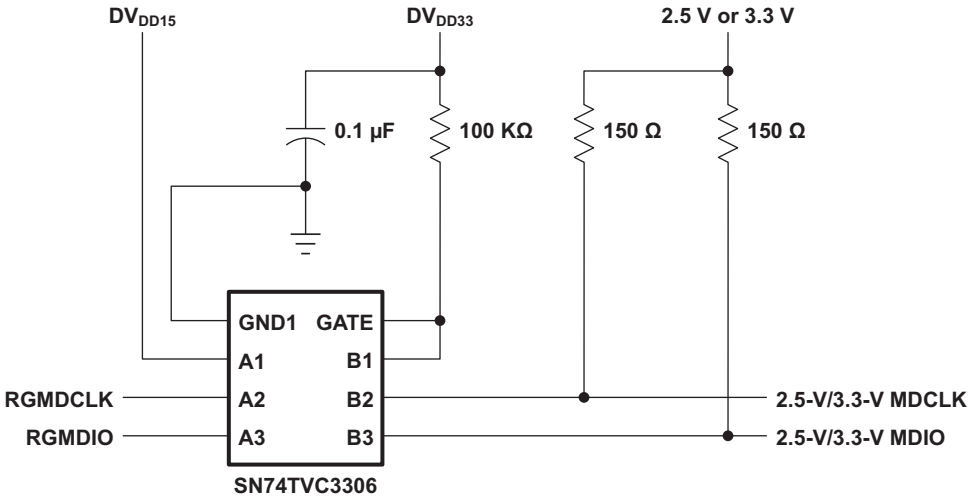

Figure 8. HSTL-to-LVCMOS Translation

9.4 S3MII Interfaces

The S3MII interface on the TCI6486/C6472 is compliant with Cisco's S3MII specification. The specification can be downloaded through the following website: www.angelfire.com/electronic2/sharads/protocols/MII_Protocols/smii.pdf.

S3MII is a source-synchronous interface with clock and sync timing propagated in both directions. It is designed for point-to-point implementations on a single board and also across a backplane. Because this interface operates at 125 MHz, trace routing and length must be controlled.

The TCI6486/C6472 DSP has two S3MII Ethernet ports available via EMAC0 and EMAC1. Table 9 lists the pins associated with an S3MII port. The I/O column is with reference to the TCI6486/C6472 (MAC).

Table 9. TCI6486/C6472 S3MII Port Signals

Name	I/O	Description
SREFCLK	I	S3MII Reference Clock (125 MHz)
STXCLK	O	S3MII Transmit Clock (125 MHz)
STXSYNC	O	S3MII Transmit Sync
STXD	O	S3MII Transmit Data
SRXD	I	S3MII Receive Data
SRXCLK	I	S3MII Receive Clock (125 MHz)
SRXSYNC	I	S3MII Receive Sync

The S3MII pins use +3.3-V I/O. The TCI6486/C6472 S3MII pins are multiplexed with other non-RGMII pins. When using the S3MII0 port on EMAC0, there are no restrictions on the available EMAC1 Ethernet interfaces (RMII1, S3MII1, and RGMII1 are useable). When using the S3MII1 port on EMAC1, the EMAC0 Ethernet interfaces not available due to pin multiplexing are GMII0/MII0. The RMII0, S3MII0, and RGMII0 ports are available EMAC0 Ethernet interfaces when using the S3MII1 port on EMAC1. Note that the internal design of the TCI6486/C6472 S3MII interface requires external logic in order to interface to PHYs and switches in multi-port configurations.

9.4.1 S3MII PHY Connectivity

Figure 9 shows representative connectivity of a TCI6486/C6472 S3MII port to an S3MII PHY. This interface is a typical MAC-to-PHY connection and uses +3.3-V I/O. Unused inputs on the PHY should not be left floating.

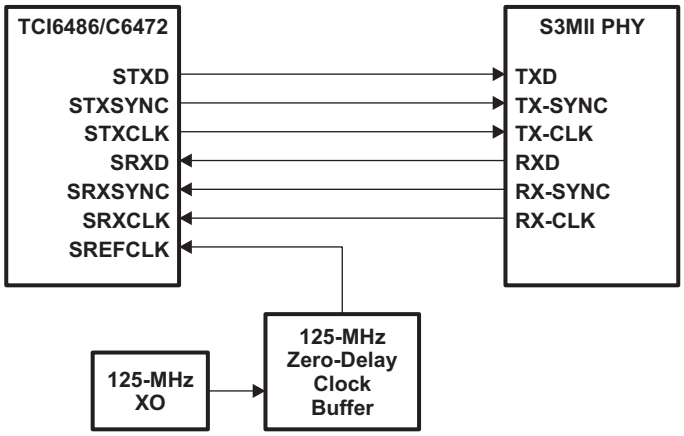

Figure 9. S3MII PHY Connectivity Diagram

Figure 10 shows the connectivity for a group of DSPs attached to a multi-port S3MII PHY. Note that the S3MII PHY only has one S3MII transmit clock input. Also note that external logic is necessary to support a multi-port PHY configuration. The external logic must synchronize the STXSYNC signals from the TCI6486/C6472 devices as the PHY has only one TX-SYNC for all ports. Also, the external logic must synchronize the STXD signals from the TCI6486/C6472 devices, since the clock phase relationship of the various TCI6486/C6472 devices can be different. The S3MII PHY sources the S3MII receive sync and receive clock to all the TCI6486/C6472 devices.

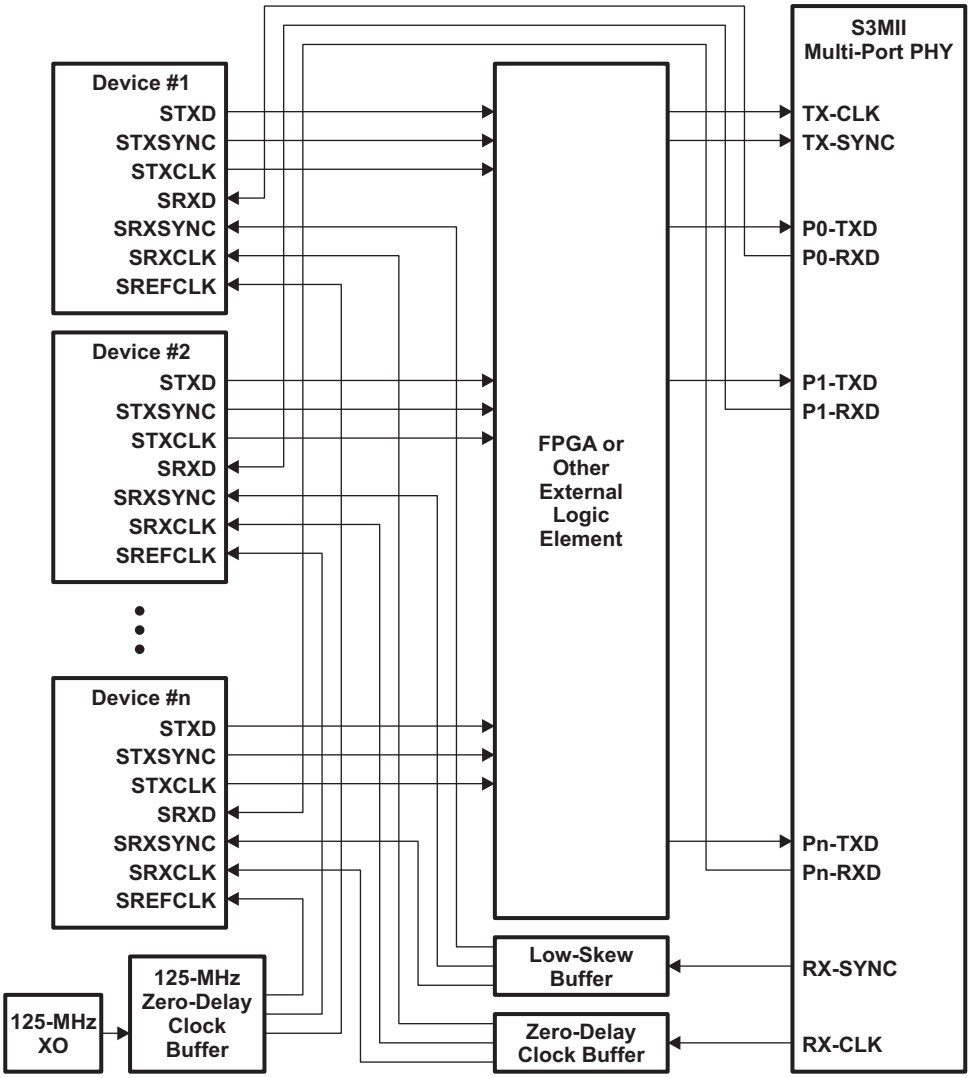

Figure 10. S3MII Multi-Port PHY Connectivity Diagram

9.4.2 S3MII Switch Connectivity

Figure 11 and Figure 12 show representative connectivity of TCI6486/C6472 S3MII ports to an Ethernet switch. This interface uses +3.3-V I/O. The 125-MHz transmit clock for the S3MII interface is sourced from the switch. The S3MII switch has only one S3MII transmit clock output.

Note that external logic is necessary to support a multi-port switch configuration. The external logic must synchronize the STXSYNC signals from the TCI6486/C6472 devices as the switch has only one TX-SYNC for all ports. Also, the external logic must synchronize the STXD signals from the TCI6486/C6472 devices, since the clock phase relationship of the various TCI6486/C6472 devices can be different.

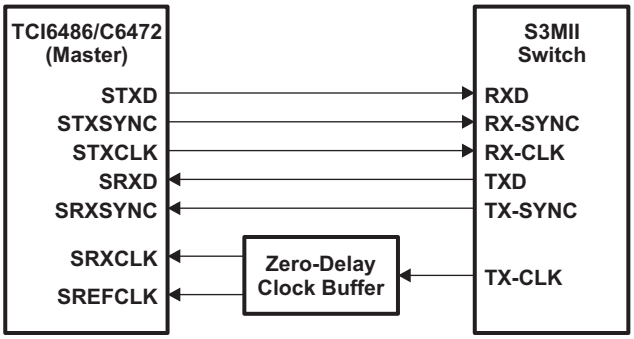

Figure 11. S3MII Switch Connectivity Diagram

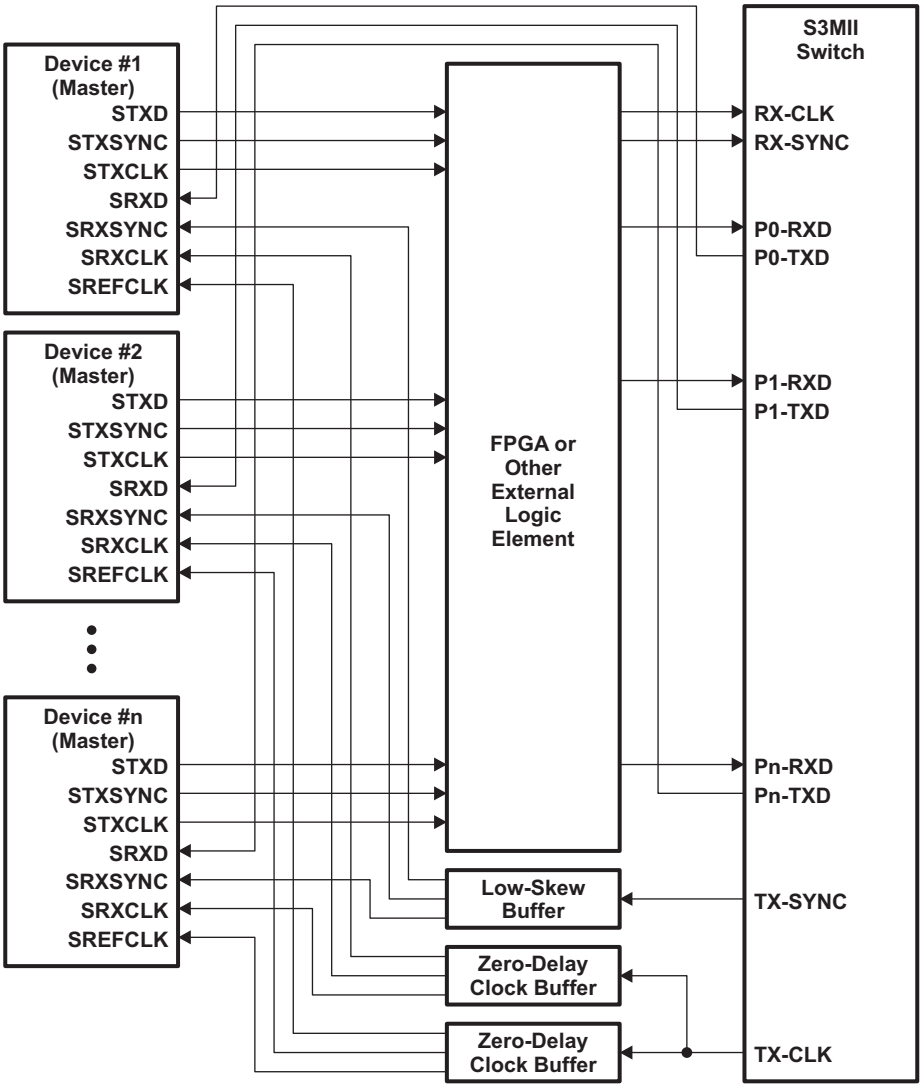

Figure 12. S3MII Multi-Switch Connectivity Diagram

10 Layout Recommendations

GMII, RGMII, and S3MII involve 125-MHz clock and data signals and their connections should be routed with high-speed interface routing rules.

Placements and terminations:

- The oscillator for generating the clock source should be placed close to the destination.
- Series termination resistors should be placed close to each clock source.
- The value of the series termination resistor should be optimized to reduce over-shoot and under-shoot while not violating the Trise/Tfall input specification. TI suggests the customer use IBIS simulations to determine the correct value of the termination resistor.

Trace routing:

- High-speed traces are created with impedance control.
- A solid ground reference plane should be under the clock traces.
- Digital signals should not be routed near or under the clock sources.
- At least 25 mil spacing or 3x as clock trace width spacing to other traces are recommended.
- Number of vias is minimized on high-speed traces and all EMAC signal traces are put into one signal plane.
- Number of vias on traces within a same net class should be the same.
- Trace length for high-speed signals is minimized, except intentional delay in RGMII mode.
- For $V_{REFHSTL}$ (RGMII), one reference voltage divider should be used for both the TCI6486/C6472 device and the reference voltage input on the attached device. The same supply should also be used for the I/O voltages between the two parts. The V_{REF} resistor divider should be placed between the two devices and the routes made as directly as possible with a minimum 20-mil wide trace. There should be a 2x trace width clearance between the routing of the reference voltage and any switching signals.

Power and ground:

- A dedicated power plane for RGMII 1.5 V/1.8 V is recommended or, at least, a split power plane solely for the HSTL circuitry is recommended.
- Solid ground planes are preferred. However, some system designs require isolated ground planes or islands. These must be tied together at an appropriate single point such as near the power source.
- Power planes should be as wide as possible. Remote sense capability allows power supplies to adapt to the IR drop across a power plane.
- If any analog or mixed-signal component exists in the system, analog ground and digital ground are separated.
- Shielding is needed if any RF component, such as a tuner, co-exists in the system.
- Sufficient decoupling is provided.

TI has various application reports for high-speed PCB layout. Two good references are the *High-Speed Layout Guidelines* application report (SCAA082) and the *High-Speed DSP Systems Design Reference Guide* (SPRU889).

Appendix A TCI6486/C6472 RGMII 1.5-V/1.8-V-to-2.5-V/3.3-V Translation

The TCI6486/C6472 device includes a variable-voltage Reduced Gigabit Media Independent Interface (RGMII) for connection to a gigabit-capable Ethernet switch or PHY. The TCI6486/C6472 interface may be configured to run at either 1.5-V or 1.8-V I/O; controlled directly by the voltage applied to the DV_{DD15} pins of the DSP. These rails are complaint with the RGMII specification. However, in practice, it has been found that in many cases level translation is required to connect to older RGMII PHYs and switches.

Voltage translation of the RGMII interface is a somewhat complicated task, insomuch as the interface must be level-translated but still support dual-data rates at up to 125-MHz operation. This can be very difficult to achieve using standard LVCMOS-type buffers for two reasons. First, such buffers often add up to 4-ns propagation delay to the buffered signals, making timing margins exceptionally small at the 125-MHz rate. Second, such buffers often provide little to no guarantee of relative propagation delays across buffers in the same device and further specify all timings with only a single output switching, which is not realistic in a gigabit Ethernet application.

As an alternative to the LVCMOS-type buffers, a good solution can be found using TVC-type buffers or CBT buffers in a TVC configuration. For more details on this configuration, see the *Selecting the Right Level-Translation Solution* application report (SCEA035). An example of this application is shown in Figure 13 using a CBT3245 in a TVC voltage-clamp configuration. The CBT3245 is an 8-in/out buffer, making it a nice fit for the six lines requiring translation in a single direction of a gigabit Ethernet application. Using this solution, two CBT3245s can be used (one for transmit, one for receive) to complete the translation.

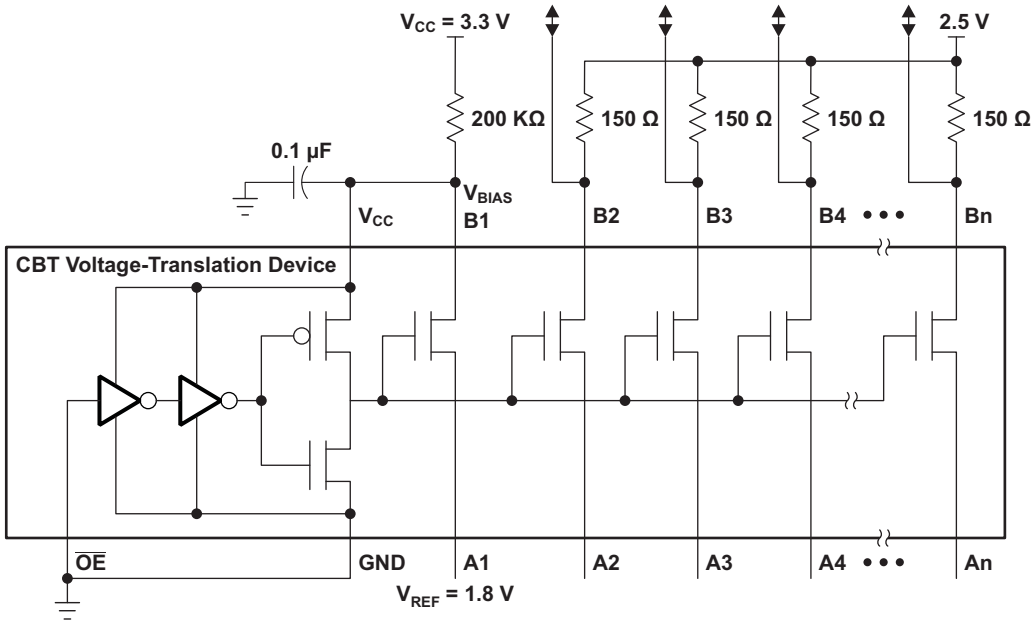

Figure 13. RGMII Voltage Level Translation Circuit

The CBT and TVC families of buffers are excellent in this application. Both are simple FET switches that offer sub-ns propagation delays. Because each FET switch is independent; the relative delays are matched very closely because process variations affect all switches equally. Unlike LVCMOS buffers however, these switches offer no additional current drive; however, since gigabit Ethernet connections are simple point-to-point connections, this is not a concern.

As an FET switch, the circuit in either the TVC or CBT application is the same. A single in/out pair is chosen to set the voltage clamp voltage to 1.8 V on the TCI6486/C6472 device side (1.5 V could also be used if that voltage is used for the TCI6486/C6472 RGMII interface). Because all the gates of the CBT/TVC in/out pairs are connected, this sets the clamp voltage for all the other pairs of ins/outs because VGS for the FET is fixed. Note that the buffer itself is powered using a 3.3-V supply, however. This is necessary to establish a voltage at least 1.0 V greater than the low-side clamp voltage (1.8 V + 1.0 V = 2.8 V, in this case).

The configuration shown above is technically a bidirectional solution, though gigabit Ethernet by its definition is unidirectional. When driving from the TCI6486/C6472 device to the switch/PHY, signals will vary from 0 V to 1.5 V/1.8 V. At the low (0 V) voltage level, the FET is turned on and both sides of the buffer and, thus, showing a low level. When a 1.5-V/1.8-V logic high is applied, the FET is turned off because this voltage matches (nearly) the voltage applied to the gate. In this case, the pull-up resistors on the high voltage side (switch/PHY side) of the buffer pull the output to the high-side rail. Therefore, in both cases the logic levels on both sides of the buffer match their respective rails. The application circuit shown above is shown for the TCI6486/C6472 device's transmit direction; that is; from the TCI6486/C6472 device to the switch. In the receive direction, the application circuit is the same except that the pull-up resistors to the 2.5-V side of the buffer, the switch/PHY side, that is, are not needed and should be omitted. In this case, pull-up resistors to 1.5 V/1.8 V are not required, as the buffer will act as a clamp and hold the output voltage to the 1.5-V/1.8-V level, providing the translation directly.

The values for the pull-up resistors on the high-voltage side of the CBT/TVC buffer are important. The basic trade-off that needs to be made is finding a value that is strong enough to pull to the high-side rail quickly to produce a good low-high edge rate (recall that this is when the FET turns off), but is not too strong so as to not allow the low side to pull the output to a level below the V_{IL} specification of the switch/PHY device when a low is driven (and the FET is on). In practice, a 150-Ω pull-up resistor is a good solution.

Shown below are several SPICE plots showing the characteristics of this solution. Figure 14 shows the relationship between V_{IN} and V_{OUT} that establishes the clamping to the low-voltage side rail even when the input voltage exceeds that rail. Figure 15 shows a square wave driven from each side and the resulting outputs. Note in all cases the extremely low propagation delay and good edge rates that result with this solution.

Setup for V_{OUT} vs. V_{IN} plot: B2 was swept from 0 to 2.5 V in 0.1-V steps and the waveform at A2 was observed. A 1MB resistor to GND was connected at A2.

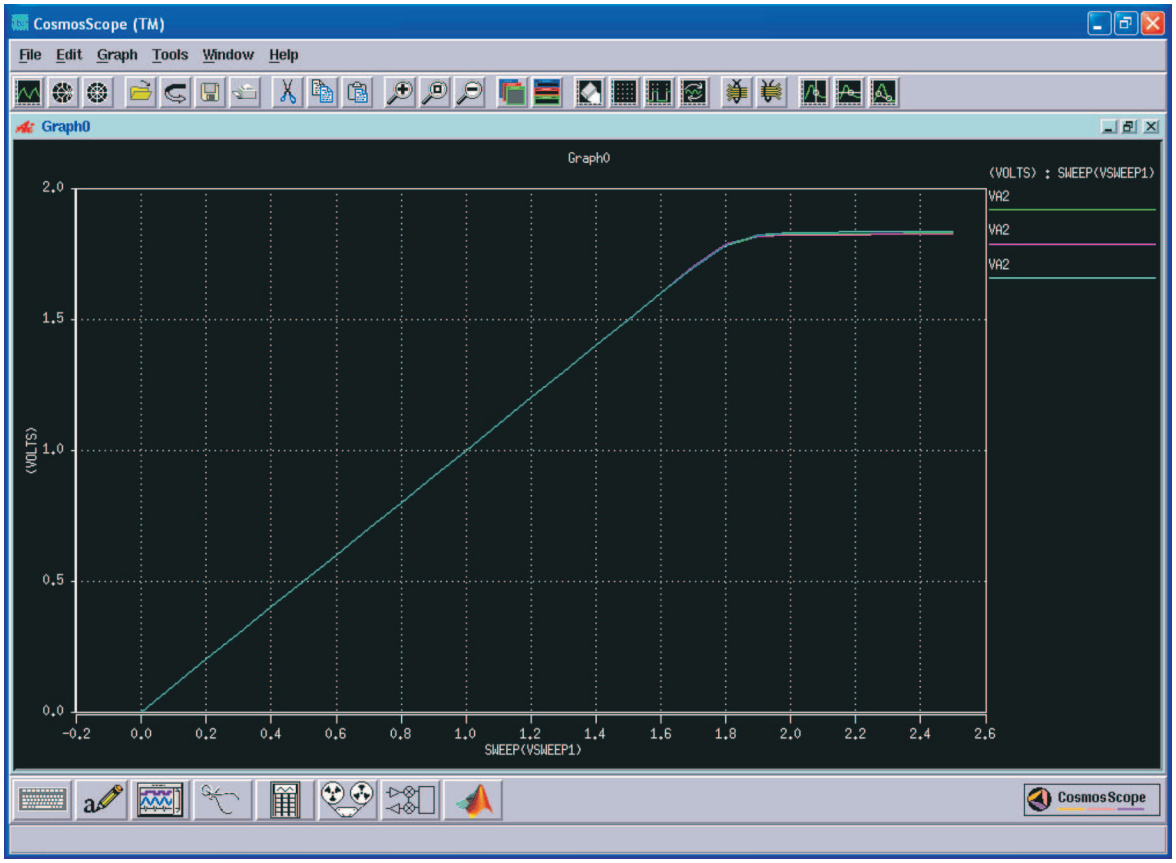

Figure 14. V_{OUT} vs. V_{IN}

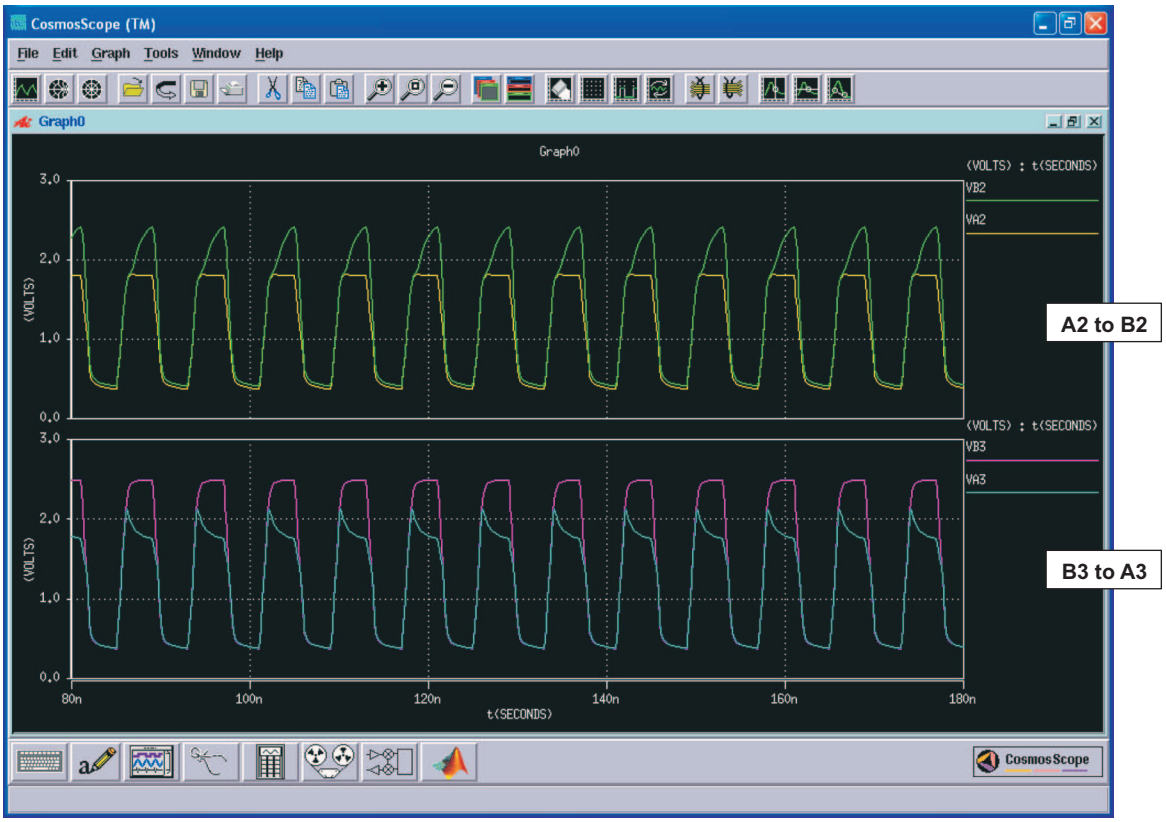

Figure 15. 125-MHz Signal From A2 to B2 and From B3 to A3

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265