User's Guide
SWCU073–December 2010

TPS659107 User Guide For i.MX27 and i.MX35 Processors

This user guide can be used as a reference for connectivity between the TPS659107 power-management integrated circuit (PMIC) and Freescale i.MX27 and i.MX35 processors.

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1 Introduction

This user guide can be used as a reference for connectivity between the TPS659107 PMIC and Freescale i.MX27 and i.MX35 processors. This user guide does not provide details about the power resources or the functionality of the device. For such information, see the full specification document, *TPS65910 Data Manual*. For information about Freescale processors, refer to official information from Freescale.

NOTE: In this document, the basis for information regarding i.MX processors is from official Freescale documents. Reference is made wherever applicable.

2 Platform Connection

Figure 1 shows the TPS659107 connections with the i.MX35 processor.

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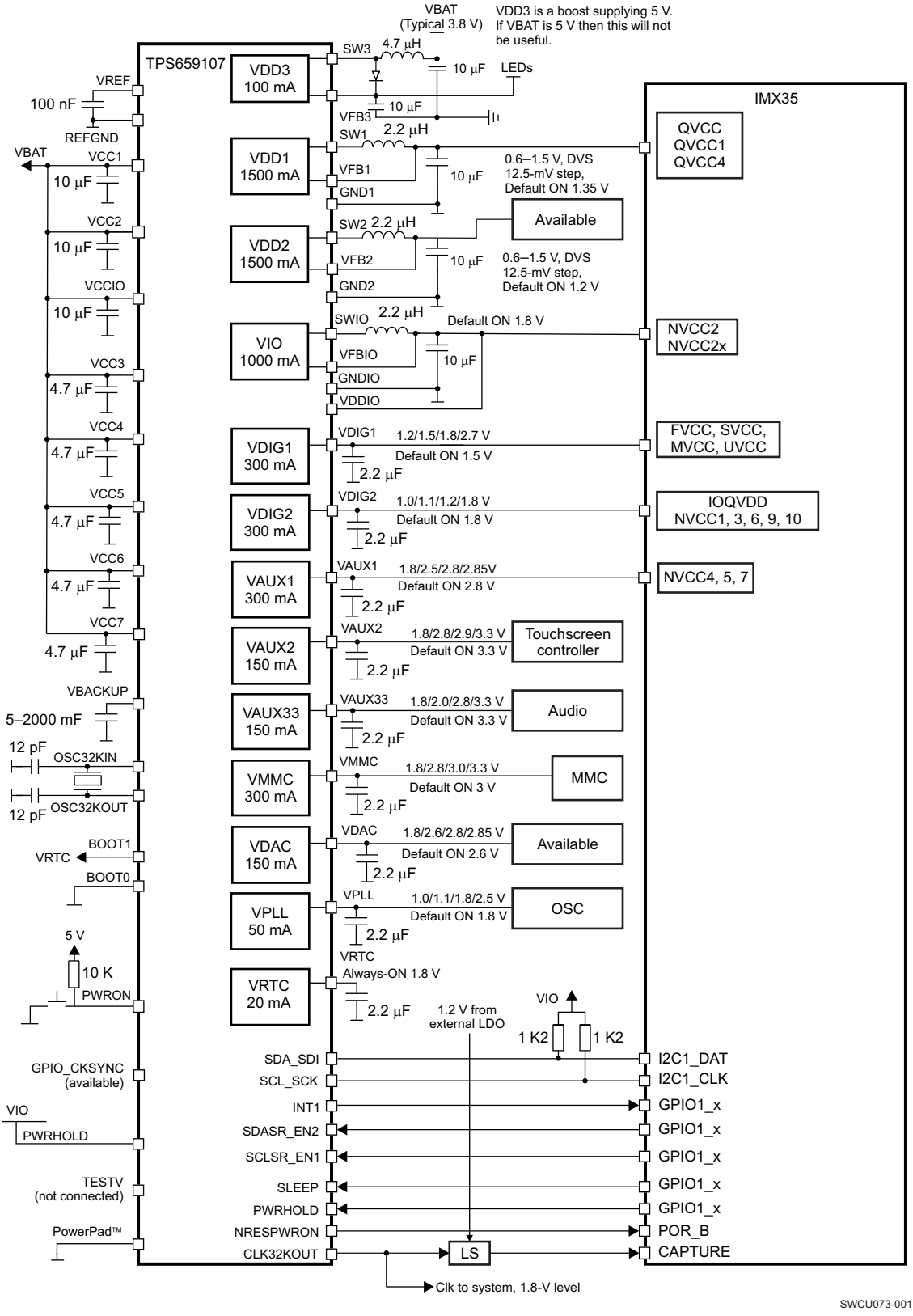

Figure 1. i.MX35 Power Supply Connections with TPS659107

At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

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- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

Based on the information in the Functional Pin Description, document MC13892, the following mapping of correct voltage level settings can be derived. The Freescale documentation provides voltage levels for different modes. The processors supported by the MC138982, according to this document, are the i.MX27 and i.MX35.

Table 1 lists the Freescale PMIC rails and the suggested voltage levels. The same levels can be achieved using the TPS659107 PMIC from Texas Instruments.

Table 1. Power Domain Mapping

MC13892 Power Rails	Voltage Levels of MC13892 for i.MX35 (V)	65910 Power Supply	Comments
SW1	1.2	VDD2	
SW2	1.35	VDD1	
SW3	1.8	VDIG2	
SW4	1.8	VIO	
SWBST	5.0	VDD3	
VUSB	3.3	VAUX2	
VUSB2	2.6	VDAC	
VPLL	1.5	VDIG1	
VDIG	1.25		
VIOHI	2.775	VAUX1 (2.8 V)	
VGEN2	3.15	VMMC (3.0 V)	

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The following tables for power-up sequence were generated from Table 3 on page 15 in application note AN3867.pdf.

See Figure 2, Table 3, and Table 4 for the power-up sequences that match the recommended PMIC and can be used with i.MX27 and i.MX35 application processors.

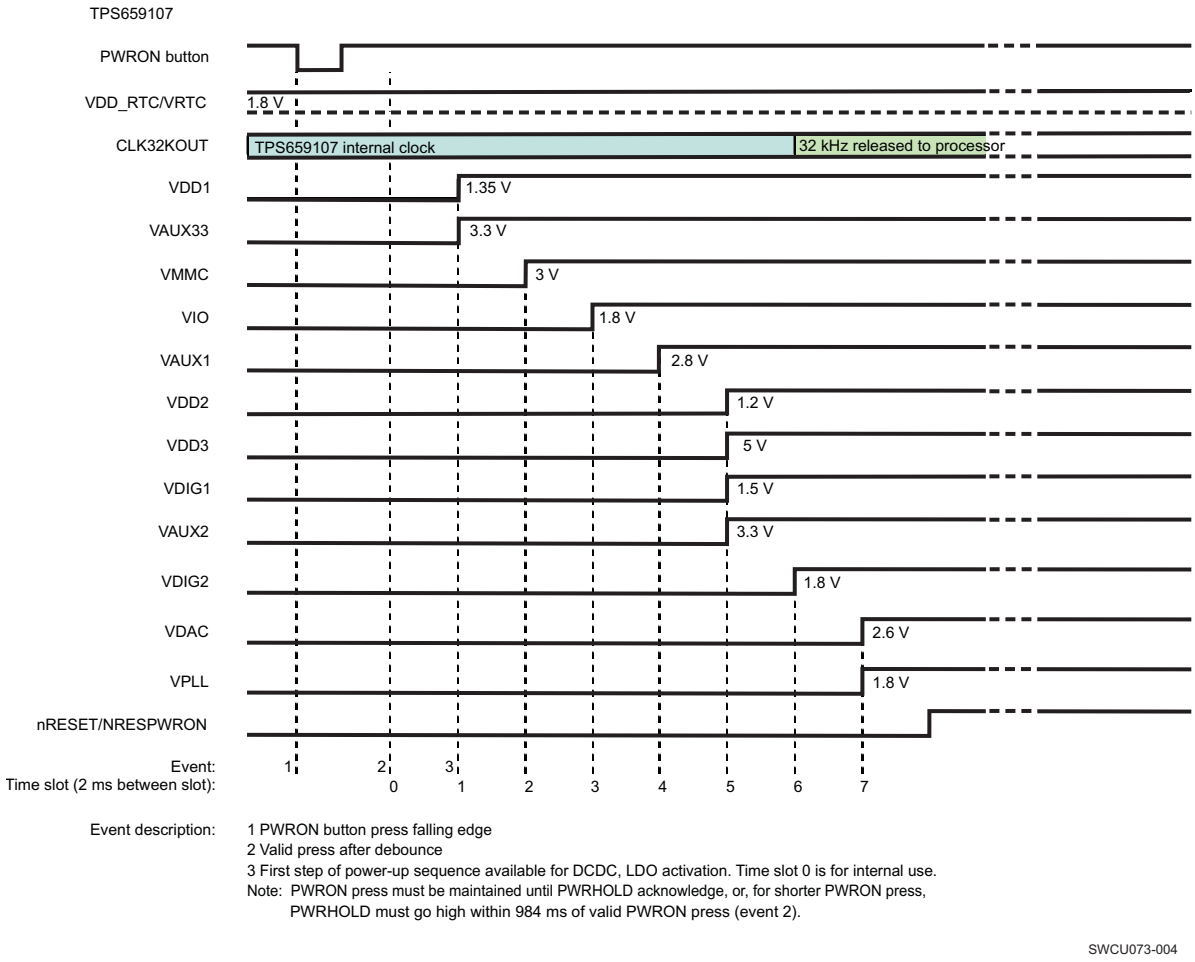

Figure 2. Power-Up Sequence for TPS659107 for i.MX27 and i.MX35

Table 2 shows the EEPROM values for the TPS659107.

Table 2. EEPROM Configuration for TPS659107

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.35 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	1
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.2 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	5
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	3
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled

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Table 2. EEPROM Configuration for TPS659107 (continued)

Register	Bit	Description	Option Selected
EEPROM		VDD3 time slot	5
VDIG1_REG	SEL	LDO voltage selection	1.5 V
EEPROM		LDO time slot	5
VDIG2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	6
VDAC_REG	SEL	LDO voltage selection	2.6 V
EEPROM		LDO time slot	7
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	7
VAUX1_REG	SEL	LDO voltage selection	2.8 V
EEPROM		LDO time slot	4
VMMC_REG	SEL	LDO voltage selection	3 V
EEPROM		LDO time slot	3
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	1
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	5
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	Crystal (0)
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = start-up is reason required before switch on.	0
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

Table 3 and Table 4 show the power-up sequence requirements as recommended by Freescale in the applications notes and data sheet.

Table 3. PUMS2 Connections for Power-Up Sequence[1][2]

Tap × 2.0 ms	PUMS2=Open (i.MX37, i.MX51)	PUMS2=GND (i.MX35, i.MX27)
0	SW2	SW2
1	SW4	VGEN2
2	VIOHI	SW4
3	VGEN2	VIOHI

(1) Time slots may be included for blocks which are defined by the PUMS pins as disabled to allow for potential activation.
(2) The following supplies are not included in the matrix, because they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO. SWBST is not included on the PUMS2=Open column.

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Table 3. PUMS2 Connections for Power-Up Sequence[1][2] (continued)

Tap × 2.0 ms	PUMS2=Open (i.MX37, i.MX51)	PUMS2=GND (i.MX35, i.MX27)
4	SW1	SWBST, VUSB[3]
5	SW3	SW1
6	VPLL	VPLL
7	VDIG	SW3
8		VDIG
9	VUSB[4], VUSB2	VUSB2

(3) SWBST = 5.0 V powers up and so does VUSB regardless of 5.0 V present on UVBUS. By default, VUSB will be supplied by SWBST.

(4) USB supply VUSB is enabled only if 5.0 V is present on UVBUS.

Table 4. Typical Connections for Power-Up Sequence[1]

i.MX	37/51	37/51	37/51	37/51	35	27/31
PUMS1	**GND**	**Open**	**VCOREDIG**	**VCORE**	**GND**	**Open**
PUMS2	**Open**	**Open**	**Open**	**Open**	**GND**	**GND**
SW1[2]	0.775	1.050	1.050	0.775	1.200	1.200
SW2[2]	1.025	1.225	1.225	1.025	1.350	1.450
SW3[2]	1.200	1.200	1.200	1.200	1.800	1.800
SW4[2]	1.800	1.800	1.800	1.800	1.800	1.800
SWBST	Off	Off	Off	Off	5.000	5.000
VUSB	3.300[3]	3.300[3]	3.300[3]	3.300[3]	3.300[4]	3.300[4]
VUSB2	2.600	2.600	2.600	2.600	2.600	2.600
VPLL	1.800	1.800	1.800	1.800	1.500	1.500
VDIG	1.250	1.250	1.250	1.250	1.250	1.250
VIOHI	2.775	2.775	2.775	2.775	2.775	2.775
VGEN2	3.150	Off	3.150	Off	3.150	3.150

(1) The following supplies are not included in the matrix, since they are not intended for activation by the startup sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO.

(2) The switchers SWx are activated in PWM pulse skipping mode, allowed when enabled by the startup sequencer.

(3) USB supply VUSB is enabled only if 5.0 V is present on UVBUS.

(4) SWBST = 5.0 V powers up and so does VUSB, regardless of 5.0 V present on UVBUS. By default, VUSB will be supplied by SWBST.

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4 Getting Started With TPS659107 and i.MX27/35

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

Program DEVCTRL2_REG.SLEEPSIG_POL according to the GPIO or SYS_CLKREQ signal from the processor. This can be set to active-low or active-high for SLEEP transitions. The software configuration will allow specific power resources to enter the low consumption state.

Set DEVCTRL_REG.DEV_SLP = 1 to allow the SLEEP transition when requested. Update the GPIO0 configuration (GPIO0_REG) based on your needs.

4.1.2 Define Wake Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.3 Backup Battery Configuration

If a backup battery is used, then enable backup battery charging by setting the BBCHEN bit to 1 in the BBCH_REG register. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

4.1.4 DCDC and Voltage Scaling Resource Configuration

If the SmartReflex™ interface is not used for voltage scaling (power saving) then these pins can be used to control the power resources.

Configure two operating voltages for DCDC1 and DCDC2:

- VDDx_OP_REG.SEL = Roof voltage (ENx ball high)
- VDDx_SR_REG.SEL = Floor voltage (ENx ball low)

Assign control for DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:

- Set EN1_SMPS_ASS_REG. VDD1_EN1 = 1
- Set EN2_SMPS_ASS_REG. VDD2_EN2 = 1
- Set SLEEP_KEEP_RES_ON_REG. VDD2_KEEPON = 1 (allow low-power mode)
- Set SLEEP_KEEP_RES_ON_REG. VDD1_KEEPON = 1 (allow low-power mode)

4.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. By default, in sleep mode all resources maintain their output voltage but transient and load capability are reduced.

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG and SLEEP_KEEP_RES_ON_REG registers.

Resources that can be set off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG and SLEEP_SET_RES_OFF_REG registers.

4.2 Event Management Through Interrupt

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that a supply (VBAT) is connected (leaving the BACKUP or NO SUPPLY State). Initialization of system is needed (see First Initialization above).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in the OFF or SLEEP state then this acts as a wake up event and resources are reinitialized.

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4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 6 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds, then the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. Software must take action to decrease the power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shutdown to prevent losing data. This interrupt is linked to VBAT but it does not apply to a system where PMIC is connected to 5-V rails and not connected directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT is the GPIO interrupt event and can be used to wake up the device from the SLEEP state. This can be an interrupt coming from any peripheral device or alike.

NOTE: This wake up event is not valid for a transition from the OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

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