Wideband Receiver Using 66AK2L06 JESD204B Attach to ADC32RF80 Design

This document focuses on the JESD attach and DFE signal processing capabilities of the 66AK2L06 SoC interfaced with TI's high performance ADC32RF80 and DAC38J84 wideband-data convertors. The demonstration consists of transmitting a sample file from the SoC through the DAC and looping it back through the ADC into the SoC. The sample data formats include dual-tone test patterns and multi-tone test patterns.

Contents

List of Figures

Trademarks

1 Overview

The TI 66AK2L06 System-on-Chip (SoC) is the industry's first JESD204B-compliant multicore DSP+ARM SoC that can interface with high performance JESD204B data convertors. The device also includes a digital front end (DFE) that can process TX and RX signals, forming a system optimized alternative to FPGAs.

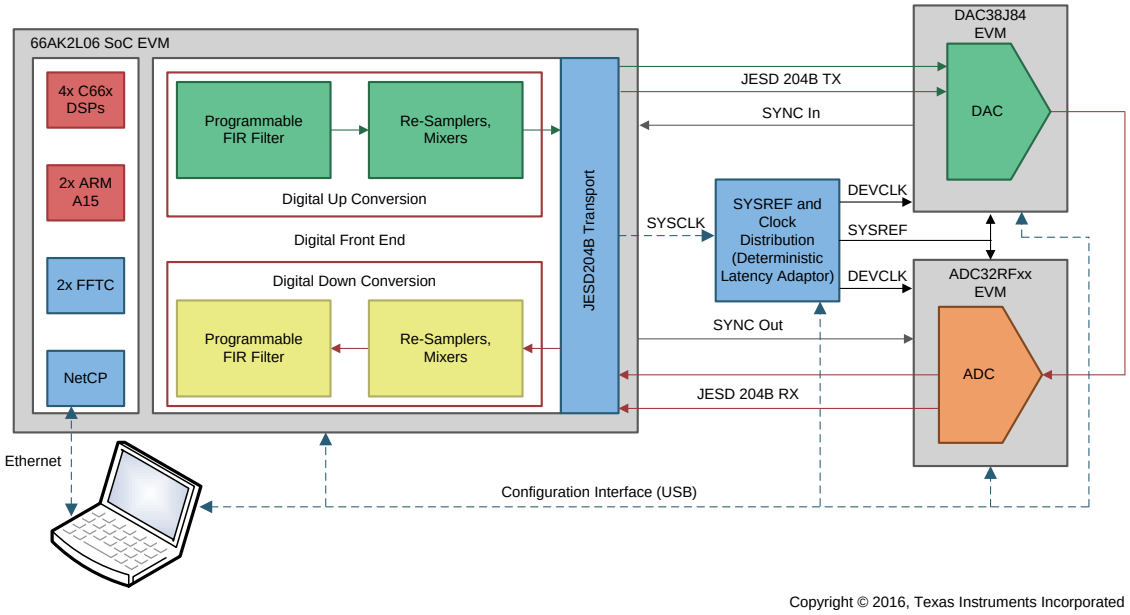

Figure 1. System Block Diagram

Two demonstrations are provided: Wideband RF sampling and Midband RF sampling. For wideband, DSP provides baseband data with sample rate of 122.88 Msps to the digital front end (DFE) of the 66AK2L06 SoC. Carrier data is up-sampled from 122.88 Msps at baseband to provide 368.64 Msps at the JESD interface. For midband, DSP provides baseband data for two carriers (FS = 92.16 Msps/carrier) to the DFE of the 66AK2L06 SoC. Carrier data is up-sampled from 92.16 Msps at baseband to provide 368.64 Msps at the JESD interface. Both demos utilize two out of four JESD Lanes on the 66AK2L06 SoC. The ADC works in real mode, and the JESD204B Serdes link rate is 7.3728 Gbps.

DAC38J84 receives parallel IQ data over JESD204B with a byte clock of 368.64 MHz. The DAC output rate is 737.28 Msps with an interpolation ratio of 2. The output of the DAC is centered at 184.32 MHz for midband demo and 92.16 MHz for wideband demo.

TI recommends using a spectrum analyzer to check the DAC output before running the loopback test. In the loopback case, the DAC output signal is sent to ADC32RF80 through a low-pass filter. The device clock provided to ADC32RF80 is 2949.12 MHz. The ADC sends real data to the SoC DFE over JESD204B with a byte clock of 368.64 MHz.

On the RX side, the DFE inside the 66AK2L06 SoC down-samples the data stream and shifts the carriers back to center frequency of zero.

2 Getting Started

2.1 Required Hardware and Software Components

2.1.1 Hardware components

- 66AK2L06 EVM, rev. 3.0, with the following accessories:
  - A 12-V Power supply
  - A mini-USB cable for universal asynchronous receiver/transmitter (UART) connection
  - An Ethernet cable
- K2L-HSP FMC Adapter Rev.A (also called Deterministic latency card - DLC) with the following accessories:
  - A mini-USB cable for connecting to a PC
- DAC38J84 EVM, rev. D, with the following accessories:
  - A 5-V DV power supply
  - A mini-USB cable for connecting to a PC
- The ADC32RFxx EVM with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for GUI SPI program
- DC-265 MHz low-pass filter
- SMA cables

2.1.2 Software Components (download links provided for GUI installers)

The demo package is provided as a Windows installer executable. Running this installer on the Windows host extracts the various software components as per the following directory structure:

- RFSDK2_<latest_version>: Top level directory, includes:
  - RFSDK2_<latest_version>_full-bin.tar.gz: demo package to be installed on top of MCSDK 3.1.4.7 on the 66AK2L06 EVM.
  - RFSDK2_<latest_version>-66AK2L06-Design-Demo-Win-GUI-Configs.zip: Board initialization and configurations files for EVM GUIs.
  - mcsdk314_rfsdk.tar.gz: MCSDK patches for the demo.
  - RFSDK2_<latest_version>-doc.tar.gz: Documentation and Release Notes.
- Configuration GUIs for data convertor EVMs (Windows based)
  - ADC32RFxx EVM GUI: http://www.ti.com/lit/zip/sbac148
  - DAC38J84 EVM GUI: http://www.ti.com/lit/zip/slac644
- Configuration GUI for K2L-HSP FMC adapter EVM (Windows based)
  - For more information about the K2L-HSP FMC adapter and the associated GUI, contact TI support in the E2E Keystone Multicore Forum.

2.2 Setup Hardware

1. Connecting the 66AK2L06, DAC38J84, and ADC32RF80 EVMs:
   (a) Plug the FMC male connector of the ADC32RF80 EVM into J11 (FMC female) of the DLC EVM.
   (b) Plug the FMC male connector of DAC38J84 EVM into J10 (FMC female) of the DLC EVM.
   (c) Plug the J4 FMC male connector of the DLC EVM into CN16 (FMC female) of the 66AK2L06 EVM. To review the setup with all the boards connected, see Figure 3.
2. Connecting the clocks:
   (a) Use two length-matching SMA cables, one to connect from J15 of the DLC to the LMK CLKIN (J7) of the ADC32RFxx EVM; one to connect from J16 of the DLC to the ADC CLK IN (J5) of the ADC32RFxxEVM. Check jumper JP3 on ADC32RFxx EVM and make sure 2-3 is connected so external clock input is selected (see Figure 2).

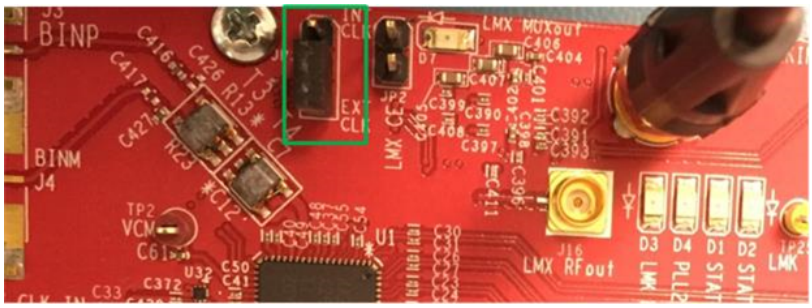

Figure 2. JP3 Setting for Ext Clock Enable

NOTE: The LMK04828 on the Deterministic Latency Card is a dual-PLL clock chip. The clock-in reference for PLL1 comes from the 66AK2L06 EVM (122.88 MHz). The on-board VCXO of 122.88 MHz on the DLC EVM is used as reference for PLL2. The output of LMK04828 provides device clock to both DAC38J84 and ADC32RF80.

3. Connecting the DAC output to the ADC input (the loopback configuration):
   (a) Connect the DAC output at J2 (IOUTAP) to the DC-265 MHz low-pass filter input
   (b) Connect the other end of the DC-265 MHz low pass filter to J3 (BINP) of the ADC32RF80 EVM to complete the loopback.
   (c) Figure 4 shows the setup with all of the clock and loopback connections made previously.
4. USB and Ethernet connections.
   (a) The 66AK2L06 EVM has two mini-USB connectors and one of them, J6, provides the BMC (Board Management Controller) and Linux serial terminal interfaces (multiplexed onto the same port).
   (b) Connect the mini-USB port J6 on 66AK2L06 EVM to the PC using a mini-USB cable.
   (c) Connect the ADC32RF80 and DAC38J84 EVMs to the PC using mini-USB cables.
   (d) Connect the DLC EVM to the Windows host using mini-USB cable.
   (e) Connect the 66AK2L06 EVM ETH-0 (lower port) to the same network as the Windows host over a 1Gbps connection (either directly or through a Gigabit Switch).

NOTE: Follow the correct power-up sequence for proper initialization of the setup. The K2L EVM is powered up first, followed by the DAC and ADC EVMs.

5. Power
   (a) Provide +12 V to 66AK2L06 EVM using the provided 12V DC power supply.
   (b) Provide +5 V to the ADC32RF80 EVM and +5V to the DAC38J84 EVM using the provided 5V DC power supplies.
6. Miscellaneous
   (a) For initial test/debug purposes, check the output of the DAC on a spectrum analyzer before trying to get the loopback working. (Connect the DAC38J84 EVM J2-IOUTAP to the spectrum analyzer input).
   (b) When the DAC38J84 J2 output is working, configure and connect the DAC38J84 and the ADC32RF80 EVM to loop back.

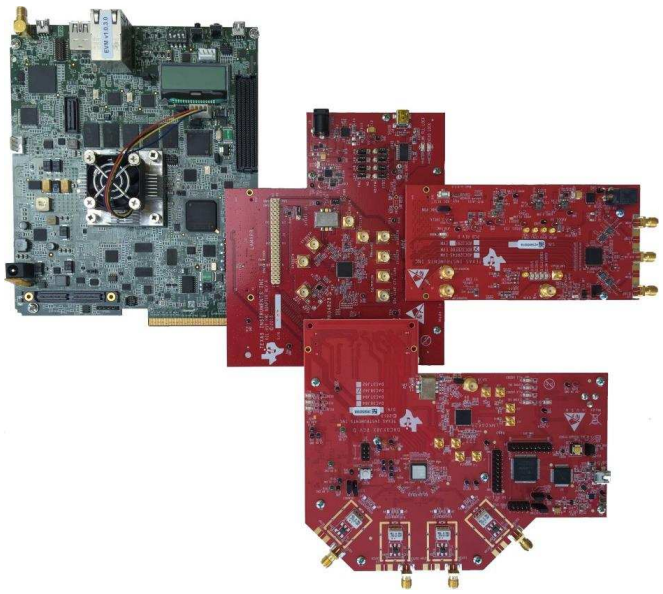

Figure 3. Boards Connected Together

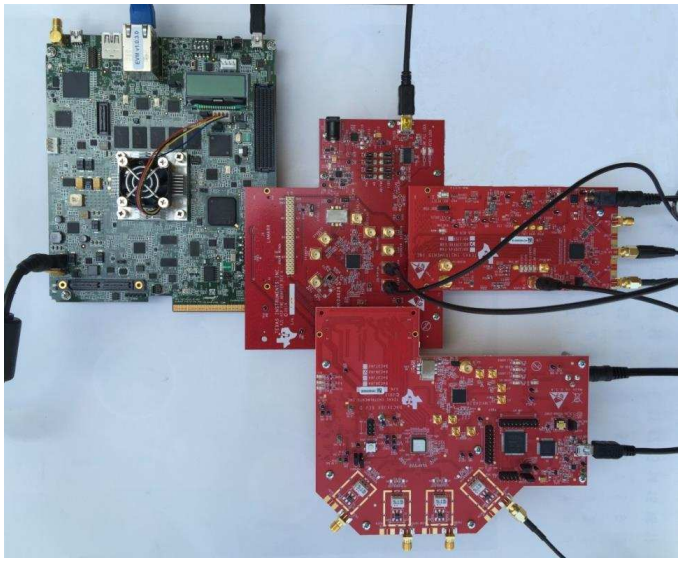

Figure 4. Complete Setup With Cables/Power Supplies Connected

2.3 Setup Software

2.3.1 Getting the 66AK2L06 EVM Ready

Connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port using the following serial port settings: Baud Rate: 115200, Data: 8 bit, Parity: None, Stop: 1 bit, Flow Control: None

NOTE: You must have the Silicon Labs cp210x vcp driver installed on the Windows host in order to be able to enumerate the 66AK2L06 EVM virtual COM ports in Windows Device Manager.

Figure 5 shows the 66AK2L06 EVM virtual COM ports listed in the Windows Device Manager.

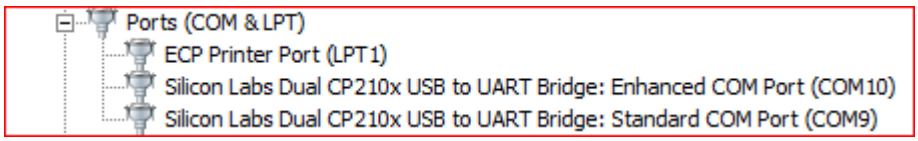

Figure 5. 66AK2L06 EVM Virtual COM Ports

The upper COM port belongs to Linux, for example, COM10 in this case (the port numbers on your system may be different).

the following procedures describe how to prepare the 66AK2L06 EVM for the demo:

1. Update the UBIFS image on the 66AK2L06 EVM:
   (a) The factory installed MCSDK image on the 66AK2L06 must be updated to the image provided with MCSDK 3.01.04.07.
   (b) A tftp server is required to update the UBIFS image on the 66AK2L06 EVM.
   (c) Download the appropriate MCSDK installer (mcsdk_3_01_04_07_setupwin32.exe for Windows or mcsdk_3_01_04_07_setuplinux.bin for Linux) for your tftp host.
   (d) Run the installer and follow the prompts to install the new MCSDK on your tftp host machine.
   (e) Once installed, the UBIFS image for 66AK2L EVM is available in the images sub-directory under the MCSDK install directory.
   (f) The image is named k2l-evm-ubifs.ubi
   (g) Follow the instructions given in the Keystone-II MCSDK User's Guide wiki under the Using UBIFS File system section to update the existing image on the EVM with the UBIFS image (mentioned in the previous step).

   NOTE: The image and directory names mentioned in this section may not match with the image name provided above, however, the general procedure is the same. Use appropriate *tftp_root* directory path, image name and *serverip* according to your setup.

   NOTE: TI recommends using the automated u-boot scripts, namely *get_ubi_net* and *burn_ubi* as defined in the update instructions to download and flash the UBIFS image, respectively.
2. Install the device tree binary (dtb) patch:
   (a) With the UBIFS image on the 66AK2L06 EVM updated as described in Step 1, the dtb file on the EVM must be updated (replaced) with the .dtb file provided under *mcsdk314_rfsdk.tar.gz* in the demo package.
   (b) Extract the dtb binary file from *mcsdk314_rfsdk.tar.gz*.
   (c) Follow the instructions given in the Keystone-II MCSDK User's Guide wiki under the Updating Boot volume images from Linux kernel section.

NOTE: The name of the patched dtb provided in the demo package may be different than the working dtb filename in the boot volume on the EVM.

NOTE: Remember the original dtb filename and ensure that you copy the new dtb file to the boot volume with the same name. Failing to do this will cause a Linux boot failure when the board is restarted.

3. Install the demo package (user interactions *italicized*):
   (a) The demo software is provided as a compressed archive named RFSDK2_<latest_version>_full-bin.tar.gz in the demo package. Copy this file to the tftp root directory of your tftp server.
   (b) With Linux booted, copy the above file to /home/root on the EVM (using tftp or scp).

```
root@k2l-evm:~# pwd
/home/root
root@k2l-evm:~# tftp -g -r RFSDK2_<latest_version>_full-bin.tar.gz <tftp_server_ip_addr>
```

   (c) Extract RFSDK2_<latest_version>_full-bin.tar.gz in the root directory

```
root@k2l-evm:~# cd /
root@k2l-evm:/# tar xvf /home/root/ RFSDK2_<latest_version>_full-bin.tar.gz
```

   (d) Create a soft link to the default board configuration to finalize the installation

```
root@k2l-evm:/# cd /etc/radio/board
root@k2l-evm:/etc/radio/board# ln -s lamarr-evm-demo4-mcsdk3147 default
root@k2l-evm:/etc/radio/board# ls -l default
lrwxrwxrwx 1 root 42005 18 Dec 12 21:30 default -> lamarr-evm-demo4-mcsdk3147
```

   (e) Reboot Linux on the EVM.

2.3.2 Installing PC Side Software

Download GUI installers for the DAC34J84 and ADC32RFxx EVMs from the links in Section 2 and install the corresponding GUIs.

- Install the ADC32RFxx GUI
- Install the DAC34J84 GUI

3 Running the Demo

3.1 Setting Up the DAC and ADC EVMs

3.1.1 Power-Up Sequence for the Boards

1. 66AK2L06 EVM
2. ADC32RFxx EVM
3. DAC38J84 EVM

3.1.2 K2L-HSP FMC Adapter

1. Start the Deterministic Latency Adapter GUI (Start → All Programs → Texas Instruments → Deterministic Latency Adapter)
2. Ensure that the USB Status indicator is green (see Figure 6).

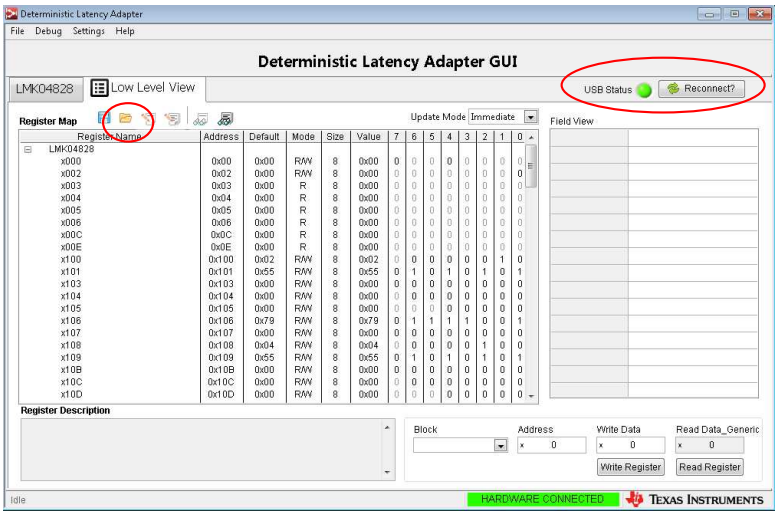

Figure 6. Deterministic Latency Adapter GUI

3. On “Low Level view” page, press the “Open Configuration” icon (see Figure 6)
4. Select the file named “66AK2L06_dac737p28.cfg” provided under RFSDK2_<latest_version>_66AK2Lx-Design-Demo-Win-GUI-Configs.zip in the demo package. This programs the required registers of the LMK04828.

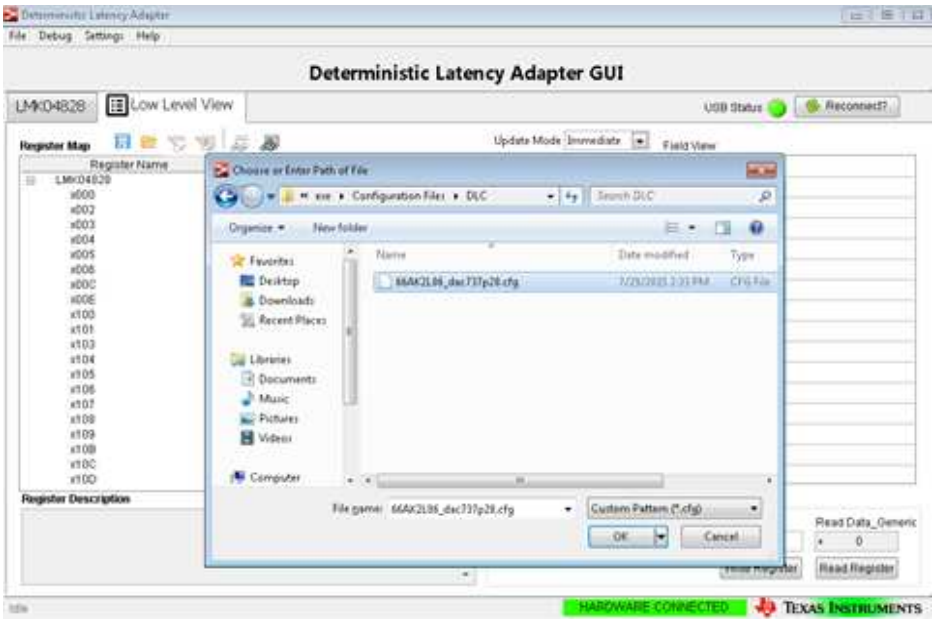

Figure 7. GUI-Load CFG

Figure 8 shows the clock output settings.

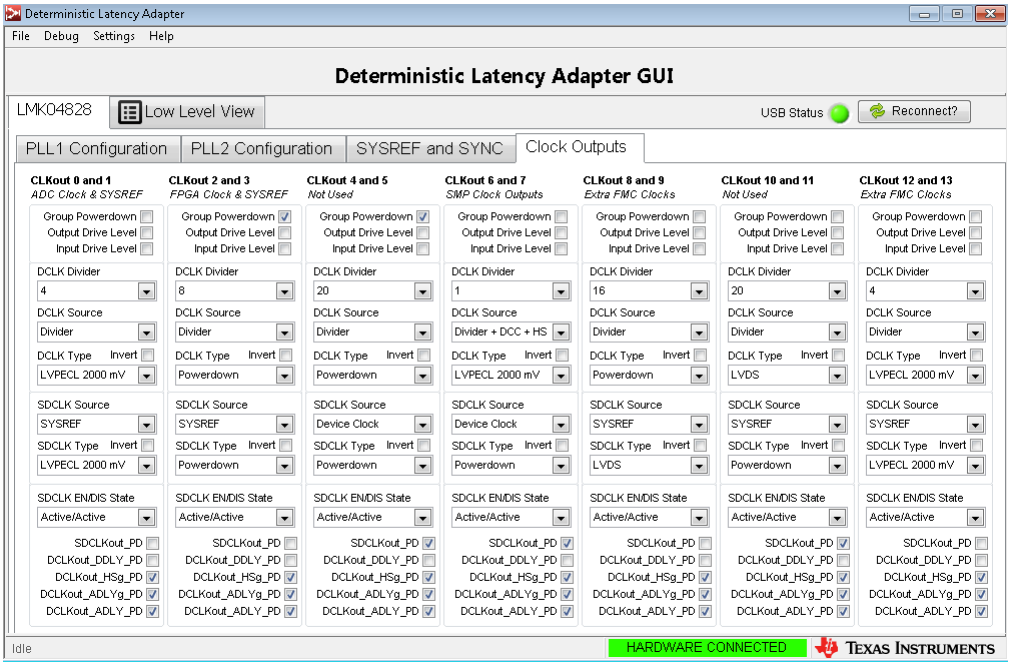

Figure 8. GUI-Clock Outputs

5. The details of the clock configuration are provided below:
   (a) CLKOUT 6: ADC32RFxx Device CLK 2949.12 MHz. ADC32RFxx SysRef is not used
   (b) CLKOUT 0: DAC38J84 Device CLK, div 4 for 737.28 MHz, LVPECL. DAC38J8x SysRef CLK is SDCLKOUT 1, LVPECL
   (c) After successful configuration, the “LMK PLL LOCK” and “VCXO LOCK” LEDS on the DLC EVM should be ON as shown. Make sure that the LMK LOCK LED is bright, otherwise, power-cycle the DLC EVM and follow the configuration instructions again.

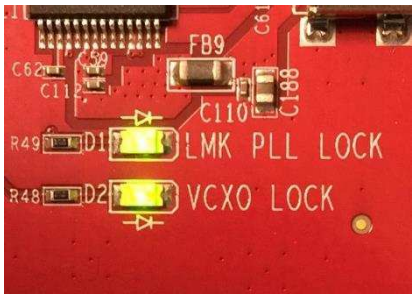

Figure 9. LED Status

3.1.3 DAC38J8x EVM GUI

1. Start the DAC34J84 GUI (Start → All Programs → Texas Instruments DACs → DAC3xJ8x GUI)
2. Make sure that “USB Status” is green.
3. Set EVM Clocking mode to “Onboard”.
4. Select Device as DAC38J84 (this demo uses two of the 4 DAC channels on the DAC38J84).
5. Select DAC Data Input Rate as 368.64 Msps
6. Select Number of Serdes Lanes as 4 (actual usage is 2) and Interpolation as 2.

7. Click the “Program LMK04828 and DAC3XJ8X” button. Figure 10 shows the DAC38J8x GUI start page.

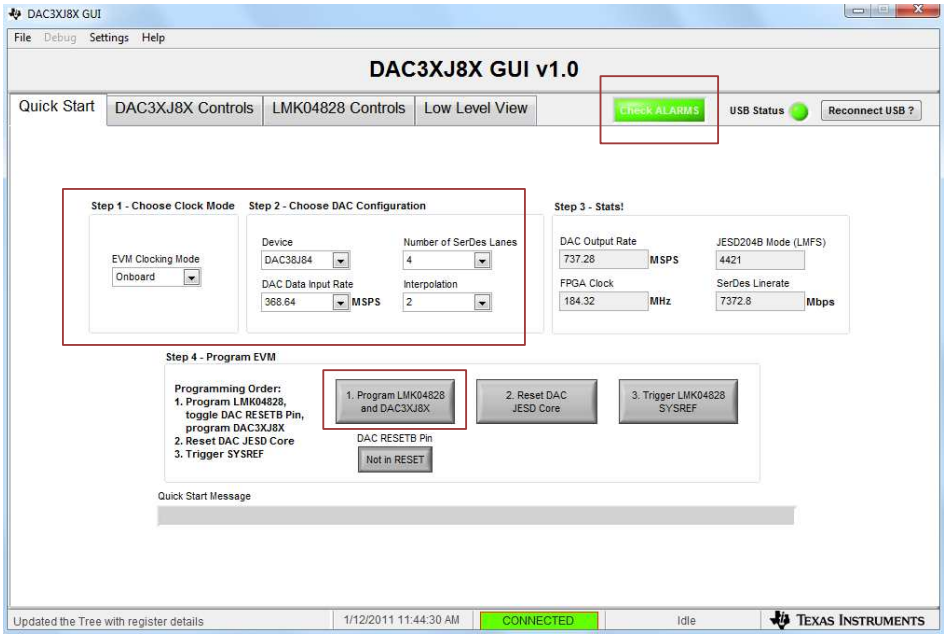

Figure 10. DAC38J8x GUI Start Page

8. Click the “Low Level View” tab and then the “Load Config” button once the programming is complete.
9. Load the file K16_66AK2L06_rev3_737p28.cfg provided under RFSDK2_<latest_version>_66AK2Lx-Design-Demo-Win-GUI-Configs.zip in the demo package for the midband demo. Load K16_66AK2L06_rev3_737p28_4w.cfg for the wideband demo.
10. Go back to the "Quick Start" tab and Press "3. Trigger LMK04828 SYSREF" button.

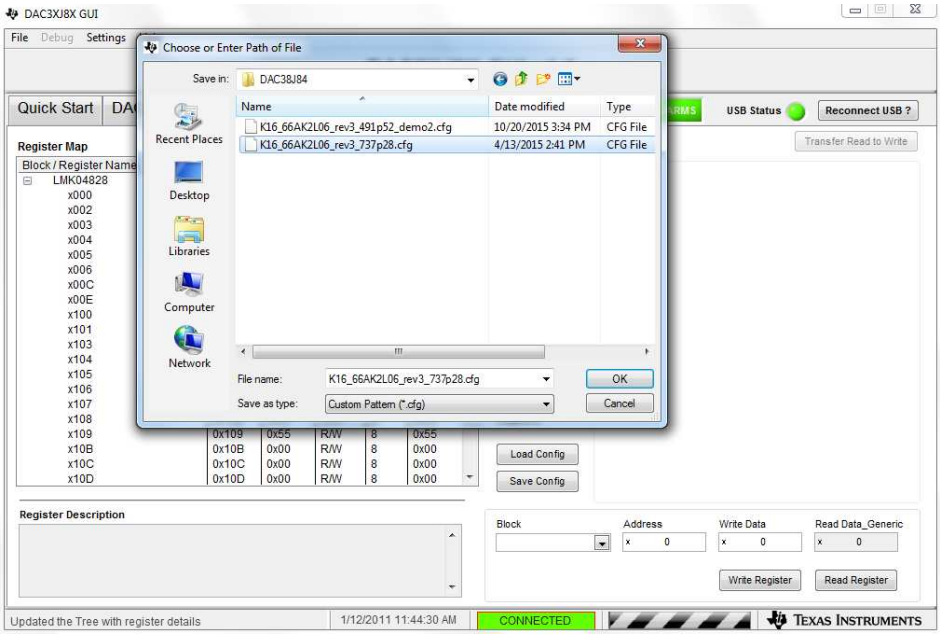

Figure 11. Low Level View to Load Registers

NOTE: For midband demo, the coarse mixer (fs/4) is enabled as shown in Figure 12. For wideband, the coarse mixer of fs/8 is selected, as shown in Figure 13. SERDES configuration for the DAC38J84 can be seen under the “SERDES and Lane Configuration” tab as shown in Figure 14, both midband and wideband demo have the same SERDES configuration.

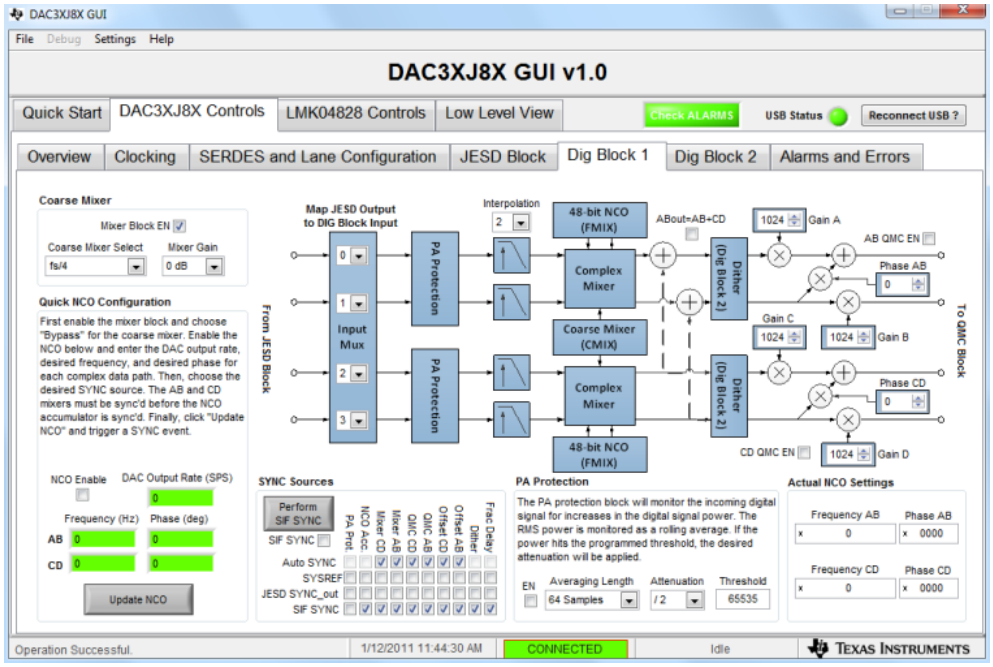

Figure 12. DAC38J8x GUI SYNC and NCO Setting - Midband

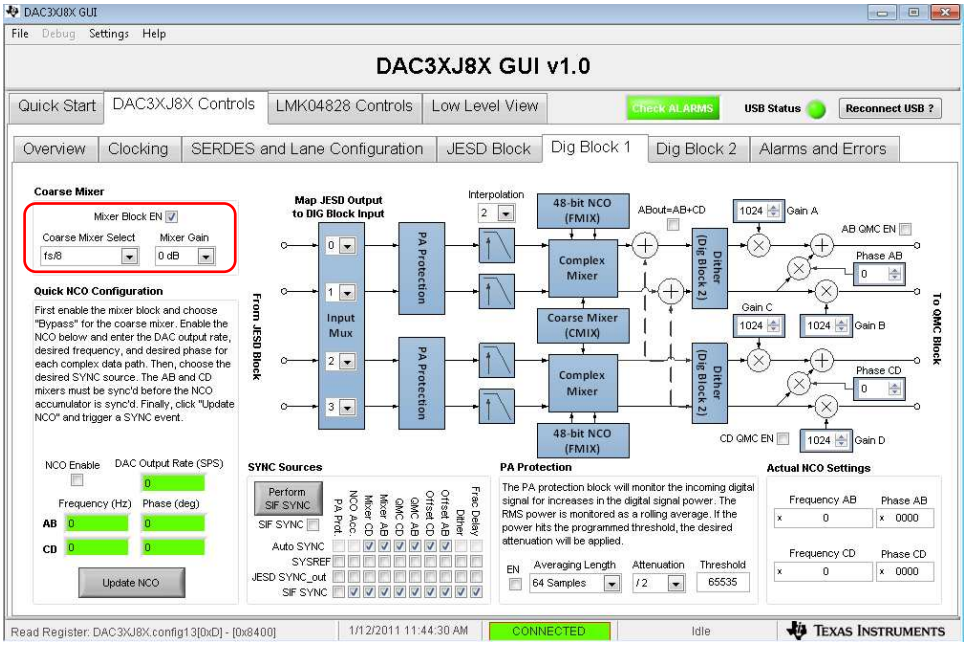

Figure 13. DAC38J8x GUI SYNC and NCO Setting -- Wideband

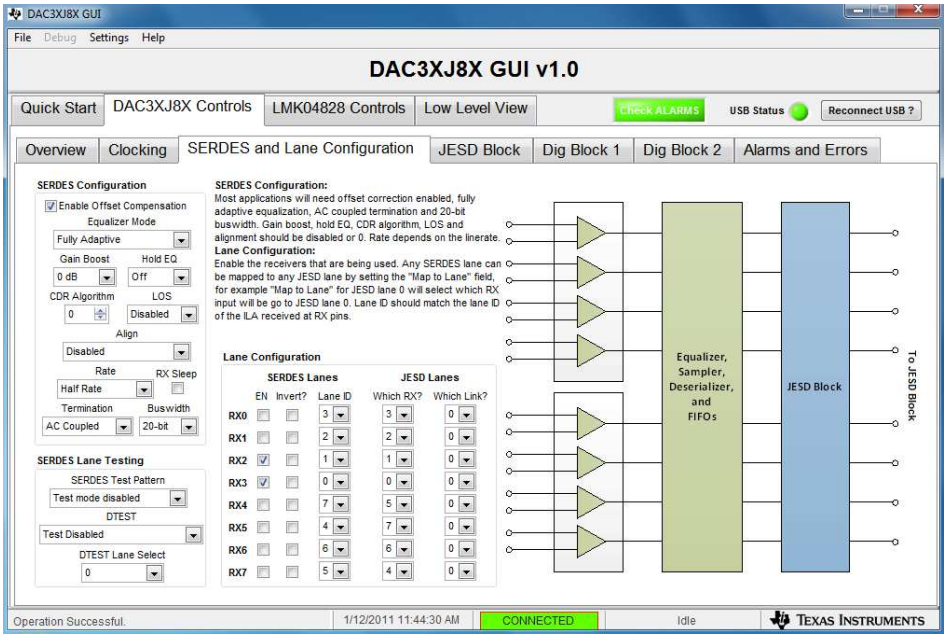

Figure 14. DAC38J8x GUI SERDES Lane Configuration

3.1.4 ADC32RFxx GUI

1. Start the ADC32RFxx GUI (Start → All Programs → Texas Instruments ADCs → ADC32RFxx GUI).
2. Make sure that the USB status is green.
3. If the GUI does not connect to the board, click on the “Reconnect FTDI button until the GUI connects to the board. This connection is indicated by a green USB Status.

NOTE: You may need to close the DAC34J8x GUI for the for the ADC32RFxx GUI to work.

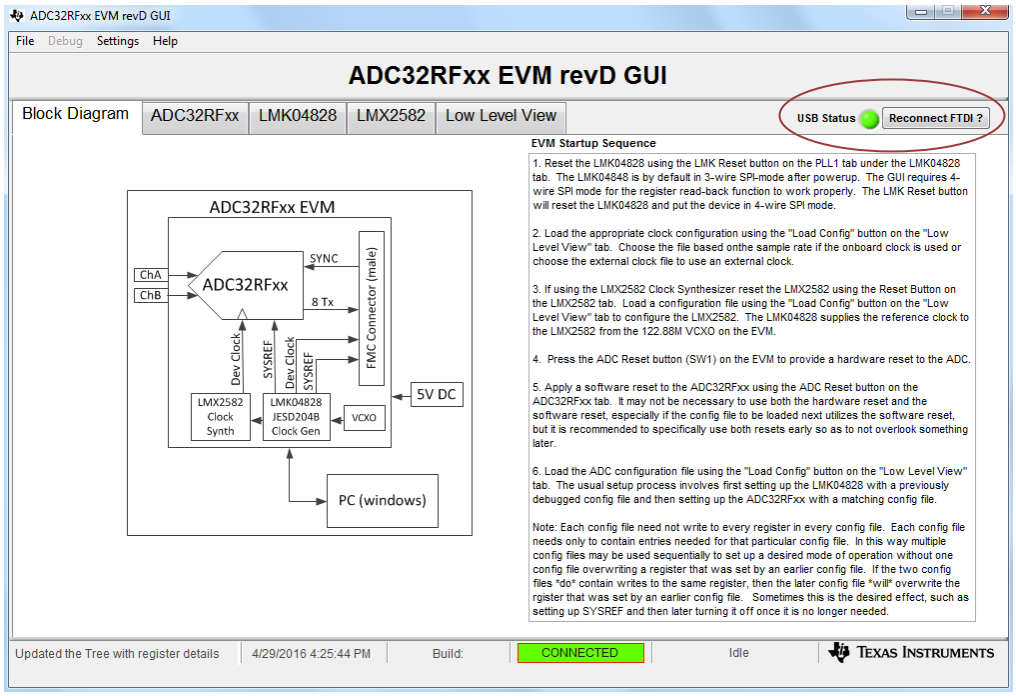

Figure 15. ADC32RFxx EVM GUI Start Page

4. Click on the “Low Level View” tab.
5. Press “Load Config” button and navigate to the “DDC Mode” folder.
6. Select “LMK_ADC32RF4x_ExtClock.cfg” and click “OK”.

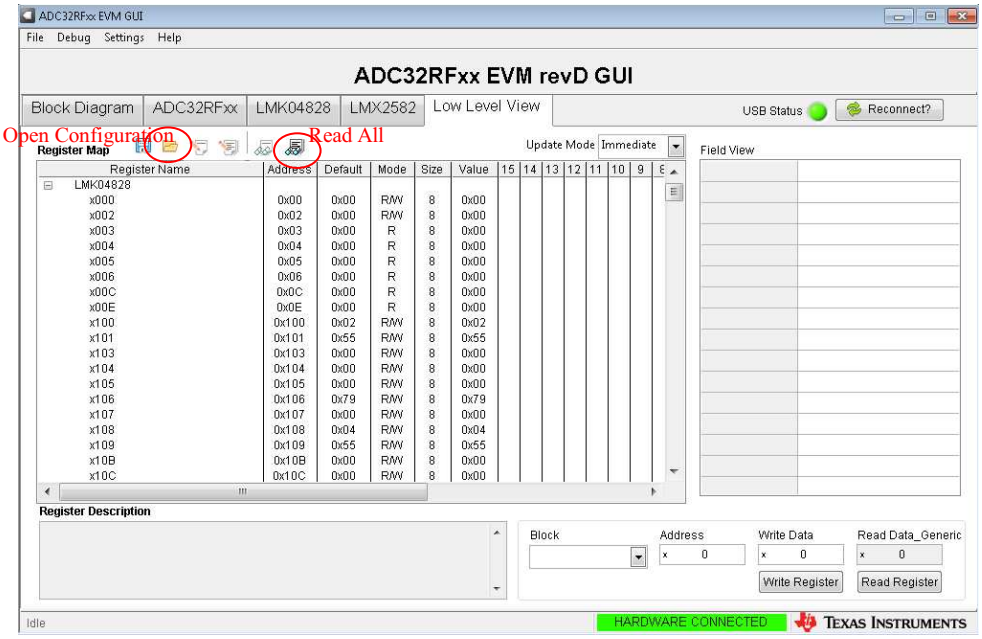

Figure 16. ADC32RFxx EVM GUI – Low Level View

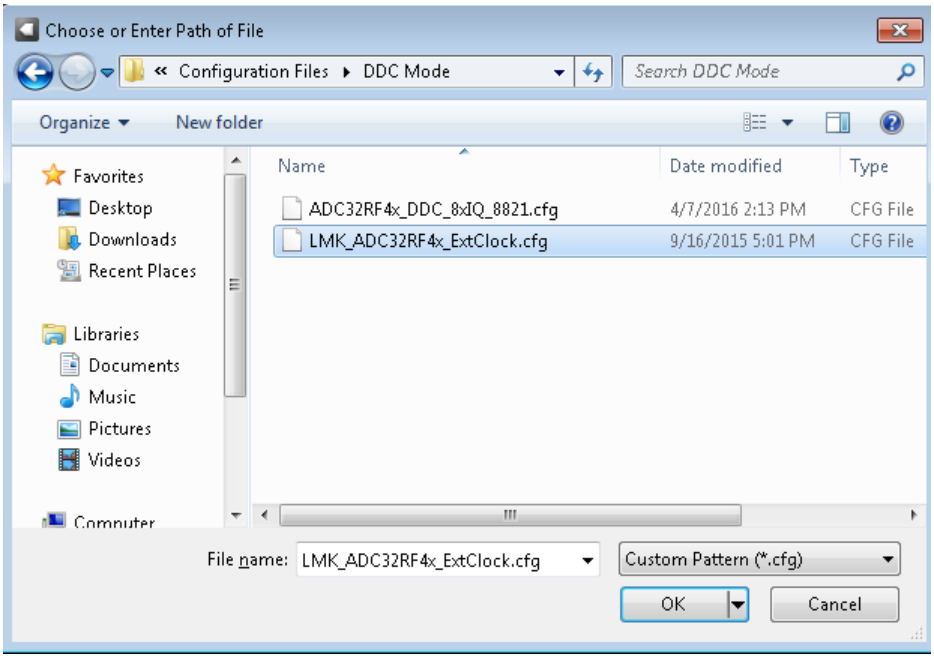

Figure 17. ADC32RFxx Clock Programming File

7. Press SW1 (ADC RESET) to provide a hardware reset to the ADC.
8. Go to the Low Level View tab and click “Load Config”.
9. Navigate to ADC32RF4xDDC_8xIQ_8821.cfg and click OK.
10. Press Read All on the low level tab.
11. Go to the ADC32RFxx tab, check if CHA and CHB DDC EN are selected. If not, go back to low level tab and press “Read All” again.
12. Enter 2949.12 in the box for Sampling Clock rate in MHz.

13. For midband demo, enter 139.32 in the box for Ch B DDC0 NCO1 frequency and enter 229.32 in the box for CHB DDC1 NCO frequency, see Figure 18. For wideband demo, enter 92.16 in the box for Ch B DD0 NCO1 frequency, see Figure 19.

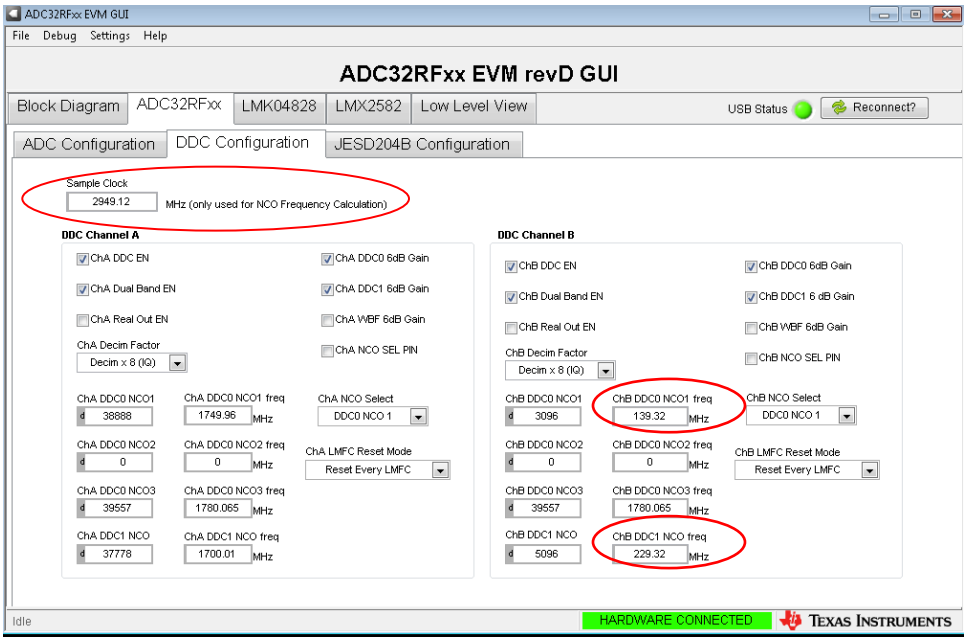

Figure 18. ADC32RFxx EVM GUI ADC Tab – Midband Demo

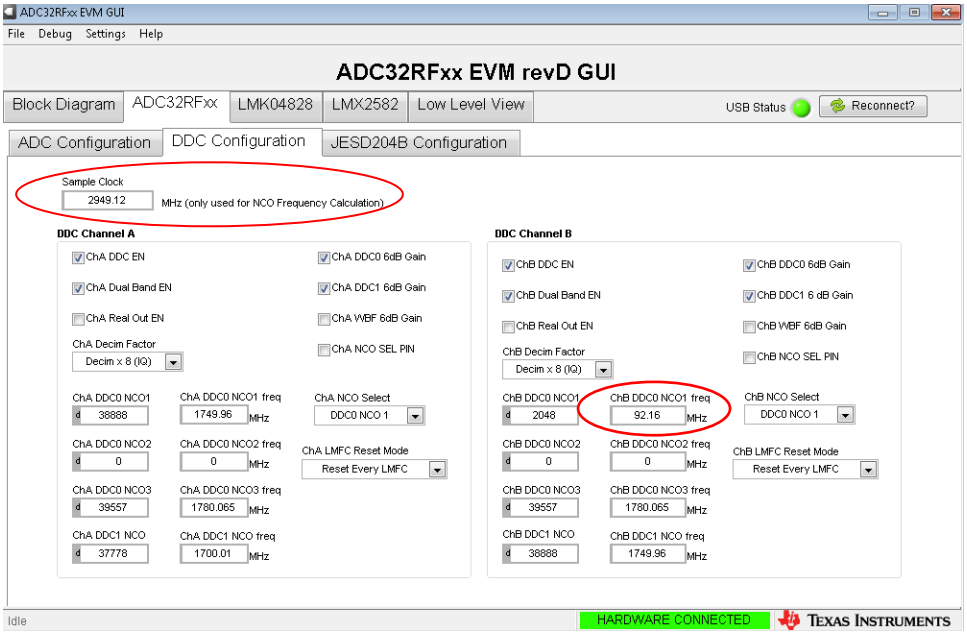

Figure 19. ADC32RFxx EVM GUI ADC Tab – Wideband Demo

NOTE: Only channel B of ADC32RFxx EVM is used. It's connected to a dual-band DDC. Midband demo: we use DDC0 and DDC1 NCO to select the two carriers. Wideband demo, we use DDC0 NCO1 alone to select one wideband carrier.

3.2 Starting the Demo on the 66AK2L06 EVM

1. Connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port and login as the root user.
2. Determine the IP address assigned to the board using ifconfig, as shown in Figure 20.

```
root@k2l-evm:~# ifconfig
eth0      Link encap:Ethernet  HWaddr 08:00:28:32:BA:5C
          inet addr:128.247.121.3  Bcast:0.0.0.0  Mask:255.255.254.0
          inet6 addr: fe80::800:2800:132:ba5c/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:11519 errors:0 dropped:0 overruns:0 frame:0
          TX packets:13 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:910369 (889.0 KiB)  TX bytes:1679 (1.6 KiB)
```

Figure 20. Querying the Board IP Address

3. Type "touch /tmp/rfsdk_stubbed_afe" in the 66AK2L06 Linux terminal. This is required running a loop back test with ADC and DAC, not when JESDlpbk configuration is selected.
4. Open a web browser on the PC and point it to <EVM_IP_ADDRESS>:8080. This should open up the RFSDK Web GUI, as shown in Figure 21.

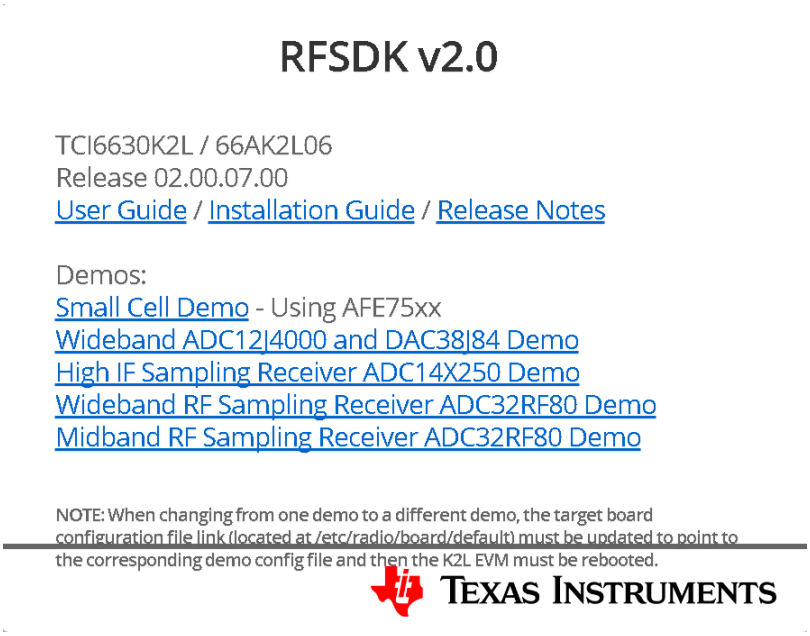

Figure 21. RFSDK Web GUI

5. The web GUI will navigate to the RFSDK v2.0 DEMO4 page for midband demo and DEMO4w page for wideband.

6. Press the Select button once the reset is complete to open up the Radio Configuration Dialog, as shown in Figure 22 and Figure 23.

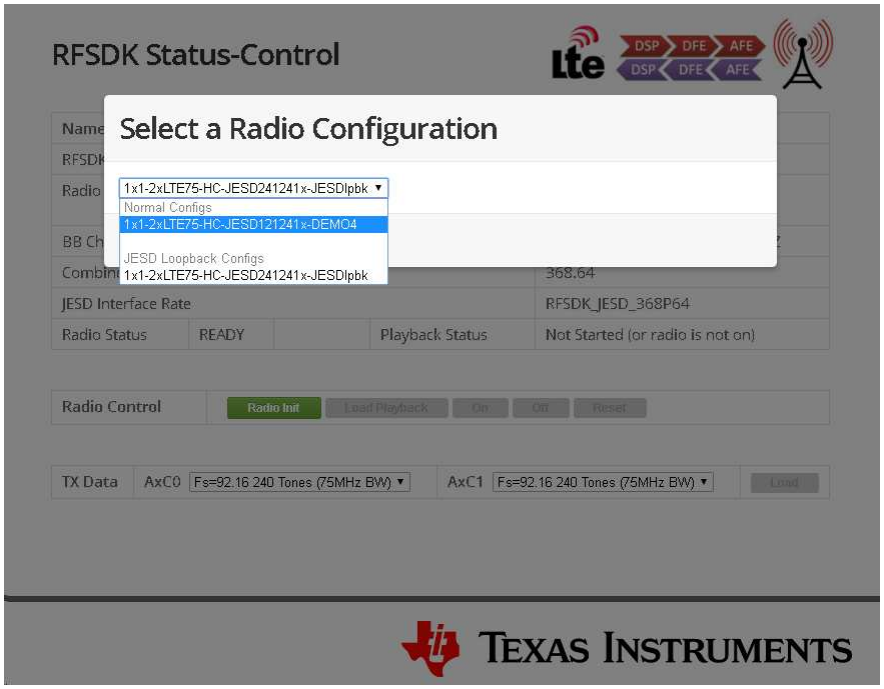

Figure 22. Radio Configuration Selection - Midband Demo

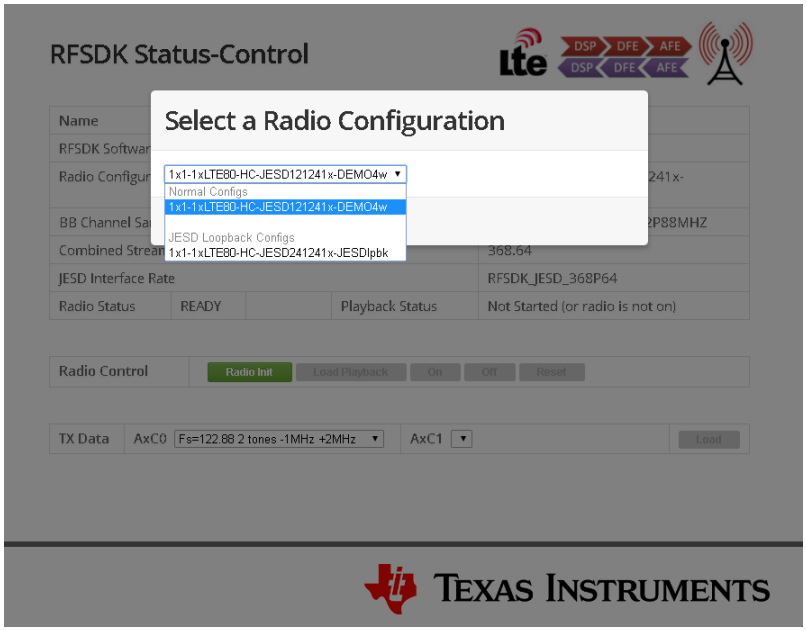

Figure 23. Radio Configuration Selection – Wideband Demo

7. Select a configuration from 1×1-2xLTE75-HC-JESD121241x-DEMO4, or 1×1-2xLTE75-HC-JESD241241x-JESDlpbk for midband demo and from 1x1-1xLTE80-HC-JESD121241x-DEMO4w or 1x1-1xLTE80-HC-JESD241241x-JESDplbk for wideband demo. Press Select.
8. In “Radio Cntrl”, press “Radio init”, then “Load Playback”, and then “On” in sequence to start the playback demonstration. (*Playback Status* should change to Started/Alive, which indicates that the test is running.)

9. Midband demo: click the AxC0 drop-down menu and select “Fs=92.16 2 tones, –1 MHz and +2 MHz” or “Fs=92.16 2 tones, –2 MHz and +4 MHz” or “Fs=92.16 240 tones(75MHz BW)”. (This loads the selected signal patterns into the corresponding transmit buffers.). Click the Load” button. The test pattern can be changed without having to stop the test. Similarly, for wideband demo two signal patterns “Fs=122.88 2 tones -1 MHz and +2 MHz” and “Fs=122.88 200 tones (100 MHz BW)” are available for AxC0 selection.

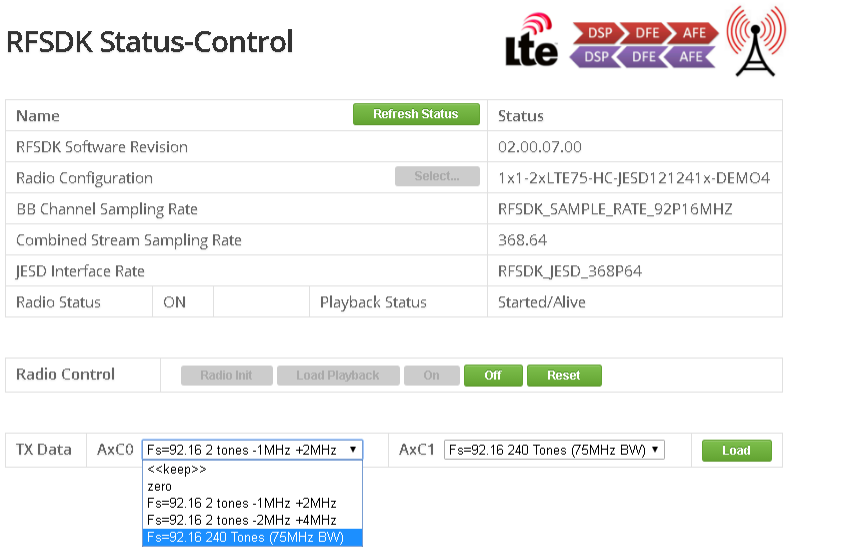

Figure 24. Loading Test Patterns – Midband Demo

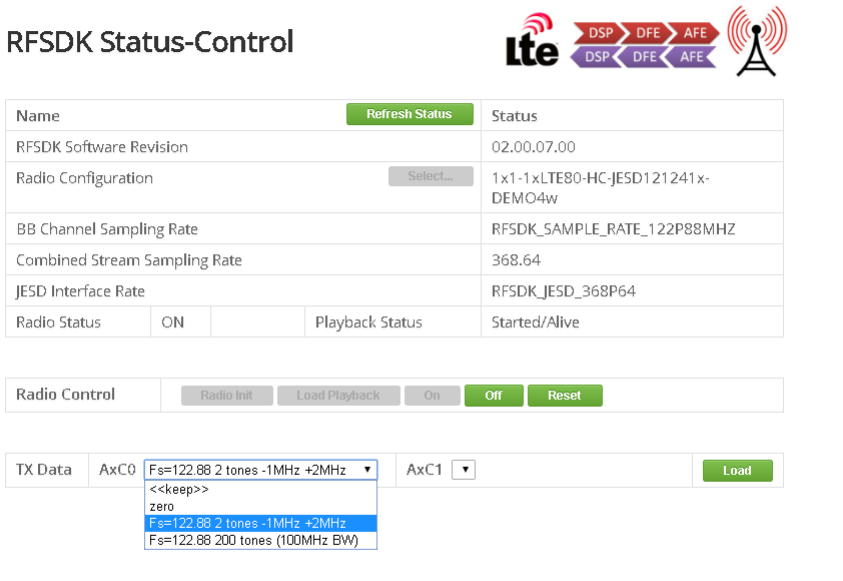

Figure 25. Loading Test Patterns – Wideband Demo

10. Navigate to the TX Signal Capture @ DSP page and press Refresh Capture. This sends a request to the DSP to perform a signal capture of the baseband data on the TX side (that is, before the signal data is sent to the DFE).

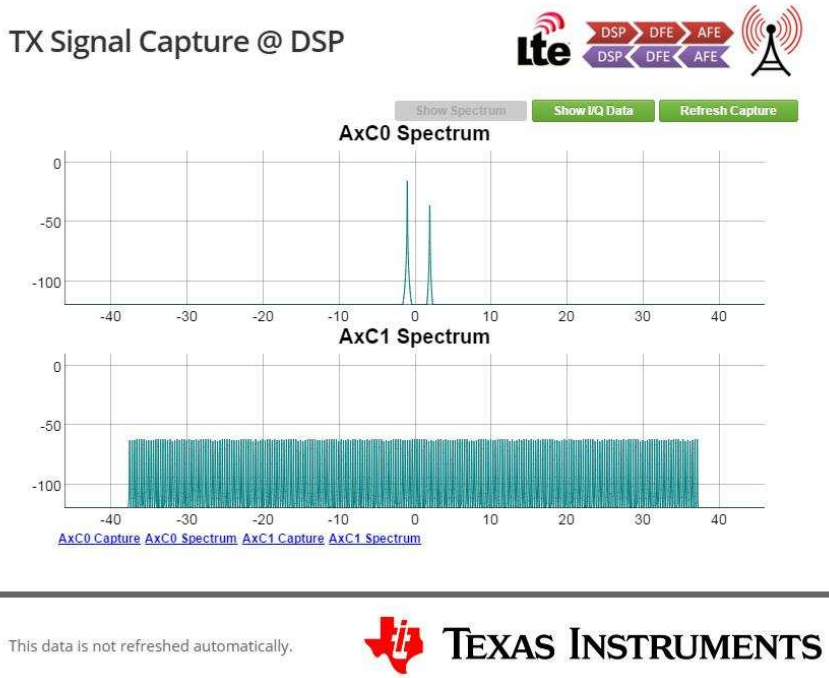

Figure 26. TX Signal Capture at DSP - Midband Demo

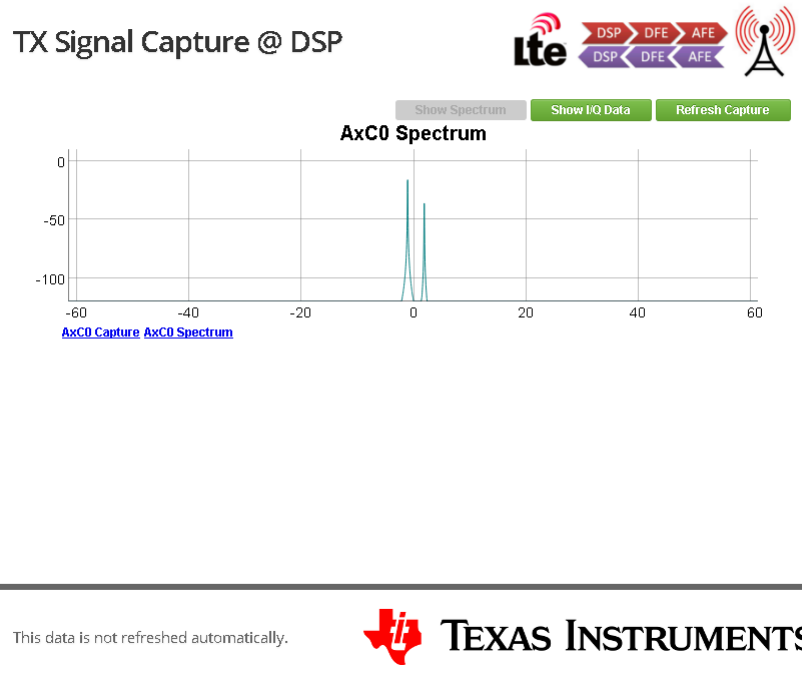

Figure 27. TX Signal Capture at DSP – Wideband Demo

11. Navigate to the RX Signal Capture @ DSP page and press Refresh Capture. This sends a request to the DSP to perform a signal capture of the baseband data on the RX side (that is, after it has been looped back from the DAC38J84 to the ADC32RF80 and after being down-converted and filtered by the DFE). The test pattern transmitted is recovered at the DSP after DAC38J84 to ADC32RF80 loopback. Figure 28 and Figure 29 show the RX Signal capture view.

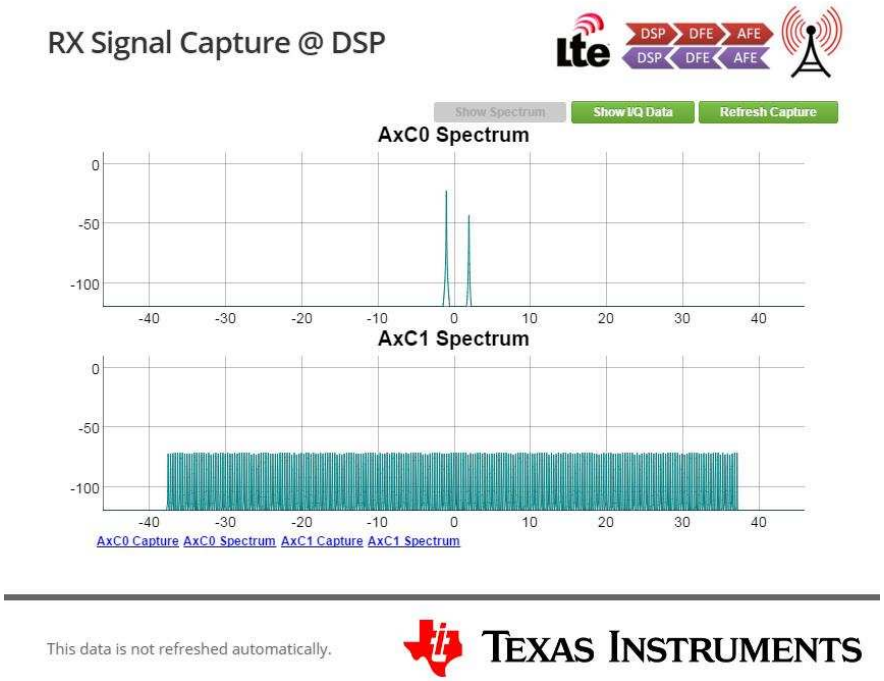

Figure 28. RX Signal Capture at DSP – Midband Demo

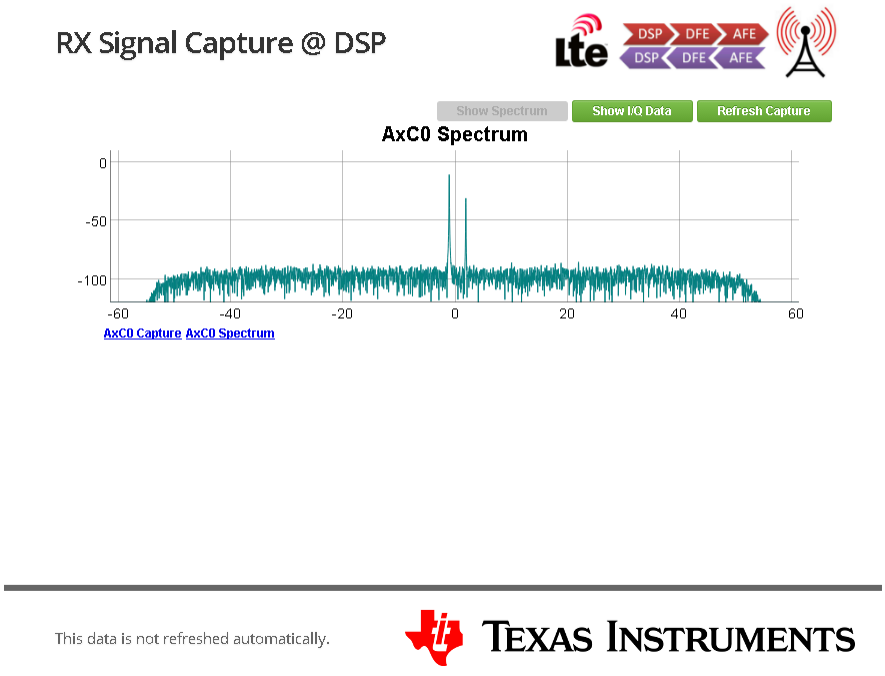

Figure 29. RX Signal Capture at DSP – Wideband Demo

12. The RX captured data is processed by FFTC co-processer and displayed under the Raw FFTC Output view as shown in Figure 30 and Figure 31 for midband and wideband demo, respectively.

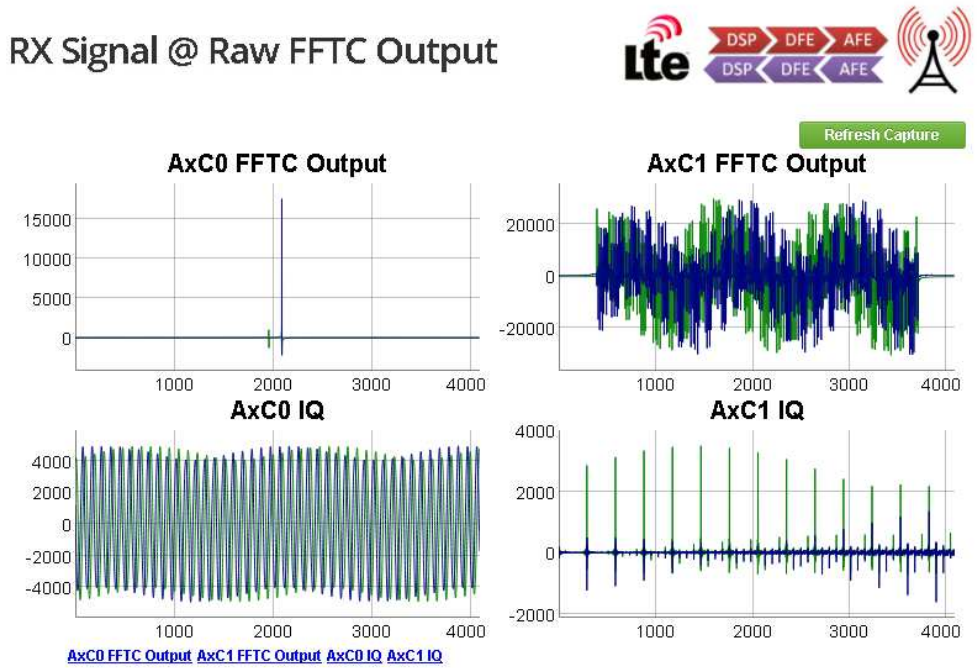

Figure 30. FFTC Output - Midband Demo

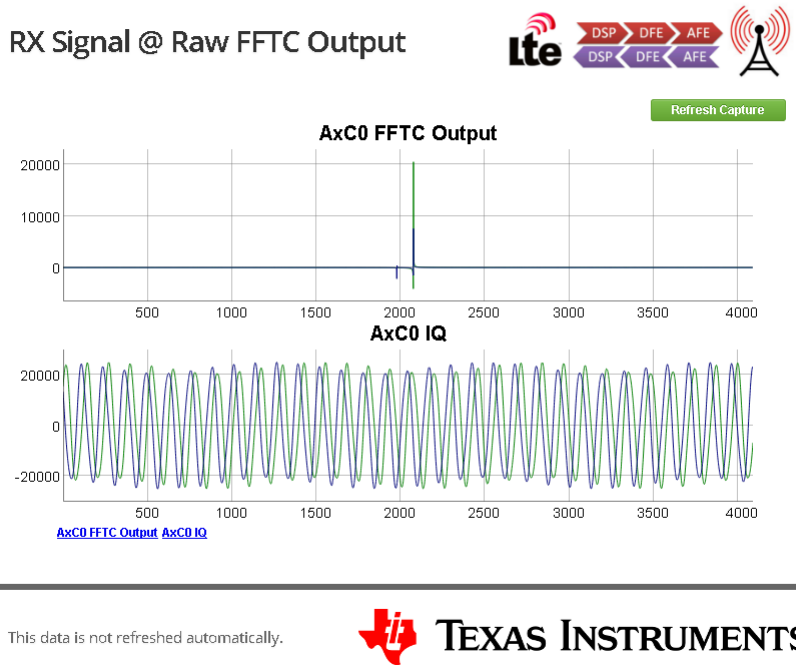

Figure 31. FFTC Output of Two-Tone Data - Wideband Demo

13. Drag the mouse to zoom-in on the graphs both vertically (to change the amplitude scale) and horizontally (to change the frequency scale). To view the zoom-in on the graphs, see Figure 32 and Figure 33.

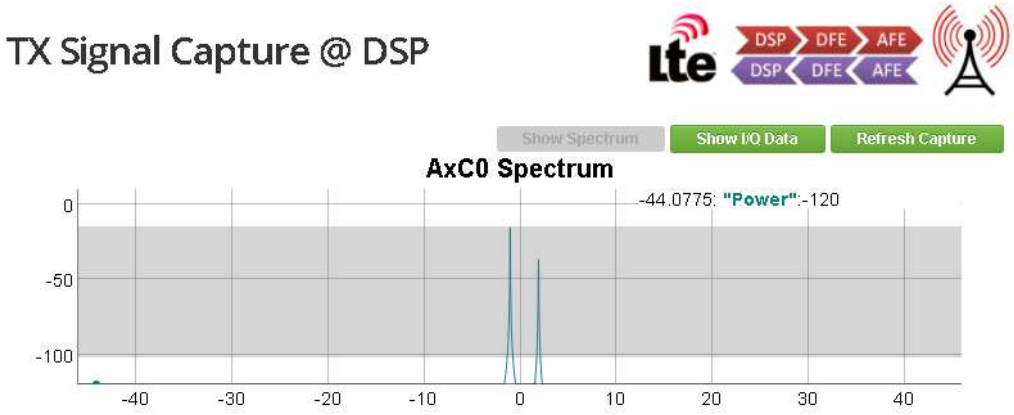

Figure 32. Changing Amplitude Scale on the GUI

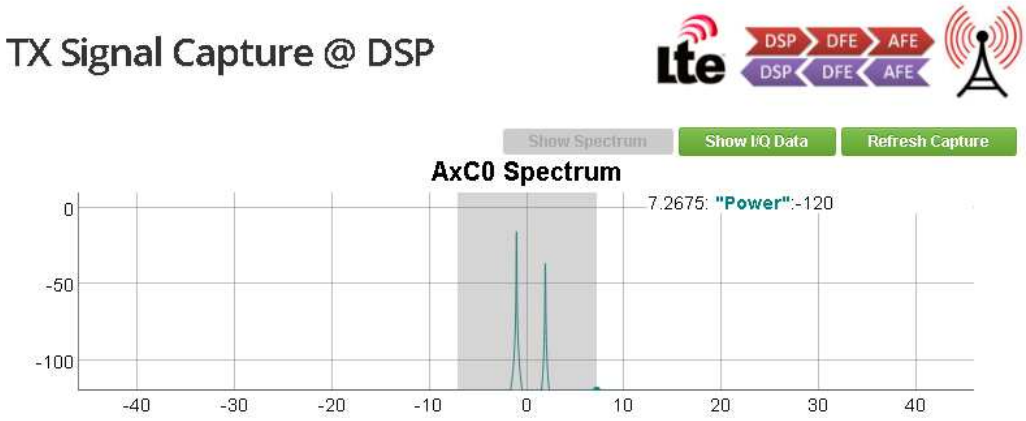

Figure 33. Changing Frequency Scale on the GUI

14. To stop the test, press “Off” (stop playback) and “Reset” (radio reset) buttons on the Status-Control page.

4 Test and Debug

It is recommended to check the DAC38J8x output using the spectrum analyzer for the first time setup. For midband demo, the signal has been mixed to 184.32 center frequency. The two-carrier (two-tone output and 240-tones output) spectrum is shown in the Figure 34. For wideband demo, the carrier is centered at 92.16 MHz, as shown in Figure 35 and Figure 36, two-tone and multi-tone carrier spectrum, respectively.

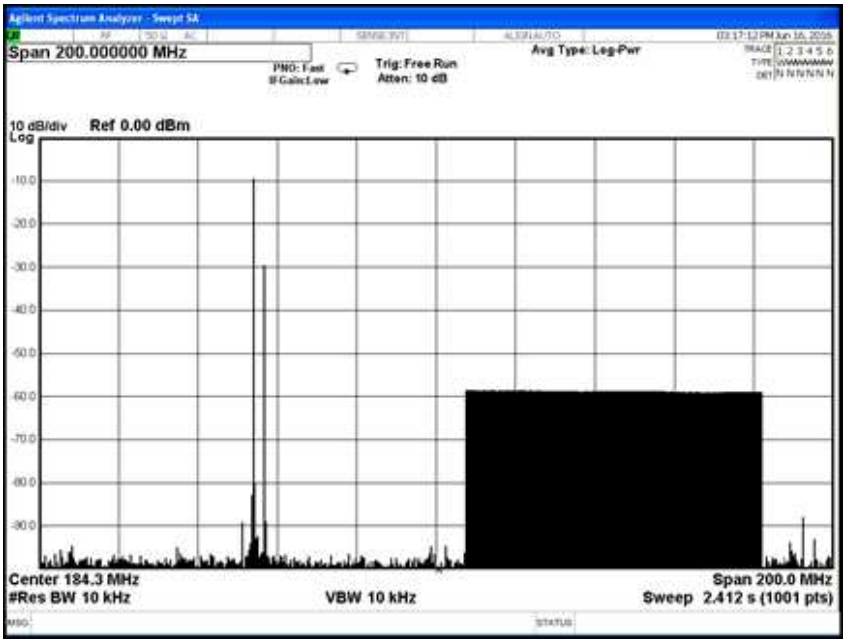

Figure 34. DAC Output – Two-Tone Data and 240-Tone Data

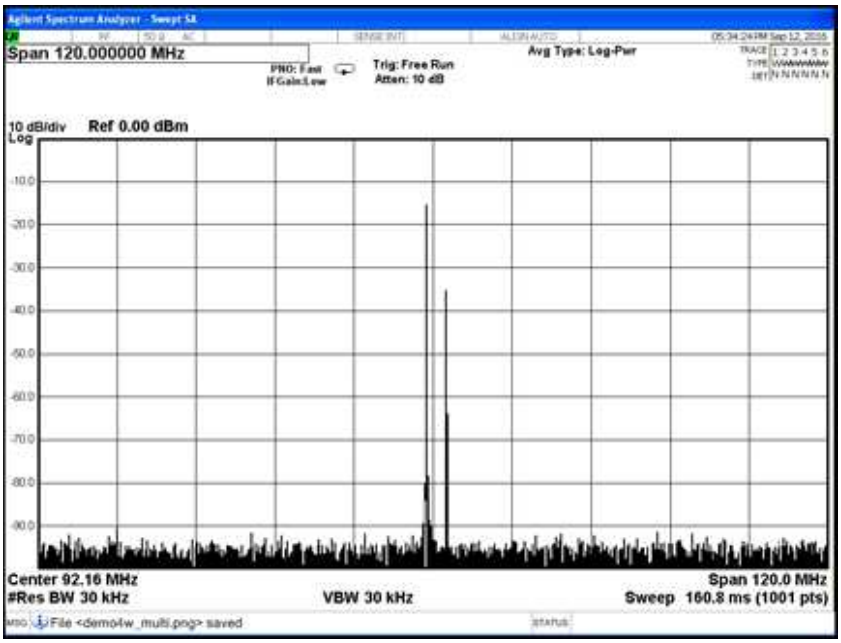

Figure 35. DAC Output Two Tone - Wideband Demo

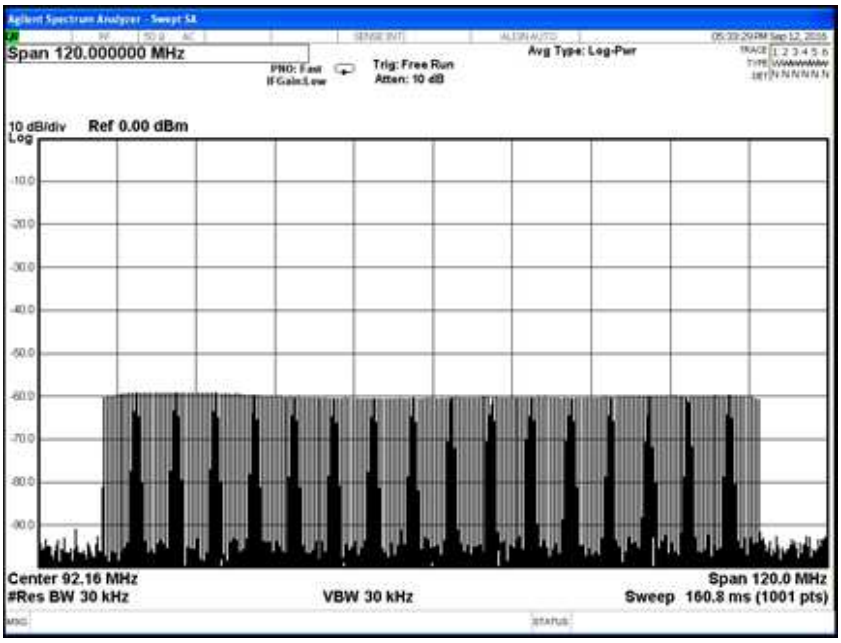

Figure 36. DAC Output Multi-Tone Signal - Wideband Demo

5 References

- 66AK2L06 EVM: https://www.einfochips.com/index.php/partnerships/texas-instruments/k2l-evm.html#5-resources
- DAC38J84 EVM: http://www.ti.com/tool/dac38j84evm
- ADC32RF45 EVM: http://www.ti.com/tool/adc32rf45evm
- Keystone-II MCSDK User Guide wiki
- Digital Front End (DFE) User Guide for Keystone II Devices User's Guide

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265