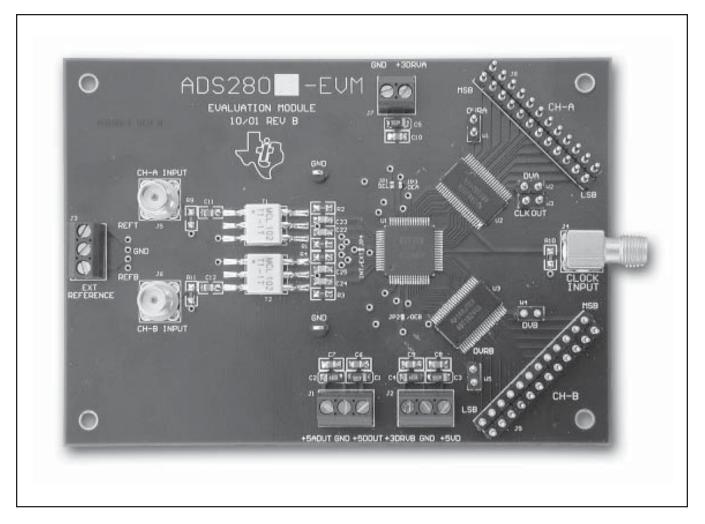


ADS280x-EVM

SBAU075A - FEBRUARY 2002 - REVISED AUGUST 2003



FEATURES

- PROVIDE FAST AND EASY PERFORMANCE TESTING FOR THE ADS2806 AND ADS2807
- SINGLE-ENDED AC-COUPLED INPUT
- SELECTABLE REFERENCE OPERATION: Internal or External
- SELECTABLE INPUT RANGE: 2Vpp or 3Vpp

DESCRIPTION

The ADS280x-EVM is designed for ease of use when evaluating the ADS2806 or the ADS2807 high-speed, dual channel Analog-to-Digital Converter (ADC). Both the ADS2806 and the ADS2807 offer 12 bits of resolution at sample rates of 32MHz and 50MHz, respectively. The evaluation module has been designed for ease of use with only a transformer-coupled input. The data outputs from the ADS280x converter are isolated from the output connectors by CMOS logic buffers.



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INITIAL CONFIGURATION

The ADS280x-EVM is designed to apply a differential signal to the ADC by utilizing a single-ended input coupled through a transformer. The input range of the ADS280x is user-selectable by the SEL jumper (J1). Table I shows the input configuration of the SEL jumper.

SEL (J1) CONNECTIONS			
2Vpp	No Connection		
3Vpp	Connected		

TABLE I. Input Range Selection.

The outputs from each channel of the ADS280x device can be enabled or disabled. In order for the outputs to be active, the $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ jumpers should be connected.

POWER SUPPLY

The evaluation module requires +5V for the analog circuitry of the ADS280x, +5V for the digital circuitry of the ADS280x, +5V for the digital output drivers (DRV) of the ADS280x, and +5V for the digital output buffers. Please note that the ADS280x devices are capable of running +3V supplies for the digital output drivers (DRV); however, the logic buffers supplied are +5V operation only. If +3V digital output levels are desired, the output logic buffers must be replaced with the SN74ALB16244DGGR. Three separate power connectors are on the board. The power supplies for the ADS280x are available on connector J1, with the analog supply labeled +5ADUT, the digital supply labeled +5DDUT and GND as the common ground. Connector J2, labeled with +3DRVB, GND, and +5VD, is the digital output supply for channel B of the ADS280x device, ground, and the digital supply to the output buffers. Connector J7, labeled with GND and +3DRVA, is ground and the digital output supply for channel A of the ADS280x device.

SIGNAL INPUT CONFIGURATION

The input configuration to the ADS280x-EVM utilizes transformers to change the single-ended inputs applied to J5 and J6 to differential inputs into the ADS280x.

CLOCK INPUT

The ADS280x-EVM requires an external clock applied to connector J4. This input represents a 50Ω impedance to the clock source. In order to preserve the specified performance of the ADS280x converter, the clock should contain very low jitter. This is particularly important if the device will be used in the evaluation of an undersampled system.

REFERENCE

The ADS280x-EVM is initially configured for operation from the internal reference. If external reference is desired, JP4 must be disconnected, JP5, JP6, JP7, and JP8 must be connected. The external reference voltages can then be applied to J3.

Note: External reference should be capable of driving a low impedance (typical 375Ω) load.

OVER-RANGE INDICATOR

The OVRA and OVRB indicators are used to show when the inputs the the ADS280x are over the selected input range. Refer to the ADS280x data sheet for a further explaination on the OVR indicators.

DATA VALID OUTPUTS

The DVA and DVB indicators are used to show when the data is valid and ready to be read.

DATA OUTPUT

The ADS280x uses Straight Offset Binary coding. CMOS buffers are used to isolate the outputs of the ADS280x device from the data bus.





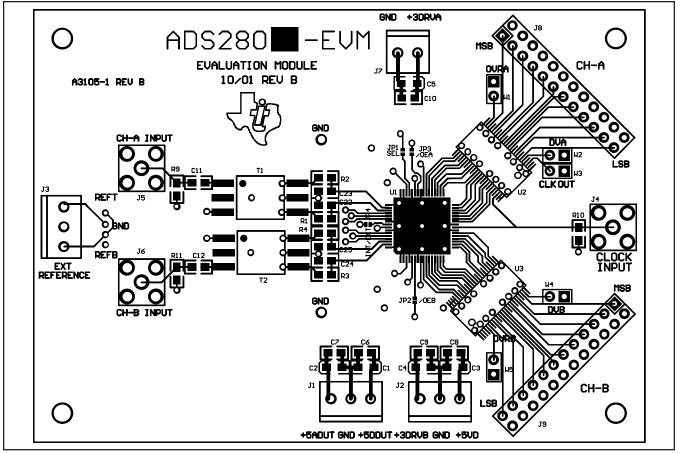


FIGURE 1. Top Layer with Silk Screen.

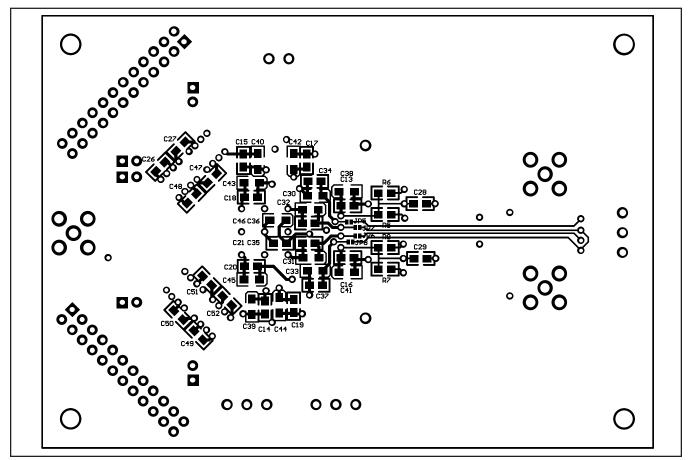


FIGURE 2. Bottom Layer with Silk Screen.



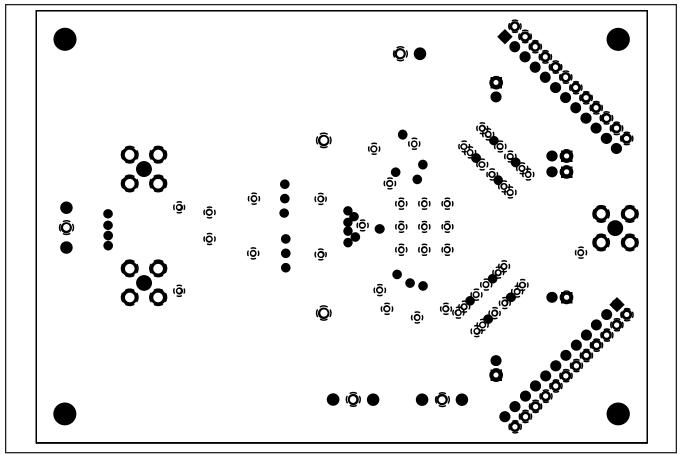


FIGURE 3. Ground Plane.

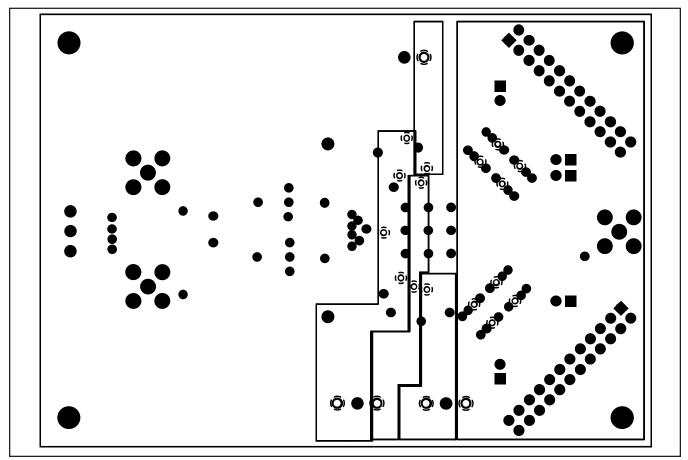


FIGURE 4. Power Plane.





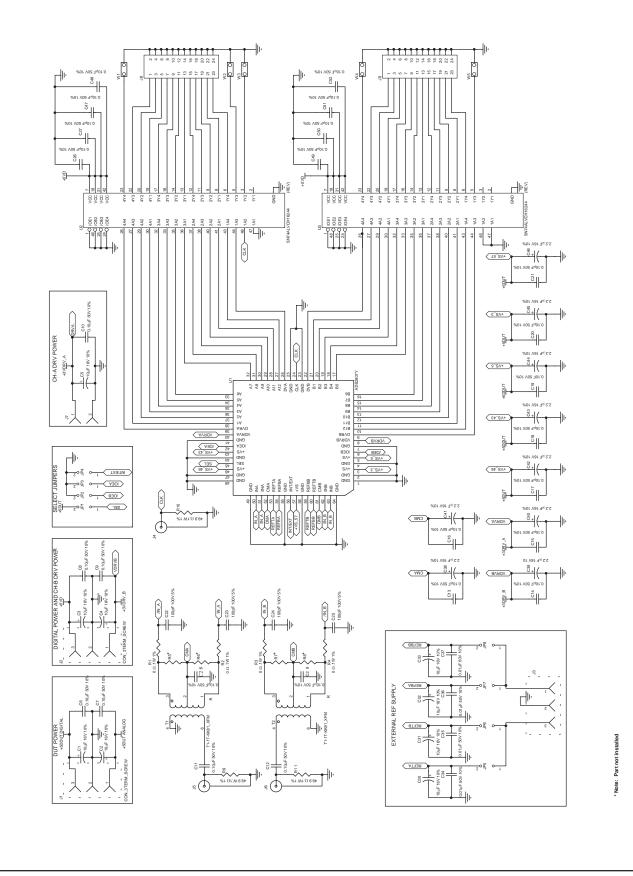


FIGURE 5. ADS2806, 2807-EVM Circuit Schematic.





BILL OF MATERIALS

USED	PART TYPE	DESIGNATOR	FOOTPRINT	DESCRIPTION	PART NUMBER
4	0.01µF 50V 10%	C34-C37	0805W	Multilayer Ceramic - 0805 Size	C0805C103K5RAC
26	0.10µF 50V 10%	C6-C21, C26-C29, C47-C52	0805W	Multilayer Ceramic	C0805C104K5RAC
4	100pF 100V 5%	C22-C25	805	Capacitor	C0805C101J1GAC
9	2.2µF 16V 10%	C38-C46	3216	Low Profile Tantalum Capacitor	T491B225K016AS
9	10µF 16V 10%	C1-C5, C30-C33	3216	Low Profile Tantalum Capacitor	T491B106K016AS
4	0Ω 0.1W 1%	R1-R4	0805W	1/10W 0805 Chip Resistor	CRCW0805000'
4	**NOT INSTALLED**	R5-R8	0805W	1/10W 0805 Chip Resistor	
3	49.9Ω 0.1W 1%	R9-R11	0805W	1/10W 0805 Chip Resistor	CRCW080549R9F
1	ADS2807Y	U1	64-PQFP (PM)	TI ADS280XY DUAL 12-BIT ADC	ADS280X
1	CON_2TERM_SCREW	J7	2P-TERM	2 Terminal Screw Connector	ED-1514-ND
3	CON_3TERM_SCREW	J1, J2, J3	3P-TERM	3 Terminal Screw Connector	ED-1515-ND
2	TERMINAL STRIP	J8, J9, W1-W5	—	32-Pin Terminal Strip (use as needed)	TS-132-G-A-2
1	SMA_PCB_MT	J4	SMA_JACK	SMA Right-Angle	142-0801-301
2	SN74ABT16244A	U2, U3	DGG	16-Bit Buffer	SN74ABT16244A
2	T1-1T-KK81_XFMR	T1, T2	T1-1T	RF Transformer MINI-Circuits T1-1T	T1-1T





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Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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