Texas Instruments

SRC4192EVM

Evaluation Module

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This document provides the information needed to setup and operate the SRC4192EVM evaluation module. For a more detailed description of the SRC4190, SRC4192, or SRC4193 products, please refer to the product data sheets available from the Texas Instruments web site at http://www.ti.com. Support documents are listed in the sections of this guide entitled Related Documentation from Texas Instruments and Additional Documentation.

How to Use This Manual

Throughout this document, the abbreviation EVM and the term *evaluation module* are synonymous with the SRC4192EVM. The abbreviation *SRC419x* refers to the SRC4190, SRC4192. and SRC4193 family of devices.

Chapter 1 provides an overview of the SRC419x family of stereo asynchronous sample rate converters. The SRC4192EVM block diagram and primary features are also discussed.

Chapter 2 provides general information regarding EVM handling and unpacking, absolute operating conditions, and the default switch and jumper configuration.

Chapter 3 is the hardware setup guide for the EVM, providing all of the necessary information needed to configure the EVM switches and jumpers for product evaluation.

Chapter 4 includes the EVM electrical schematic, PCB layout, and the Bill of Materials.

Information About Cautions and Warnings

This book contains cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the SRC4192EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision, which is current at the time of the writing of this User's Guide. Newer revisions may be available from the TI web site at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center at (972) 644–5580. When ordering, identify the booklet(s) by both title and literature number.

Data sheets	Literature number
SRC4192/4193 Data Sheet	SBFS022
DIT4192 Data Sheet	SBOS229
PLL1705 Data Sheet	SLES046
REG1117 Data Sheet	SBVS001
SN74AHC32	SCLS247G
SN74AHC244	SCLS226I
SN74AHC1G04	SCLS318L
SN74AHC1G14	SCLS321K
SN74ALVC125 Data Sheet	SCES110E
SN74ALVC244 Data Sheet	SCES188B
SN74ALVC245 Data Sheet	SCES271B
SN74CBTLV3245A Data Sheet	SCDS034J
SN74LVC04A Data Sheet	SCAS281M
SN74LVC1G07 Data Sheet	SCES296K
SN74LVC1G125 Data Sheet	SCES223G

Additional Documentation

The following documents provide information regarding selected non–TI components, which are used in the assembly of the SRC4192EVM. These documents are available from the corresponding manufacturers.

Document	Manufacturer
CS8414 Data Sheet	Cirrus Logic, http://www.cirrus.com
HCM49 Series Crystals	Citizen, http://www.citizencrystal.com
SC937–02 Data Sheet	Scientific Conversion http://www.scientificonversion.com
SC979–03 Data Sheet	Scientific Conversion http://www.scientificonversion.com

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Chapter 1

Introduction

This chapter provides a brief technical overview for the SRC4190, SRC4192, and SRC4193 asynchronous sample rate converters, as well as a general description and feature list for the SRC4192EVM.

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1.1 The SRC4190, SRC4192, and SRC4193

The SRC4192 and SRC4193 are stereo asynchronous sample rate converters designed for professional and broadcast audio applications. Operation at input and output sampling frequencies up to 212kHz is supported, with an input/output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and THD+N are achieved by employing high performance, linear phase digital filtering with better than 140dB of image rejection. The SRC4190 is a lower–cost version of the SRC4192 with reduced performance specifications, but it is functionally equivalent to the SRC4192 and shares the same pin configuration.

The SRC4190 and SRC4192 are both stand–alone, pin–programmed devices, with control inputs for mode, data format, mute, bypass, and low group delay functions. The SRC4193 includes a three–wire serial peripheral interface (SPI) port, which allows access to on–chip control registers for device function configuration. The SPI port can be easily interfaced to microprocessors or digital signal processors with synchronous serial port interfaces.

All three devices offer filtering options, which allow for lower group delay processing. These options include a low group delay mode for the interpolation function and a direct down–sampling mode (SRC4193 only) for the decimation function.

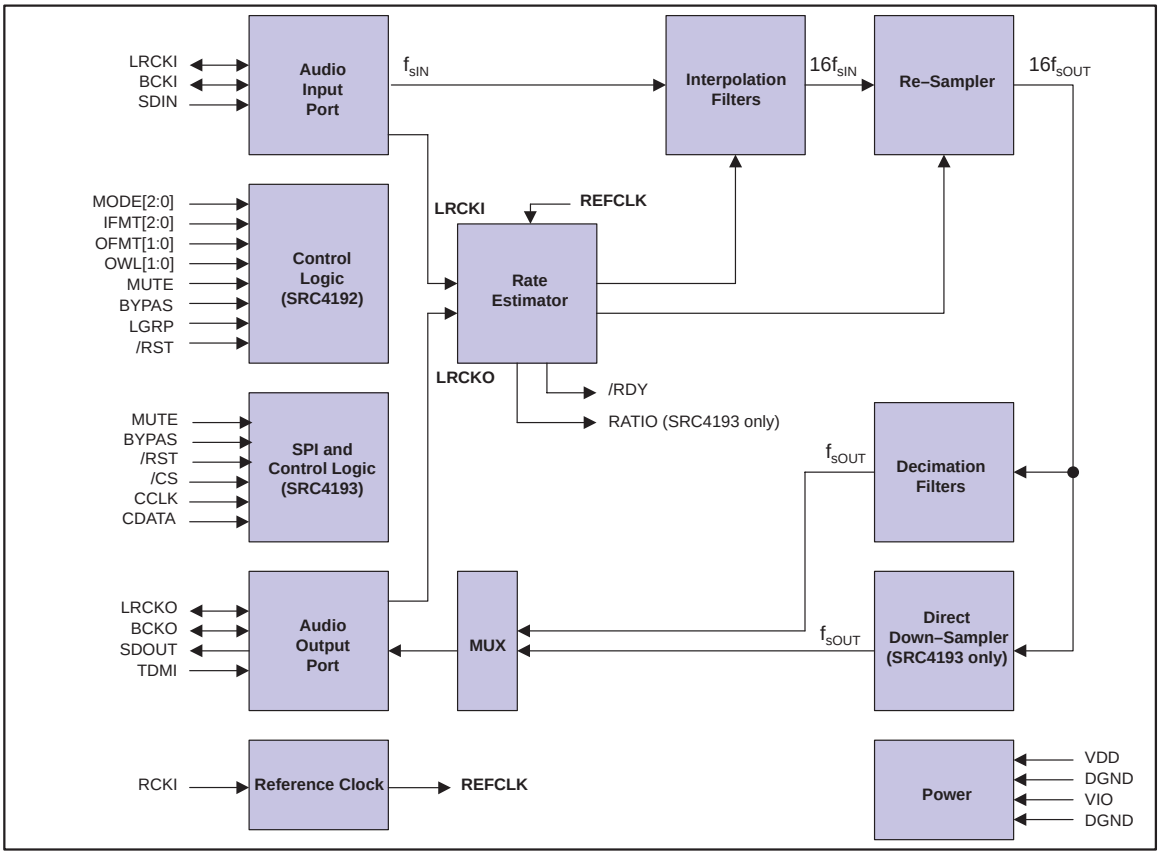
The audio input and output ports support standard audio data formats, as well as a TDM interface mode. Word lengths of 24–, 20–, 18–, and 16–bits are supported. Both ports may operate in Slave mode, deriving their word (LRCK) and bit (BCK) clocks from external input and output devices. Alternatively, one port may be operated in Master mode while the other remains in Slave mode. In Master mode, the LRCK and BCK clocks are derived from the reference clock (RCKI) input. The flexible configuration of the audio ports allows connection to a wide variety of audio data converters, digital audio interface devices, and digital signal processors.

A bypass mode is also included. This mode allows data to be passed directly from the audio input port to the audio output port, bypassing the sample rate converter function. The bypass option is useful for passing through encoded or compressed audio data, or non–audio control and status data. The input and output port clocks must be synchronous with one another in bypass mode.

A soft mute function is included in all three devices. A digital attenuation function is available only for the SRC4193. Both soft mute and digital attenuation functions provide artifact free operation, while allowing muting or level adjustment of the audio output signal. The mute attenuation is typically –144dB for the SRC4192 and SRC4193, and –128dB for the SRC4190. The SRC4193 digital attenuation function is adjustable from 0dB to –127.5dB in 0.5dB steps.

A block diagram of the SRC4192 and SRC4193 is shown in Figure 1–1. The SRC4190 offers the same functionality as the SRC4192.

Figure 1–1. Functional Block Diagram for the SRC4192 and SRC4193



1.2 EVM Block Diagram

The block diagram for the SRC4192EVM is shown in Figure 1–2. The EVM includes buffered audio input and output ports that support I^2S, Left Justified, Right Justified, and TDM data formats. These ports may be connected to external receivers and transmitters, data converters, or digital signal processors. An on–board 96kHz receiver is provided, as well as a 192kHz transmitter. The receiver and transmitter provide for convenient connection to both test and commercial audio equipment supporting AES3 or S/PDIF interfaces.

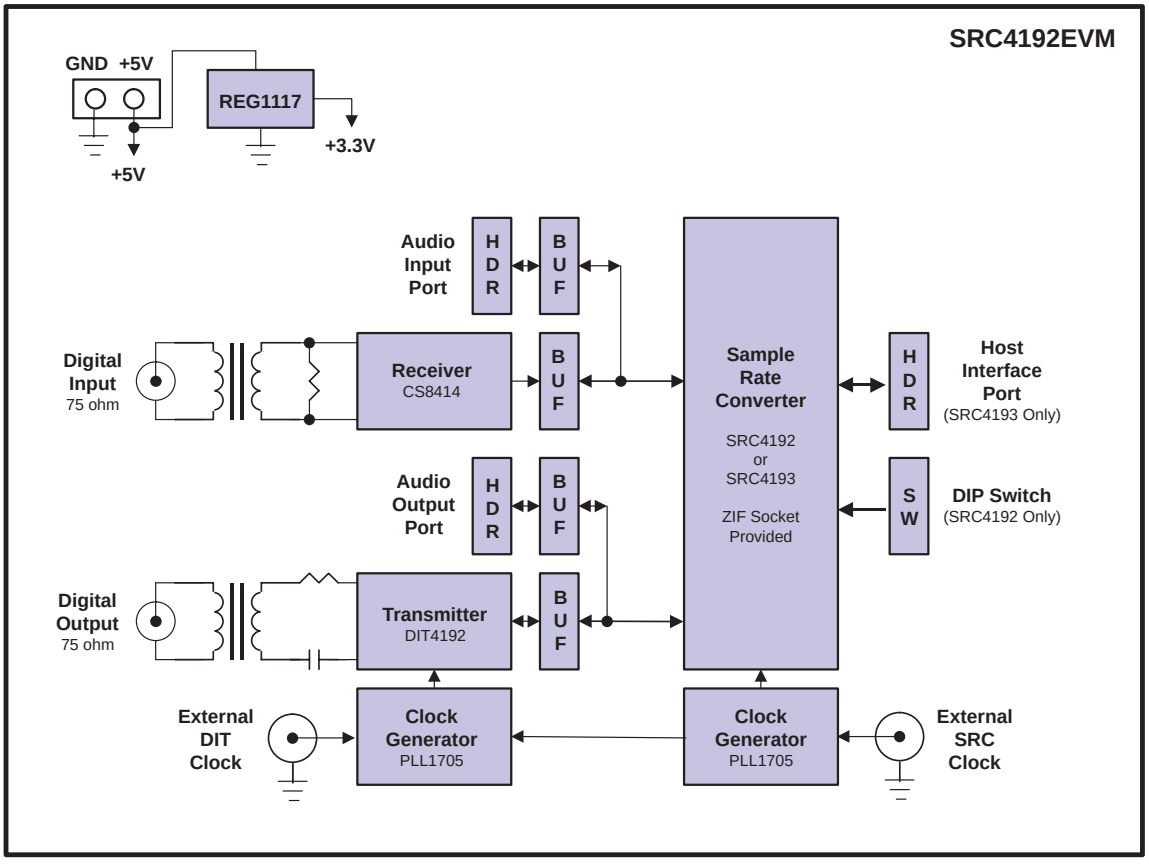
The SRC4192 and DIT4192 have their own external phase locked loop circuits for on–board clock generation. External clock inputs are also available and provide for additional flexibility. The EVM is configured using on–board switches and jumpers, in addition to a buffered host port, which supports the SRC4193 SPI interface. A single +5 volt power supply is all that is needed to power the EVM. A +3.3 volt supply is derived from the +5 volt supply using an on–board voltage regulator.

1.3 EVM Features

Key features for the SRC4192EVM include:

- ❑ Zero Insertion Force (ZIF) socket for easily interchanging SRC4190, SRC4192 and SRC4193 devices. The Analog Devices AD1895 and AD1896 are also supported for head–to–head testing.
- ❑ On–board or external clock generation.
- ❑ On–board receiver and transmitter supports AES3 input and output (75 Ω BNC connections provided).
- ❑ Buffered audio input and output ports using standard dual in–line headers.
- ❑ Buffered Host Port supports connection to an external controller (SRC4193 only).
- ❑ Operation from a single +5 volt power supply.

Figure 1–2. Functional Block Diagram for the SRC4192EVM



Chapter 2

Getting Started

This chapter provides information regarding SRC4192EVM handling and unpacking, absolute operating conditions, and a description of the factory default switch and jumper configuration.

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2.1 Electrostatic Discharge Warning

Many of the components on the SRC4192EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

Caution: Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Absolute Maximum Operating Conditions

The user should be aware of the absolute maximum operating conditions for the SRC4192EVM. Exceeding these conditions may result in damage to the EVM. Table 2–1 summarizes the critical data points.

Table 2–1. Absolute Maximum Operating Conditions

Parameter	Maximum Condition
Power Supply	+5.5 VDC maximum
Audio Input and Output Ports, Host Port, External SRC Clock, External DIT Clock	
V_{IH}	+4.0 Volts maximum
V_{IL}	–0.5 Volts minumum
Digital Audio Input (Connector J2)	
V_{IH}	+12 Volts maximum
V_{IL}	–12 Volts minumum

2.3 Unpacking the EVM

Upon opening the SRC4192EVM package, please check to make sure that the following items are included:

- ❑ One SRC4192EVM.
- ❑ One SRC4192IDB installed in the EVM ZIF socket.

If either of these items are missing, please contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

2.4 Default Configuration

The factory default switch and jumper settings are shown in Table 2, and result in the following EVM configuration:

- ❑ The SRC4192 Input Port is set to Slave mode, with the CS8414 receiver selected as the input source.
- ❑ The SRC4192 Output Port is set to Slave mode, with the DIT4192 transmitter selected as the output device.
- ❑ The SRC PLL (U16) is selected as the SRC419x reference clock source and is set to 24.576MHz.
- ❑ The SRC4192 input and output port data formats are set to 24–Bit Left Justified.
- ❑ The CS8414 receiver output format is set to 24–Bit Left Justified
- ❑ The DIT4192 transmitter input format is set to 24–Bit Left Justified
- ❑ The DIT4192 transmitter MCLK frequency is set to 256fs, with fs = 48kHz.
- ❑ The transmitter PLL (U6) is selected as the DIT4192 MCLK source and is set to 12.288MHz.
- ❑ The DIT4192 transmitter output mode is set to stereo.
- ❑ The SRC4192 Low Group Delay, Bypass, and Mute modes are all disabled.

Table 2–2. Default Switch and Jumper Settings

SW1	Set To:	SW3	Set To:	SW6	Set To:	SW7	Set To:
M0	LO	CLK1	LO	TSR	LO	LGRP	LO
M1	LO	CLK0	HI	TFS2	LO	BYPAS	LO
M2	LO	FMT0	LO	TFS1	LO	IFMT0	LO
		FMT1	LO	TPLL	LO	IFMT1	LO
						IFMT2	LO
						MUTE	LO
						~4193	HI
						IS/M	HI

SW9	Set To:	SW10	Set To:	J8	Set To:
SFS1	LO	MODE2	LO	1–2 (I2S/RJ)	OPEN
SFS2	LO	MODE1	LO		
SSR	HI	MODE0	LO	3–4 (LJ)	SHORT
~PLL	LO	~PORT	HI		
OM/~S	LO	OFMT0	LO		
~IPORT	HI	OFMT1	LO		
MONO	LO	OWL0	LO		
MDAT	LO	OWL1	LO		

Chapter 3

Setup Guide

This chapter provides a step–by–step guide to configuring the SRC4192EVM for device evaluation. Follow the sections to walk through the setup of the SRC4192EVM.

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3.1 Power Supply Configuration

The SRC4192EVM requires a single +5 volt regulated dc power supply, connected at the +5V terminal of J9. The GND terminal of J9 should be connected to the power supply ground or common terminal. The supply should not be connected to terminal block J9 while hot, as damage may occur to the EVM. At no time should the power supply exceed the absolute maximum rating.

3.2 Device Selection

The ~4193 element of switch SW7 is utilized to select the device under test.

When ~4193 is set to LO, the EVM is configured for the SRC4193. The SRC4193 is a software–controlled device, which employs an SPI port to access internal control registers. The SPI port is accessed through the buffered Host Port at connector J5. The Host Port supports connection to an external microprocessor or DSP for host control.

When ~4193 is set to HI, the EVM is configured for the SRC4190 or SRC4192. These units are stand–alone devices and do not require an external host for operation. The user configures the EVM by means of the on–board switches and jumpers. The Analog Devices AD1895 and AD1896 are also supported in this mode, enabling head–to–head comparison testing.

3.3 Selecting the Input & Output Port Modes

The input and output ports of the SRC419x devices support seven modes of operation. Table 3–1 summarizes the mode settings for the SRC419x devices. In Master mode, the LRCK and BCK clocks are outputs, derived from the reference clock (RCKI) input. In Slave mode, the LRCK and BCK clocks are inputs, which are generated by the audio input or output device.

When ~4193 is set to HI, the port modes are selected using the MODE0, MODE1, and MODE2 elements of switch SW10.

When ~SRC4193 is set to LO, the MODE[2:0] bits in Control Register 1 of the SRC4193 are used to select the port modes.

Table 3–1. SRC419x Input & Output Port Mode Selection

MODE2	MODE1	MODE0	Serial Port Mode
LO	LO	LO	Both Input and Output Ports are in Slave mode
LO	LO	HI	Output Port is in Master mode with RCKI = $128f_S$
LO	HI	LO	Output Port is in Master mode with RCKI = $512f_S$
LO	HI	HI	Output Port is in Master mode with RCKI = $256f_S$
HI	LO	LO	Both Input and Output Ports are in Slave mode
HI	LO	HI	Input Port is in Master mode with RCKI = $128f_S$
HI	HI	LO	Input Port is in Master mode with RCKI = $512f_S$
HI	HI	HI	Input Port is in Master mode with RCKI = $256f_S$

3.4 Selecting the Input & Output Data Formats

The SRC419x devices support a flexible set of audio data formats. Table 3–2 summarizes the input and output format options for the sample rate converters. Section 3.5 of this chapter describes the format configuration for the digital audio receiver and transmitter devices.

When ~4193 is set to HI, the IFMT0, IFMT1 and IFMT2 elements of switch SW7 are used to select the input port data format. The OFMT0, OFMT1, OWL0, and OWL1 elements of switch SW10 are used to select the output port data format and word length.

When ~4193 is set to LO, Control Register 3 of the SRC4193 is used to select the input and output data formats.

Table 3–2. SRC419x Input & Output Port Data Format Configuration

IFMT2	IFMT1	IFMT0	Input Port Data Format
LO	LO	LO	24–Bit Left Justified
LO	LO	HI	24–Bit I^2S
LO	HI	LO	Unused
LO	HI	HI	Unused
HI	LO	LO	16–Bit Right Justified
HI	LO	HI	18–Bit Right Justified
HI	HI	LO	20–Bit Right Justified
HI	HI	HI	24–Bit Right Justified

OFMT1	OFMT0	Output Port Data Format
LO	LO	Left Justified
LO	HI	I^2S
HI	LO	TDM
HI	HI	Right Justified

OWL1	OWL0	Output Port Data Word Length
LO	LO	24–Bits
LO	HI	20–Bits
HI	LO	18–Bits
HI	HI	16–Bits

3.5 Selecting an Input Source and an Output Port

The ~IPORT element of switch SW9 is utilized to select the input source.

When ~IPORT is set to LO, the buffered Audio Input Port at connector J1 is selected as the input source. This port is designed to interface to devices that support Left Justified, Right Justified, and I^2S formatted digital audio data.

When selecting the Audio Input Port as the input source, the IS/~M element of switch SW7 must be set to match the mode of the SRC419x input port (Master or Slave), as described in Section 3.3 of this chapter. The data format of the external audio device must be set to match the format of the Audio Input Port.

When ~IPORT is set to HI, connector J2 at the input of the CS8414 digital audio receiver (U1) is selected as the input source. This port is designed to interface to digital audio signal generators and devices that output AES3 formatted digital audio data. This includes the S/PDIF outputs of CD and DVD players.

When selecting the digital audio receiver (U1) as the input source, the IS/~M element of switch SW7 must be set to LO (Slave mode), and the SRC419x input port must be set to Slave mode, as described in Section 3.3 of this chapter. The output data format of the digital audio receiver must be selected using switch SW1 and jumper block J8. The receiver output format must match the input data format of the SRC419x device, as described in Section 3.4 of this chapter. Table 3–3 summarizes the configuration of switch SW1 and jumper block J8 for the supported data formats.

Table 3–3. Digital Audio Receiver Output Data Format Configuration

M2	M1	M0	J8	Data Format
LO	LO	LO	Short 3–4 (LJ)	Left Justified, 16– to 24–Bits
LO	HI	LO	Short 1–2 (I2S/RJ)	Philips I^2S, 16– to 24–Bits
HI	LO	HI	Short 1–2 (I2S/RJ)	Right Justified, 16–Bits
HI	HI	LO	Short 1–2 (I2S/RJ)	Right Justified, 18–Bits

The ~PORT element of switch SW10 is utilized to select the output port.

When ~PORT is set to LO, the buffered Audio Output Port at connector J3 is selected as the output port. This port is designed to interface to devices that support Left Justified, Right Justified, and I^2S formatted digital audio data.

When selecting the Audio Output Port as the output port, the OM/~S element of switch SW9 must be set to match the mode of the SRC419x output port (Master or Slave), as described in Section 3.3 of this chapter. The data format of the external audio device must be set to match the format of the Audio Output Port.

When ~PORT = HI, the output of the DIT4192 digital audio transmitter (U5) at connector J4 is selected as the output port. This port is designed to interface to digital audio signal analyzers and devices that accept AES3 formatted digital audio data. This includes the S/PDIF inputs of A/V receivers and digital recording devices.

When selecting the digital audio transmitter (U5) as the output port, the setting of the OM/~S element of switch SW9 will correctly set the Master or Slave mode for both the SRC419x and DIT4192 devices. The input data format of the transmitter must be selected using the FMT0 and FMT1 elements of switch SW3. The format must match the output data format of the SRC419x device, as described in Section 3.4 of this chapter. Table 3–4 summarizes the transmitter format configuration options using switch SW3.

Table 3–4. Digital Audio Transmitter Input Data Format Configuration

FMT1	FMT0	Data Format
LO	LO	Left Justified, 16– to 24–Bits
LO	HI	Philips I^2S, 16– to 24–Bits
HI	LO	Right Justified, 24–Bits
HI	HI	Right Justified, 16–Bits

3.6 Selecting the SRC419x Reference Clock Source and Frequency

The ~PLL element of switch SW9 is used to select the reference clock source for the SRC419x. The reference clock input is utilized by the SRC419x rate estimator, as well as the input or output port when configured in Master mode. The Master mode port derives the LRCK and BCK clock outputs from the reference clock input.

When ~PLL is set to LO, the PLL1705 (U16) is selected as the reference clock source for the SRC419x. Table 3–5 summarizes the output rate selections for the PLL1705.

When ~PLL is set to HI, the EXT SRC CLK input (J6) is selected as the reference clock input. The EXT SRC CLK input supports +3.3V CMOS external clock sources with frequencies up to 50MHz.

Table 3–5. PLL Reference Clock Selection for the SRC419x

SSR	SFS2	SFS1	PLL Output Rate (MHz)
LO	LO	LO	12.288
LO	LO	HI	11.2896
LO	HI	LO	8.192
LO	HI	HI	Reserved
HI	LO	LO	24.576
HI	LO	HI	22.5792
HI	HI	LO	16.384
HI	HI	HI	Reserved

3.7 Selecting the DIT4192 Master Clock Source and Frequency

The OM/~S element of switch SW9 and the ~TPLL element of SW6 are used to select the master clock source for the DIT4192 digital audio transmitter. The master clock (or MCLK) frequency determines the output frame (or sampling) rate of the transmitter, in addition to determining the SYNC and SCLK output rates when the DIT4192 is configured in Master mode. Table 3–6 summarizes the DIT4192 master clock source options.

When OM/~S is set to HI (that is, the SRC419x output port is the Master and the DIT4192 is a Slave), the reference clock source for the SRC419x will also be used as the master clock source for the DIT4192. This ensures synchronization between the SRC419x output port and DIT4192 audio serial port.

Table 3–6. DIT4192 Master Clock Selection

~TPLL	OM/~S	DIT4192 MCLK Source
LO	LO	PLL1705 (U6)
HI	LO	EXT DIT CLK (J7)
X	HI	SRC419x Ref Clock

X = Don't Care

When OM/~S is set to LO (that is, the SRC419x output port is a Slave and the DIT4192 is the Master), the ~TPLL element of switch SW6 is utilized to select the DIT4192 master clock source, as shown in Table 3–6.

When the PLL1705 (U6) is selected as the master clock source, the TSR, TFS1, and TFS2 elements of switch SW6 are utilized to select the PLL output rate. Table 3–7 summarizes the PLL output rate options.

Table 3–7. PLL Master Clock Source Selection for the DIT4192

TSR	TFS2	TFS1	PLL Output Rate (MHz)
LO	LO	LO	12.288
LO	LO	HI	11.2896
LO	HI	LO	8.192
LO	HI	HI	Reserved
HI	LO	LO	24.576
HI	LO	HI	22.5792
HI	HI	LO	16.384
HI	HI	HI	Reserved

When the EXT DIT CLK input at connector J7 is selected as the master clock source, the device will support an external +3.3V CMOS logic level clock source with frequencies up to 25MHz.

In addition to DIT4192 master clock source selection, the DIT4192 master clock divider must be selected using the CLK0 and CLK1 elements of switch SW3. The master clock source frequency will be divided by the factor listed in Table 3–8 to determine the transmitter output frame rate, as well as the SYNC and SCLK clock rate when the DIT4192 is configured in Master mode.

Table 3–8. PLL Master Clock Selection for the DIT4192

CLK1	CLK0	DIT4192 MCLK Divider
LO	LO	Divide by 128
LO	HI	Divide by 256
HI	LO	Divide by 384
HI	HI	Divide by 512

3.8 Miscellaneous Functions

This section provides information regarding several SRC419x and DIT4192 functions not described previously in this chapter.

Low group delay operation is controlled using the LGRP element of switch SW7, or by the LGRP bit in Control Register 2 when using the SRC4193. The low group delay option reduces the overall latency of the interpolation filter by $32/f_{sIN}$, where f_{sIN} is the input sampling rate in hertz (Hz). Table 3–9 summarizes Low Group Delay operation.

Table 3–9. Low Group Delay Configuration

LGRP	Low Group Delay Mode
LO	Disabled
HI	Enabled

Bypass mode operation is controlled using the BYPAS element of switch SW7, or by the BYPAS bit in Control Register 1 when using the SRC4193. When Bypass mode is enabled, the audio data is passed directly from the input port to the output port without sample rate conversion. This process is useful for passing through encoded audio or non–audio data. In Bypass mode, the mute, dithering, and digital attenuation (SRC4193 only) functions are not available. Table 3–10 summarizes Bypass mode operation.

Table 3–10. Bypass Mode Configuration

BYPAS	Bypass Mode
LO	Disabled
HI	Enabled

The Mute function is controlled using the MUTE element of switch SW7, or by the MUTE bit of Control Register 1 when using the SRC4193. This function employs a soft mute technique, which provides for artifact–free muting of the SRC419x output port. Table 3–11 summarizes Mute function operation.

Table 3–11. Mute Function Configuration

MUTE	Soft Mute Function
LO	Disabled
HI	Enabled

A Direct Down–Sampling option is available only when using the SRC4193. It is accessed using the DFLT bit in Control Register 2. Refer to the SRC4192/4193 data sheet for more details regarding the use of this mode.

The DIT4192 digital audio transmitter supports Single Channel Double Frequency operation, also referred to as Mono mode in the DIT4192 data sheet. In this mode, the DIT4192 output frame rate is one half the input SYNC clock rate, with two consecutive samples of a single channel replacing the Left and Right channel samples of the normal Stereo mode transmission. This mode is useful when testing 176.4kHz and 192kHz sampling rates on an Audio Precision System Two Cascade/Cascade Plus Dual Domain system, configured in Dual Channel mode. Only one channel at a time may be tested in this fashion.

The MONO and MDAT elements of switch SW9 are utilized to configure Mono mode operation. Table 3–12 summarizes the MONO and MDAT options.

Table 3–12. DIT4192 Mono Mode Configuration

Mono	Stereo/Mono Mode Operation
LO	Stereo
HI	Mono

MDAT	Audio/Channel Status Data Selection
LO	Left Channel Audio Data / Channel A CS Data
HI	Right Channel Audio Data / Channel B CS Data

3.9 Reset Functions

The SRC4192EVM includes three reset switches, one each for the SRC419x (SW8), the CS8414 receiver (SW2), and the DIT4192 transmitter (SW4). Each switch is a momentary contact, normally open push–button with 10kΩ pull–up resistors to the +3.3V supply. To reset a device, momentarily press, then release, the corresponding reset switch. This allows the user to reset the devices at will, if necessary or desired.

Chapter 4

Schematic, PCB Layout and Bill of Materials

This chapter provides the electrical and physical layout information for the SRC4192EVM. The bill of materials is included for component and manufacturer reference.

The schematic diagram is shown, beginning on page 4-2. The printed circuit board layouts are shown on pages 4-4 through 4-6. The bill of materials is shown starting on page 4-7.

Topic **Page**

4.1 Schematic

The complete electrical schematics of for the SRC4192EVM are shown in Figure 4–1 and Figure 4–2.

Figure 4–1. SRC4192EVM Schematic Diagram (page 1 of 2)

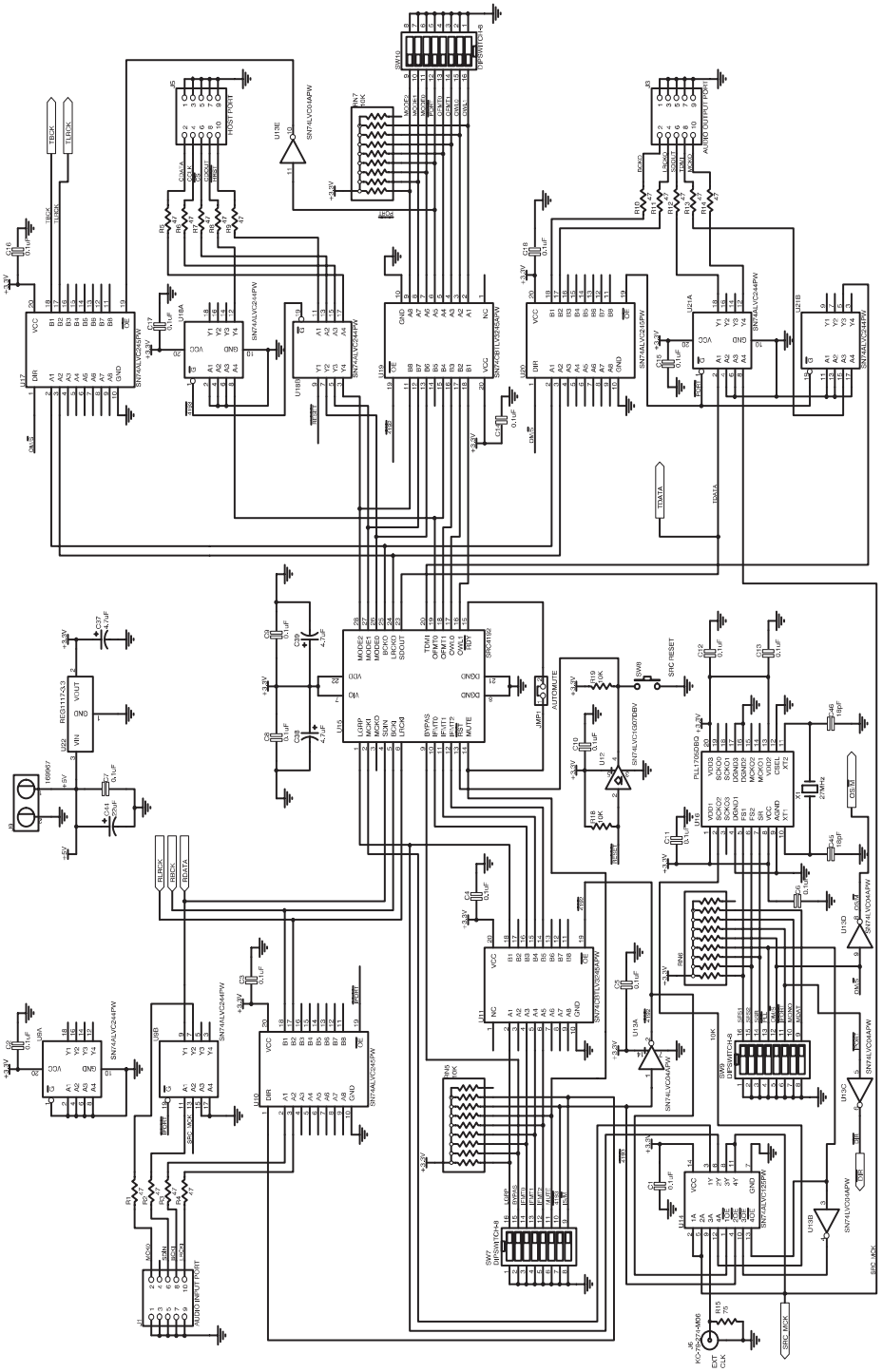
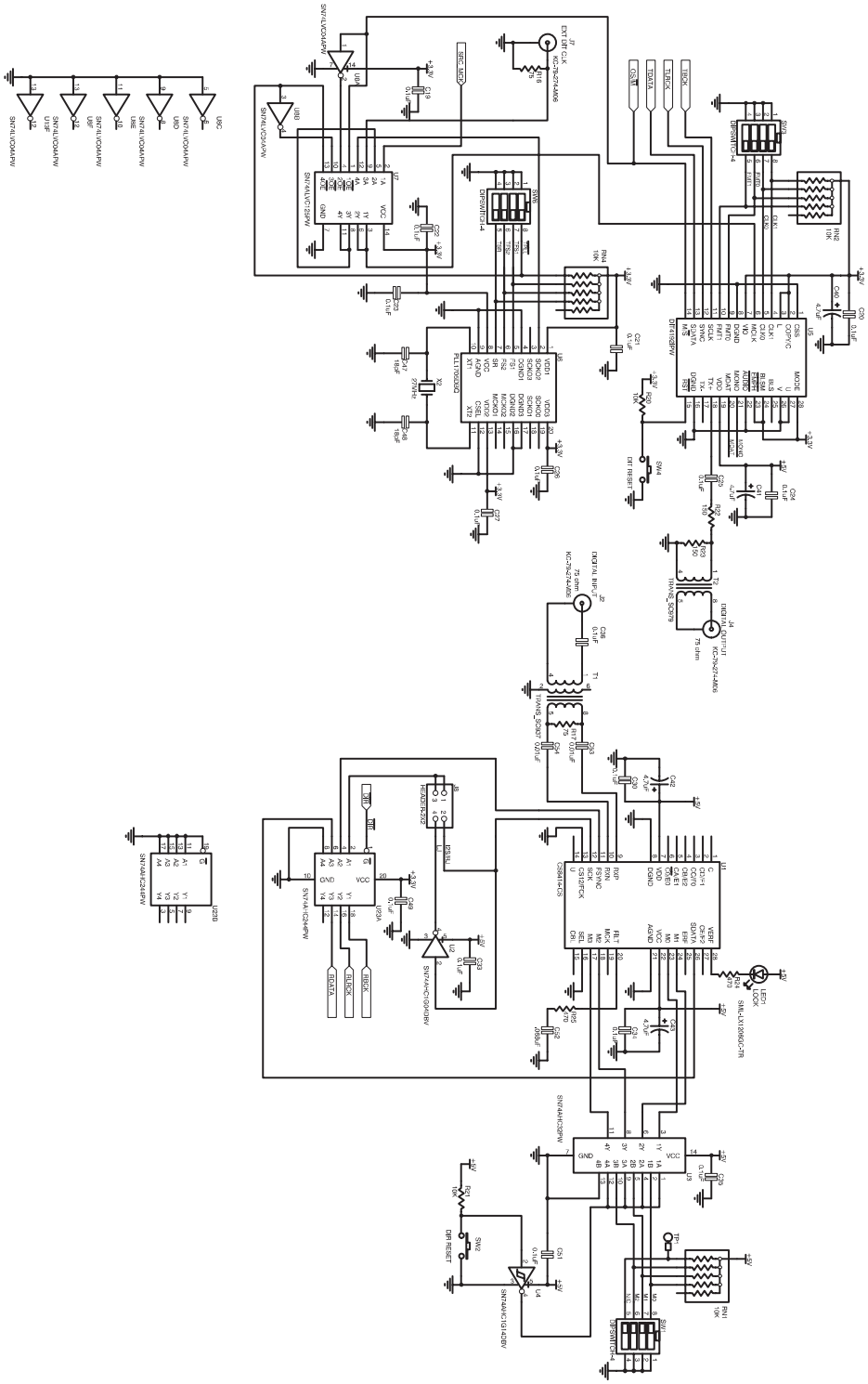


Figure 4–2. SRC4192EVM Schematic Diagram (page 2 of 2)



4.2 Component Layout

The printed circuit board plots for the SRC4192EVM are shown in Figure 4–3 through Figure 4–5. The PCB is a two–layer board, with most components mounted on the top (or component) side. The power supply bypass capacitors for U15 are mounted on the bottom (or solder) side of the PCB.

Figure 4–3. PCB Silkscreen, Top Layer

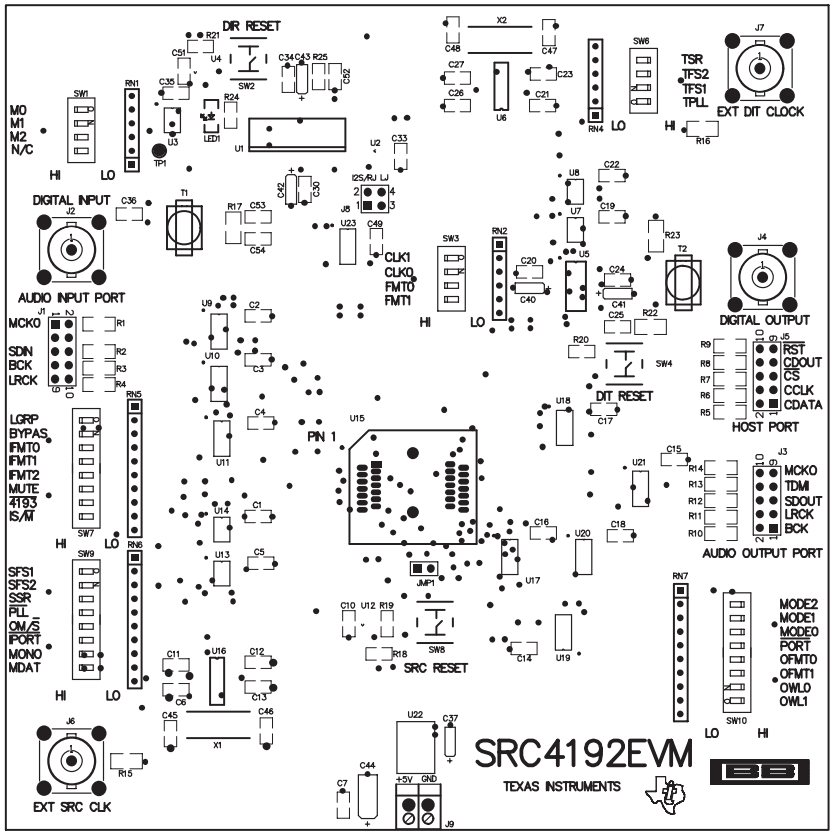


Figure 4–4. Top Side Layout (Component Side)

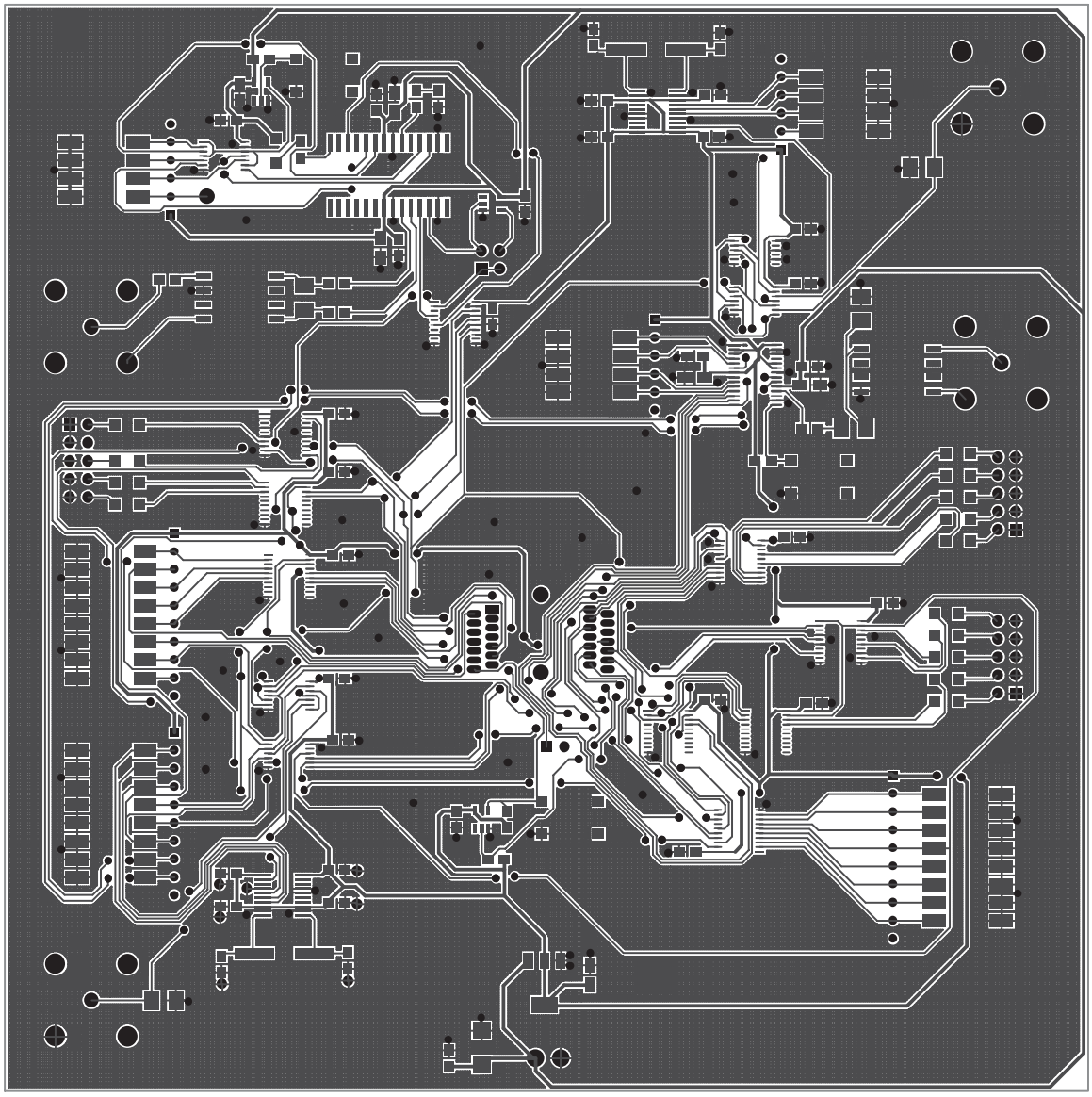
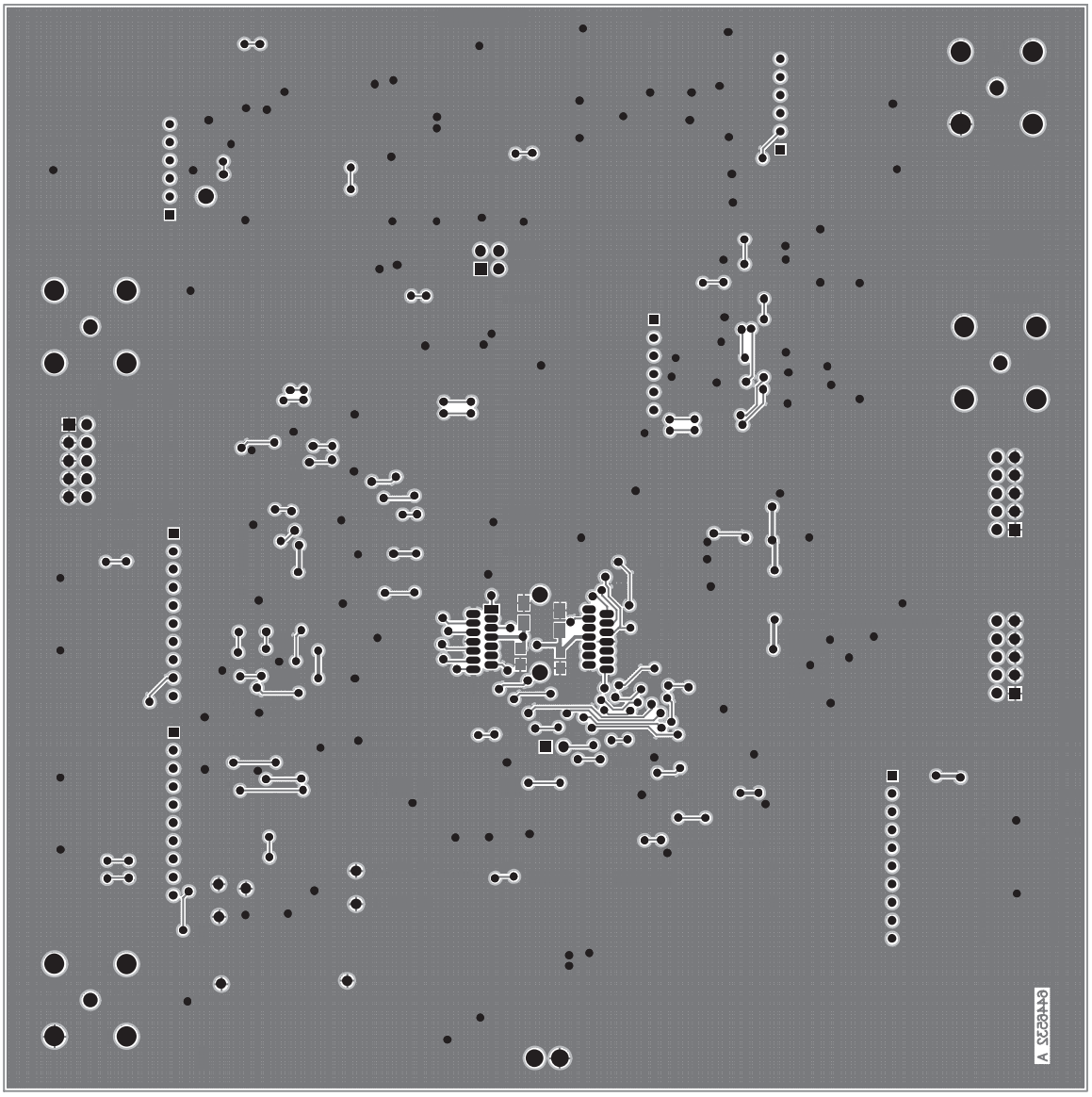


Figure 4–5. Bottom Side Layout (Solder Side)



4.3 Bill of Materials

Table 4–1. Bill of Materials

Item	Value	Reference Designator	Qty Per Bd	Manufacturer	Mfg Part Number	Description
1	18pF	C45–C48	4	Panasonic or equivalent	ECJ–2VC1H180J	Chip Capacitor, Ceramic NPO/C0G, 18pF +/– 5%, 50WV, Size = 0805
2	68000 pF	C52	1	Panasonic or equivalent	ECJ–2YB1H683K	Chip Capacitor, Ceramic X7R, 68000pF +/–10%, 50WV, Size = 0805
3	0.01µF	C53, C54	2	Kemet	C0805C103K5RACTU	Chip Capacitor, Ceramic X7R, 0.01µF +/–10%, 50WV, Size = 0805
4	0.1µF	C1—C36	36	Kemet	C0805C104K5RACTU	Chip Capacitor, Ceramic X7R, 0.1µF +/–10%, 50WV, Size = 0805
5	4.7µF	C37—C43	7	Kemet	T491A475K010AS	Chip Capacitor, Tantalum, 4.7µF +/–10%, 10WV, Size = A
6	22µF	C44	1	Kemet	T491C226K010AS	Chip Capacitor, Tantalum, 22µF +/–10%, 10WV, Size = C
7		J2, J4, J6, J7	4	Kings Electronics	KC–79–274–M06	BNC Connector, Female, PC Mount
8		J1, J3, J5	3	Samtec	TSW–105–07–G–D	Terminal Strip, 10–pin (5x2)
9		J8	1	Samtec	TSW–102–07–G–D	Terminal Strip, 4–pin (2x2)
10		J9	1	Weidmuller	1699670000	Terminal Block, 3.5mm PCB, 2 poles
11		JMP1	1	Samtec	TSW–102–07–G–S	Terminal Strip, 2–pin (2x1)
12		LED1	1	LUMEX	SML–LX1206GC–TR (DK# 67–1357–1–ND)	Green LED, SMT, Size = 1206
13	47.5	R1—R14	14	Panasonic or equivalent	P47.5FCT–ND	Resistor, 47.5 ohms, +/– 1%, 1/8W, Thick Film Chip, Size = 1206
14	75	R15—R17	3	Panasonic or equivalent	P75AACT–ND	Resistor, 75 ohms, +/– 1%, 1/4W, Thick Film Chip, Size = 1210
15	150	R22, R23	2	Panasonic or equivalent	P150AACT–ND	Resistor, 150 ohms, +/– 1%, 1/4W, Thick Film Chip, Size = 1210
16	470	R24, R25	2	Panasonic or equivalent	P470CCT–ND	Resistor, 470 ohms, +/– 1%, 1/10W, Thick Film Chip, Size = 0805

(continued on next page)

Table 4–1. Bill of Materials (continued)

Item	Value	Reference Designator	Qty Per Bd	Manufacturer	Mfg Part Number	Description
17	10K	R18—R21	4	Panasonic or equivalent	P10KCCT–ND	Resistor, 10K ohms, +/– 1%, 1/10W, Thick Film Chip, Size = 0805
18	10K	RN1, RN2, RN4	3	Bourns	4606X–101–103	Resistor Network, Single–In–Line, ThruHole Bussed, 6 terminal, 5 element
19	10K	RN5—RN7	3	Bourns	4310R–101–103	Resistor Network, Single–In–Line, ThruHole Bussed, 10 terminal, 9 element
20		SW1, SW3, SW6	3	Grayhill	90HBW04P	DIP Switch, SMT Gull Leaded Sealed, 4 position
21		SW7, SW9, SW10	3	Grayhill	90HBW08P	DIP Switch, SMT Gull Leaded Sealed, 8 position
22		SW2, SW4, SW8	3	OMRON	B3S–1000	Momentary Tact Switch, SMT w/o Ground Terminal
23		T1	1	Scientific Conversion	SC937–02	SMT Transformer for Digital Interface Receiver
24		T2	1	Scientific Conversion	SC979–03	SMT Transformer for Digital Interface Transmitter
25		U1	1	Cirrus Logic	CS8414–CS	Digital Audio Receiver
26		U2	1	Texas Instruments	SN74AHC1G04DBV	Single Inverter
27		U3	1	Texas Instruments	SN74AHC32PW	Quadruple 2–Input OR Gate
28		U4	1	Texas Instruments	SN74AHC1G14DBV	Single Schmitt Trigger Inverter
29		U5	1	Texas Instruments	DIT4192IPW	Digital Audio Interface Transmitter
30		U6, U16	2	Texas Instruments	PLL1705DBQ	Dual PLL Multiclock Generator
31		U7, U14	2	Texas Instruments	SN74ALVC125PW	Quad Buffer w/ Tri–State Outputs
32		U8, U13	2	Texas Instruments	SN74LVC04APW	Hex Inverter
33		U9, U18, U21	3	Texas Instruments	SN74ALVC244PW	Octal Buffer/Driver
34		U10, U17, U20	3	Texas Instruments	SN74ALVC245PW	Octal Bus Transceiver
35		U11, U19	2	Texas Instruments	SN74CBTLV3245APW	Octal Bus Switch
36		U12	1	Texas Instruments	SN74LVC1G07DBV	Single Buffer w/ Open Drain Output

(continued on next page)

Table 4–1. Bill of Materials (continued)

Item	Value	Reference Designator	Qty Per Bd	Manufacturer	Mfg Part Number	Description
37		U15 (DUT)	1	Texas Instruments	SRC4192IDB	Asynchronous Sample Rate Converter
38		U22	1	Texas Instruments	REG1117–3.3	Voltage Regulator, +3.3V
39		U23	1	Texas Instruments	SN74AHC244PW	Octal Buffer/Driver
40		X1, X2	2	Citizen	HCM49–27.000MABJT	Quartz Crystal, SMT, 27MHz, +/– 50ppm
41			1	Enplas–Tesco	OTS–28(34)–0.65–01	ZIF Socket for SSOP–28, Pinch (2–contact) type
42			4	3M Bumpon	SJ–5003	Rubber Feet, Adhesive Backed
43			2	Samtec	SNT–100–BK–G–H	Shorting Blocks